A

Project Report

ON

Implementation of Even Parity Generator Using Dynamic CMOS(NORA)Logic

Submitted to

Rajiv Gandhi University of Knowledge Technologies,

RK Valley, KADAPA.

in partial fulfillment of the requirements for the award of the Degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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RK VALLEY, KADAPA (DIST.), ANDHRA PRADESH, PINCODE -516330.

April – 2022.

RAJIV GANDHI UNIVERSITY OF KNOWLEDGE TECHNOLOGIES,

RK VALLEY, KADAPA (DIST.), ANDHRA PRADESH,

PINCODE -516330.April – 2022.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that the project report entitled **"Implemention of Even Parity Generator Using Dynamic CMOS (Nora) Logic "** a bonafide record of the project work done and submitted by

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Project Internal GUIDE

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External Viva-Voce Exam Held on _____

INTERNAL EXAMINER **EXTERNAL EXAMINER**

DECLARATION

We hereby declare that the project report entitled "**Implementation of Even Parity Generator Using Dynamic CMOS(Nora) Logic**" submitted to the Department of **ELECTRONICS AND COMMUNICATION ENGINEERING** in partial fulfillment of requirements for the award of the degree of **BACHELOR OF TECHNOLOGY.** This project is the result of our own effort and that it has not been submitted to any other University or Institution for the award of any degree or diploma other than specified above.

By,

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ACKNOWLEDGEMENTS

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We have great pleasure in expressing our hearty thanks to our beloved Director **Dr. SANDHYA RANI** for spending her valuable time with us to complete this project.

Successful completion of any project cannot be done without proper support and encouragement. We sincerely thanks to the Management for providing all the necessary facilities during the course of study.

We would like to thank our parents and friends, who have the greatest contributions in all our achievements, for the great care and blessings in making us successful in all our endeavors.

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ABSTRACT

Since we are keen interested on searching for new areas and exploring new things and in Electronics World especially related to the area of VLSI.As we want to enhance and to Build our career, from the VLSI Design which is a core subject in Electronics and Communication Engineering ,This research that made by us helps us to gain Confidence and research further in the field of VLSI.The Main Objective of our Project is to make and implement " **Even Parity Generator using Dynamic CMOS (NORA) Logic**".The Objective of the Dynamic CMOS (a Race Free) Logic is Low Power Design.Low power design is a collection of techniques and methodologies aimed at reducing the overall dynamic and static power consumption of an integrated circuit (IC).

The power and cost savings by upgrading these systems with newer and more power efficient ICs can be significant.The Proposed Project was Designed and Simulated in DSCH2(Digital Schematic software) and Microwind Softwares and could be Performed through Software Simulation.The Even Parity Generator could be designed by using CMOS Transistors which is a Combination of Both PMOS and NMOS Transistors .

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LIST OF ABSERVATION

CMOS	Complementary metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
PMOS	Ptype(Material)metal oxide semiconductor
NMOS	Ntype(Material)metal oxide semiconductor
DSCH	Dynamic Software
NORA	No Race Condition

1. INTRODUCTION

In digital data transmission, the Parity generator and the parity checker is effective method to find the error in the destination end.Power consumption has emerged as a primary design constraint for integrated Circuits (IC's). So this generation of parity of the bits are designed by the dynamic CMOS NORA Logic which reduces the number of transistors and power consumption than the conventional Static CMOS design method.

2. PARITY CHECKER

Now a days , In Modern Digital Communication,the digital data are Transmitted in form of Binary data(0’s and 1’s), while transmitting the data due to external noise addition, the noise can alter 0’s to 1’s and 1’s to 0’s.To check whether the recieved the data is correct or not, we use few techniques to detect the errors at the reciever.

2.1.Parity Bit:-

It is one of the most widely used error detection Techniques in data transmission. Therefore,a Parity Bit is added to the word containing data in order to make number of 1s either even or odd.

The message containing the data bits along with parity bit is transmitted from transmitter to the receiver.At the reciever, the number of 1s in the message is counted and if it doesn’t match with the transmitted one, it means there is an error in the data.

Therefore in similar way, the Parity Bit it is used to detect errors, during the transmission of binary data.

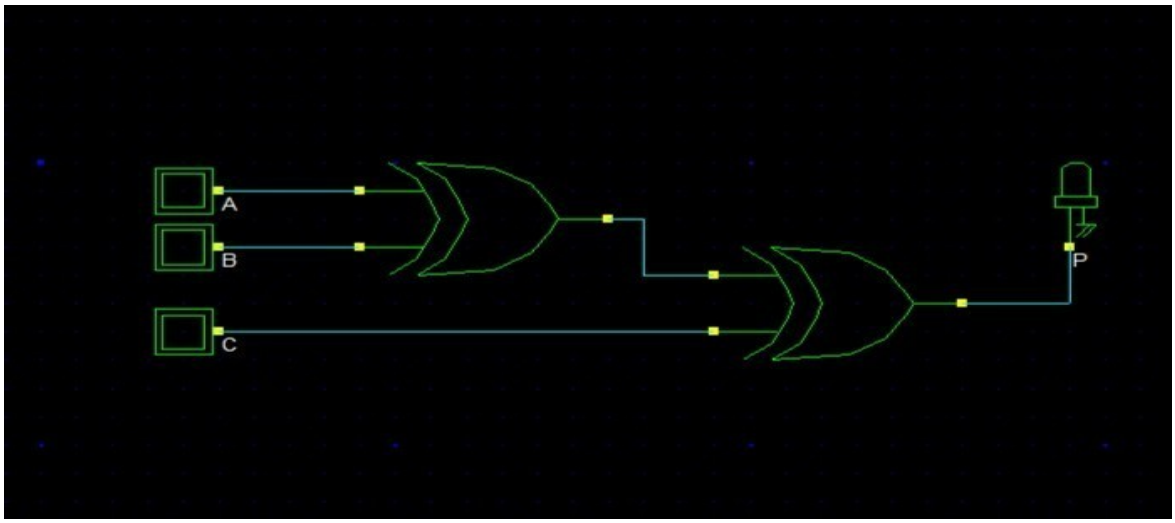
3.PARITY GENERATOR

A parity generator is nothing but a combinational logic circuit that generates the additional bit known as parity bit in the Transmitter.

3.1.*Even parity Generator:-*

In even parity generator , the parity bit is ‘0’ if there are even number of 1’s in bit stream.The parity bit is ‘1 ’ if there are Odd number of 1’s in Data stream.

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



3.2.Odd parity Generator:-

In Odd parity generator, the parity bit is ‘1’ if there are even number of 1’s in data stream.The parity bit is ‘0’ if there are Odd number of 1’s in data stream.

4.CMOS TECHNOLOGY

Complementary metal–oxide–semiconductor(C-MOS), is a type of metal oxide semiconductor field effect (MOSFET) Fabrication process that uses complementary p-type and n-type MOSFETs for logic functions.CMOS technology is used for constructing integrated Circuit(IC) chips, including microprocessors.

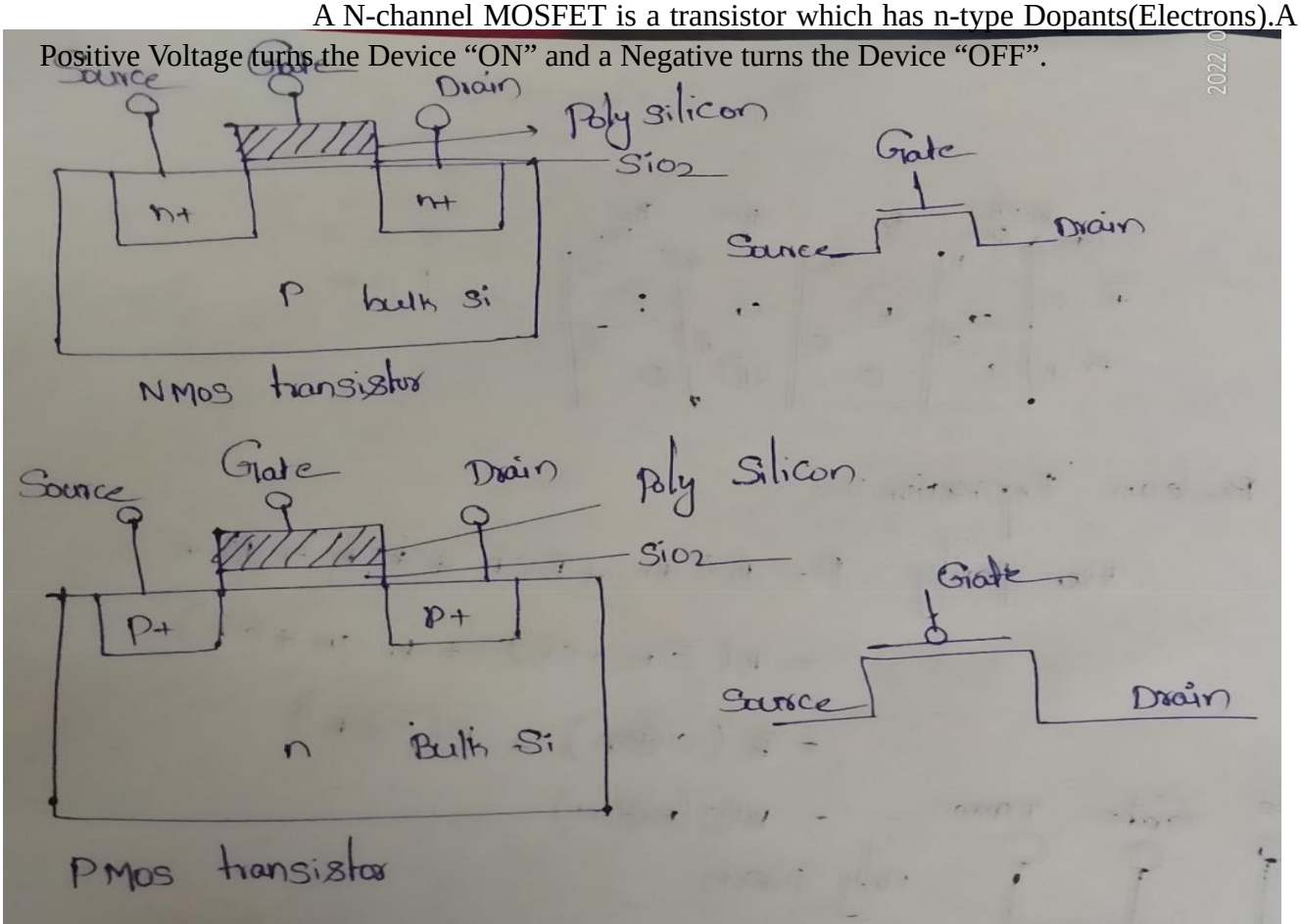
At First a new type of MOSFET logic combining both the PMOS and NMOS processes was developed, called complementary MOS (CMOS), by Chih-Tang Sah and Frank Wanlass at Fairchild. In February 1963, they published the invention in a Research paper.

4.1.P-channel MOSFET (PMOS) :

A P-Channel MOSFET is a transistor which p-type Dopants(Holes).A Negative Voltage on the gate turns the Device “ON” and a Positive voltage turns the Device “OFF”.

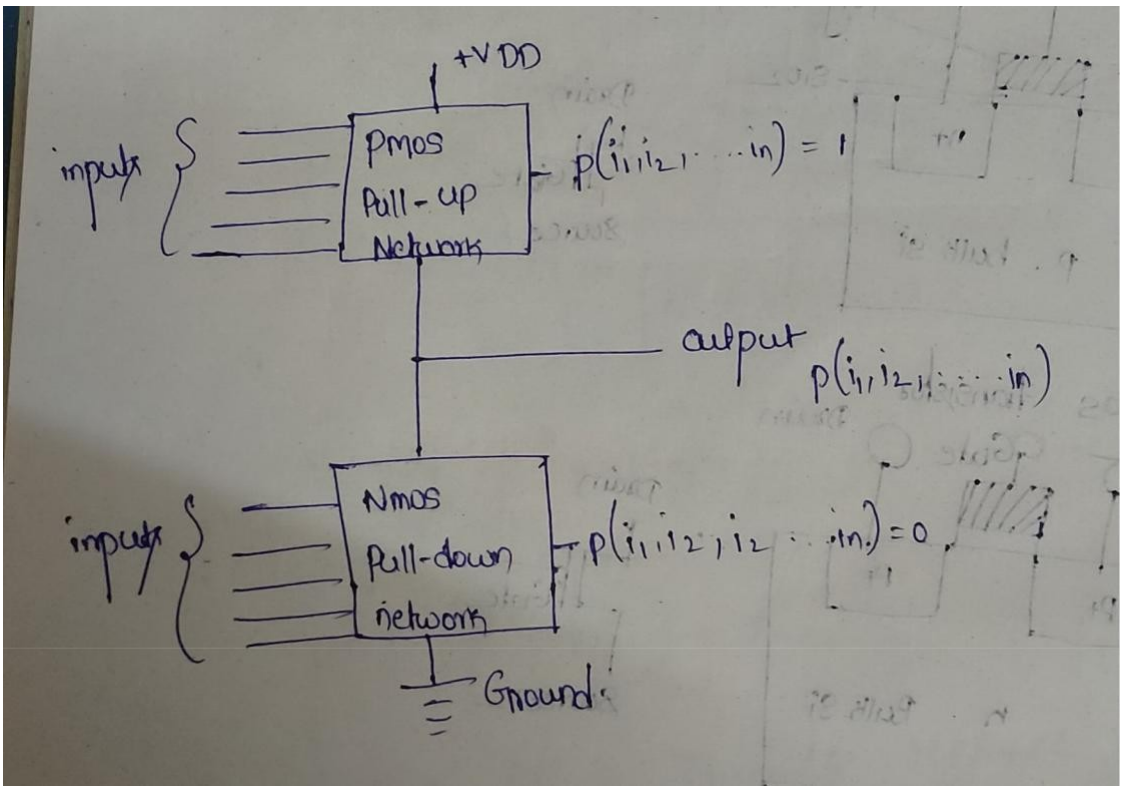
4.2.N-Channel MOSFET (NMOS) :

A N-channel MOSFET is a transistor which has n-type Dopants(Electrons).A Positive Voltage turns the Device “ON” and a Negative turns the Device “OFF”.



4.3.General CMOS Logic Structure:

A Complementary Metal Oxide semiconductor(CMOS) has a Combination of Both PULL UP & PULL DOWN Network.The NMOS network is connected between the Output and the ground, Where as the Pull-up network is connected between the Output and the power supply.



5.STATIC CMOS TECHNOLOGY

It is a logic circuit design which the Output of the CMOS is Strongly driven due to it is always being connected to either Vcc or Ground(gnd).Static CMOS circuits use complementary NMOS pulldown and pMOS pullup networks to implement logic gates or logic functions in integrated circuits.

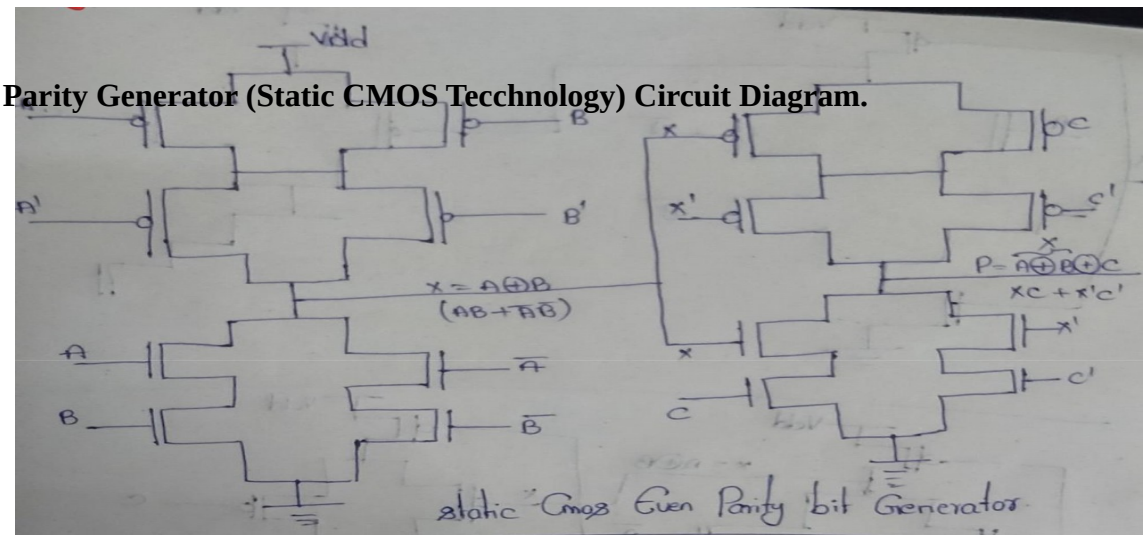
A static CMOS circuit Consists of 16 MOSFET Transistors and a combination of two types of networks:Pull-up network (PUN) - a set of PMOS transistors connected between Vcc and the output line.Pull-down network (PDN) - a set of NMOS transistors connected between GND and the output line.The Devices that are made up of PUN (or) PDN are always strongly driven and therefore offers strong immunity from noise.

5.1.LOGIC :

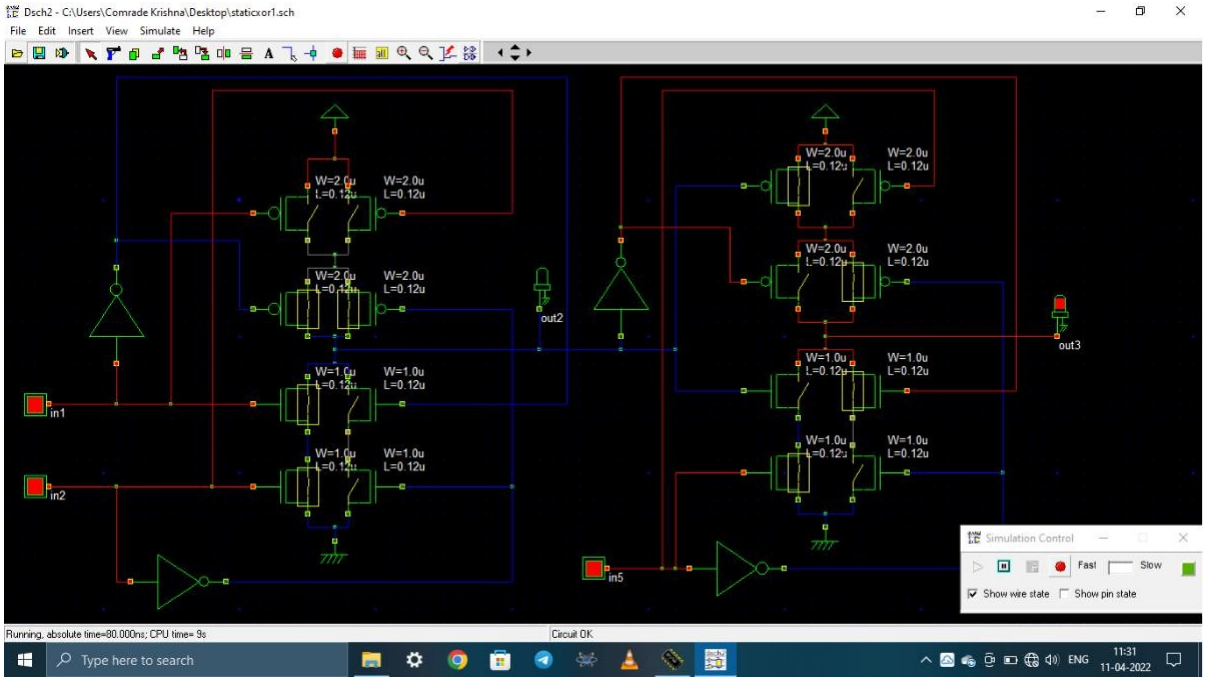
	PUN OFF	PUN ON
PDN OFF	HIGH Z	1
PDN ON	0	Crowbarred Level

If Both PDN and PUN are in “OFF” State,the result is High Impedance.If both PDN and PUN are in “ON” State , it is a crowbarred level condition which is unwanted.

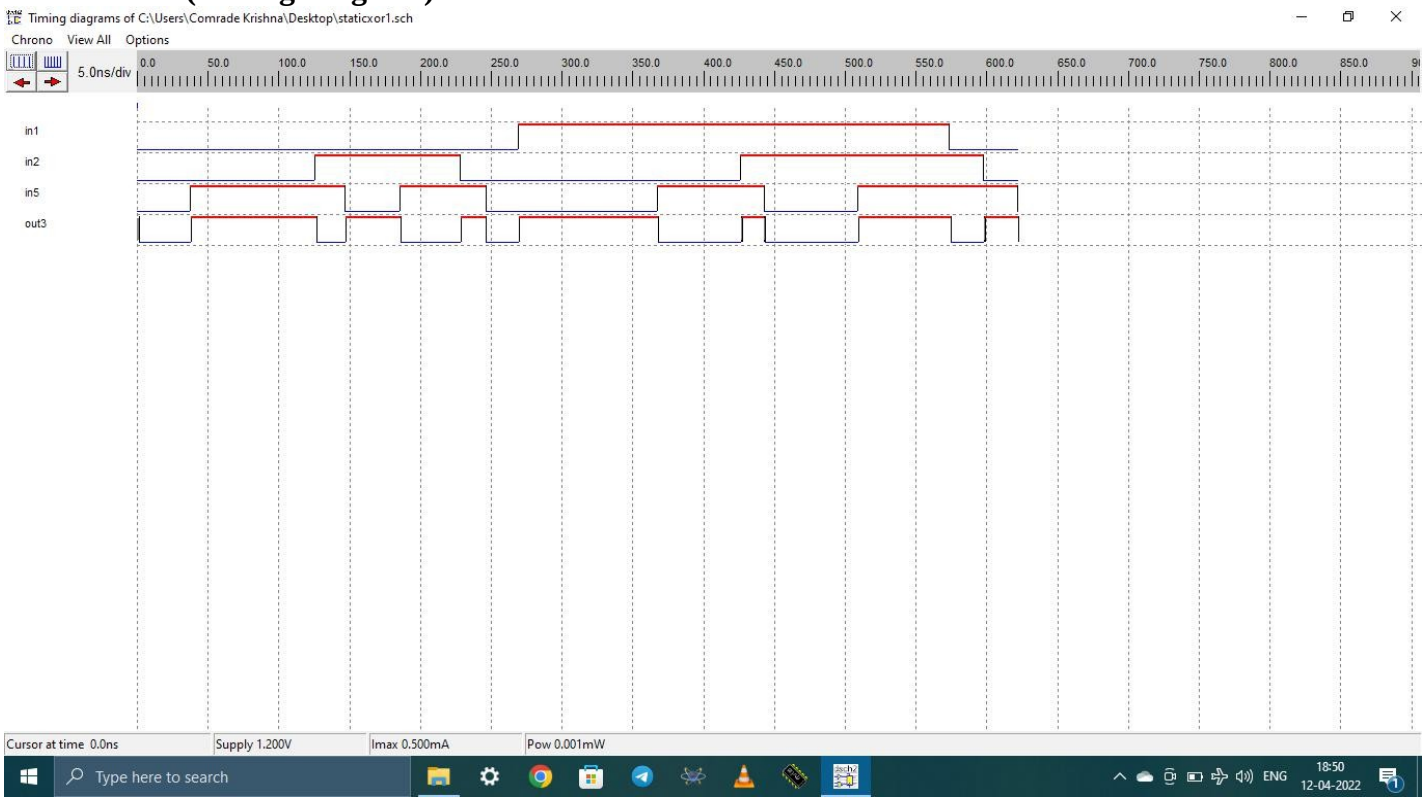
5.2.Even Parity Generator (Static CMOS Tecchnology) Circuit Diagram.



5.3.Even Parity Generator (Static CMOS Tecchnology) In DSCH Software.



5.4.Even Parity Generator (Static CMOS Tecchnology) In DSCH Software.(Timing Diagram)



5.5.Even Parity Generator (Static CMOS Tecchnology) In DSCH Software.(Verilog Code)

staticxor1 - Notepad

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```
// DSCH 2.7a
// 11-04-2022 08:27:02
// C:\Users\Comrade Krishna\Desktop\staticxor1.sch

module staticxor1( in1,in2,in5,out2,out3);
 input in1,in2,in5;
 output out2,out3;
 pmos #(24) pmos(w2,vdd,in1); // 2.0u 0.12u
 pmos #(52) pmos(out2,w2,w3); // 2.0u 0.12u
 pmos #(24) pmos(w2,vdd,in2); // 2.0u 0.12u
 pmos #(52) pmos(out2,w2,w6); // 2.0u 0.12u
 nmos #(52) nmos(out2,w7,in1); // 1.0u 0.12u
 nmos #(10) nmos(w7,vss,in2); // 1.0u 0.12u
 nmos #(52) nmos(out2,w8,w3); // 1.0u 0.12u
 nmos #(10) nmos(w8,vss,w6); // 1.0u 0.12u
 not #(17) inv(w3,in1);
 not #(17) inv(w6,in2);
 pmos #(24) pmos(w9,vdd,out2); // 2.0u 0.12u
 pmos #(31) pmos(out3,w9,w10); // 2.0u 0.12u
 pmos #(24) pmos(w9,vdd,in5); // 2.0u 0.12u
 pmos #(31) pmos(out3,w9,w13); // 2.0u 0.12u
 nmos #(31) nmos(out3,w14,out2); // 1.0u 0.12u
 nmos #(31) nmos(out3,w15,w10); // 1.0u 0.12u
 nmos #(10) nmos(w14,vss,in5); // 1.0u 0.12u
 nmos #(10) nmos(w15,vss,w13); // 1.0u 0.12u
 not #(17) inv(w13,in5);
 not #(17) inv(w10,out2);
endmodule

// Simulation parameters in Verilog Format
always
#1000 in1=~in1;
#2000 in2=~in2;
#4000 in5=~in5;

// Simulation parameters
// in1 CLK 10 10
// in2 CLK 20 20
```

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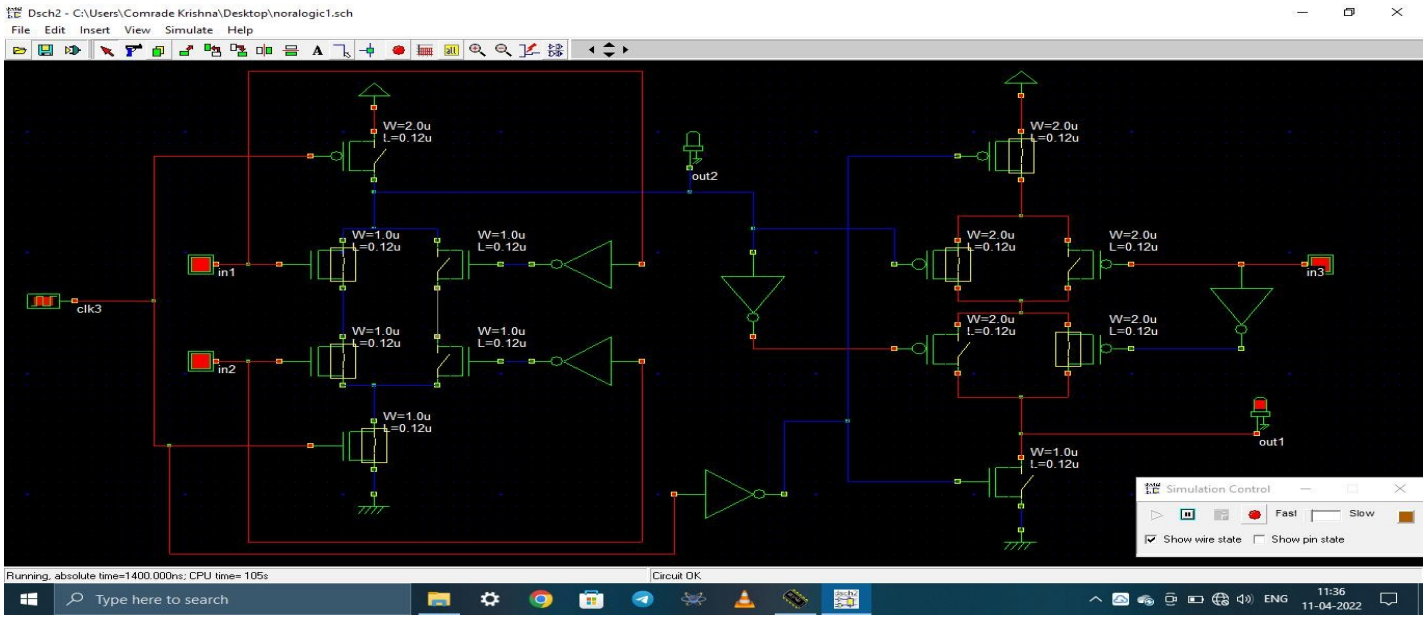
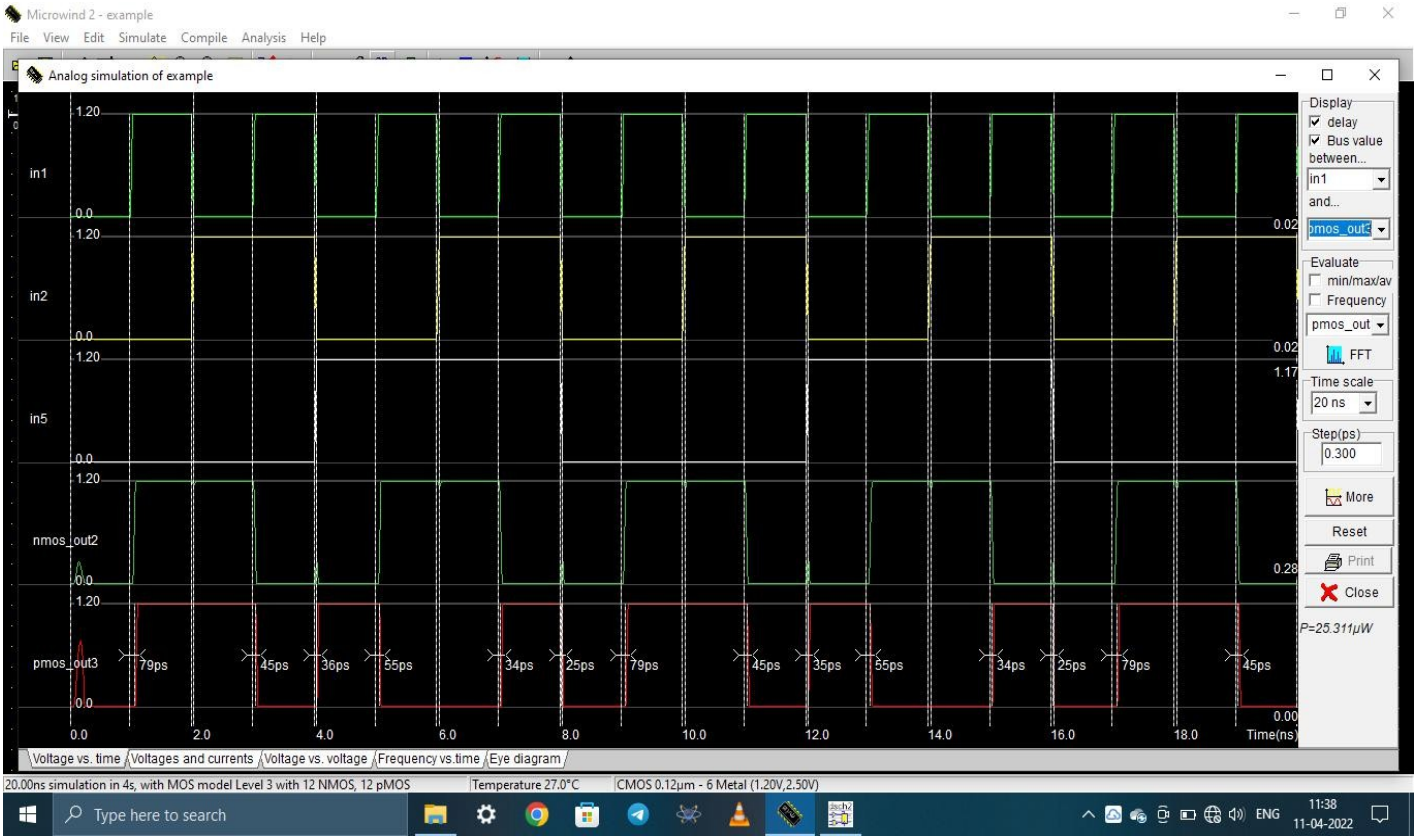
5.6.Even Parity Generator (Static CMOS Tecchnology) In DSCH Software.(Layout Simulation)



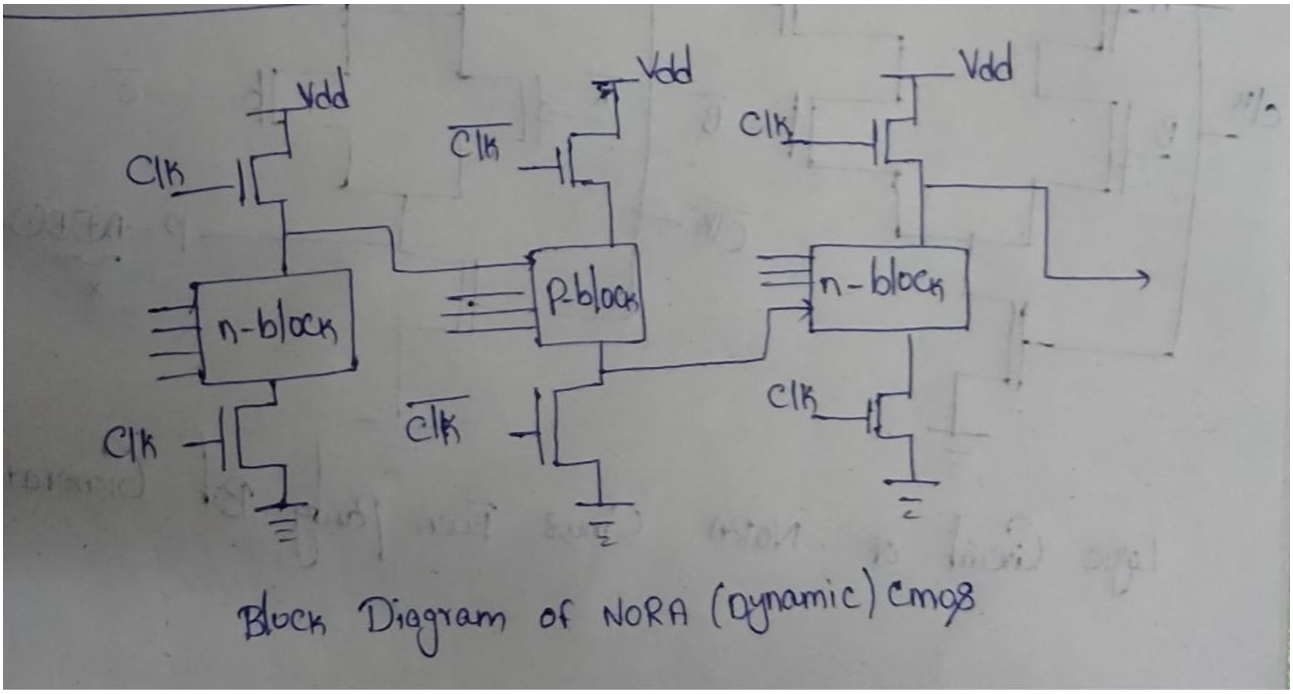
5.7.Even Parity Generator (Static CMOS Tecchnology) In DSCH Software.(Time VS VOLTAGE Power Analysis)



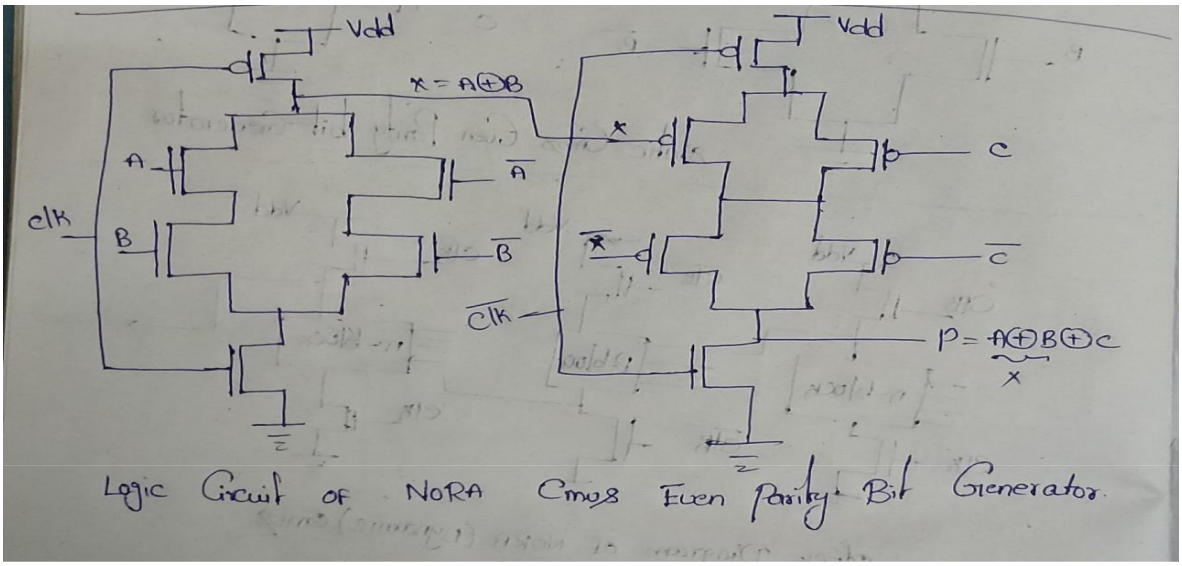
6.DYNAMIC NORA CMOS TECHNOLOGY

This Technique is also called as Race Free or No-Race Technique.The Dynamic gates uses a clocked PMOS PULL UP.The NORA technique is used to reduce complexity and space in VLSI Designing and the main objective is to reduce the Power consumption as compared to Static CMOS gates.

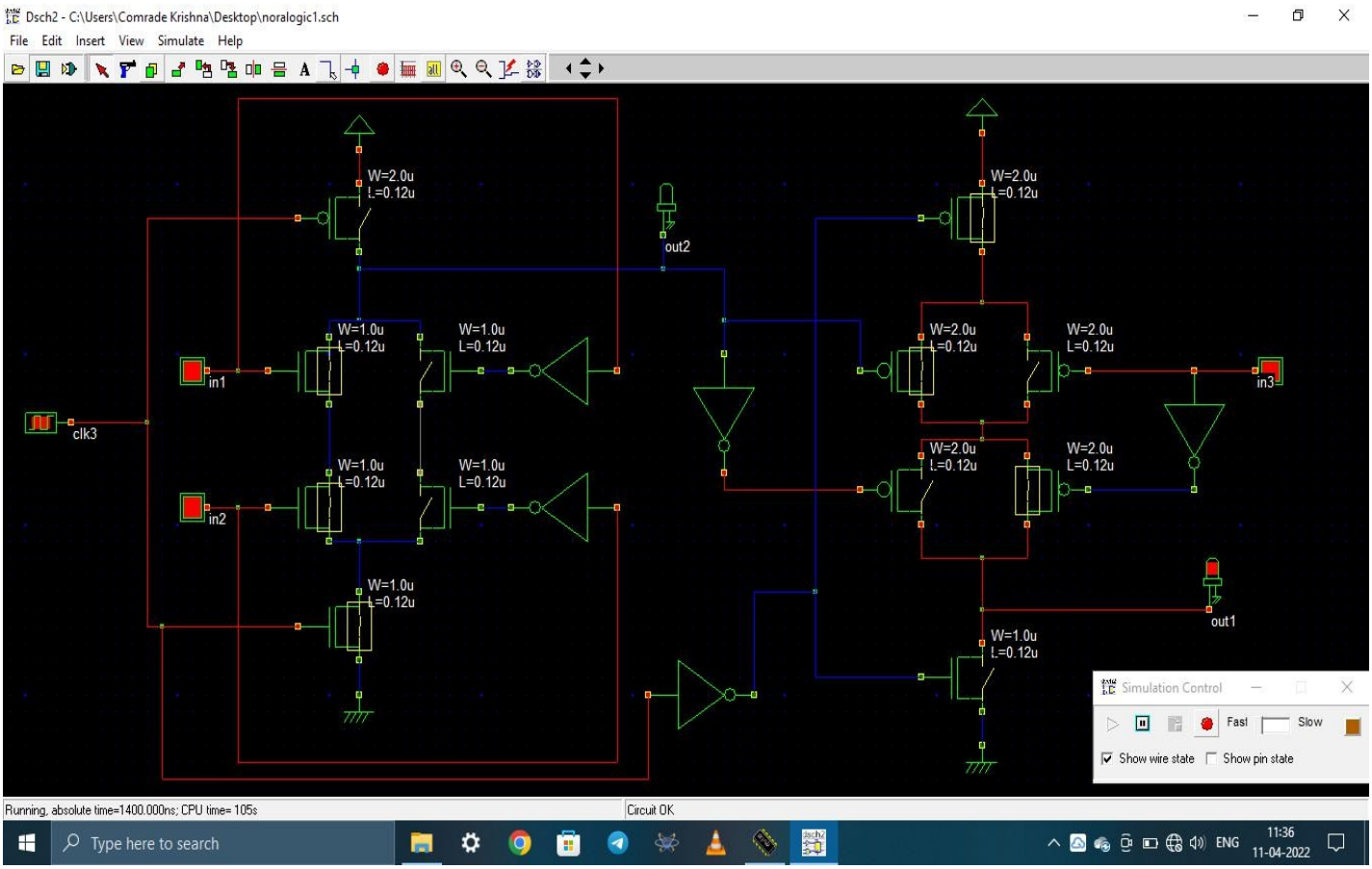
6.1.Block Diagram of Dynamic NORA CMOS Technology



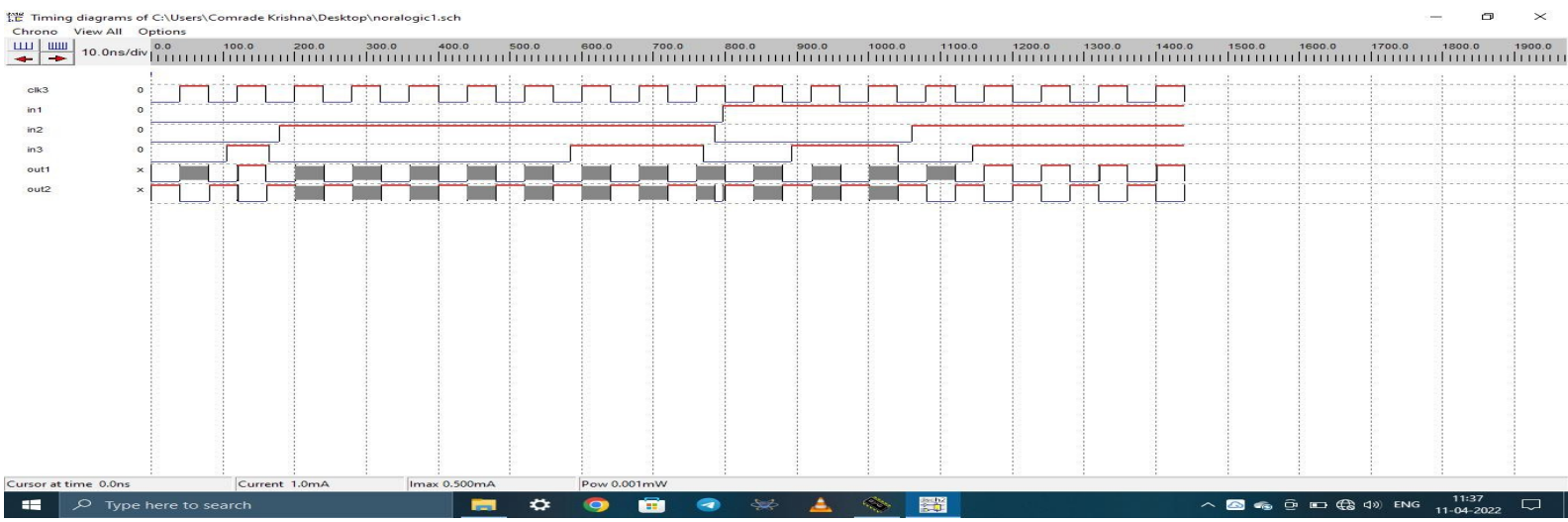
6.2.Even Parity Generator Using Dynamic NORA CMOS Technology



6.3.Even Parity Generator (Dynamic NORA CMOS Technology) in DSCH Software



6.4.Timing Diagram Even Parity Generator (Dynamic NORA CMOS Technology) in DSCH Software.



6.5.Verilog Code of Even Parity Generator (Dynamic NORA CMOS Technology) in DSCH Software.

noralogic1 - Notepad

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```
// C:\Users\Comrade Krishna\Desktop\noralogic1.sch

module noralogic1( in2,in1,in3,clk3,out2,out1);
 input in2,in1,in3,clk3;
 output out2,out1;
 pmos #(38) pmos(out2,vdd,clk3); // 2.0u 0.12u
 nmos #(38) nmos(out2,w3,in1); // 1.0u 0.12u
 nmos #(38) nmos(out2,w5,w6); // 1.0u 0.12u
 nmos #(10) nmos(w3,w7,in2); // 1.0u 0.12u
 nmos #(10) nmos(w5,w7,w9); // 1.0u 0.12u
 nmos #(17) nmos(w7,vss,clk3); // 1.0u 0.12u
 not #(10) inv(w6,in1);
 not #(10) inv(w9,in2);
 not #(10) inv(w10,out2);
 pmos #(17) pmos(w12,vdd,w11); // 2.0u 0.12u
 pmos #(24) pmos(w13,w12,out2); // 2.0u 0.12u
 pmos #(24) pmos(w13,w12,in3); // 2.0u 0.12u
 pmos #(24) pmos(out1,w13,w10); // 2.0u 0.12u
 pmos #(24) pmos(out1,w13,w16); // 2.0u 0.12u
 nmos #(24) nmos(out1,vss,w11); // 1.0u 0.12u
 not #(10) inv(w16,in3);
 not #(17) inv(w11,clk3);
endmodule

// Simulation parameters in Verilog Format
always
#1000 in2=~in2;
#2000 in1=~in1;
#4000 in3=~in3;
#4000 clk3=~clk3;

// Simulation parameters
// in2 CLK 10 10
// in1 CLK 20 20
// in3 CLK 40 40
// clk3 CLK 40.00 40.00
```

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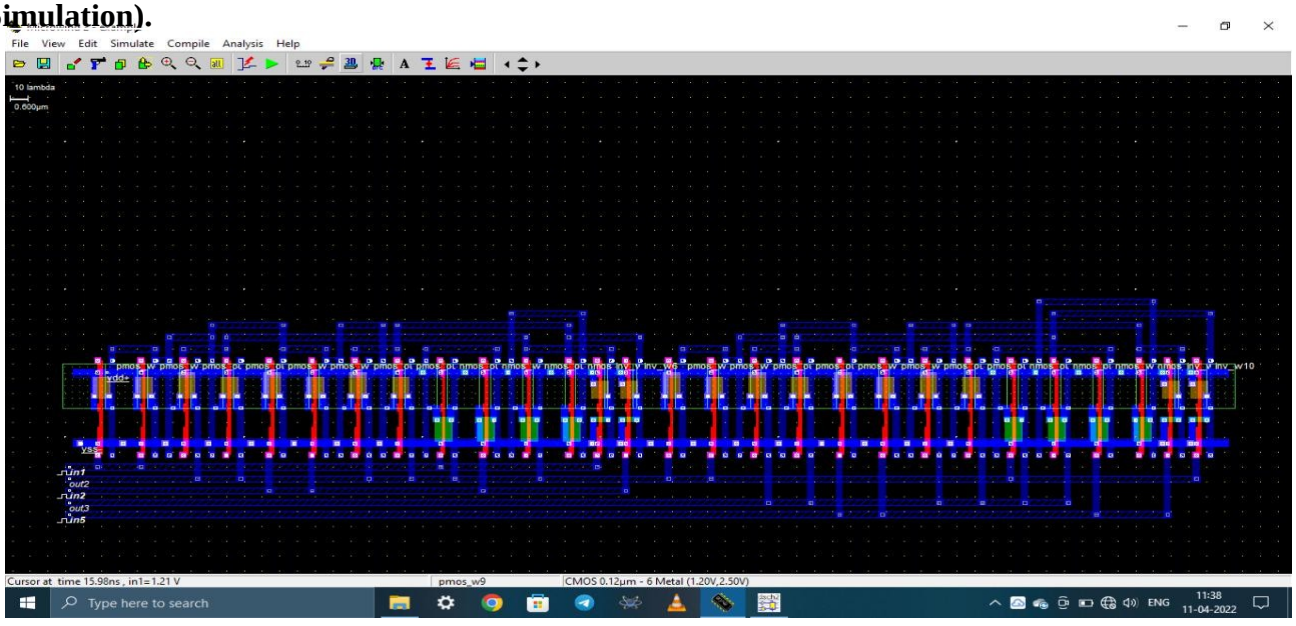
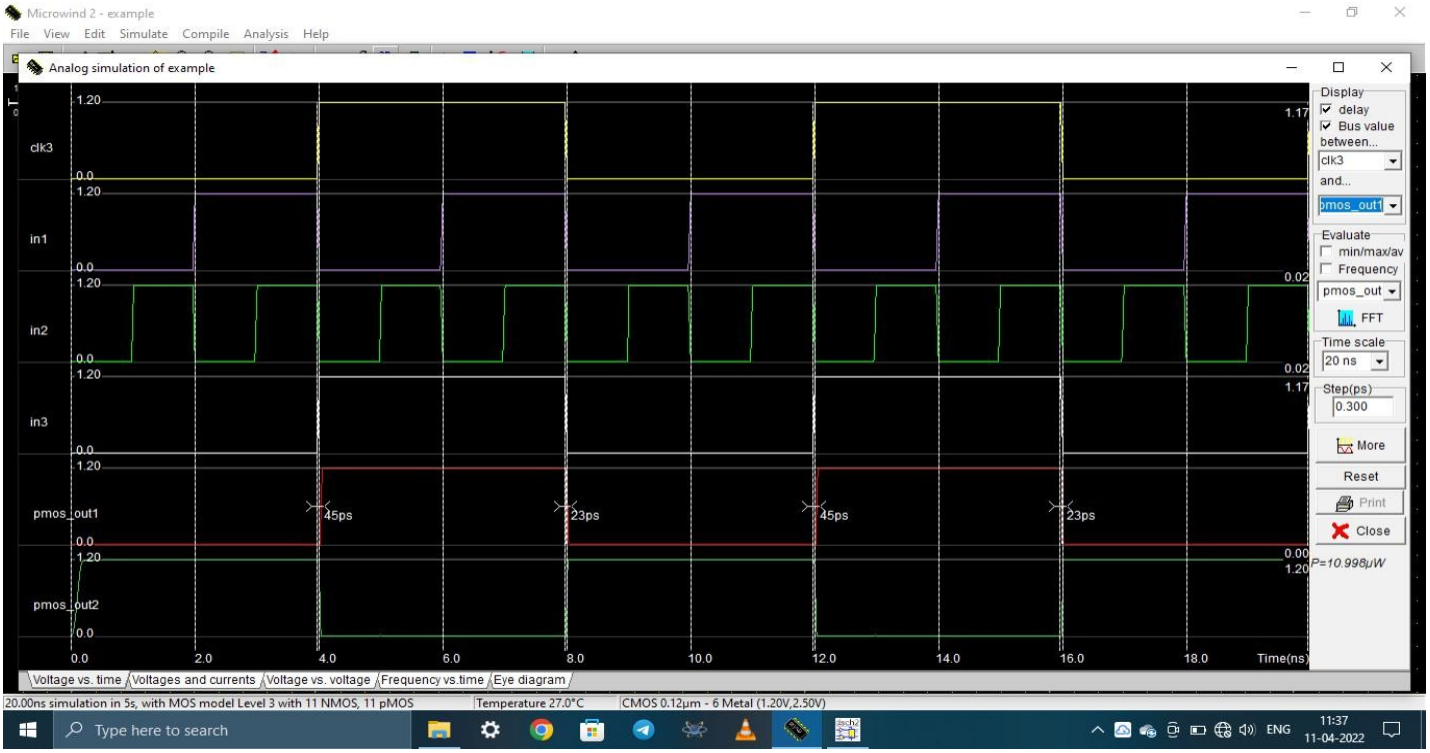
6.6.Even Parity Generator (Dynamic NORA CMOS Technology) in DSCH Software.(Layout Simulation).



6.7.Even Parity Generator (Dynamic NORA CMOS Technology) in DSCH Software. (Voltage VS Time (Power Analysis).



7.CONCLUSION

The Even parity generator using Dynamic CMOS (NoRa) Logic is useful to reduce the Overall power consumption of the logic Block/ Circuit and reduces complexity and Area occupied by the Circuit as compared with Static or General CMOS structure. The Implementation of the Static and Dynamic CMOS circuits are Simulated in DSCH and Microwind Softwares and Power consumption(Voltage vs Time) graphs for both are Observed.The Dynamic CMOS Technology is applicable in Low power VLSI Design.