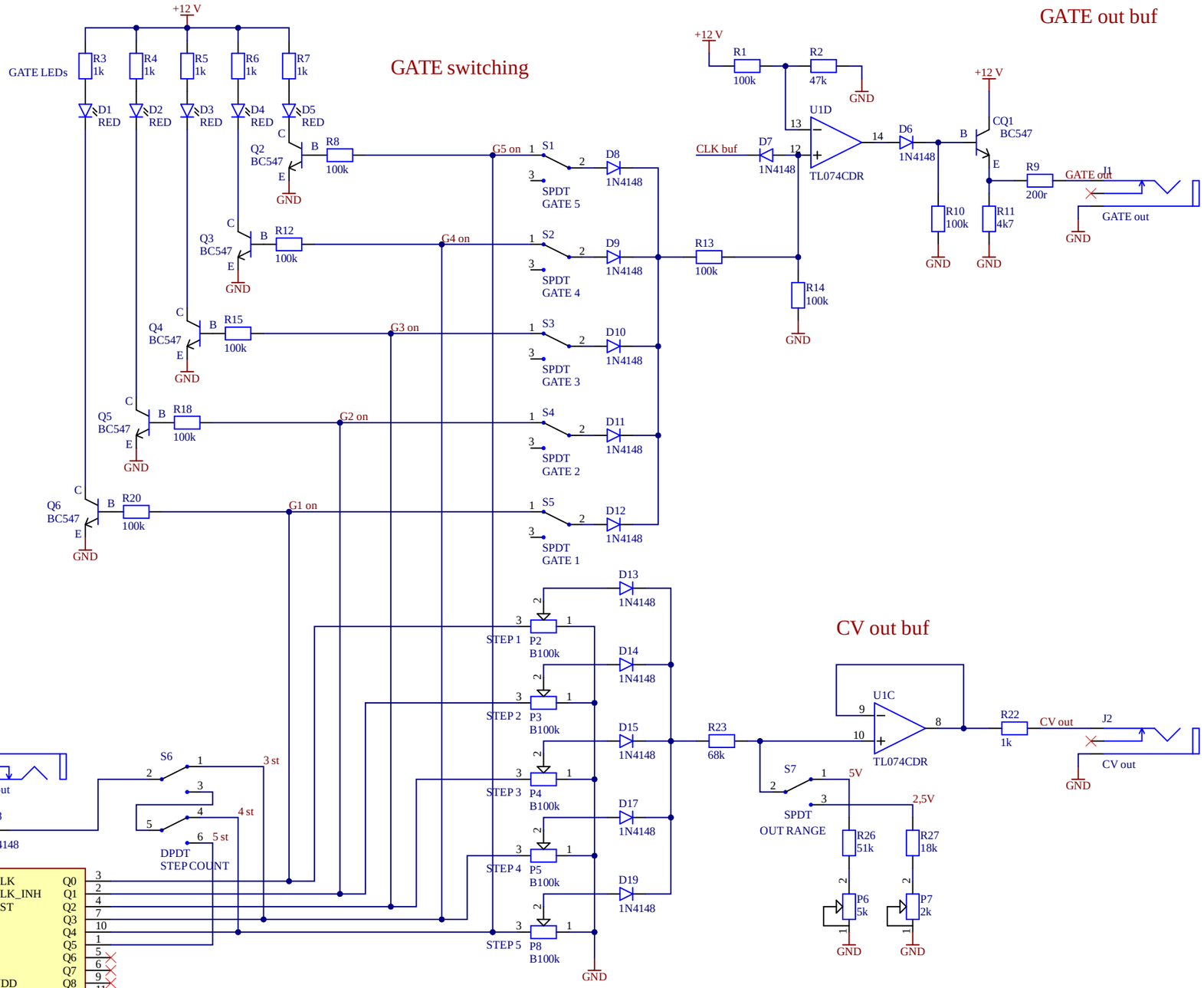
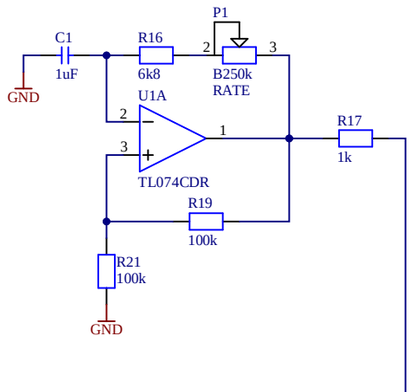
GATE switching



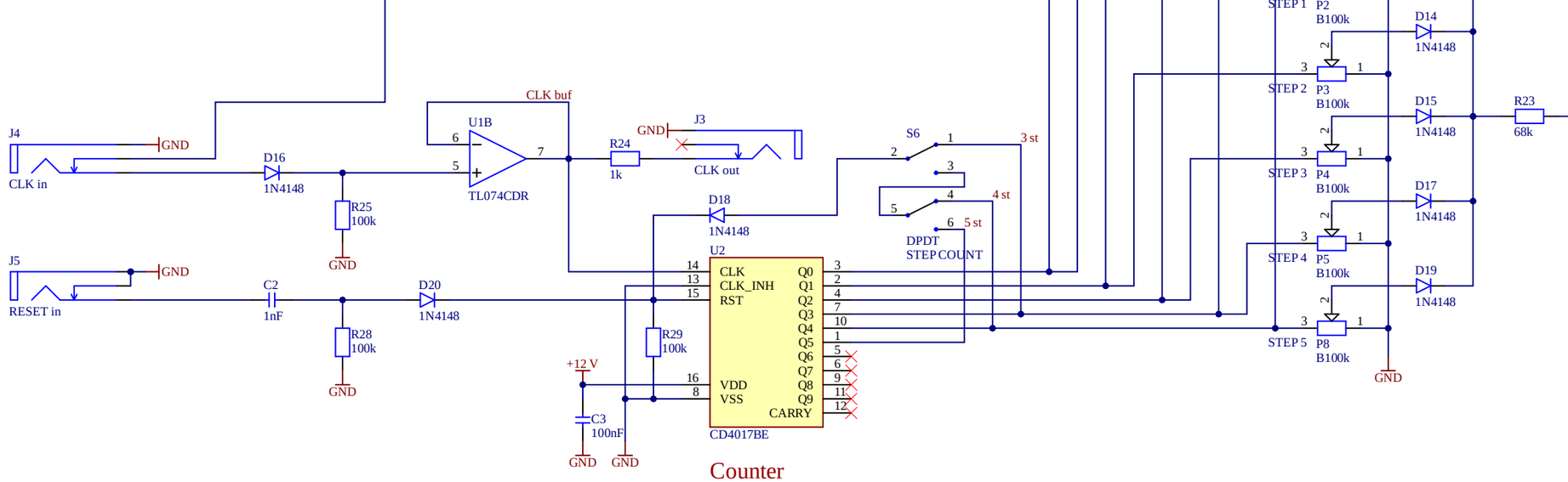
GATE out buf

Internal CLK gen

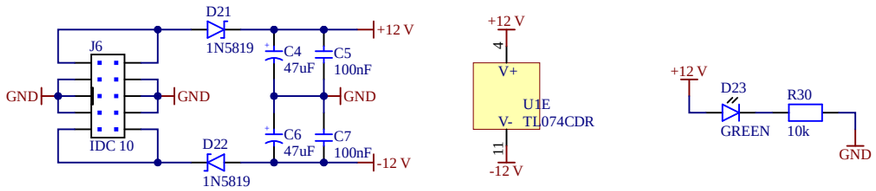


CV out buf

Counter



Power section



PROJECT: **5_step_seq.PrjPcb**	
SCHEMATIC: **Sequencer_board**	REV: 1.1 DATE: 19.08.2025
DRAWN BY: **Jakub Orzechowski**	FILENAME: 5_step_seq.SchDoc SHEET: 1 out of 1