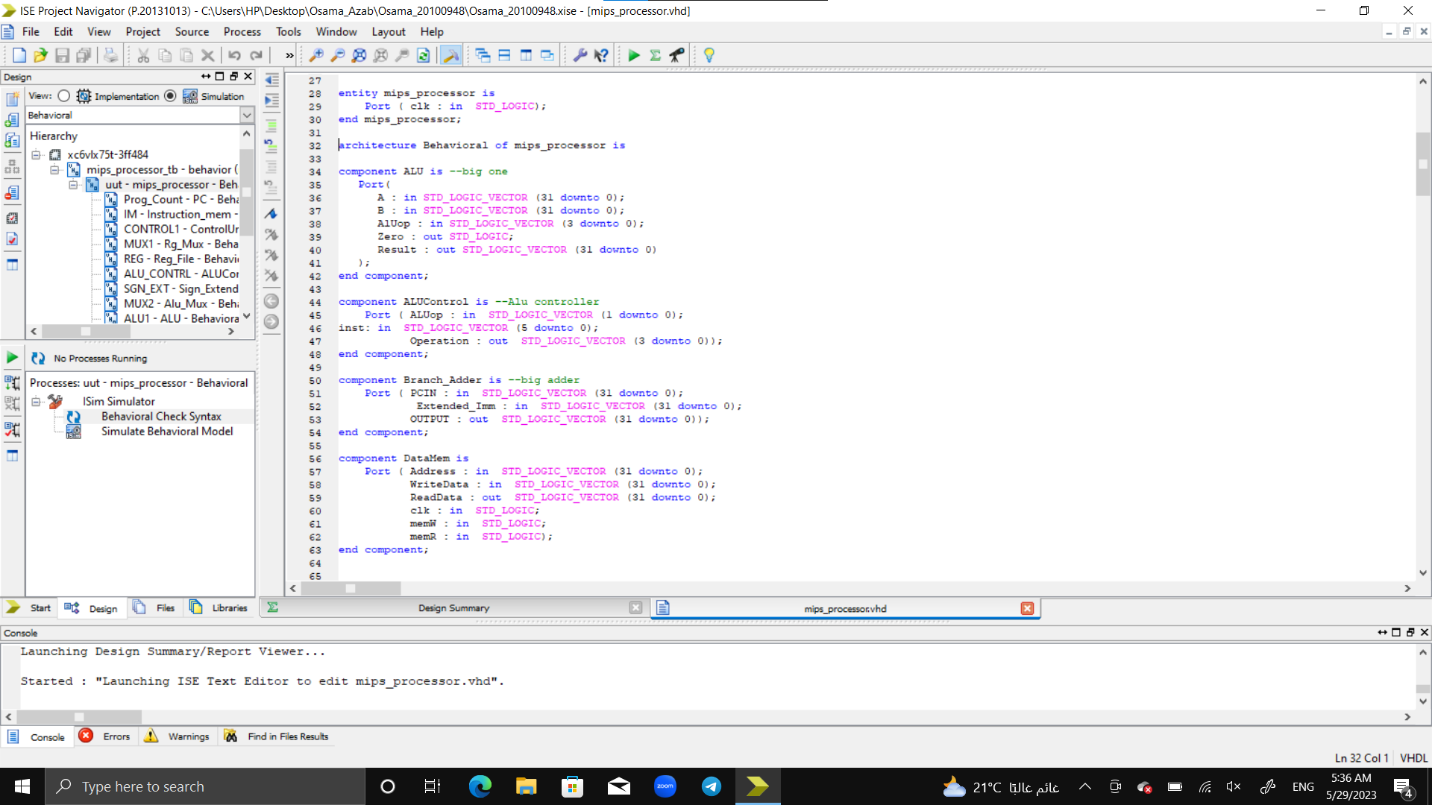
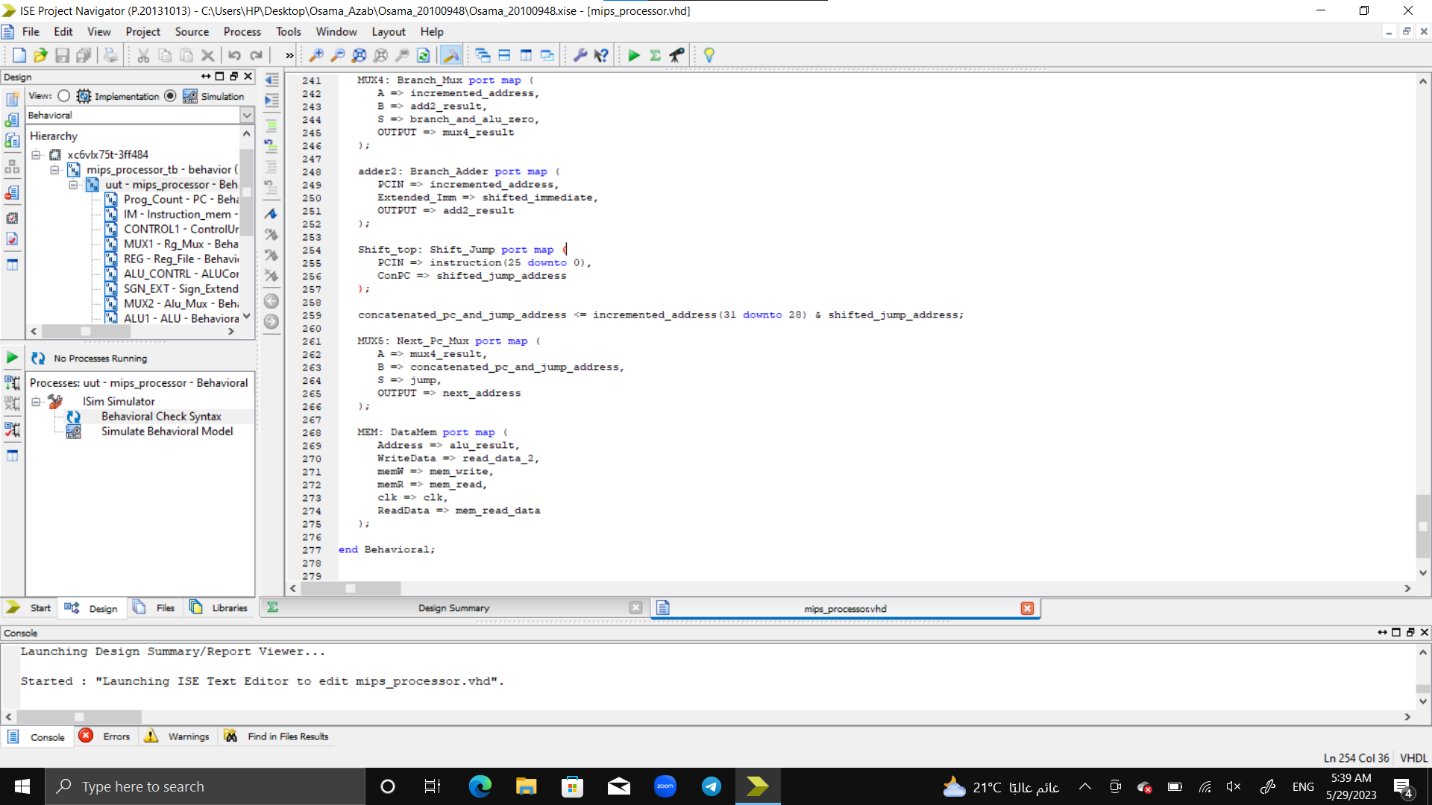
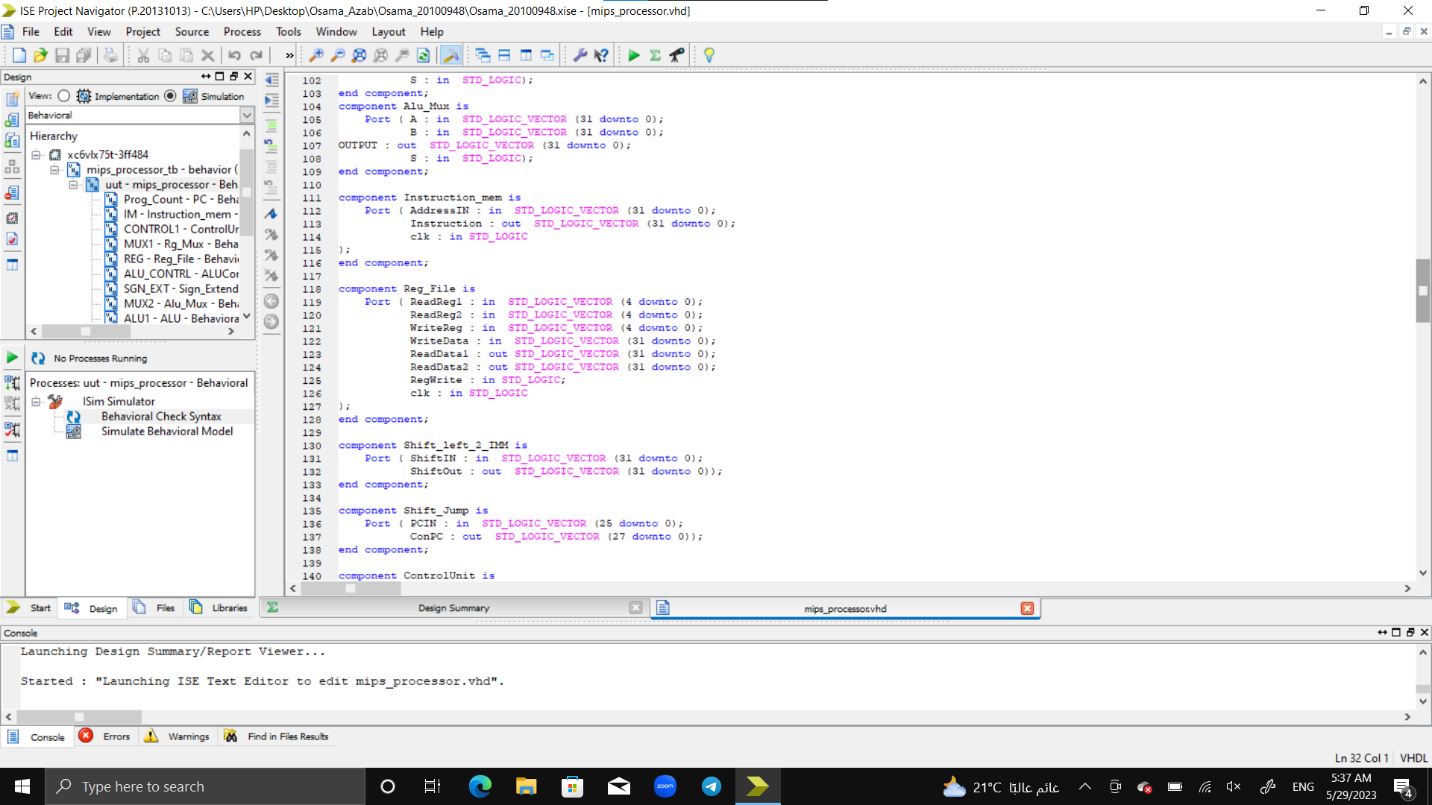
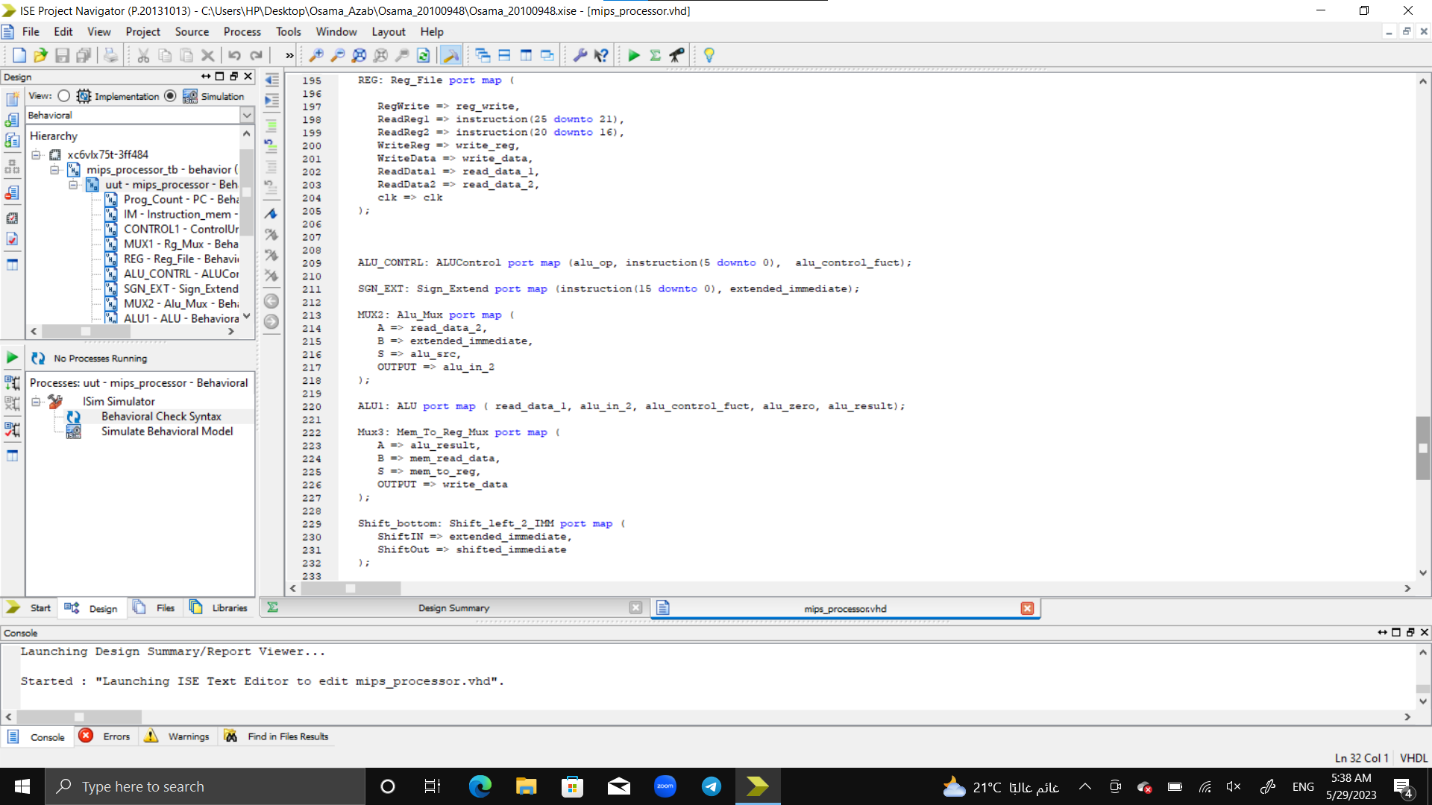
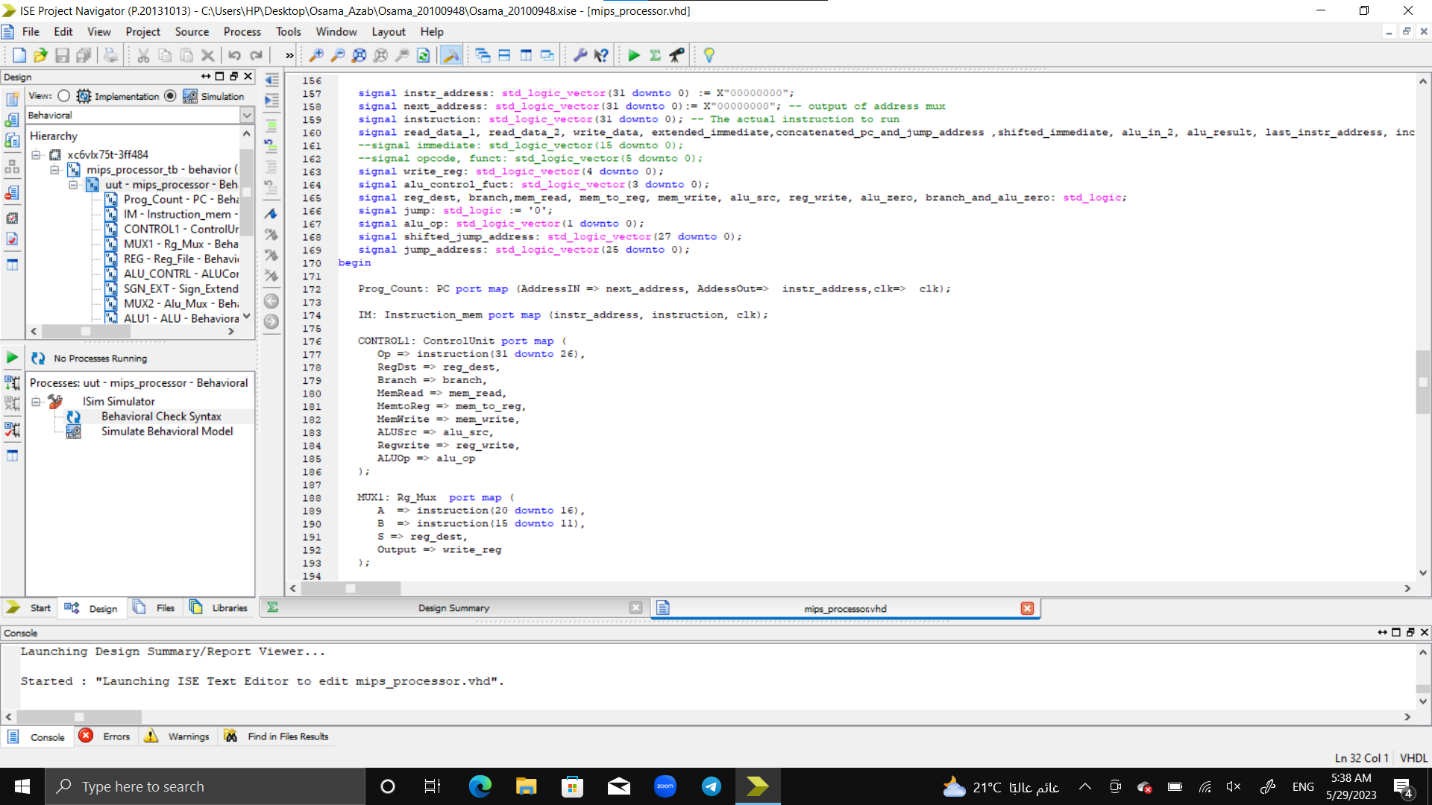
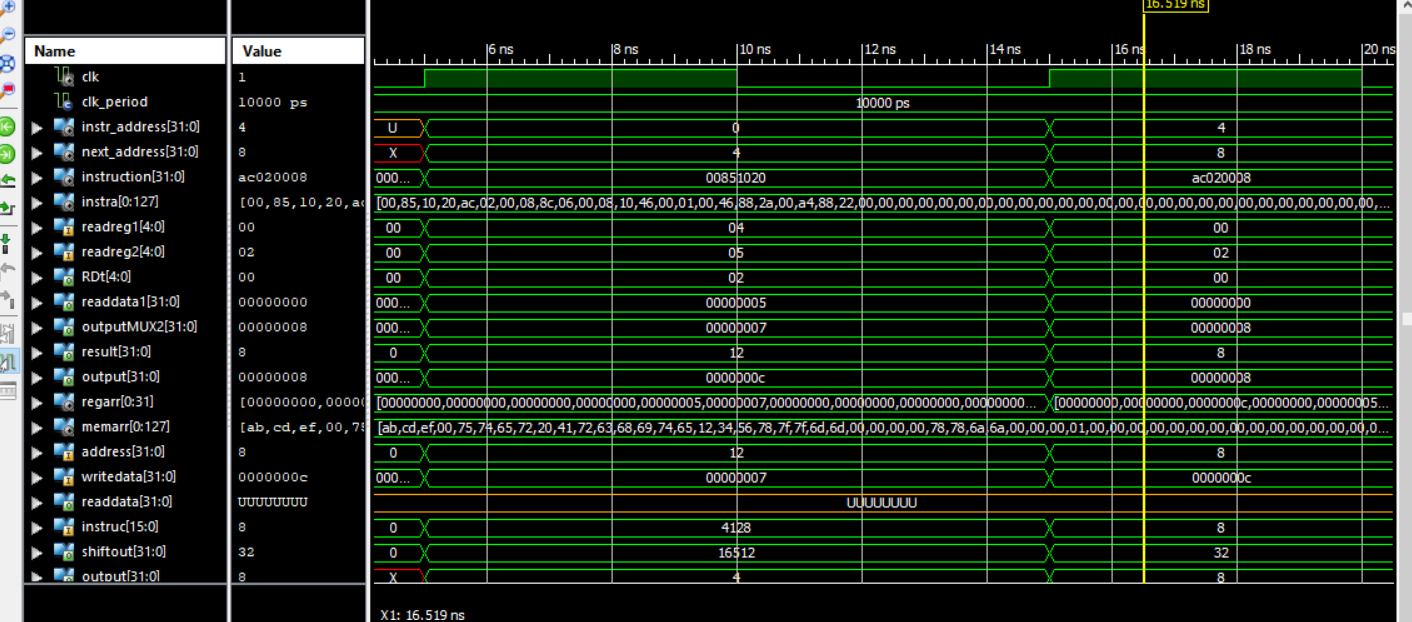
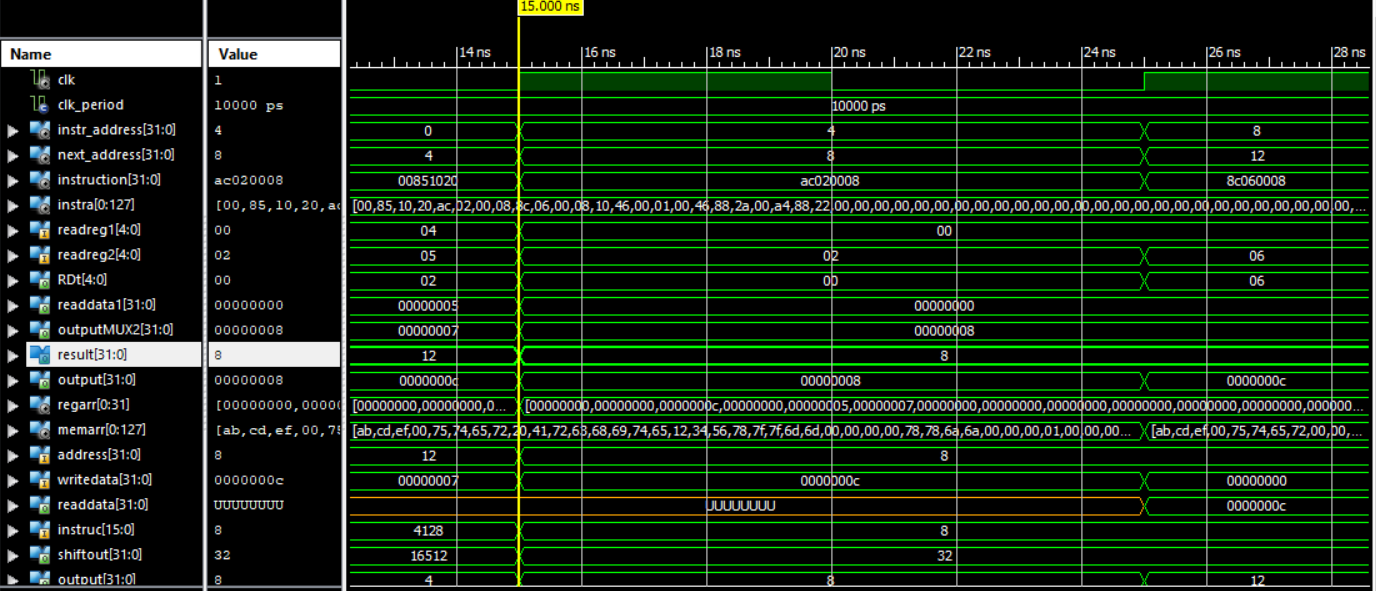
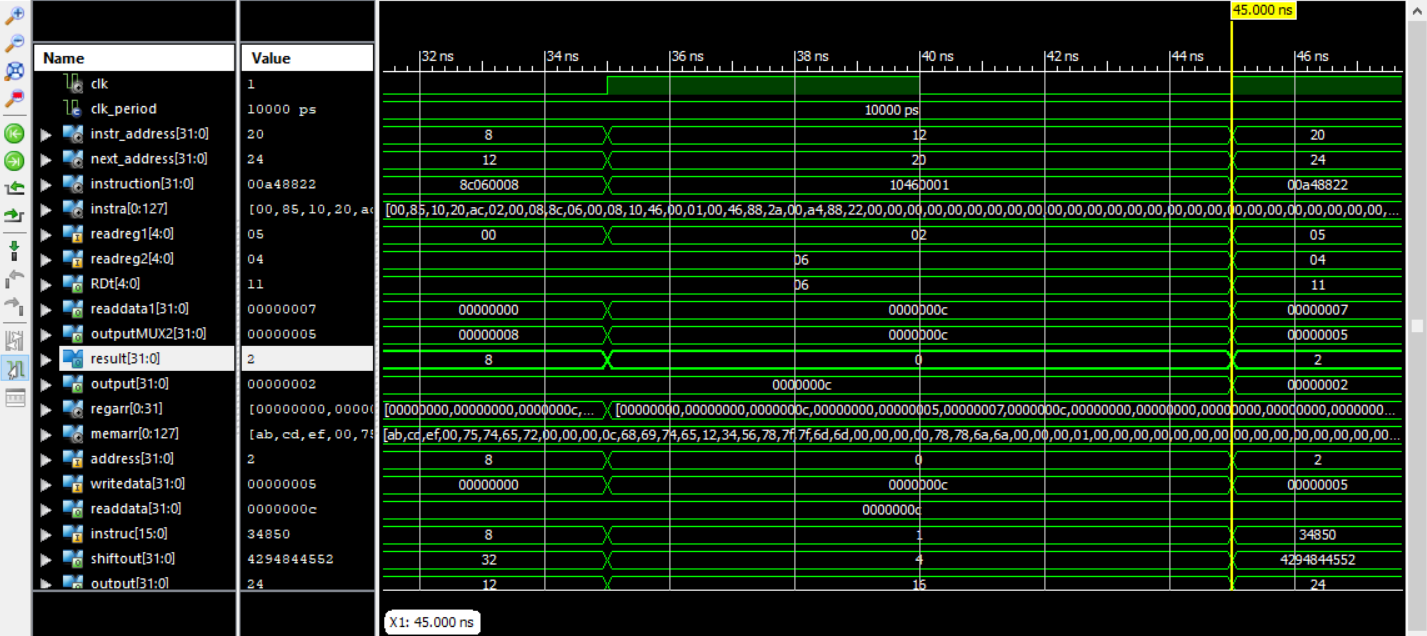
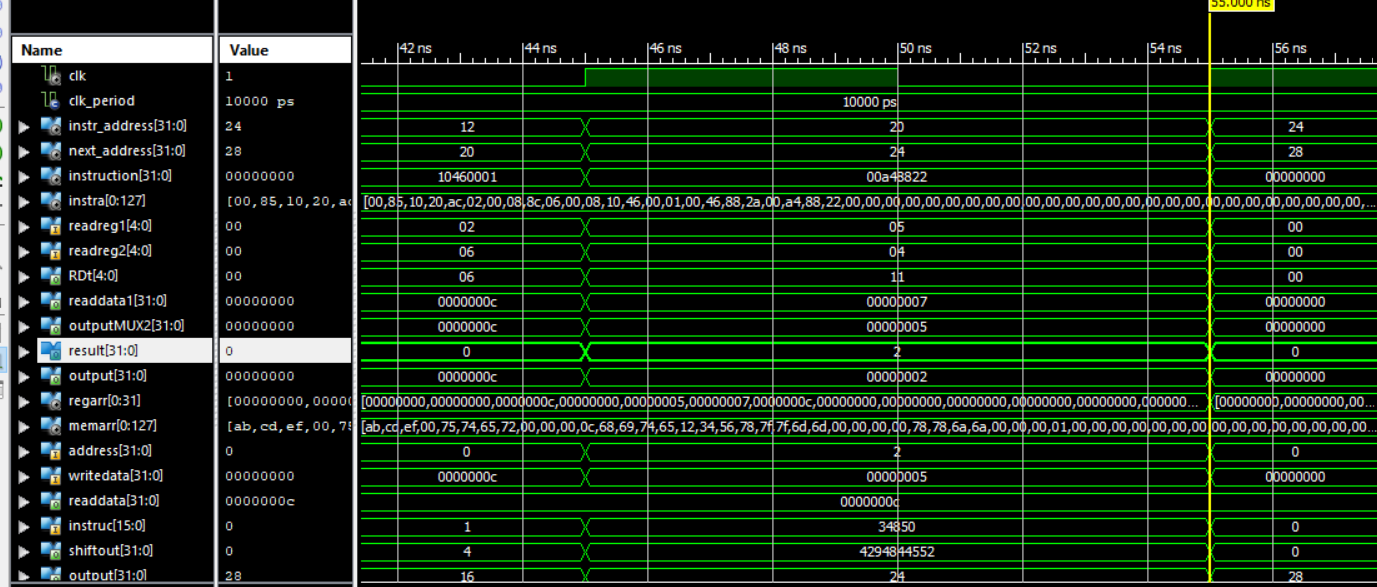
A screenshot of a computer

Description automatically generated







I added to mips processor components like: pc, pc adder, alu, alu control ,branch adder , data mem , shift left for the immediate and shift left for jump address 26 to 28 bits and muxes.

I added signals to connect each component with each others and then I port maped the component with signals.

In the first clk cycle the pc address is 0 which will be the instruction address and the next pc address will be 4 cause we use byte addressing , the fist instruction will be add $v0, $a0, $a1 at v0 is in reg array[2] and a0 is in reg array[4] and a1 in reg array[5] , operation code is 0 and funct is 20 hex, the alu control will be assigned as Regdst is 1 , jump 0, branch 0, memread 0 cause we won’t enter the data memory, mem to reg 0 cause we want the alu result, alu op is 10 which is add, mem write is 0 , alusrc 0 , reg write is 1 . now read data 1(rs) + read data2 (rt ) is 5+7=12 so rd = 12 or 0000000c hexa.

In the second clk cycle pc address is 4 which will be the instruction address and the next pc address will be 8, the second instruction is sw $v0, 8($zero) which will store add the immediate offset address to rs address which will be 8 and store it in the mem with the value of $v0 which has the value of 00000c hexa.

In the third clk cycle pc address is 8 which will be the instruction address and the next pc address will be 12, the third instruction is lw $a2, 8($zero) which is the longest instruction the immediate will be extended to be 32 bits instead of 16 bits and add the immediate address which the offset to rs address this will be the mem address , we will read from the mem address 8 and store the value to rt which is register rt[6] .

In the fourth clk cycle pc address is 12 which will be the instruction address , the fourth instruction is beq $v0, $a2, Good\_Processor , we will compare thee value of v0 and a2 if the value is equal the zero flag will be 1 , the immediate will be extended and shift left by 2 and added to pc +4 and this address will become the new pc address which is 20.

In the sixth clk cycle pc address is 20 which will be the instruction address and the next pc address will be 24 the last instruction is sub $s1, $a1, $a0 , we will subtract the value of a1 and a0 and store it in s1,

The value of a1 is 7 and value of a0 is 5 so $s1 value will become 2 and stored in reg array [17].