GPU implementation of a ray-surface intersection algorithm in CUDA (Compute Unified Device Architecture)

Raymond Leung

Australian Centre for Field Robotics Faculty of Engineering The University of Sydney

September 6, 2022

ABSTRACT

These notes accompany the open-source code published in GitHub which implements a GPU-based line-segment, surface-triangle intersection algorithm in CUDA. It mentions some relevant works and discusses issues specific to this implementation. The goal is to provide software documentation and greater clarity on collision buffer management which is sometimes omitted in online literature. For real-world applications, CPU-based implementations of the test are often deemed too slow to be useful. In contrast, the code described here targets Nvidia GPU devices and offers a solution that is vastly more efficient and scalable. The main API is also wrapped in Python. This geometry test is applied in various engineering problems, so the software developed can be reused in new situations. I

1 Motivation

The objective is to determine for each line segment $l_i = (\mathbf{r}_i^{\text{start}}, \mathbf{r}_i^{\text{end}})$ whether it crosses a user-supplied surface, given N_r rays, each described by start and end points $\mathbf{r}_i^{\text{start}} \in \mathbb{R}^3$ and $\mathbf{r}_i^{\text{end}} \in \mathbb{R}^3$, and a mesh surface that comprises N_t triangles, each described by a triplet $\mathbf{t}_j = [t_{j,1}, t_{j,2}, t_{j,3}]$ which references the three vertices $\mathbf{v}(\mathbf{t}_j) \equiv [\mathbf{v}_{t_{j,1}}, \mathbf{v}_{t_{j,2}}, \mathbf{v}_{t_{j,3}}]$ from the collection $\mathcal{V} = \{\mathbf{v}_n\}_{1 \leq n \leq N_v}$. The result is stored in a boolean array, $\mathbf{y} \in \{0,1\}^{N_r}$ by default. However, the program can be configured to return the intersecting point and triangle for each surface-intersecting ray. In the envisaged application, ray segments can point in arbitrary directions. Their starting points $\mathbf{r}_i^{\text{start}}$ may be all different. There is no requirement for the rays to originate from a single or multiple shared light sources.

The principal motivation for writing the ray-surface intersection test code in C++/CUDA is to harness the power of GPUs [5] and increase productivity in an R&D project that is geared towards geotechnical investigations / stratigraphic modelling. As such, achieving real-time rendering performance (e.g. 25 fps) is not the real goal, rather the goal is to surpass the speed of off-the-shelf CPU-based solutions, such as python's vtk and pyvista packages. For instance, the latter takes ~ 60 s to test 10M rays against a surface with approx. 30k triangles, even with OpenMP under the hood.² A reasonable goal is to reduce this duration by 10 to 100 fold. In general, GPU programming requires a different mindset and conceptual organisation; a good summary of its philosophy and applications can be found in [7].

¹The practical applications of the ray-surface intersection test are well understood in computer graphics. For instance, it is used to render photo-realistic objects in a scene [1] and evaluate user cursor interactions with a 3D terrain height map [2]. Apart from these examples, it is also used in spatial algorithms in geoscience, for instance, to label geological domains in orebody grade-block models [3]. Its reach extends to fabrication of nanoelectronic devices and 3D topography simulation for etching and deposition processes, where ray-surface intersection tests are used to model particle transport and surface evolution [4].

²OpenMP (Open Multi-Processing) is an application programming interface (API) that supports multi-platform shared-memory multiprocessing programming in C, C++, and Fortran, on many platforms, instruction-set architectures and operating systems, including Solaris, AIX, FreeBSD, HP-UX, Linux, macOS, and Windows. It consists of a set of compiler directives, library routines, and environment variables that influence run-time behavior (Wikipedia, 2022) [6].

2 Implementation

Our initial CUDA design choices were informed by findings reported by Jimenez et al. in [8] which influenced how the problem was partitioned and translated to CUDA architecture [9, 10]. In accordance, each grid (j) loads data pertaining to a single triangle (t_i) , the first thread in each thread-block computes shared attributes such as the edges of the triangle with a synchronisation barrier. The thread index (i) is mapped to a ray-segment $(l_{i+\lambda B})$, it cycles over multiplier $\lambda \in \mathbb{Z}$ until all rays have been considered, with stride B = 1024 being equal to the block size. Each thread is responsible for applying the Moller-Trumbore test to each triangle-ray $(i, i + \lambda B)$ combination. A number of algorithms—Badouel, Moller-Trumbore, Segura-Feito (tetrahedra sign test) and Jimenez et al. (barycentric coordinates of segment endpoint)—were considered in [11] and the study in [8] demonstrated that Moller-Trumbore [12] is the most efficient general-purpose algorithm for detecting ray-triangle intersections, requiring only 1 division, 4 dot-products and 2 vector-products in the worst case. Although not specifically mentioned by Jimenez, our initial implementation also included a naïve screening or culling step that checks for ray-triangle AABB (axis-aligned bounding box) overlap before the exact test is applied. A major conclusion in Jimenez's study [8] was that precalculating quantities is "typically counterproductive in the GPU environment" as the time required to compute these values may be smaller than the time required to fetch them from memory. In our experience, if the ray-segment bounding boxes were precomputed in the context of the bounding-box prescreening strategy, it increases the throughput roughly by 25%. In this preliminary implementation (v1), the cost is still significant even with the screening step, as it applies the overlap test to all $(N_t \times N_r)$ combinations. Nonetheless, it is faster than some of CPU-based alternatives. This is shown in Table 1 where speed is measured in million intersection tests per second (Mi/s) using an Nvidia GTX Titan X GPU.

	Time (s)	Speed (Mi/s)	GPU gain			
CPU-based solutions						
PyVista (ray_trace)	384.5	761.5	16.2×			
PyVista (multi_ray_trace) OpenMP with 8 logical processors	60.6	4832.5	$2.55 \times$			
VTK (obbTree.IntersectWithLine)	92.3	3171.3	$3.89 \times$			
Our preliminary GPU CUDA implementation						
Jimenez-like strategy (v1)	23.7	12340.5				
Reference GPU implementation						
Jimenez [8] Table 2 (original reported figure)	_	2742.0 [†]				
Jimenez [8] Table 2 (hardware adjusted)	_	9651.9 [‡]	$1.27 \times$			

Table 1: Timing comparison for the preliminary implementation

All this illustrates is that our preliminary CUDA implementation [13] and Jimenez' reference implementation achieve quite similar performance. To achieve more significant speedup, the screening step cannot be applied in a brute force manner to all possible ray-triangle pairs. Embedding location information about the triangles in a hierarchical structure is key to avoiding needless evaluations. Hence, our final implementation (version v2) makes use of more advanced data structures and performs tree search to eliminate possibilities of overlap. Online resources provide excellent practical guidance. Our approach is guided by Marcus [14] which in turn is based on Apetrei's fast, agglomerative approach [15] for building a linear bounding volume hierarchy (LBVH [16]). The idea is to construct a binary radix tree for a set of objects (viz., triangles on the mesh surface) which are sorted using morton codes. This allows the tree structure to be traversed in parallel by individual threads, each associated with a particular ray-segment. A common choice is to use the centroid of the triangle vertices, $\mathbf{c}_j = [\mathbf{v}_{t_{j,1}} + \mathbf{v}_{t_{j,2}} + \mathbf{v}_{t_{j,3}}]/3$, to represent the location of each triangle.

The first step is to compute the support intervals over $\{\mathbf{c}_j\}$. Then, each triangle centroid, $\mathbf{c}_j \in \mathbb{R}^3$, is quantised as $\mathbf{q}_j \in \mathbb{Z}^3$ to utilise the range effectively (with up to 2^{21} levels along the x, y and z axes). The quantised triangle coordinates, $[q_{j,x},q_{j,y},q_{j,z}]$, are subsequently bit-wise interleaved and converted into 64-bit long unsigned Morton code, \mathbf{z}_j . This has the effect that when all the codes (\mathbf{z}_j) are sorted, spatial locality will be preserved, which essentially means the triangles are grouped/clustered locally following a Z-curve scanning pattern [17] in 3D space. Once the triangles $\mathbf{q}_t \equiv Q(\mathbf{c}_t)$ are mapped to Morton codes \mathbf{z}_j , they are sorted to correspond to leaf nodes. The second step is to construct the binary radix tree (LBVH) by setting up left and right child node pointers for each parent in a bottom-up manner starting from the leaf nodes (each associated with an individual triangle). Apetrei [15] devised a single-pass procedure for propagating the index range and bounding box values from children to parents. This construction is implemented as GPU device code; for details, refer to the bvhConstruct kernel in "bvh_structure.h".

[†] Reported figure using GeForce GTX560Ti.

[‡] Adjusted figure using an estimated speedup factor of 3.52 assuming GTX Titan X is used today. Test surface contains 29,284 triangles, 1×10^7 (10 million) rays were used.

Once the LBVH is built, there needs to be a way for querying bounding-box overlap with individual line-segment bounding box using the triangle binary radix tree. The relevant structures for the latter are stored in two device memory arrays: internalNodes and leafNodes. On paper, the size of these are always $N_t - 1$ and N_t . However, it is convenient to actually store the *root node* as the left child of the last internal node (in internalNodes[$N_t - 1$]). This pointer is accessed as a shared variable in the relevent kernel launch (bvhIntersectionKernel) which provides the starting point for searching the tree. At the thread-block level, each thread executes the device code bvhFindCollisions(..., idx). This GPU code plays two major roles: a) it conducts efficient overlap feasibility testing using bvhTraverse (iterative tree search) to identify a small set of triangles capable of intersecting with each ray; b) it invokes the lib_rsi::checkRayTriangleIntersection function to verify if there is an actual crossing between the ray and surface. Pictures and further explanation of the BVH traversal function can be found in (Kerras, 2012) [18].

2.1 Program structure

The code repository contains four essential files.

- gpu_ray_surface_intersect.cu contains the main program which handles I/O, allocates host/device memory and launches the relevant kernels.
- bvh_structure.h implements the bounding volume hierarchy in the lib_bvh namespace. It defines __device__ functions and provides __global__ functions (such as bvhConstruct and bvhIntersectionKernel) used in main.
- rsi_geometry.h implements the Moller-Trumbore ray-triangle intersection algorithm (and associated algebraic operations) in the lib_rsi namespace. It provides the checkRayTriangleIntersection interface function used in lib_bvh::bvhFindCollisions.
- morton3D.h inherits some of the Morton code procedures written by Jeroen Baert which is distributed under an MIT license.

2.2 Compilation

The code is compiled using

/usr/local/cuda/bin/nvcc gpu_ray_surface_intersect.cu -o gpu_ray_surface_intersect

2.3 Standard usage

The basic command is

```
./gpu_ray_surface_intersect ${vertices_file} ${triangles_file} ${rayfrom_file} ${rayto_file}
```

If the input files are named "vertices_f32", "triangles_i32", "rayFrom_f32", "rayTo_f32" and located in ./input relative to the source directory, the last four command line arguments may be omitted.

To suppress terminal output, the string silent may be added as the 5th argument.

```
./\texttt{gpu\_ray\_surface\_intersect $\{vertices\} $\{triangles\} $\{rayfrom\} $\{rayto\} $ silent $$ for each $$ $\{triangles\} $\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $$ for each $$\{triangles\} $$ for each $$ for each $$\{triangles\} $
```

2.4 Extended usage

To return results in the form of (intersecting_rays, distances, intersecting_triangles, intersecting_points) in lieu of a crossing_detected binary array, the string barycentric is added as the 6th argument.

```
./gpu_ray_surface_intersect ${vertices} ${triangles} ${rayfrom} ${rayto} default barycentric
```

To return results in the form of (num ray surface intersecting points), use

```
./gpu_ray_surface_intersect ${vertices} ${triangles} ${rayfrom} ${rayto} default intercept_count
```

2.5 Required input

The input consists of four binary files in little-endian format.

- vertices contains $3 \times N_{\text{vertices}} \times \text{sizeof(float32)}$ bytes. The N_{vertices} surface vertices are arranged as $v_{1,x}, v_{1,y}, v_{1,z}, v_{2,x}, v_{2,y}, v_{2,z}, \dots$
- triangles contains $3 \times N_{\text{triangles}} \times \text{sizeof(int32)}$ bytes. The $N_{\text{triangles}}$ surface triangles are arranged as $t_{1,1}, t_{1,2}, t_{1,3}, t_{2,1}, t_{2,2}, t_{2,3}, \dots$

- rayFrom contains $3 \times N_{\rm rays} \times {\rm sizeof(float32)}$ bytes. The $N_{\rm rays}$ line-segment start points are arranged as $r_{1,x}^{\rm start}, r_{1,y}^{\rm start}, r_{1,z}^{\rm start}, r_{2,x}^{\rm start}, r_{2,z}^{\rm start}, \dots$
- ${\bf rayTo}$ contains $3 \times N_{\rm rays} \times {\it sizeof(float32)}$ bytes. The $N_{\rm rays}$ line-segment end points are arranged as $r_{1,x}^{\it end}, r_{1,y}^{\it end}, r_{1,z}^{\it end}, r_{2,x}^{\it end}, r_{2,z}^{\it end}, \ldots$

Sample input data may be generated using scripts/input_synthesis.py [13].

2.6 Python wrapper

For convenience, scripts/gpu_ray_surface_intersect.py implements a wrapper class PyGpuRSI that encapsulates the functionality of gpu_ray_surface_intersect.cu. The notebook scripts/demo.ipynb illustrates how this is used. Part A shows how the data manipulation, compilation, run and clean-up steps can be managed using a with statement. Part B shows how the program can be configured to return (intersecting_rays, distances, intersecting_triangles, intersecting_points) as python objects (numpy arrays) in reference to the extended usage described in Sec. 2.4. The notebook scripts/experimental_feature.ipynb contains an example in Part C where (num_intersecting_points) is returned instead. The odd parity test may be used to find ray starting points that lie inside a closed surface.

3 Discussion

In this section, we comment on specific aspects of the implementation that may seem a little obscure.

3.1 Bounding box and node definitions

The axis-aligned bounding box (AABB) and node are defined in rsi_geometry.h and bvh_structure.h, respectively.

```
struct AABB
{
    float xMin, xMax, yMin, yMax, zMin, zMax;
};

struct BVHNode
{
    AABB bounds;
    BVHNode *childLeft, *childRight;
    BVHNode *parent; *
    BVHNode *self; *
    int idxSelf, idxChildL, idxChildR, isLeafChildL, isLeafChildR; *
    int triangleID;
    int atomic;
    int rangeLeft, rangeRight;
};
```

Most of these fields are explained in Robbin Marcus' blog [14], thus there is no point repeating except in noting that attributes marked with \star are not strictly necessary. These are included for debugging purpose during development to verify that parent points correctly to the parent node and one of its children nodes points to the current node self, for example, when we trace and expand a portion of the tree using the testSimulateTreeExpansion function and examines its contents with testPrintNode. The reason for having the redundant variables idxSelf, idxChildL, idxChildR, isLeafChildL, isLeafChildR is to explicitly identify the array indices and knowing whether idxChild? refers to an element in the internalNodes or leafNodes. This is because the BVHNode pointers become invalid when the structure is copied from device to host memory, dereferencing them would lead to illegal memory access, so instead we use testDecipherDescendent to interpret idxChild? to find the corresponding address in host memory.

The attribute bounds obviously describes the spatial extent of the bounding box for triangles[triangleID] while [rangeLeft, rangeRight] describes the range covering the node indices of its descendants. In our implementation, an internal node is assigned a triangleID value of -1, the root node in particular is given a unique value of -2. All leaf nodes have non-negative values $0 \le \text{triangleID} < N_{\text{t}}$. The atomic variable is used during BVH construction (see bvhUpdateParent) to ensure the internal nodes only compute the bounds from their children bounding boxes when both children have been identified.

3.2 Bounding box collision detection

The non-trivial part of the implementation revolves around bvhFindCollisions and bvhInsert. Although there is an excellent description of stack pointers in [18] which also explains the thinking behind BVH tree traversal in GPU, details about the management of the collision list are somewhat lacking. Our intention here is to highlight one feasible approach and discuss this in practical terms. Conceptually, the TRAVERSE step begins by comparing the bounding box of a given ray-segment (henceforth denoted Ξ) with the bounds in the current node N_i . The process starts at the root node, and when an overlap occurs, the left and right child nodes are expanded. If Ξ intersects with the left child's bounding box, Ω_{L_i} , and the left child happens to be a leaf node, node $[L_i]$. triangleID is inserted into the collision buffer. Similarly, if Ξ intersects with the right child's bounding box, Ω_{R_i} which happens to be a leaf node, node $[R_i]$.triangleID is inserted into the collision buffer. This represents part 1 of 2 functions performed by bvhTraverse—refer to code between $\widehat{I} \to \mathrm{and} \leftarrow \widehat{I}$.

```
__device__ void bvhTraverse(const AABB& queryBox, NodePtr &bvhNode,
                            NodePtr* &stackPtr, CollisionList &hits)
    NodePtr node(bvhNode);
   bool bufferFull(false);
   do (1) \rightarrow
        //check each child node for overlap
        NodePtr childL = node->childLeft;
        NodePtr childR = node->childRight;
        bool overlapL = overlap(queryBox, childL);
        bool overlapR = overlap(queryBox, childR);
        //query overlaps a leaf node => report collision
        if (overlapL && isLeaf(childL))
            bufferFull = bvhInsert(hits, childL->triangleID); *
        if (overlapR && isLeaf(childR))
            bufferFull \mid= bvhInsert(hits, childR->triangleID); \leftarrow(1)
        //query overlaps an internal node \Rightarrow traverse (2) \rightarrow
        bool traverseL = (overlapL && !isLeaf(childL));
        bool traverseR = (overlapR && !isLeaf(childR));
        if (!traverseL && !traverseR)
            node = *--stackPtr; //pop
        else
            node = (traverseL) ? childL : childR;
            if (traverseL && traverseR)
                 *stackPtr++ = childR; //push
        } ←(2)
    while (node != NULL && !bufferFull);
    bvhNode = node;
```

The problem is that STL containers and adaptors (such as std::vector and std::stack|queue) cannot be used in device or kernel code as they lie outside the scope of a device function. Although it is possible to allocate memory dynamically and adjust the amount of device memory available for the heap using CUDA runtime APIs, this would be painfully slow if each thread allocates its own memory dynamically and memory is not coalesced. Thus, the collision buffer really needs to be statically allocated using cudaMalloc. Effectively, access to the relevant portion of the collision buffer is compartmentalised for each individual thread. The buffer size is finite and fixed. For instance, in the following listing, MAX_COLLISION may be set to 32, say. Since there is no telling how many triangle bounding boxes would overlap with a given ray-segment, there needs to be a way to manage this triangleID INSERT operation to prevent array overrun. This is accomplished with byhInsert which returns true when the hits buffer occupancy is nearing capacity. The ray-specific collision buffer occupancy state is reflected by the bufferFull thread-local variable

```
struct CollisionList
{
    uint32_t hits[MAX_COLLISIONS];
    int count;
};
__device__ bool inline bvhInsert(CollisionList &collisions, int value)
{
    //insert value into the hits[] array. Returned value indicates
    //if buffer is full (true => not enough room for two elements).
    collisions.hits[collisions.count++] = static_cast < uint32_t > (value);
    return (collisions.count < MAX_COLLISIONS - 1)? false : true;
}</pre>
```

In the next listing, we see that bvhTraverse is wrapped in the device function bvhFindCollisions which performs two critical roles. First, it performs broad-based ray-triangle bounding box collision detection. Second, it performs the Moller-Trumbore check (an exact intersection test) on viable candidates (a small subset of triangles) for which a ray-triangle crossing is possible. The code in ③ initialises the stackPtr array and sets up the bvhRoot as the first node to visit. This is consistent with the description in [18]. Where it differs, or perhaps just some design choices specific to our implementation, is the coupling with checkRayTriangleIntersection in ④ instead of running coarse and fine-grained checks in separate stages. It applies the Moller-Trumbore test to the thread-specific ray-segment and a set of triangle candidates reported in the collisions list. If this list contains all potential collision candidates (the entire subset of triangles to test for), all is good. In the event the collisions buffer is full and there are more BVH nodes remaining to check, the nextNode returned will not be NULL; this means the do-while loop will continue unless a ray-triangle intersection has already been found by the Moller test. Another important observation is the internal state (or stack content) will persist in memory if the bvhTraverse function is called a second time within the do-while loop. As should be obvious, the ray-surface intersection result is affirmed in (written to) detected[rayIdx].

```
__device__ void bvhFindCollisions(const float* vertices,
                                   const int* triangles,
                                   const float* rayFrom,
                                   const float* rayTo,
                                    const AABB* rayBox,
                                   const NodePtr bvhRoot,
                                   CollisionList &collisions,
                                   int* detected,
                                   int rayIdx)
   //argument 'collisions' provides access to a thread-local
   //portion of device memory that holds the collisions array.
   //allocate traversal stack from thread-local memory,
    //push NULL to indicate that there are no postponed nodes.
   (3)\rightarrow
   NodePtr stack[MAX_STACK_PTRS];
   NodePtr* stackPtr = stack;
   *stackPtr++ = NULL;
   NodePtr nextNode(bvhRoot);
   ←(3)
   (4)\rightarrow
        collisions.count = 0;
        bvhTraverse(rayBox[rayIdx], nextNode, stackPtr, collisions);
        //check for actual intersections with the triangles found so far
```

³The stack pointer "queue" is actually a static array with known dimension at compile time.

To give an indication of the time cost associated with BVH construction in GPU, the following table shows the cumulative time as each step of the process is added. Overall, it is quite inexpensive for a test surface with about 29k triangles.

Incremental steps	Elpased time (ms)
rbxKernel (compute ray bounding boxes)	4.32
+ discretisation / normalisation of triangle coordinates	5.47
+ create Morton code for triangles	7.75
+ sort Morton code for triangles	24.23
+ bvhResetKernel (initialise BVH and leaf nodes)	24.62
+ byhConstruct (update parent nodes, create binary radix tree)	24.94

Table 2: Timing associated with triangle BVH construction

3.3 The byhIntersect kernel

Putting everything together, the bvhFindCollisions device code is launched through the bvhIntersectKernel. The bvhRoot represents a shared attribute that is initialised by the first thread (within a thread-block) with barrier synchronisation. Akin to version 1 of our implementation, each thread (i) iterates over the rays with a stride of $i+\operatorname{gridDim}\times B$ where B=1024 is the typical size of a thread-block, and $0\leq\operatorname{gridDim}< N_{\operatorname{grid}}$.

```
__global__ void bvhIntersectionKernel(const float* __restrict__ vertices, const int* __restrict__ triangles,
                                        const float* __restrict__ rayFrom,
                                        const float* __restrict__ rayTo,
                                        const BVHNode* __restrict__ internalNodes,
                                        const AABB* __restrict__ rayBox,
                                        CollisionList* __restrict__ raytriBoxHitIDs,
                                        int* __restrict__ detected,
                                        int numTriangles, int numRays)
   //load BVH root node into shared memory
    __shared__ NodePtr bvhRoot;
    __shared__ int stride;
    if (threadIdx.x == 0) {
        bvhRoot = internalNodes[numTriangles-1].childLeft;
        stride = gridDim.x * blockDim.x;
    __syncthreads();
   int threadStartIdx = blockIdx.x * blockDim.x + threadIdx.x;
   int bufferIdx = threadStartIdx;
                                       (*)
    //iterate if numRays exceeds dimension of thread-block
   for (int idx = threadStartIdx; idx < numRays; idx += stride) {</pre>
        if (idx < numRays) {</pre>
            //access thread-specific collision array
            CollisionList &collisions = raytriBoxHitIDs[bufferIdx];
            bvhFindCollisions(vertices, triangles, rayFrom, rayTo, rayBox,
                               bvhRoot, collisions, detected, idx);
```

```
}
}
```

Two grid-size configurations, $N_{grid} \in \{1, 16\}$, were considered. This requires device memory allocation as follows.

```
CollisionList *d_hitIDs;
cudaMalloc(&d_hitIDs, nGrids * threadBlockSize * sizeof(CollisionList));
```

Essentially, it comes down to a memory and speed trade-off. As the timing measurements show, $N_{\rm grid}=1$, results in a $4.7\times$ improvement relative to version v1. However, with $N_{\rm grid}=16$, it results in a $51\times$ improvement relative to v1—this emphasizes the importance of incorporating an accelerating (tree) structure. It exploits the fact that multiple blocks can be run concurrently on a streaming multiprocessor. For each thread within a given grid-block, the bufferIdx in line * is key to stepping correctly into the dedicated portion of device memory that registers collision. Note: the threadStartIdx incorporates the stride, a grid-block specific offset into the rays.

4 Indicative Results

4.1 Processing time

Table 3: Timing comparison for the final implementation

	Time (s)	Speed (Mi/s)	GPU/CPU gain	Change (vs ‡)	
CPU-based solutions					
PyVista (multi_ray_trace) with OpenMP	60.6	4832.5★	1×	_	
PyVista (ray_trace)	384.5	761.5	$0.15 \times$	_	
VTK (obbTree.IntersectWithLine)	92.3	3171.3	$0.656 \times$	_	
Our GPU CUDA implementation					
Jimenez-like strategy (v1)	23.729	12340.5	$2.5 \times$	‡	
- with BVH, $N_{\text{grid}} = 1 \text{ (v2.0)}$	5.022	58978.1	$12\times$	$4.7 \times$	
- with BVH, $N_{\text{grid}} = 16$ (v2.1) preferred	0.463	632071.5	130×	$51 \times$	
- with BVH, sorted rays and $N_{\rm grid} = 16$ (v2.2)	0.228	1284357.7	$265 \times$	$104 \times$	

In terms of speed, the adopted implementation (v2.1) is $130 \times$ faster on a GeForce GTX Titan X GPU than the best CPU-based solution which uses PyVista's multi_ray_trace method. The difference is stark, it completes in 463ms compared with >60s. Furthermore, the rays used for our testing have been randomised. If the rays were first sorted using Morton code, execution divergence can be minimised and the compute time can be halved to about 228ms. However, there is a substantial cost associated with sorting 10M rays. So, one feasible use case would be to sort these rays once and evaluate against multiple surfaces if the line segments remain fixed throughout an experiment.

4.2 Memory use

The figures on page 9 show memory usage on the GeForce GTX Titan X GPU device when the program is run. Apart from minor formatting, this output was produced by /usr/local/cuda/bin/nvprof --print-gpu-trace ./gpu_ray_surface_intersect. The main observation is that bvhIntersectionKernel uses 40 registers per thread (a total of 40960 per block) which is less than the 65536 registers available (see Appendix A.1). This kernel uses 12 bytes of static shared memory per block which is tiny compared to the 49152 bytes available. In terms of device global memory, it uses 267.8 MB in the test case which is about 2% of the 12GB available.

Operation Start Duratio				SSMem I	OSMem	Size	Throughput	Src/DstMem
[CUDA	ــــــــــــــــــــــــــــــــــــــ	:	-====:	======	-====	=======		
[CUDA memset] 238.94 ms 153.35		ingDetecte	a			29 147MD	242.93GB/s	Day/
[CUDA memcpy HtoD]			_		_	36.14/NID	242.930b/ 8	Dev/ -
239.13 ms 17.088		ces				175.38KB	9.7880GB/s	Da / Day
[CUDA memcpy HtoD]		oles –	_	_	_	1/3.36KD	9.7000CD78	rg/Dev
239.23 ms 30.497			_		_	343 17KB	10.731GB/s	Pg / Dev
[CUDA memcpy HtoD]		o.m				343.17 KB	10.731GD/3	1 g/ DCV
239.50ms 23.796			_		_	114 44MB	4.6965GB/s	Pg/Dev
[CUDA memcpy HtoD]						111.11.11	1.0702 GB/ 5	18/201
263.44 ms 22.907		_	_		_	114.44MB	4.8788GB/s	Pg/Dev
[kernel code]	lib rsi	::rbxKerne	el					- 8,
286.39ms 4.2089				7 OB	0B	_	_	-/-
[CUDA memcpy HtoD]								
310.83 ms 21.793			-		_	228.78KB	10.012GB/s	Pg/Dev
[CUDA memcpy HtoD]	d_sorte	dTriangleI	Ds					
310.87ms 11.328	us -		-		_	114.39KB	9.6302GB/s	Pg/Dev
[kernel code]	[kernel code] lib_bvh::bvhResetKernel							
310.89ms 83.682	us (29	(1024,)	26	6 0B	0B	_	_	-/-
[kernel code]	bvhCon	structKerne	el					
310.98 ms 207.94					0B	_	_	-/-
[kernel code]								
311.20ms 489.58		6,) (1024,)) 12B	0B	_	_	-/-
[CUDA memcpy DtoH]		ingDetecte	d					
800.81 ms 3.2842	ms -	-	-		_	38.147MB	11.343GB/s	Dev/Pg
Regs: Number of registers used per CUDA thread. This number includes registers used internally by the CUDA driver/tools and can be more than what the compiler shows SSMem: Static shared memory allocated per CUDA block. DSMem: Dynamic shared memory allocated per CUDA block.								
Src/DestMem: The type of source/destination memory accessed by memory operation/copy Abbreviations: Pg=Pageable, Dev=Device								

A Appendix: System/device properties

A.1 GPU specification

```
CUDA Device Query (Runtime API) version (CUDART static linking)
Detected 1 CUDA Capable device(s)
Device O: "GeForce GTX TITAN X"
  CUDA Driver Version / Runtime Version
                                                   11.2 / 11.2
  CUDA Capability Major/Minor version number:
  Total amount of global memory:
                                                   12213 MBytes (12806062080 bytes)
  (24) Multiprocessors, (128) CUDA Cores/MP:
                                                   3072 CUDA Cores
  GPU Max Clock rate:
                                                   1076 MHz (1.08 GHz)
  Memory Clock rate:
                                                   3505 Mhz
  Memory Bus Width:
                                                   384-bit
  L2 Cache Size:
                                                   3145728 bytes
  Maximum Texture Dimension Size (x,y,z)
                                                   1D = (65536), 2D = (65536, 65536),
                                                   3D = (4096, 4096, 4096)
  Maximum Layered 1D Texture Size, (num) layers
                                                   1D = (16384), 2048  layers
  Maximum Layered 2D Texture Size, (num) layers
                                                   2D=(16384, 16384), 2048 layers
  Total amount of constant memory:
                                                   65536 bytes
  Total amount of shared memory per block:
                                                   49152 bytes
  Total number of registers available per block: 65536
  Warp size:
  Maximum number of threads per multiprocessor:
                                                   2048
  Maximum number of threads per block:
                                                   1024
  Max dimension size of a thread block (x,y,z): (1024, 1024, 64)
  Max dimension size of a grid size
                                        (x,y,z): (2147483647, 65535, 65535)
  Maximum memory pitch:
                                                   2147483647 bytes
                                                   512 bytes
  Texture alignment:
  Concurrent copy and kernel execution:
                                                   Yes with 2 copy engine(s)
  Run time limit on kernels:
  Integrated GPU sharing Host Memory:
  Support host page-locked memory mapping:
                                                   Yes
  Alignment requirement for Surfaces:
                                                   Yes
  Device has ECC support:
                                                   Disabled
  Device supports Unified Addressing (UVA):
                                                   Yes
  Device PCI Domain ID / Bus ID / location ID:
                                                   0 / 2 / 0
  Compute Mode:
     < Default (multiple host threads can use ::cudaSetDevice() with device simultaneously) >
deviceQuery, CUDA Driver = CUDART, CUDA Driver Version = 11.2,
CUDA Runtime Version = 11.2, NumDevs = 1, DeviceO = GeForce GTX TITAN X
Result = PASS
NVIDIA-SMI driver version is 460.27.04.
```

A.2 Host machine

Linux OS (RedHat 7.9 x86_64) with 16x Intel[®] Xeon[®] Platinum 8259CL CPU @ 2.50GHz. Experiments with PyVista and VTK were run on a Windows machine with Intel[®] CoreTM i7-8665U CPU @ 1.90GHz, 4 cores/8 logical processors and 32 GB RAM.

B Source code

The open-source code is distributed under the BSD 3-clause license and is available at https://github.com/raymondleung8/gpu-ray-surface-intersection-in-cuda [13].

Acknowledgements

This work is supported by the Australian Centre for Field Robotics and the Rio Tinto Centre for Mine Automation.

References

- [1] Matt Pharr, Wenzel Jakob, and Greg Humphreys. *Physically based rendering: From theory to implementation*. Morgan Kaufmann, 2016.
- [2] Tim Sjöstrand. Efficient intersection of terrain geometry in real-time applications. B.Eng. Thesis, University of Gothenburg, 2017.
- [3] Raymond Leung. Modelling orebody structures: Block merging algorithms and block model spatial restructuring strategies given mesh surfaces of geological boundaries. Available at: https://doi.org/10.5311/JOSIS. 2020.21.582. *Journal of Spatial Information Science*, 21:137–174, 2020.
- [4] Paul Ludwig Manstetten. Ray-surface intersection tests for particle transport. In *Efficient Flux Calculations for Topography Simulation*. PhD Thesis. Technischen Universität Wien, 2018.
- [5] André R Brodtkorb, Trond R Hagen, and Martin L Sætra. Graphics processing unit (GPU) programming strategies and trends in GPU computing. *Journal of Parallel and Distributed Computing*, 73(1):4–13, 2013.
- [6] Wikipedia. OpenMP. URL https://en.wikipedia.org/wiki/OpenMP.
- [7] John D Owens, Mike Houston, David Luebke, Simon Green, John E Stone, and James C Phillips. GPU computing. *Proceedings of the IEEE*, 96(5):879–899, 2008.
- [8] Juan J Jiménez, Carlos J Ogáyar, José M Noguera, and Félix Paulano. Performance analysis for GPU-based ray-triangle algorithms. In 2014 International Conference on Computer Graphics Theory and Applications (GRAPP), pages 1–8. IEEE, 2014.
- [9] Danilo De Donno, Alessandra Esposito, Luciano Tarricone, and Luca Catarinucci. Introduction to GPU computing and CUDA programming: A case study on FDTD [EM programmer's notebook]. *IEEE Antennas and Propagation Magazine*, 52(3):116–122, 2010.
- [10] David B Kirk and W Hwu Wen-Mei. *Programming Massively Parallel Processors: A Hands-on Approach*. Morgan Kaufmann, 2016.
- [11] Juan J Jiménez, Rafael J Segura, and Francisco R Feito. A robust segment/triangle intersection algorithm for interference tests. Efficiency study. *Computational Geometry*, 43(5):474–492, 2010.
- [12] Tomas Möller and Ben Trumbore. Fast, minimum storage ray-triangle intersection. *Journal of Graphics Tools*, 2(1):21–28, 1997.
- [13] Raymond Leung. GPU implementation of a ray-surface intersection algorithm in CUDA. Source code available at https://github.com/raymondleung8/gpu-ray-surface-intersection-in-cuda under the bsd 3-clause license.
- [14] Robbin Marcus. Real-time raytracing part 2.1. Published on 2015-10-29. Available at http://robbinmarcus.blogspot.com/2015/12/real-time-raytracing-part-21.html.
- [15] Ciprian Apetrei. Fast and simple agglomerative LBVH construction. In Rita Borgo and Wen Tang, editors, EG UK Computer Graphics & Visual Computing. The Eurographics Association. Available at: http://diglib.eg.org/bitstream/handle/10.2312/cgvc.20141206.041-044/041-044. pdf?sequence=1&isAllowed=y, 2014.
- [16] Wikipedia. Bounding volume hierarchy. URL https://en.wikipedia.org/wiki/Bounding_volume_hierarchy.
- [17] Wikipedia. Z-order (Lebesgue, Morton space filling) curve. URL https://en.wikipedia.org/wiki/Z-order_curve.
- [18] Tero Kerras. Thinking Parallel, Part II: Tree Traversal on the GPU. Published on 2012-11-26. Available at https://developer.nvidia.com/blog/thinking-parallel-part-ii-tree-traversal-gpu.