CHAPTER 13

Lithography and Etching

Lithography is the process of transferring patterns of geometric shapes on a mask to a thin layer of radiation-sensitive material (called resist) covering the surface of a semiconductor wafer.[1] These patterns define the various regions in an integrated circuit such as the implantation regions, the contact windows, and the bonding-pad areas. The resist patterns defined by the lithographic process are not permanent elements of the final device but only replicas of circuit features. To produce circuit features, these resist patterns must be transferred once more into the underlying layers comprising the device. The pattern transfer is accomplished by an etching process that selectively removes unmasked portions of a layer.[2]

Specifically, we cover the following topics:

- The importance of a clean room for lithography.
- The most widely used lithographic method —optical lithography and its esolution-enhancement techniques.
- Advantages and limitations of other lithographic methods.
- Mechanisms for wet chemical etching of semiconductors, insulators, and metal films.
- Dry etching (also called plasma-assisted etching) for high-fidelity pattern transfer.

13.1 OPTICAL LITHOGRAPHY

The vast majority of lithographic equipment for integrated-circuit (IC) fabrication is optical equipment using ultraviolet light ($\lambda \cong$ 0.2–0.4 μm). In this section we consider the exposure tools, the masks, the resists, and resolution-enhancement techniques used for optical lithography. We also consider the pattern transfer process, which serves as a basis for other lithographic systems. We first briefly consider the *clean room*, because all lithographic processes must be performed in an ultraclean environment.

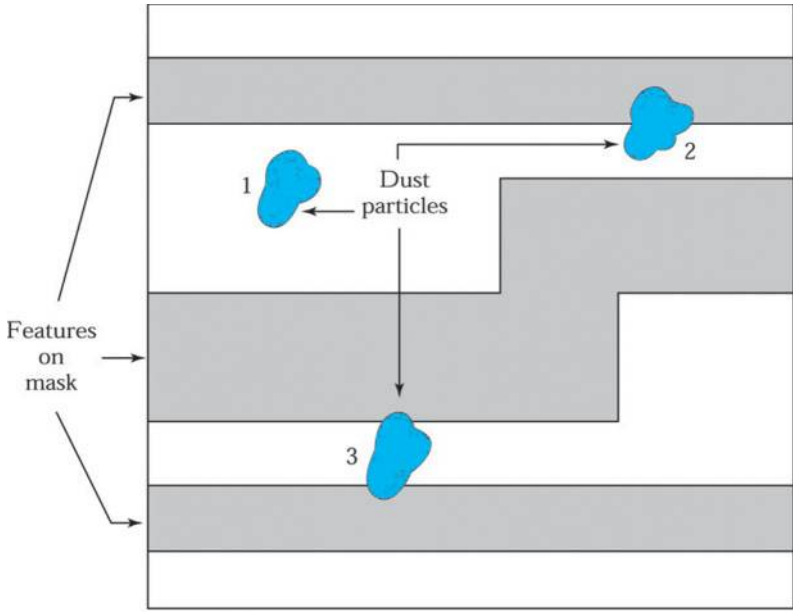

Fig. 1 **Various ways in which dust particles can interfere with photomask patterns.**[3]

13.1.1 The Clean Room

An IC fabrication facility requires a clean processing room, especially in the area used for lithography. The need for such a clean room arises because dust particles in the air can settle on semiconductor wafers and lithographic masks and can cause defects in the devices and hence circuit failure. For example, a dust particle on a semiconductor surface can disrupt the single-crystal growth of an epitaxial film, causing the formation of dislocations. A dust particle incorporated into the gate oxide can result in enhanced conductivity and cause device failure due to low breakdown voltage. The situation is even more critical in the lithographic area. When dust particles adhere to the surface of a photomask, they behave as opaque patterns on the mask, and these patterns will be transferred to the underlying layer along with the circuit patterns on the mask. Figure 1 shows three dust particles on a photomask.[3] Particle 1 may result in the formation of a pinhole in the underlying layer. Particle 2 is located near a pattern edge and may cause a constriction of current flow in a metal runner. Particle 3 can lead to a short circuit between the two conducting regions and render the circuit useless.

In a clean room, the total number of dust particles per unit volume must be tightly controlled along with the temperature and humidity. Figure 2 shows the particle-size distribution curves for various *classes* of clean rooms. We have two systems to define the classes of clean room.[4] In the English system, the numerical designation of the class is taken from the maximum allowable number of particles 0.5 μm and larger, per *cubic foot*. For the metric system, the class is taken from the logarithm (base 10) of the maximum allowable number of particles 0.5 μm and larger, per *cubic meter*. For example, a class 100 clean room (English system) has a dust count of 100 particles/ft^3 with particle diameters of 0.5 μm and larger, whereas a class M 3.5 clean room (metric system) has a dust count of $10^{3.5}$ or about 3500 particles/m^3 with particle diameters of 0.5 μm and larger. Since 100 particles/ft^3 = 3500 particles/m^3, a class 100 in English system corresponds to a class M 3.5 in the metric system.

For most IC fabrication areas, a class 100 clean room is required, that is, the dust count must be about four orders of magnitude below that of ordinary room air. However, for the lithography area, a class 10 clean room or one with a lower dust count is required.

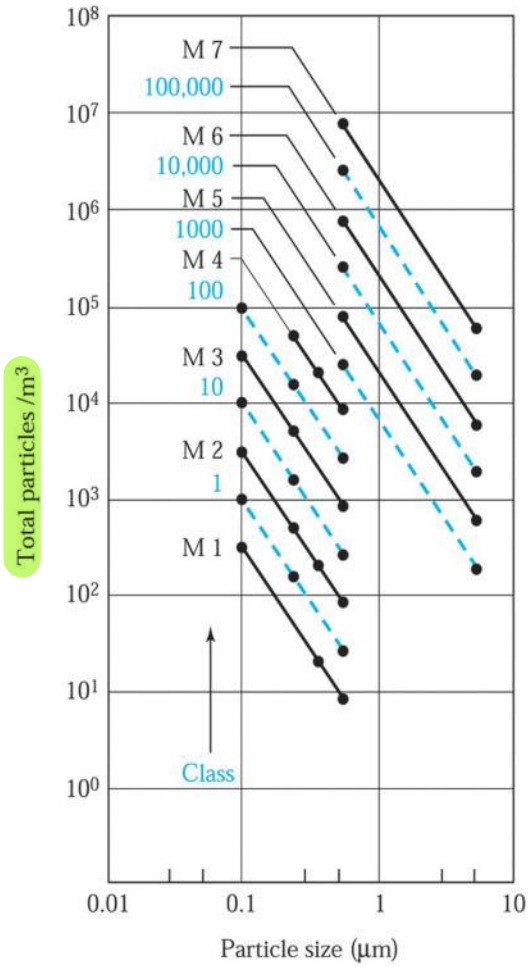

Fig. 2 **Particle-size distribution curve for English (- - -) and metric (—) classes of clean rooms.**[4]

▶ EXAMPLE 1

If we expose a 300-mm wafer for 1 minute to an air stream under a laminar-flow condition at 30 m/min, how many dust particles will land on the wafer in a class-10 clean room?

SOLUTION For a class 10 clean room, there are 350 particles (0.5 μm and larger) per cubic meter. The air volume that goes over the wafer in 1 minute is

$$30 \text{ m/min} \times \pi \left(\frac{0.3 \text{ m}}{2} \right)^2 \times 1 \text{ minute} = 2.12 \text{ m}^3.$$

The number of dust particles (0.5 μm and larger) contained in the air volume is 350 × 2.12 = 742 particles. Therefore, if there are 800 IC chips on the wafer, the particle count amounts to one particle on each of 92% of the chips. Fortunately, only a fraction of the particles that land adhere to the wafer surface, and of those only a fraction are at a circuit location critical enough to cause a failure. However, the calculation indicates the importance of the clean room. ◀

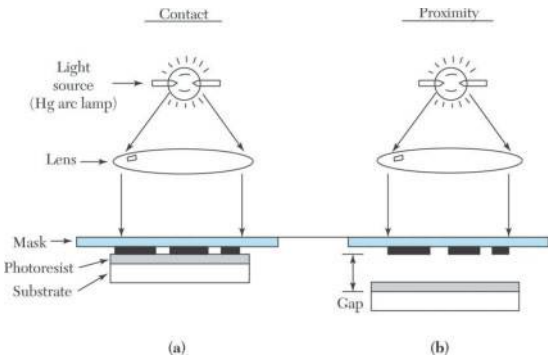

Fig. 3 **Schematic of optical shadow printing techniques:[1] (*a*) contact printing, (*b*) proximity printing.**

13.1.2 Exposure Equipment

The pattern transfer process is accomplished by using lithographic exposure equipment. The performance of exposure equipment is determined by three parameters: resolution, registration, and throughput. *Resolution* is the minimum feature dimension that can be transferred with high fidelity to a resist film on a semiconductor wafer. *Registration* is a measure of how accurately patterns on successive masks can be aligned (or overlaid) on previously defined patterns on the wafer. *Throughput* is the number of wafers that can be exposed per hour for a given mask level.

There are basically two optical exposure methods: shadow printing and projection printing.[5,6] Shadow printing may have the mask and wafer in direct contact with each other as in *contact printing*, or in close proximity as in *proximity printing*. Figure 3*a* shows a basic setup for contact printing where a resist-coated wafer is brought into physical contact with a mask, and the resist is exposed by a nearly collimated beam of ultraviolet light through the back of the mask for a fixed time. The intimate contact between resists and mask provides a resolution of ~1 μm. However, contact printing suffers a major drawback caused by dust particles. A dust particle or a speck of silicon dust on the wafer can be imbedded into the mask when the mask makes contact with the wafer. The imbedded particle causes permanent damage to the mask and results in defects in the wafer with each succeeding exposure.

To minimize mask damage, the proximity exposure method is used. Figure 3*b* shows the basic setup. It is similar to the contact printing method except that there is a small gap (10–50 μm) between the wafer and the mask during exposure. The small gap results in optical diffraction at feature edges on the photomask: that is, when light passes by the edges of an opaque mask feature, fringes are formed and some light penetrates into the shadow region. As a result, the resolution is degraded to the 2–5 μm range.

In shadow printing, the minimum linewidth [or critical dimension (CD)] that can be printed is roughly

$$\boxed{\mathrm{CD} \cong \sqrt{\lambda g},} \tag{1}$$

where λ is the wavelength of the exposure radiation and g is the gap between the mask and wafer and includes the thickness of the resist. For $\lambda = 0.4$ μm and $g = 50$ μm, the CD is 4.5 μm. If we reduce λ to 0.25 μm (the wavelength range of 0.2–0.3 μm is in the deep-UV spectral region) and g to 15 μm, CD becomes 2 μm. Thus, there is an advantage in reducing both λ and g. However, for a given distance g, any dust particle with a diameter larger than g can potentially cause mask damage.

To avoid the mask damage problem associated with shadow printing, projection-printing exposure equipment has been developed to project an image of the mask patterns onto a resist-coated wafer many centimeters away from the mask. To increase resolution, only a small portion of the mask is exposed at a time, allowing a uniform source of light. The small image area is scanned or stepped over the wafer to cover the entire wafer surface. Figure 4*a* shows a 1:1 wafer scan projection system.[6,7] A narrow, arc-shaped image field ~1 mm in width serially transfers the slit image of the mask onto the wafer. The image size on the wafer is the same as on the mask.

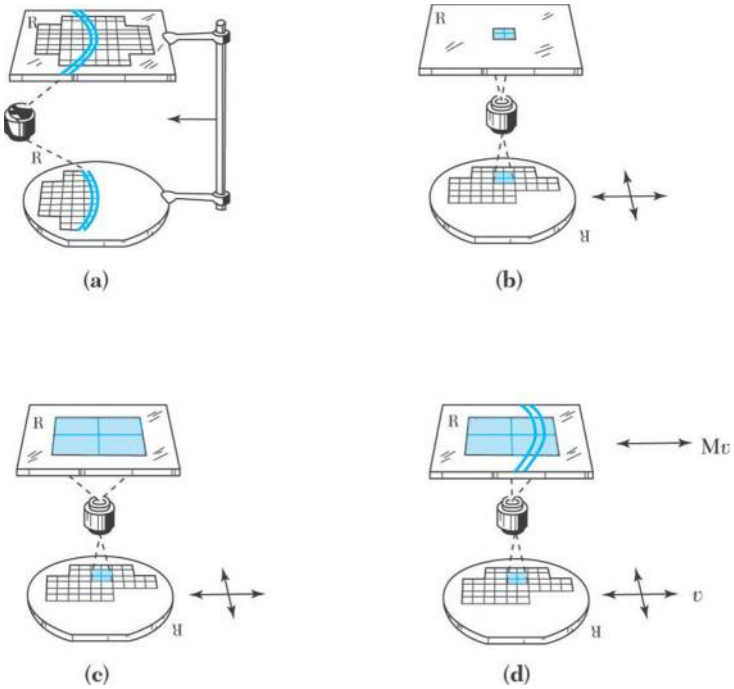

Fig. 4 **Image-partitioning techniques for projection printing: (*a*) annual-field wafer scan, (*b*) 1:1 step-and-repeat, (*c*) *M*:1 reduction step-and repeat, and (*d*) *M*:1 reduction step-and-scan.**[6,7]

The small image field can also be stepped over the surface of the wafer by two-dimensional translations of the wafer only, while the mask remains stationary. After the exposure of one chip site, the wafer is moved to the next chip site and the process is repeated. Figure 4*b* and 4*c* show the partitioning of the wafer image by *step-and-repeat projection* with a ratio of 1:1 or at a demagnification ratio *M*:1 (e.g., 10:1 for a 10 times reduction on the wafer), respectively. The demagnification ratio is an important factor in our ability to produce both the lens and the mask from which we wish to print. The 1:1 optical systems are easier to design and fabricate than 10:1 or 5:1 reduction systems, but it is much more difficult to produce defect-free masks at 1:1 than at a 10:1 or a 5:1 demagnification ratio.

Reduction projection lithography can also print larger wafers without redesigning the stepper lens as long as the field size (i.e., the exposure area onto the wafer per se) of the lens is large enough to contain one or more IC chips. When the chip size exceeds the field size of the lens, further partitioning of the image on the mask is necessary. In Fig. 4*d* the image field on the mask can be a narrow, arc-shaped for *M*:1 step-and-scan projection lithography. For the step-and-scan system, we have two-dimensional translations of the wafer with speed v, and one-dimensional translation of the mask with *M* times that of the wafer speed.

The resolution of a projection system l_m is usually determined by the quality of the lens, but is ultimately limited by diffraction and given by

$$l_m = k_1 \frac{\lambda}{\text{NA}}, \tag{2}$$

where λ is again the exposure wavelength, k_1 is a process-dependent factor, and NA is the numerical aperture, which is given by

$$\text{NA} = \bar{n} \sin\theta = \bar{n} \sin(\tan^{-1} D/2f) \approx \bar{n}\,(D/2f) \tag{3}$$

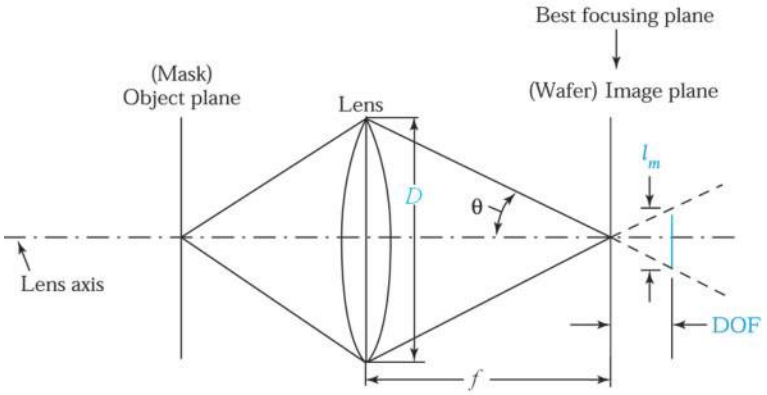

Fig. 5 **Simple image system.**[5]

with $\bar{n}$ the index of refraction in the image medium (usually air, where $\bar{n} = 1$), θ the half-angle of the cone of light converging to a point image at the wafer, D the diameter of the lens and f the focal length, as shown[5] in Fig. 5. Hence the numerical aperture of an optical system is a dimensionless number that characterizes the range of angles over which the system can accept or emit light. Also shown in the figure is the depth of focus (DOF), which can be expressed as

$$\text{DOF} = \frac{\pm l_m / 2}{\tan\theta} \approx \frac{\pm l_m / 2}{\sin\theta} = k_2 \frac{\lambda}{(\text{NA})^2}, \tag{4}$$

where k_2 is another process-dependent factor. The depth of focus is a measure of the distance from the lens in which the film or sensor plane will remain in focus. In photolithography, it is useful to specify the flatness and thickness of the resist to assure sharp focus.

Equation 2 indicates that resolution can be improved (i.e., smaller l_m) by either reducing the wavelength or increasing NA or both. However, Eq. 4 indicates that the DOF degrades much more rapidly by increasing NA than by decreasing λ. This explains the trend toward shorter-wavelength sources in optical lithography.

The high-pressure mercury-arc lamp is widely used in exposure equipment because of its high intensity and reliability. The mercury-arc spectrum is composed of several peaks. The terms G-line, H-line, and I-line refer to the peaks at 436 nm, 405 nm, and 365 nm, respectively. I-line lithography with 5:1 step-and-repeat projection can offer a resolution of 0.3 μm with resolution enhancement techniques (see Section 13.1.6). Advanced exposure equipment such as the 248 nm lithographic system using a KrF excimer laser, the 193 nm lithographic system using an ArF excimer laser, and the immersion 193 nm system (in which the lens is immersed in water to increase the index of refraction from 1 to 1.33) have been developed for mass production with resolutions of 180 nm, 100 nm, and below 70 nm, respectively.

13.1.3 Masks

Reduction techniques are usually used to fabricate masks for IC manufacturing. The first step in mask making is to use a computer-aided design (CAD) system in which designers can completely describe the circuit patterns electrically. The digital data produced by the CAD system then drives a pattern generator, which is an electron-beam lithographic system (see Section 13.2.1) that transfers the patterns directly to electron-sensitized mask. The mask consists of a fused silica substrate covered with a chrominum layer. The circuit pattern is first transferred to the electron-sensitized layer (electron resist), which is transferred once more into the underlying chrominum layer for the finished mask. The details of pattern transfer are considered in Section 13.1.5.

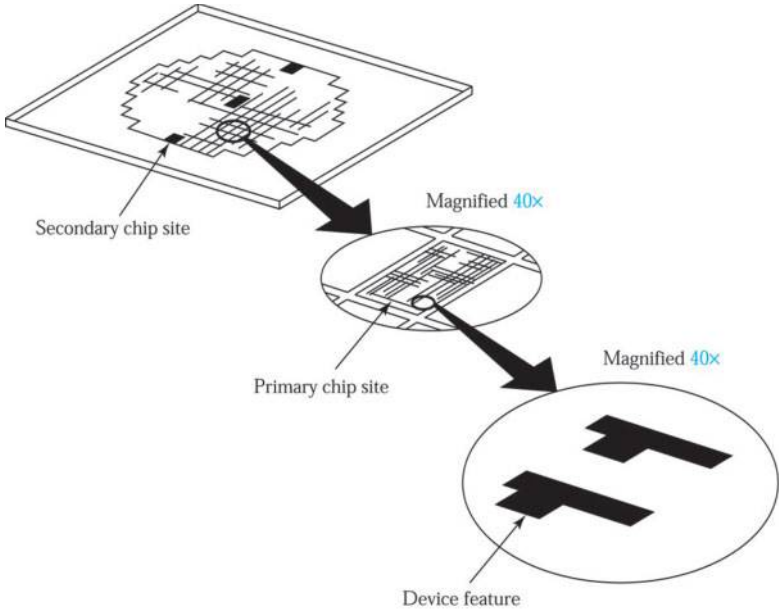

Fig. 6 **An integrated-circuit photomask.**[1]

The patterns on a mask represent one level of an IC design. The composite layout is broken into mask levels that correspond to the IC process sequence such as the isolation region on one level, the gate region on another, and so on. Typically, 15–20 different mask levels are required for a complete IC process cycle.

The standard-size mask substrate is a fused silica plate 15 × 15 cm square and 0.6 cm thick. The size is needed to accommodate the lens field sizes for 4:1 or 5:1 optical exposure equipment, whereas the thickness is required to minimize pattern placement errors due to substrate distortion. The fused silica plate is needed for its low coefficient of thermal expansion, high transmission at shorter wavelengths, and mechanical strength. Figure 6 shows a mask on which patterns of geometric shapes have been formed. A few secondary-chip sites used for process evaluation are also included in the mask.

One of the major concerns about masks is the defect density. Mask defects can be introduced during the manufacture of the mask or during subsequent lithographic processes. Even a small mask-defect density has a profound effect on the final IC yield. The *yield* is defined as the ratio of good chips per wafer to the total number of chips per wafer. As a first-order approximation, the yield Y for a given masking level can be expressed as

$$Y \cong e^{-DA}, \tag{5}$$

where D is the average number of "fatal" defects per unit area and A is the area of an IC chip. If D remains the same for all mask levels (e.g., $N = 10$ levels), then the final yield becomes

$$Y \cong e^{-NDA}. \tag{6}$$

Figure 7 shows the mask-limit yield for a 10-level lithographic process as a function of chip size for various values of defect densities. For example, for $D = 0.25$ defect/cm^2, the yield is 10% for a chip size of 90 mm^2, and it drops to about 1% for a chip size of 180 mm^2. Therefore, inspection and cleaning of masks are important to achieve high yields on large chips. Of course, an ultraclean processing area is mandatory for lithographic processing.

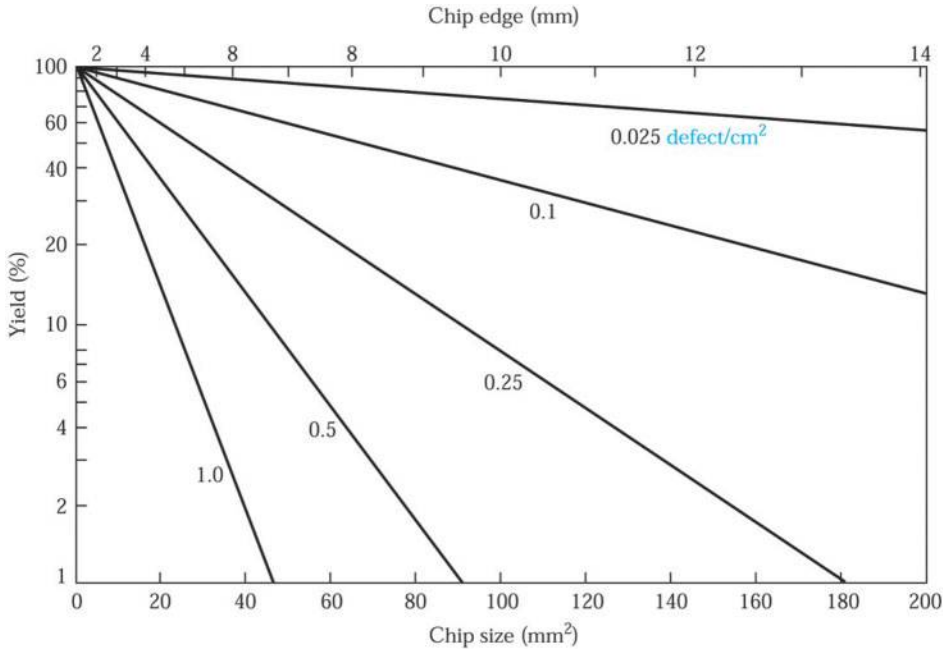

Fig. 7 **Yield for a 10-mask lithographic process with various defect densities per level.**

13.1.4 Photoresist

The photoresist is a radiation-sensitive compound. Photoresists are classified as positive and negative, depending on how they respond to radiation. For positive resists, the exposed regions become more soluble and thus more easily removed in the development process. The net result is that the patterns formed (also called images) in the positive resist are the same as those on the mask. For negative resists, the exposed regions become less soluble, and the patterns formed in the negative resist are the reverse of the mask patterns.

Positive photoresists have three components: a photosensitive compound, a base resin, and an organic solvent. Prior to exposure, the photosensitive compound is insoluble in the developer solution. After exposure, the photosensitive compound absorbs radiation in the exposed pattern areas, changes its chemical structure, and becomes soluble in the developer solution. After development, the exposed areas are removed.

Negative photoresists are polymers combined with a photosensitive compound. After exposure, the photosensitive compound absorbs the optical energy and converts it into chemical energy to initiate a polymer linking reaction. This reaction causes cross linking of the polymer molecules. The cross-linked polymer has a higher molecular weight and becomes insoluble in the developer solution. After development, the unexposed areas are removed. One major drawback of a negative photoresist is that in the development process, the whole resist mass swells by absorbing developer solvent. This swelling action limits the resolution of negative photoresists.

Figure 8*a* shows a typical exposure response curve and image cross section for a positive resist.[1] The response curve describes the percentage of resist remaining after exposure and development versus the exposure energy. Note that the resist has a finite solubility in its developer, even without exposure to radiation. As the exposure energy increases, the solubility gradually increases until at a threshold energy E_T, the resist becomes completely soluble. The sensitivity of a positive resist is defined as the energy required to produce complete solubility in the exposed region. Thus, E_T corresponds to the sensitivity. In addition to E_T, a parameter γ, the contrast ratio, is defined to characterize the resist:

$$\gamma \equiv \left[\ln\left(\frac{E_T}{E_1} \right) \right]^{-1}, \tag{7}$$

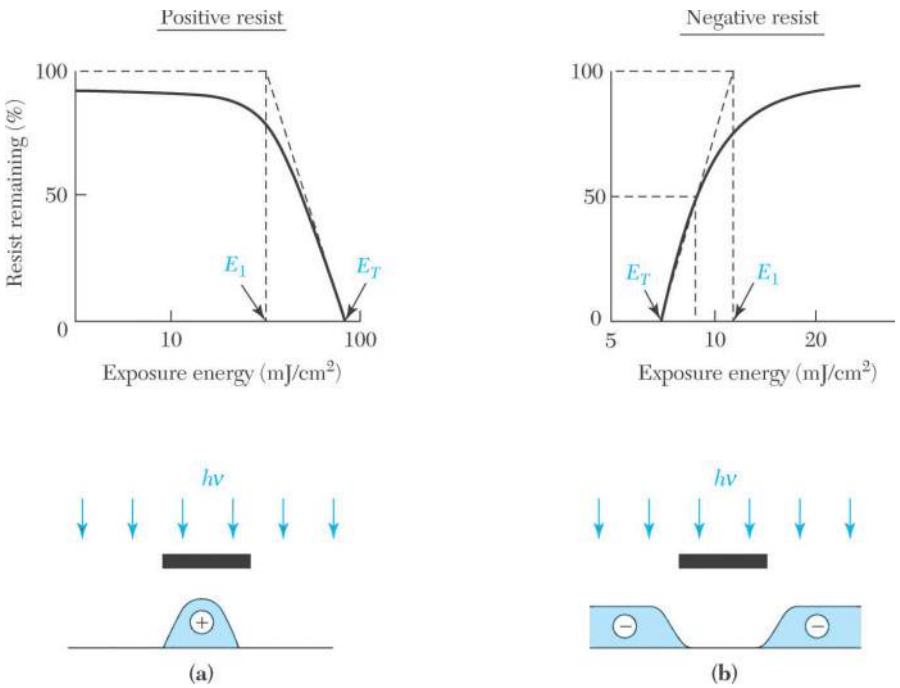

Fig. 8 Exposure-response curve and cross section of the resist image after development.[1] (*a*) Positive photoresist; (*b*) negative photoresist.

where E_1 is the energy obtained by drawing the tangent at E_T to reach 100% resist thickness as shown in Fig. 8*a*. A larger γ implies a higher solubility of the resist with an incremental increase of exposure energy and yields sharper images.

The image cross section in Fig. 8*a* illustrates the relationship between the edges of a photomask image and the corresponding edges of the resist images after development. The edges of the resist image are generally not at the vertically projected positions of the mask edges because of *diffraction*. The edge of the resist image corresponds to the position where the total absorbed optical energy equals the threshold energy E_T.

Figure 8*b* shows the exposure-response curve and image cross section for a negative resist. The negative resist remains completely soluble in the developer solution for exposure energies lower than the threshold energy E_T. Above E_T, more of the resist film remains after development. At exposure energies twice the threshold energy, the resist film becomes essentially insoluble in the developer. The sensitivity of a negative resist is defined as the energy required to retain 50% of the original resist film thickness in the exposed region. The parameter γ is defined similarly to γ in Eq. 7 except that E_1 and E_T are interchanged. The image cross section for the negative resist (Fig. 8*b*) is also influenced by the diffraction effect.

▶ EXAMPLE 2

Find the parameter γ for the photoresists shown in Fig. 8.

SOLUTION For the positive resist, $E_T = 90$ mJ/cm^2 and $E_1 = 45$ mJ/cm^2:

$$\gamma = \left[\ln\left(\frac{E_T}{E_1}\right)\right]^{-1} = \left[\ln\left(\frac{90}{45}\right)\right]^{-1} = 1.4.$$

For the negative resist, $E_T = 7$ mJ/cm^2 and $E_1 = 12$ mJ/cm^2:

$$\gamma = \left[\ln\left(\frac{E_1}{E_T}\right)\right]^{-1} = \left[\ln\left(\frac{12}{7}\right)\right]^{-1} = 1.9. \quad \blacktriangleleft$$

For deep UV lithography (e.g., 248 and 193 nm), we cannot use conventional photoresists because these resists require a high-dose exposure in deep UV, which will cause lens damage and lower throughput. The chemical-amplified resist (CAR) has been developed for the deep UV process. CAR consists of a photo-acid generator, a resin polymer, and a solvent. CAR is very sensitive to deep UV radiation and the exposed and unexposed regions differ greatly in their solubility in the developer solution.

13.1.5 Pattern Transfer

Figure 9 illustrates the steps to transfer IC patterns from a mask to a silicon wafer that has an insulating SiO_2 layer on its surface.[8] The wafer is placed in a clean room that is typically illuminated with yellow light, since photoresists are not sensitive to wavelengths greater than 0.5 μm. To ensure satisfactory adhesion of the resist, the surface must be changed from hydrophilic to hydrophobic. This change can be made by the application of an adhesion promoter, which can provide a chemically compatible surface for the resist. The most common adhesion promoter for silicon ICs is hexa-methylenedi-siloxane (HMDS). After the application of this adhesion layer, the wafer is held on a vacuum spindle and 2–3 cc of liquid resist is applied to the center of wafer. The wafer is then rapidly accelerated up to a constant rotational speed that is maintained for about 30 seconds. Spin speed is generally in the range of 1000–10,000 rpm (2000–5000 rpm is common) to coat a uniform film about 0.5 to 1 μm thick, as shown in Fig. 9*a*. The thickness of photoresist is correlated with its viscosity.

After the spinning step, the wafer is given a soft bake (typically at 90°–120°C for 60–120 seconds) to remove the solvent from the photoresist film and to increase resist adhesion to the wafer. The wafer is aligned with respect to the mask in an optical lithographic system, and the resist is exposed to UV light, as shown in Fig. 9*b*. If a positive photoresist is used, the exposed resist is dissolved in the developer, as shown in the left side of Fig. 9*c*. Photoresist development is usually done by flooding the wafer with the developer solution. The wafer is then rinsed and dried. After development, postbaking at ~100°–180°C may be required to increase the adhesion of the resist to the substrate. The wafer is then put in an ambient that etches the exposed insulation layer but does not attack the resist, as shown in Fig. 9*d*. Finally, the resist is stripped (e.g., using solvent or plasma oxidation), leaving behind an insulator image (or pattern) that is the same as the opaque image on the mask (left side of Fig. 9*e*).

For the negative photoresist, the procedures described are also applicable, except that the unexposed areas are removed. The final insulator image (right side of Fig. 9*e*) is the reverse of the opaque image on the mask.

The insulator image can be used as a mask for subsequent processing. For example, we use ion implantation to dope the exposed semiconductor region, but not the area covered by the insulator. The dopant pattern is a duplicate of the design pattern on the photomask (for a negative photoresist) or is its complementary pattern (for a positive photoresist). The complete circuit is fabricated by aligning the next mask in the sequence to the previous pattern and repeating the lithographic transfer process.

A related pattern-transfer process is the liftoff technique, shown in Fig. 10. A positive resist is used to form the resist pattern on the substrate (Fig. 10*a* and 10*b*). The film (e.g., aluminum) is deposited over the resist and the substrate (Fig. 10*c*); the film thickness must be smaller than that of the resist. Those portions of the film on the resist are removed by selectively dissolving the resist layer in an appropriate liquid etchant so that the overlying film is lifted off and removed (Fig. 10*d*). The liftoff technique is capable of high resolution and is used extensively for discrete devices such as high-power MESFETs. However, it is not as widely applicable for ultralarge-scale integration, in which dry etching is the preferred technique.

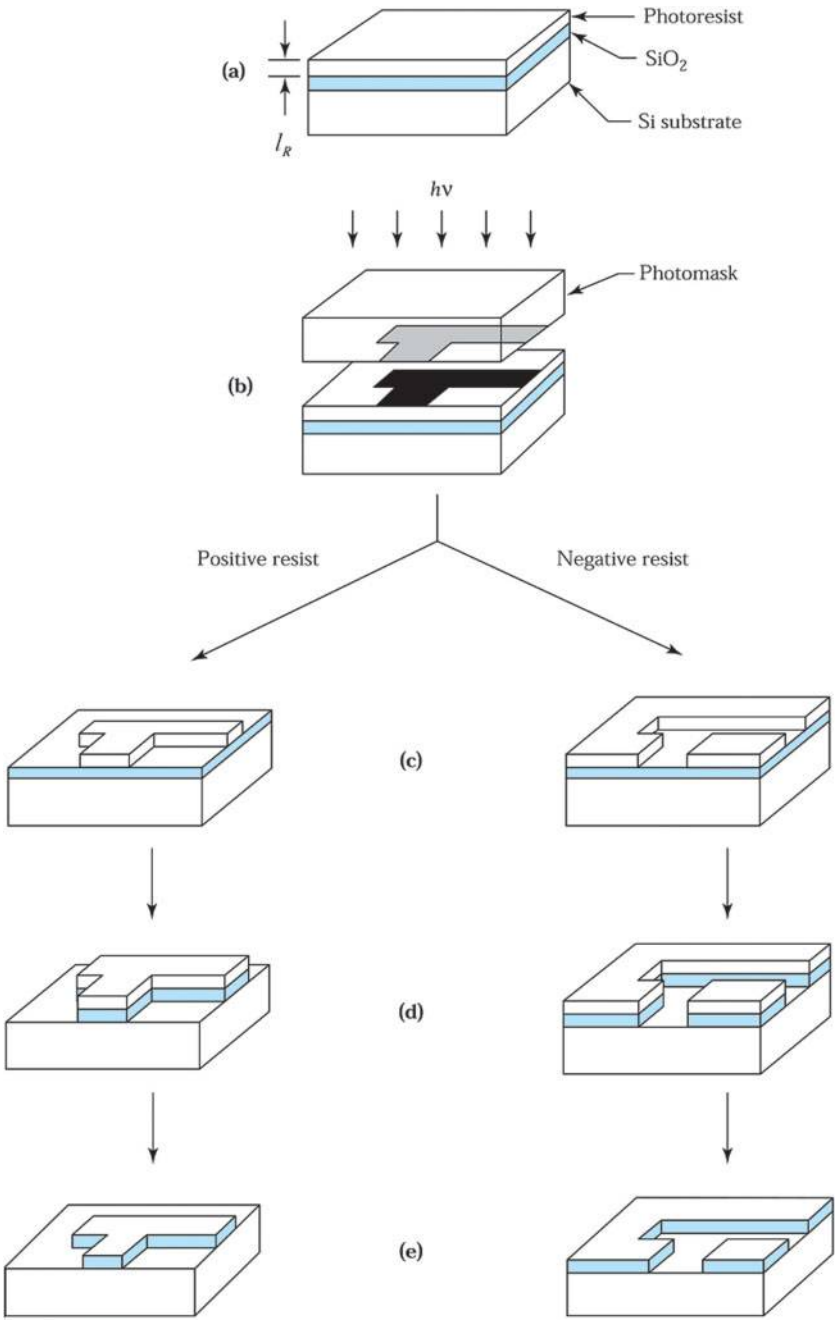

Fig. 9 Details of the optical lithographic pattern transfer process.[8] (*a*) Application of resist. (*b*) Resist exposure through the mask. (*c*) Development of resist. (*d*) Etching of SiO_2. (*e*) Removal of resist.

Wet Photoresist Stripping

The photoresist can be stripped off with a strong acid such as H_2SO_4 or an acid-oxidant combination such as H_2SO_4–Cr_2O_3 attacking the resist but not the oxide or the Si. Other liquid strippers are organic-solvent strippers and alkaline strippers. Acetone can be used if the postbaking was not too long or at too high a at 120 °C we can

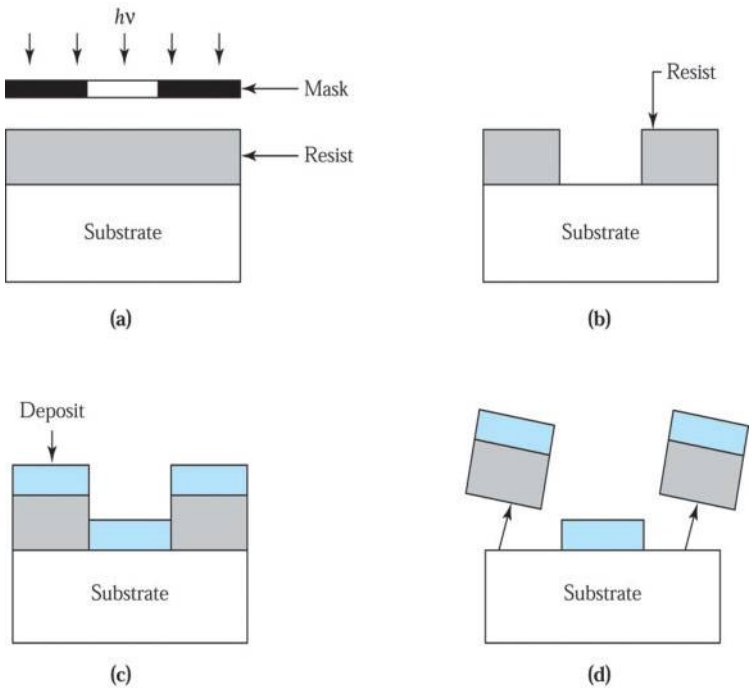

Fig. 10 Liftoff process for pattern transfer. (*a*) Resist exposure through the mask. (*b*) Resist. (*c*) Film deposition. (*d*) Liftoff.

use acetone. However, with a post-bake at 140 °C, the resist develops a tough skin and has to be burned away in oxygen plasma.

Dry Photoresist Stripping

Dry resist stripping (or ashing) can provide a cleaner surface than wet resist stripping. It also has fewer problems with toxic, flammable, and dangerous chemicals. The stripping rate is almost a constant and causes no undercutting and broadening of the resist. In addition, it is less corrosive with respect to metal features on the wafer.

There are three methods for dry resist stripping. Oxygen plasma stripping employs a low-pressure plasma discharge to split molecular oxygen (O_2) into its more reactive atomic form (O). This atomic oxygen converts an organic resist into a gaseous product that may be pumped away. In ozone strippers, ozone attacks the resist at atmosphere pressure. In UV/ozone stripping, the UV helps to break bonds in the resist, so that ozone can make a more efficient attack. Ozone strippers have the advantage that no plasma damage can occur on the devices in the process. The barrel plasma reactor has been used primarily for resist stripping and will be discussed in Section 13.5.

13.1.6 Resolution Enhancement Techniques

Optical lithography has been continuously challenged to provide better resolution, greater depth of focus (DOF), and wider exposure latitude in IC processing. These challenges have been met by reducing the wavelength of the exposure equipment and developing new resists. In addition, many resolution–enhancement techniques have been developed to extend the capability of optical lithography to even smaller feature lengths.

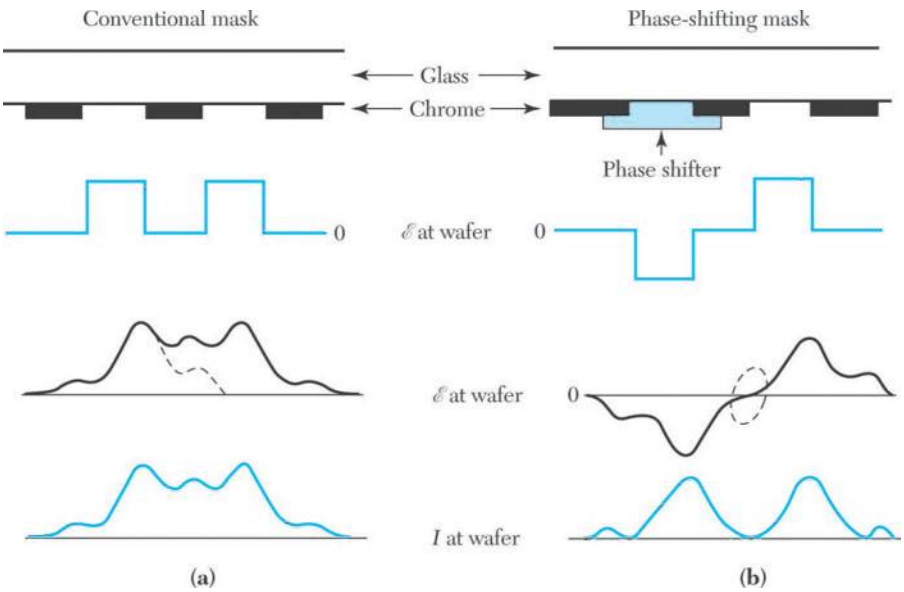

Fig. 11 **The principle of phase-shift technology. (*a*) Conventional technology; (*b*) phase-shift technology.**[9]

Phase Shift Technology

An important resolution enhancement technique is the phase-shifting mask (PSM). The basic concept is shown[9] in Fig. 11. For a conventional mask, the electric field has the same phase at every aperture (clear area) in Fig. 11*a*. Diffraction and the limited resolution of the optical system spread the electric field at the wafer, as shown by the dotted lines. Interference between waves diffracted by the adjacent apertures enhances the field between them. Because the intensity I is proportional to the square of the electric field, it becomes difficult to separate the two images that are projected close to one another. The phase-shift layer that covers adjacent apertures reverses the sign of the electric field, as shown in Fig. 11*b*. Because the intensity at the mask is unchanged, the electric field of the images at the wafer can be cancelled. Therefore, images that are projected close to one another can be separated. A 180° phase change can be obtained by using a transparent layer with the thickness of $d \quad \lambda / 2(\overline{n} \quad 1)$, where $\overline{n}$ is the refractive index and λ is the wavelength, that covers one aperture, as shown in Fig. 11*b*.

Optical Proximity Correction

High-performance optical projection imaging for lithography is strongly impacted by diffraction effects. The individual pattern features do not image independently, but rather interact with neighboring pattern features. The result from the diffraction overlap is the so-called proximity effect. The proximity effect becomes much more prominent as the feature sizes and spaces between the feature sizes approach the resolution limits of the projection optics.

A resolution-enhancement technique to minimize this effect is optical proximity correction (OPC), which uses modified shapes of adjacent subresolution geometry to compensate for image errors due to diffraction effects. For example, a line with a width near the resolution limit will print a line with round corners as shown as Fig. 12*a* due to the diffraction effect. Modifying the edge of the line pattern with additional geometrics at the corners as shown in Fig. 12*b* will help print a more accurate line. The addition of OPC features to the mask layout allows tighter design rules and significantly improves process reliability and yield.

Immersion Lithography

As mentioned in Sec. 13.1.2, immersion lithography is an advanced photolithography system in which the usual air gap between the lens and the wafer surface is replaced with a liquid medium that has a refractive index greater

Fig. 12 **Optical proximity effects. (*a*) Round corners by standard mask. (*b*) Accurate line shape by OPC mask.**

than air. The resolution can be enhanced by increasing the numerical aperture (Eq. 2), which is proportional to the refractive index of the image medium (Eq. 3). Therefore, the resolution is increased by a factor equal to the refractive index. Current immersion-lithography equipment uses highly purified water ($\bar{n} = 1.33$) for this liquid to fabricate new-generation nano-scaled CMOS ICs. Immersion lithography is being developed for processes below 32 nm.

13.2 NEXT-GENERATION LITHOGRAPHIC METHODS

Why is optical lithography so widely used and what makes it such a promising method? The reasons are that it has high throughput, good resolution, low cost, and ease of operation. However, due to IC process requirements for features below 100 nm, optical lithography has some limitations not yet solved. Although we can use PSM, OPC, or immersion lithography to extend its useful span, the complexity of mask production and mask inspection can not be easily resolved. In addition, the cost of the masks is very high. Therefore, we need to find postoptical lithography to process nanometer ICs. Various types of next-generation lithographic methods for IC fabrication are discussed in this section.

13.2.1 Electron-Beam Lithography

Electron-beam lithography is primarily used to produce photomasks. Relatively little equipment is dedicated to direct exposure of the resist by a focused electron beam without a mask. Figure 13 shows a schematic of an electron-beam lithography system.[10] The electron gun is a device that can generate a beam of electrons with a suitable current density. A tungsten thermionic-emission cathode or single-crystal lanthanum hexa-boride (LaB_6) is used for the electron gun. Condenser lenses are used to focus the electron beam to a spot size 10–25 nm in diameter. Beam-blanking plates that turn the electron beam on and off and beam deflection coils are computer controlled and operated at MHz or higher rates to direct the focused electron beam to any location in the scan field on the substrate. Because the scan field (typically 1 cm) is much smaller than the substrate diameter, a precision mechanical stage is used to position the substrate to be patterned.

The advantages of electron-beam lithography include the generation of nanometer resist geometries, highly automated and precisely controlled operation, greater depth of focus than available from optical lithography, and direct patterning on a semiconductor wafer without using a mask. The disadvantage is that electron beam lithographic machines have low throughput—approximately 2 wafers per hour at less than 100 nm resolution. This throughput is adequate for the production of photomasks, for situations that require small numbers of custom circuits, and for design verification. However, for maskless direct writing, the machine must have the highest possible throughput and therefore the largest beam diameter possible consistent with the minimum device dimensions.

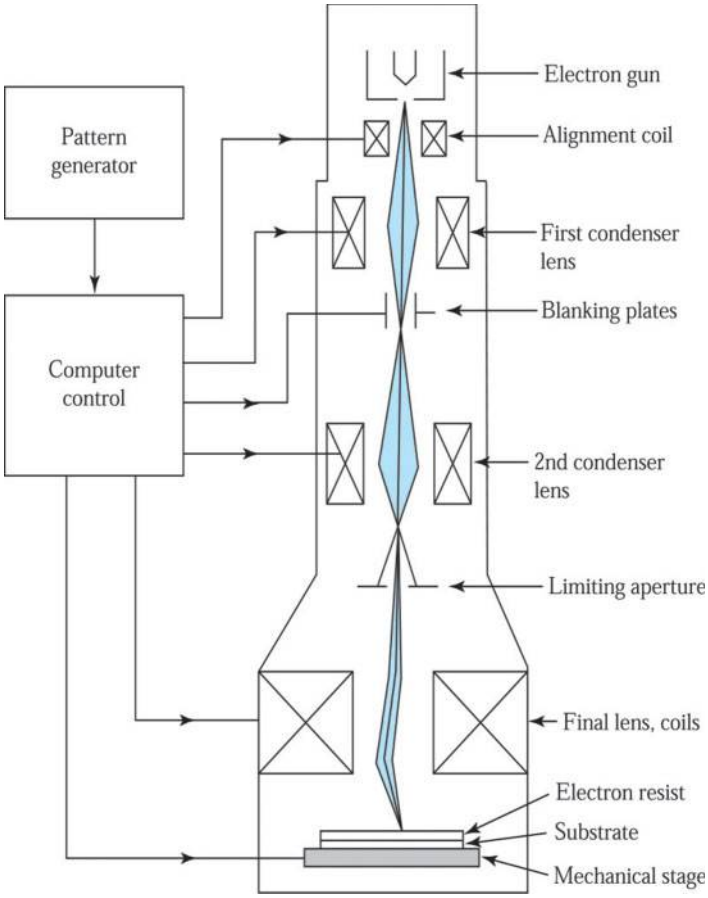

Fig. 13 **Schematic of an electron-beam machine.**[10]

There are basically two ways to scan the focused electron beam: raster scan and vector scan.[11] In a raster scan system, resist patterns are written by a beam that moves through a regular mode, vertically oriented, as shown in Fig. 14*a*. The beam scans sequentially over every possible location on the mask and is blanked (turned off) where no exposure is required. All patterns on the area to be written must be subdivided into individual addresses, and a given pattern must have a minimum incremental interval that is evenly divisible by the beam address size.

In the vector scan system, as shown in Fig. 14*b*, the beam is directed only to the requested pattern features and jumps from feature to feature, rather than scanning the whole chip, as in raster scan. For many chips, the average exposed region is only 20% of the chip area, so we can save time by using a vector-scan system.

Figure 14*c* shows several types of electron beams employed for e-beam lithography: the Gaussian spot beam (round beam), variable-shaped beam, and cell projection. In variable-shaped beam system, the patterning beam has a rectangular cross section of variable size. Therefore, the vector scan method using variable-shaped beam has higher throughout than the conventional Gaussian spot beam. It is also possible to pattern a complex geometric shape in one exposure with an electron beam system; this is called cell projection, as shown in the far right of Fig. 14*c*. The cell projection technique[12] is particularly suitable for highly repetitive designs, as in MOS memory cells, because several memory cell patterns can be exposed at once. Cell projection has not yet achieved the throughput of optical exposure equipment.

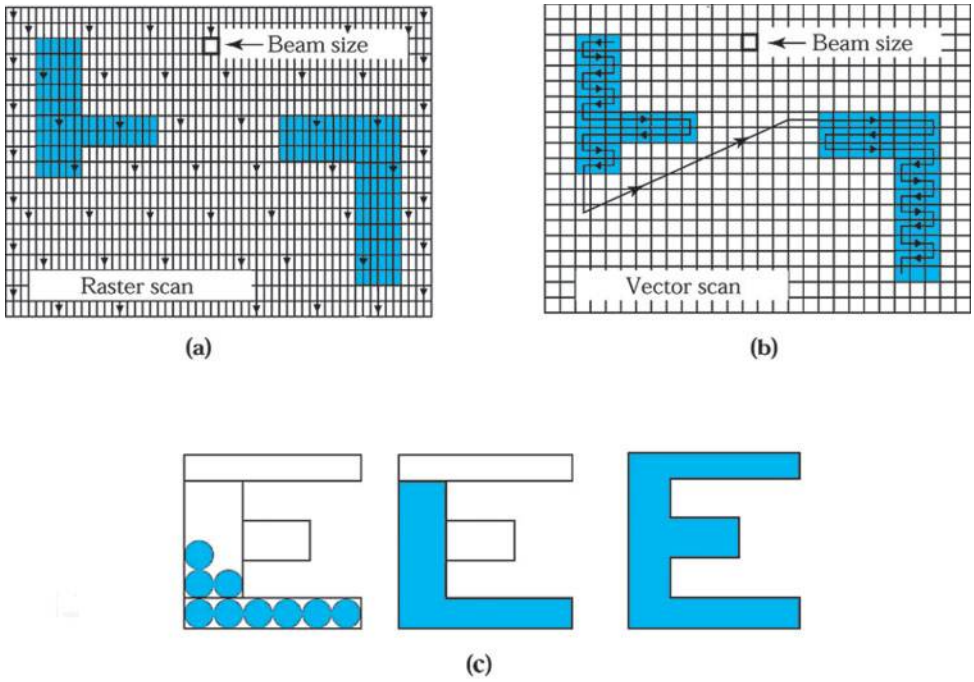

Fig. 14 **(*a*) Raster-scan writing scheme; (*b*) vector-scan writing schemes; (*c*) shapes of electron beam: round, variable, cell projection.[12]**

Electron Resist

Electron resists are polymers. The behavior of an electron-beam resist is similar to that of a photoresist: that is, a chemical or physical change is induced in the resist by irradiation. This change allows the resist to be patterned. For a positive electron resist, the polymer-electron interaction causes chemical bonds to be broken (chain scission) to form shorter molecular fragments, as shown[13] in Fig. 15*a*. As a result, the molecular weight is reduced in the irradiated area, which can be dissolved subsequently in a developer solution that attacks the low-molecular-weight material. Common positive electron resists include poly-methyl methacrylate (PMMA) and poly-butene-1 sulfone (PBS). Positive electron resists can achieve resolutions of 0.1 μm or better.

For a negative electron resist, the irradiation causes radiation-induced polymer linking, as shown in Fig. 15*b*. The cross linking creates a complex three-dimensional structure with a molecular weight higher than that of the nonirradiated polymer. The nonirradiated resist can be dissolved in a developer solution that does not attack the high-molecular-weight material. Poly-glycidyl methacrylate-co-ethyl acrylate (COP) is a common negative electron resist. COP, like most negative photoresists, also swells during development, so the resolution is limited to about 1 μm.

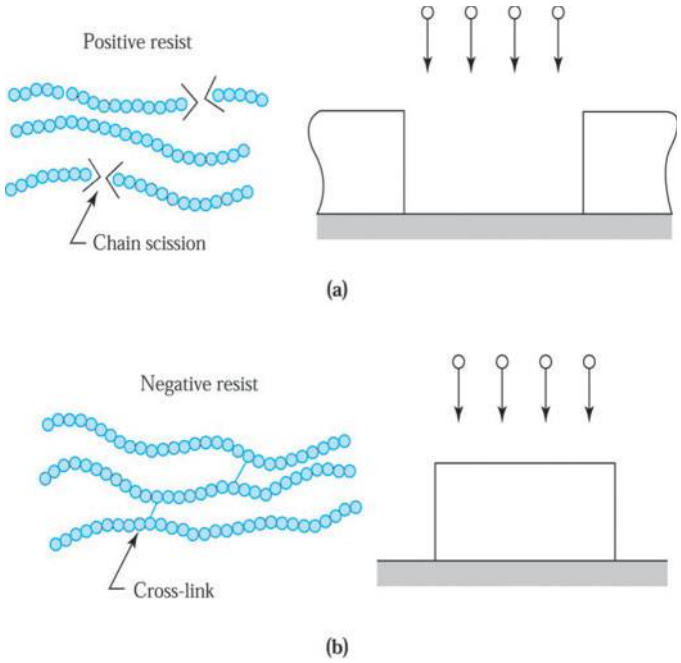

Fig. 15 **Schematic of (*a*) positive and (*b*) negative resists used in electron-beam lithography.**[13]

The Proximity Effect

In optical lithography, the resolution is limited by diffraction of light. In electron-beam lithography, the resolution is limited not by diffraction (because the wavelengths associated with electrons of a few keV and higher energies are less than 0.1 nm) but by electron scattering. When electrons penetrate the resist film and underlying substrate, they undergo collisions that lead to energy losses and path changes. Thus, the incident electrons spread out as they travel through the material until either all of their energy is lost or they leave the material because of backscattering.

Figure 16*a* shows computed electron trajectories of 100 electrons with initial energy of 20 keV incident at the origin of a 0.4 μm PMMA film on a thick silicon substrate.[14] The electron beam is incident along the *z*-axis, and all trajectories have been projected onto the *xz* plane. This figure shows qualitatively that the electrons are distributed in an oblong pear-shaped volume with a diameter on the same order of magnitude as the electron penetration depth (~3.5 μm). Also, there are many electrons that undergo backscattering collisions and travel backward from the silicon substrate into the PMMA resist film and leave the material.

Figure 16*b* shows the normalized distributions of the forward-scattering and backscattering electrons at the resist-substrate interface. Because of the backscattering, electrons can irradiate several micrometers away from the center of the exposure beam. Since the dose of a resist is given by the sum of the irradiations from all surrounding areas, the electron-beam irradiation at one location will affect the irradiation in neighboring locations. This phenomenon is called the *proximity effect*. The proximity effect places a limit on the minimum spacings between pattern features. To correct for the proximity effect, patterns are divided into smaller segments. The incident electron dose in each segment is adjusted so that the integrated dose from all its neighboring segments is the correct exposure dose. This approach further decreases the throughput of the electron-beam system because of the additional computer time required to expose the subdivided resist patterns.

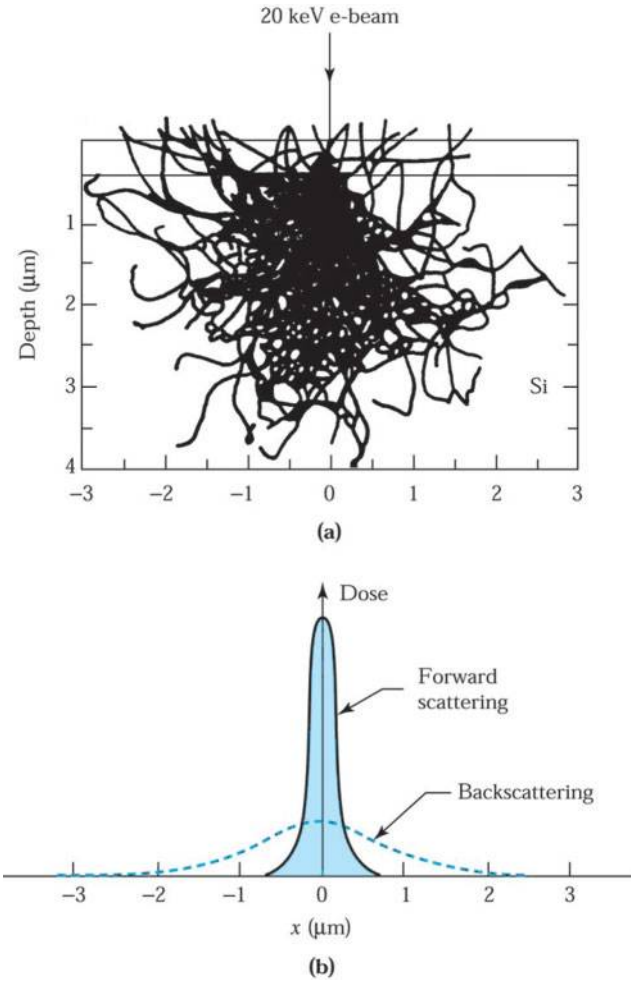

Fig. 16 (*a*) Simulated trajectories of 100 electrons in PMMA for a 20-keV electron beam.[14] (*b*) Dose distribution for forward scattering and backscattering at the resist-substrate interface.

13.2.2 Extreme-Ultraviolet Lithography

Extreme-ultraviolet (EUV) lithography is a promising next-generation lithographic technology to extend minimum linewidths below 30 nm without throughput loss.[15] Figure 17 shows a schematic diagram of an EUV lithographic system. A laser-produced plasma or synchrotron radiation can serve as the EUV source of $\lambda = 10$–14 nm EUV light. The EUV radiation is reflected by a mask that is produced by patterning an absorber material deposited on a multilayer-coated flat silicon or glass-plate mask blank. EUV radiation is reflected from the nonpatterned regions (i.e., nonabsorbing regions) of the mask through a 4× reduction camera and imaged into a thin layer of resist on the wafer.

Since the EUV radiation beam is narrow, the mask must be scanned by the beam to illuminate the entire pattern field that describes the circuit mask layer. Also, for a 4× four-mirror (i.e., the two-paraboloid, one-ellipsoid, and one-plane mirrors) reduction camera, the wafer must be scanned at one-fourth the mask speed in a direction opposite to the mask movement to reproduce the image field on all chip sites on the wafer surface. A precision system is required to perform

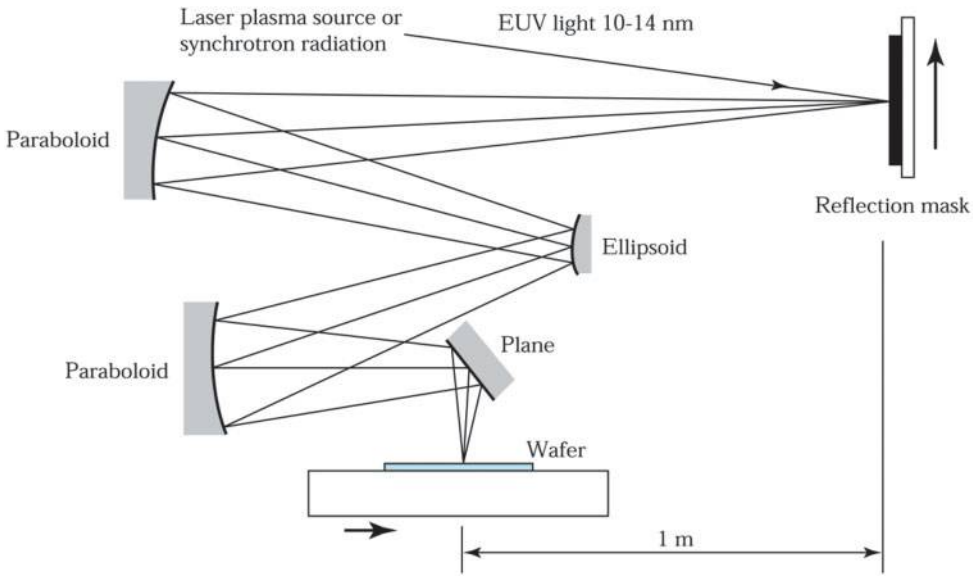

Fig. 17 **Schematic representation of an extreme-ultraviolet (EUV) lithography system.**[15]

the chip-site alignment and to control the wafer and mask stage movements and exposure dose during the scanning process. EUV lithography is capable of printing 50-nm features with PMMA resist using 13-nm radiation. However, the production of EUV exposure equipment has a number of challenges. Since EUV is strongly absorbed in all materials, the lithography process must be performed in vacuum. The camera must use reflective-lens elements, and the mirrors must be coated with multilayer coatings that produce distributed quarter-wave Bragg reflectors. In addition, the mask blank must also be multilayer coated to maximize its reflectivity at $\lambda = 10–14$ nm.

13.2.3 Ion-Beam Lithography

Ion-beam lithography can achieve higher resolution than optical or electron-beam lithographic techniques because ions have a greater mass and therefore scatter less than electrons. The most important application is the repair of masks for optical lithography, a task for which commercial systems are available.

The computer-simulated trajectories of 50 H^+ ions implanted at 60 keV into PMMA and various substrates[16] shows that the spread of the ion beam at a depth of 0.4 μm is only 0.1 μm in all cases (compare with Fig. 16 for electrons). The backscattering is completely absent for the silicon substrate, and there is only a small amount of backscattering for the gold substrate. However, ion-beam lithography may suffer from a random (or stochastic) space-charge effect, causing broadening of the ion beam.

There are two types of ion-beam lithography systems: a scanning focused-beam system and a mask-beam system. The former system is similar to the electron-beam machine (Fig. 13), in which the ion source can be Ga^+ or H^+. The latter system is similar to an optical 5× reduction projection step-and-repeat system, which projects 100 keV light ions such as H^+_2 through a stencil mask.

13.2.4 Comparison of Various Lithographic Methods

The lithographic methods discussed above all have 100 nm or better resolution. However, each method has its own limitations. For IC fabrication, many mask levels are involved. However, it is not necessary to use the same lithographic method for all levels. A mix-and-match approach can take advantage of the unique features of each lithographic process to improve resolution and to maximize throughput. For example, a 4:1 EUV method can be used for the most critical mask levels, whereas 4:1 or 5:1 optical system can be used for the rest.

According to the Roadmap of the Semiconductor Industry Association, IC manufacturing technology will reach the 15 nm generation around 2020. With each new technology generation, lithography has become an even more important key driver for the semiconductor industry because of the requirements of smaller feature size and tighter overlay tolerance. In addition, lithography equipment costs have become higher relative to the total equipment costs for IC manufacturing facility. Currently, the technology development of next-generation lithography is conducted by multinational research projects or industrial partners.

▶ 13.3 WET CHEMICAL ETCHING

Wet chemical etching is used extensively in semiconductor processing. Starting from the sawed semiconductor wafers, chemical etchants are used for lapping and polishing to give an optically flat, damage-free surface. Prior to thermal oxidation or epitaxial growth, the semiconductor wafers are chemically cleaned to remove contamination that results from handling and storing. Wet chemical etchings are especially suitable for blanket etches (i.e., over the whole wafer surface) of polysilicon, oxide, nitride, metals, and III-V compounds.

The mechanisms for wet chemical etching involve three essential steps: the reactants are transported by diffusion to the reacting surface, chemical reactions occur at the surface, and the products from the surface are removed by diffusion. Both agitation and the temperature of the etchant solution will influence the etch rate, which is the amount of film removed by etching per unit time. In IC processing, most wet chemical etchings proceed by immersing the wafers in a chemical solution or by spraying the wafers with the etchant solution. For immersion etching, the wafer is immersed in the etch solution. Mechanical agitation is usually required to ensure etch uniformity and a consistent etch rate. Spray etching has gradually replaced immersion etching because it greatly increases the etch rate and uniformity by constantly supplying fresh etchant to the wafer surface.

Etch rates must be uniform across a wafer, from wafer to wafer, from run to run, and for any variations in feature sizes and pattern densities. Etch rate uniformity is given by:

$$\text{Etch rate uniformity } (\%) = \frac{(\text{maximum etch rate} \quad \text{minimum etch rate})}{\text{maximum etch rate} + \text{minimum etch rate}} \times 100\%. \tag{8}$$

▶ EXAMPLE 3

Calculate the Al average etch rate and etch rate uniformity on a 300 mm diameter silicon wafer, assuming the etch rates at the center, left, right, top, and bottom of the wafer are 750, 812, 765, 743, and 798 nm/min, respectively.

SOLUTION

Al average etch rate = (750 + 812 + 765 + 743 + 798) ÷ 5 = 773.6 nm/min.

Etch rate uniformity = (812 – 743) ÷ (812 + 743) × 100% = 4.4 %. ◀

13.3.1 Silicon Etching

For semiconductor materials, wet chemical etching usually starts with oxidation followed by dissolution of the oxide by a chemical reaction. For silicon, the most commonly used etchants are mixtures of nitric acid (HNO_3) and hydrofluoric acid (HF) in water or acetic acid (CH_3COOH). Nitric acid oxidizes silicon to form a SiO_2 layer.[17] The oxidation reaction is

$$Si + 4HNO_3 \rightarrow SiO_2 + 2H_2O + 4NO_2. \tag{9}$$

Hydrofluoric acid is used to dissolve the SiO_2 layer. The reaction is:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O. \tag{10}$$

Water can be used as a diluent for this etchant. However, acetic acid is preferred because it reduces the dissolution of the nitric acid.

Some etchants dissolve a given crystal plane of single-crystal silicon much faster than another plane; this results in orientation-dependent etching.[18] For a silicon lattice, the (111)-plane has more available bonds per unit area than the (110)- and (100)-planes; therefore, the etch rate is expected to be slower for the (111)-plane. A commonly used orientation-dependent etch for silicon consists of a mixture of KOH in water and isopropyl alcohol. For example, a solution with 19 wt% KOH in deionized (DI) water at about 80°C removes the (100)-plane at a much greater rate than the (110)- and (111)-planes. The ratio of the etch rates for the (100)-, (110)-, and (111)-planes is 100:16:1.

Orientation-dependent etching of <100>-oriented silicon through a patterned silicon dioxide mask creates precise V-shaped grooves,[10] the edges being (111)-planes at an angle of 54.7° from the (111)-surface, as shown at the left of Fig. 18*a*. If the window in the mask is sufficiently large or if the etching time is short, a U-shaped groove will be formed, as shown at the right of Fig. 18*a*. The width of the bottom surface is given by

$$W_b = W_0 - 2l\cot 54.7°$$

or

$$\boxed{W_b = W_0 - \sqrt{2}\, l,} \tag{11}$$

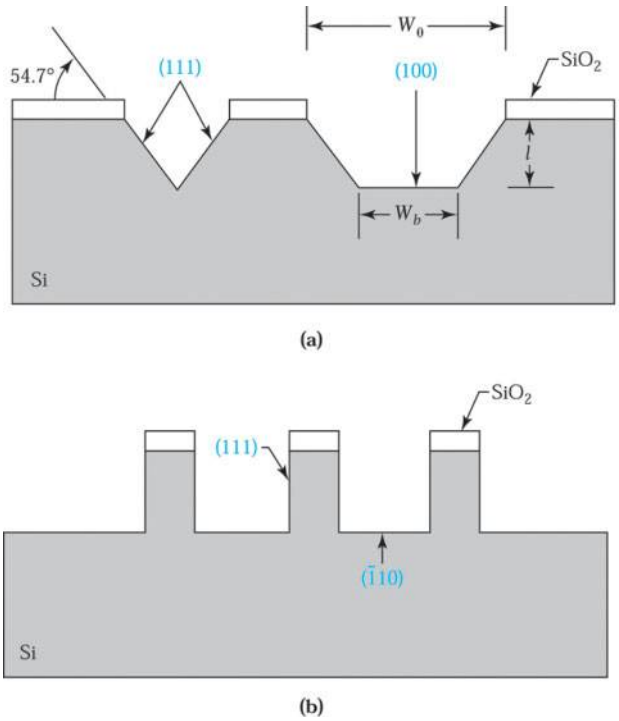

Fig. 18 Orientation-dependent etching. (*a*) Through window patterns on <100>-oriented silicon; (*b*) through window patterns on <$\bar{1}$00>-oriented silicon.[18]

where W_0 is the width of the window on the wafer surface and l is the etched depth. If <$\bar{1}$10>-oriented silicon is used, essentially straight-walled grooves with sides of (111)-planes can be formed, as shown in Fig. 18*b*. We can use the large orientation dependence in the etch rates to fabricate device structures with submicron feature lengths.

13.3.2 Silicon Dioxide Etching

The wet etching of silicon dioxide is commonly achieved in a dilute solution of HF with or without the addition of ammonium fluoride (NH_4F). Adding NH_4F is referred to as a buffered HF solution (BHF), also called buffered-oxide-etch (BOE). The addition of NH_4F to HF controls the pH value and replenishes the depleted fluoride ions, thus maintaining stable etching performance. The overall reaction for SiO_2 etching is the same as that in Eq. 10. The etch rate of SiO_2 etching depends on the etchant solution, etchant concentration, agitation, and temperature. In additional, density, porosity, microstructure, and the presence of impurities in the oxide also influence the etch rate. For example, a high concentration of phosphorus in the oxide results in a rapid increase in the etch rate, and a loosely structured chemical-vapor deposition (CVD) or sputtered oxide exhibits a faster etch rate than thermally grown oxide.

Silicon dioxide can also be etched in vapor-phase HF. Vapor-phase-HF oxide-etch technology has a potential for etching feature lengths below 100 nm because the process can be well controlled.

13.3.3 Silicon Nitride and Polysilicon Etching

Silicon nitride films can be etched at room temperature in concentrated HF or buffered HF and in a boiling H_3PO_4 solution. Selective etching of nitride to oxide is done with 85% H_3PO_4 at 180ºC because this solution attacks silicon dioxide very slowly. The etch rate is typically 10 nm/min for silicon nitride, but less than 1 nm/min for silicon dioxide. However, photoresist adhesion problems are encountered when etching nitride with boiling H_3PO_4 solution. Better patterning can be achieved by depositing a thin oxide layer on top of the nitride film before resist coating. The resist pattern is transferred to the oxide layer, which then acts as a mask for subsequent nitride etching.

Etching polysilicon is similar to etching single-crystal silicon. However, the etch rate is considerably larger because of grain boundaries. The etch solution is usually modified to ensure that it does not attack the underlying gate oxide. Dopant concentrations and temperature may affect the etch rate of polysilicon.

13.3.4 Aluminum Etching

Aluminum and aluminum alloy films are generally etched in heated solutions of phosphoric acid, nitric acid, acetic acid, and DI water. The typical etchant is a solution of 73% H_3PO_4, 4% HNO_3, 3.5% CH_3COOH, and 19.5% DI water at 30°–80°C. The wet etching of aluminum proceeds as follows: HNO_3 oxidizes aluminum, and H_3PO_4 then dissolves the oxidized aluminum. The etch rate depends on etchant concentration, temperature, agitation of the wafers, and impurities or alloys in the aluminum film. For example, the etch rate is reduced when copper is added to the aluminum.

Wet etching of insulating and metal films is usually done with the similar chemicals that dissolve these materials in bulk form. Generally, film materials will be etched more rapidly than their bulk counterparts. Also, the etch rates are higher for films that have a poor microstructure, built-in stress, departure from stoichiometry, or have been irradiated. Some useful etchants for insulating and metal films are listed in Table 1.

13.3.5 Gallium Arsenide Etching

A wide variety of etches has been investigated for gallium arsenide; however, few of them are truly isotropic.[19] This is because the surface activities of the (111)-Ga and (111)-As faces are very different. Most etches give a polished surface on the arsenic face, but the gallium face tends to show crystallographic defects and etches more slowly. The most commonly used etchants are the H_2SO_4-H_2O_2-H_2O and H_3PO_4-H_2O_2-H_2O systems. For an etchant with an 8:1:1 volume ratio of H_2SO_4:H_2O_2:H_2O, the etch rate is 0.8 μm/min for the <111>-Ga face and 1.5 μm/min for all other faces. For an etchant with 3:1:50 volume ratio of H_3PO_4:H_2O_2:H_2O, the etch rate is 0.4 μm/min for <111>-Ga face and 0.8 μm/min for all other faces.

TABLE 1 ETCHANTS FOR INSULATORS AND CONDUCTORS

Material	Etchant composition		Etch rate (nm/min)
SiO_2	28 ml of HF 170 ml of HF 113 g of NH_4F	Buffered HF	100
	15 ml of HF 10 ml of HNO_3 300 ml of H_2O	P — etch	12
Si_3N_4	Buffered HF		0.5
Al	H_3PO_4		10
	4 ml of HNO_3 3.5 ml of CH_3COOH 73 ml of H_3PO_4 19.5 ml of H_2O		30
Au	4 g KI		1000
Mo	1 g of I_2 40 ml of H_2O 5 ml of H_3PO_4 2 ml of HNO_3 4 ml of CH_3COOH 150 ml of H_2O		500
Pt	1 ml of HNO_3 7 ml of HCl 8 ml of H_2O		50
W	34 g of KH_2PO_4 13.4 g of KOH 33 g of $K_3Fe(CN)_6$ H_2O to make 1 liter		160

13.4 DRY ETCHING

In pattern-transfer operations, a resist pattern is defined by a lithographic process to serve as a mask for etching of its underlying layer (Fig. 19*a*).20 Most of the layer materials (e.g., SiO_2, Si_3N_4, and deposited metals) are amorphous or polycrystalline thin films. If they are etched in a wet chemical etchant, the etch rate is generally isotropic (i.e., the lateral and vertical etch rates are the same), as illustrated in Fig. 19*b*. If h_f is the thickness of the layer material and l the lateral distance etched underneath the resist mask, we can define the degree of anisotropy A_f by

$$A_f \equiv 1 - \frac{l}{h_f} = 1 - \frac{R_l t}{R_v t} = 1 - \frac{R_l}{R_v}, \tag{12}$$

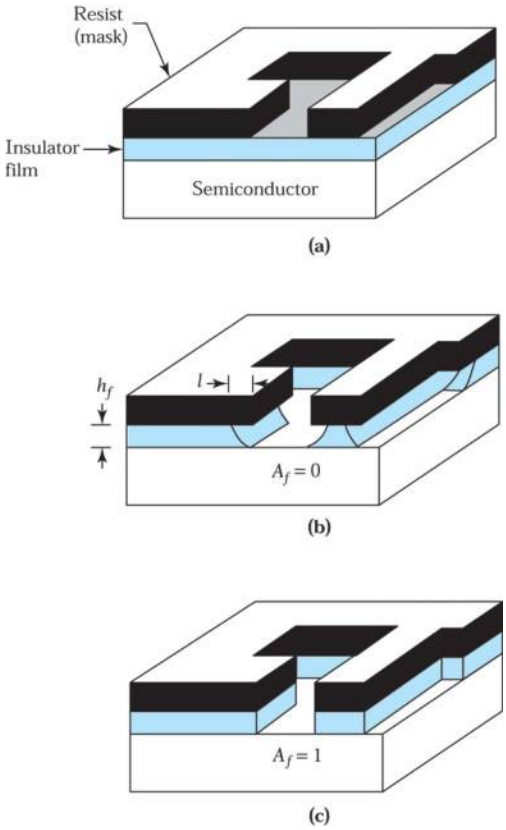

Fig. 19 (*a*) Resist pattern formation. Comparison of (*b*) wet chemical etching and (*c*) dry etching for pattern transfer.[20]

where t is the time and R_l and R_v are the lateral and vertical etch rates, respectively. For isotropic etching, $R_l = R_v$ and $A_f = 0$.

The major disadvantage of wet chemical etching for pattern transfer is the undercutting of the layer underneath the mask, resulting in a loss of resolution in the etched pattern. In practice, for isotropic etching, the film thickness should be about one-third or less of the resolution required. If patterns are required with resolutions much smaller than the film thickness, anisotropic etching (i.e., $1 \geq A_f > 0$) must be used. In practice, the value of A_f is chosen to be close to unity. Figure 19*c* shows the limiting case where $A_f = 1$, corresponding to $l = 0$ (or $R_l = 0$).

To achieve high-fidelity transfer of the resist patterns required for ultralarge-scale integration processing ($A_f = 1$), dry etching methods have been developed. Dry etching is synonymous with plasma-assisted etching, which denotes several techniques that use plasma in the form of low-pressure discharges. Dry-etch methods include plasma etching, reactive ion etching (RIE), sputter etching, magnetically enhanced RIE (MERIE), reactive ion beam etching, and high-density plasma (HDP) etching.

13.4.1 Plasma Fundamentals

Plasma is a fully or partially ionized gas composed of equal numbers of positive and negative charges and a different number of unionized molecules. A simple capacitively coupled radio frequency (rf) plasma etcher schematically shown in Fig. 20 is used to demonstrate the plasma fundamentals. The cathode is capacitively coupled to an rf generator and the anode is grounded, similarly to the sputtering discussed in the previous chapter. The rf frequency is typically 13.56 MHz because of its non-interference with radio-transmitted signals. The plasma is initiated by free electrons always present in a gas, generated by cosmic rays, thermal excitation, or other means. The free electrons oscillate and gain kinetic energy from the rf electric field and collide with gas molecules. The energy transferred

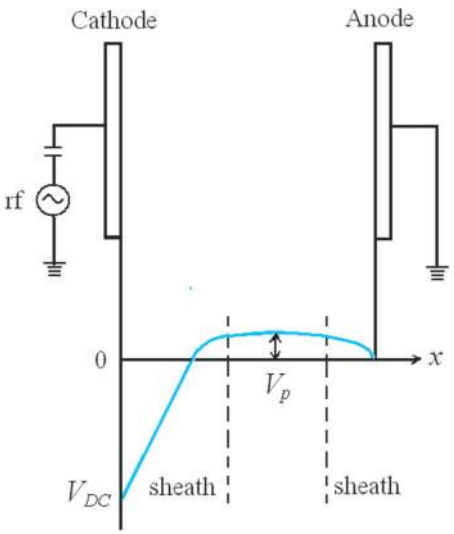

Fig. 20 Schematic system and approximate time-averaged potential distribution of a capacitively coupled rf plasma system.

in the collision causes the gas molecules to be ionized. When the applied voltage is larger than the breakdown potential of the gas, sustainable plasma is generated throughout the reaction chamber. The ionization rate is on the order of 10^{-4} to 10^{-6}.

Sheath

The formation of sheath in dry etching is similar to that in rf sputtering discussed in Chapter 12. Plasma is electrically neutral in the central region of the chamber. Electrons are more mobile than positive ions, and therefore more electrons are attracted to the front surface of the electrodes during the positive half cycle than positive ions in the negative half cycle. Therefore, the current is larger in the positive cycle than that in the negative cycle. The resultant electron current charges up the capacitively coupled electrode (powered electrode) since no charge can be transferred through the capacitor. The powered electrode (cathode) acquires an increasing negative bias voltage during successive cycles until the negative average voltage V_{DC} (also called 'self-bias') is sufficiently high to retard the electrons and the net charge arriving at the surface is zero. The magnitude of the powered electrode self-bias voltage depends on the amplitude and frequency of the voltage applied to the electrode. Since the powered electrode develops a negative self-bias, the plasma forms a compensating positive potential V_p relative to the grounded anode, as shown in the lower part of Fig. 20.

The voltage gradients near the cathode and anode form intense electric fields near plasma-electrode interfaces known as sheaths (also called dark space because the high-energy electrons there are more likely to cause ionization than light-generating excitation) that play a significant role in the plasma etching processes. Since typical sheaths are thin (~ 10 μm to 1 mm) and conformal with the electrode surface, positive ion energy gain is primarily in the direction normal to the surface and the ion beam is essentially unidirectional there. Anisotropic etching relies on bombardment of unidirectional energetic ions at the substrate surface, which can be placed on the cathode or anode. This is achieved in plasma etching reactors by accelerating positive ions in the sheath above the substrate surface. The asymmetric voltage distribution at the cathode and anode causes a very large field in front of the cathode in comparison with the field in front of the anode or in the glow region. Anisotropic etching is very strong on the cathode surface due to the very strong field there, and is weaker on anode surface due to the relatively weaker field.

13.4.2 Surface Chemistry

The plasma used for etching is not in thermal equilibrium. As a result, the temperature of electrons, which are the lightest component of the plasma, is substantially higher than the neutral gas and ion temperature. The electron temperature is approximately in the range of 20,000~100,000 K; the ion temperature might be up to 2,000 K, while neutral radicals and molecules are less than 1,000 K. These energetic electrons can therefore generate reactive radicals and ions and enhance chemical reactions that cannot be achieved by other means. Radicals produced during dissociation tend to be more reactive than the parent gases and these radicals can further enhance the surface processes and plasma chemistry.

Plasma etching has to satisfy many stringent requirements simultaneously, including control of feature sidewall and bottom surface profiles, etch selectivity to other exposed materials, uniformity of the etch process over large substrate surfaces, and interaction with preceding and following processing steps. The crucial points related to fundamental surface processes are physical sputtering, reactive ion etching (RIE), chemical etching, and polymer deposition.

Physical Sputtering

One of the simplest material removal processes is physical sputtering, which involves the bombardment of target material by energetic ions or neutrals. However, sputtering tends to be non-selective.

Reactive Ion Etching

Most plasma etching processes rely primarily on reactive ion etching for material removal. RIE involves simultaneous bombardment of energetic ions and reactive neutral radicals onto the material surface. Ions bombard the substrate surface almost normally and etching by the reactive neutral radicals occurs anisotropically. RIE is similar to sputtering, but more selective than physical sputtering due to its partially chemical nature from reactive neutral radicals.

Chemical Etching

A simple example of chemical plasma etching is Si etching using F, which has a high etch rate even at room temperature:

$$\mathrm{Si\ (solid)} + 4\mathrm{F} \rightarrow \mathrm{SiF_4\ (gas)}. \tag{13}$$

Chemical etching is often isotropic as incoming neutral etchants have a uniform angular distribution. However, for some crystalline materials, chemical etching can be sensitive to crystallographic orientation. During the fabrication of submicron-sized features in CMOS devices, chemical etching often cannot be tolerated due to its isotropic nature. Processing conditions are therefore chosen so as to minimize chemical etching.

Polymer Deposition

To generate small features, anisotropic etching also requires that etching take place only in the vertical direction with no etching in the horizontal direction. Although careful design of the plasma etching reactor and appropriate choice of etching gases can help to achieve these goals, one surface mechanism that has proven indispensable is polymer deposition. Presence of these films on vertical surfaces limits contact of the material surface with the etchant species to inhibit horizontal etching.

There are at least two mechanisms that can account for this buildup of sidewall passivation. The first is the deposition of polymeric material that is known to occur in plasma discharges with carbon-containing source gases. In the case of fluorine-containing Freons as source gases, this polymer deposition is linked to the formation of unsaturated CF_2 radicals generated by the plasma. The second source of material on feature sidewalls is the etch product species generated at horizontal surfaces exposed to ion bombardment. These products are frequently nonvolatile and can stick to and react with vertical surfaces not exposed to ion bombardment. This source of sidewall building is termed redeposition.

A series of sequential cross sections depicting the anisotropic etching of a feature with sidewall redeposition is shown in Fig. 21, in which the six sequential profiles result from five etch-redeposition-etch steps.

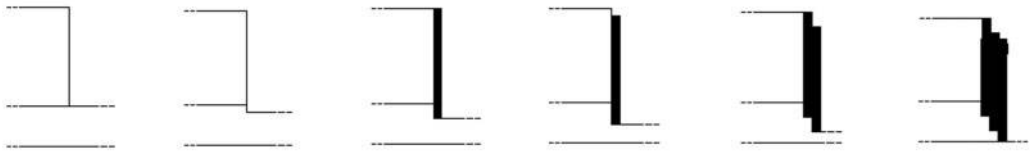

Fig. 21 **The sequential formation, from left to right, of an etching feature profile in the presence of redeposition. The etching of horizontal surfaces and redeposition onto vertical surfaces are assumed to occur sequentially.**

Substrate Temperature

Many of the above-mentioned fundamental surface processes take place simultaneously in etching processes. Plasma operating conditions must be carefully monitored to enhance or reduce the contribution of individual surface process and control the final results. One parameter that is particularly useful is the substrate temperature because many fundamental surface processes exhibit strong temperature dependence. For example, the chemical etching rate generally increases with surface temperature. Therefore, for processes in which both physical and chemical etching components are present, one can vary the degree of anisotropic or isotropic etching by varying the substrate temperature to control the feature profile.

13.4.3 Capacitively Coupled Plasmas Etchers

Dry etching technology in the IC industry has changed dramatically since the first application of plasma processing to photoresist stripping. A reactor for dry etching contains a vacuum chamber, pump system, power supply generators, pressure sensors, gas flow control units, and end-point detector. Each reactor uses a particular combination of pressure, electrode configuration and type, and source frequency to control the two primary etch mechanisms—chemical and physical. Higher etch rates and automation are required for most etchers used in IC fabrication. There are basically two groups of dry etchers based on how the plasma is produced: the capacitively coupled etchers and the inductively coupled etchers.[1]

In the simplest form of a capacitively coupled plasma etcher, etchant gases are injected between two parallel metallic electrodes with symmetrical size and position to which voltage is applied on one electrode. The potential drop across the gas breaks it down and generates the plasma. A significant fraction of the input power is consumed by ions accelerating in the sheaths, and is dissipated at the electrode surfaces (or substrates placed on them) during ion bombardment. Therefore, a small fraction of the input power is used for plasma generation. The gas dissociation fraction is low and electron density is also low (~ 10^9 to 10^{10} cm^{-3}). In addition, simple commercial capacitively coupled plasma etchers are typically operated at moderate gas pressures (~ 50 to 500 mTorr) and the scattering of gas prevents their use for fabrication of extremely small features.

As shown in Fig. 20, a wafer can be placed on the grounded electrode. This is the plasma etch mode with energetic ion bombardment since the plasma potential is always above the grounded potential. If a wafer is placed on the powered electrode (cathode), it is operated in the reactive ion etch mode with higher energetic ion bombardment due to higher self-bias V_{DC}. Physical and chemical etch mechanisms occur in both the plasma etch mode and the reactive ion etch mode. However, energies of bombarding ions are about ten times higher in the reactive ion etch mode.

Reactive Ion Etcher

A capacitively coupled plasma etcher operated in the reactive ion etch mode is called a reactive ion etcher (RIE) or a reactive sputter etcher (RSE). RIE has been extensively used in the microelectronic industry. The wafers are placed on the powered electrode (cathode). This allows the grounded electrode to have a significantly larger area, as shown in Fig. 22, and leads to significantly higher plasma-sheath potentials (20-500 V) at the wafer surface. The process can be explained as follows.

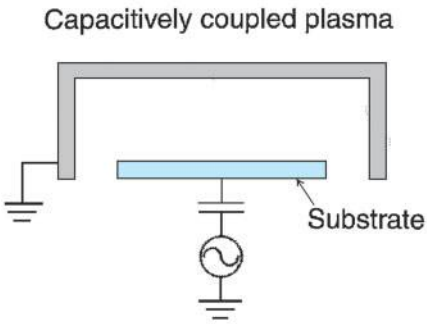

Fig. 22 **Capacitively coupled plasma etcher with larger area for the grounded electrode.**

The glow region of the plasma is a good electrical conductor. The dark spaces in plasma are areas of limited conductivity and can be modeled as capacitances, i.e., $C = A/d$, where A is the electrode area and d is the sheath thickness of the dark space. A voltage will split between two capacitances in series, i.e.

$$V_C/V_A = C_A/C_C = (A_A/d_A)/(A_C/d_C) \tag{14}$$

where V_C (C_C) and V_A (C_A) are the voltage drops (capacitances) over the sheath thicknesses of the dark space on the cathode and anode and A_C, A_A are the areas of the cathode and anode. The current between two electrodes is dominated by space-charge-limited current in a capacitively coupled plasma system. The space-charge-limited current (described in Section 2.7, Chapter 2) of positive ions must be equal on both anode and cathode, i.e.

$$V_C^{3/2}/d_C^2 = V_A^{3/2}/d_A^2 \tag{15}$$

Therefore,

$$V_C/V_A = (A_A/A_C)^4 \tag{16}$$

That is to say, the potential difference across the dark space of each electrode will be the same if the electrodes are of similar area. The increase of the relative surface area of the grounded electrode can increase the sheath voltage at the powered electrode. The etching rate can be much enhanced, but the etch selectivity of this system is relatively low because of strong physical sputtering. However, selectivity can be improved by choosing the proper etch chemistry, for example by polymerizing the silicon surface with fluorocarbon polymers to obtain selectivity of SiO_2 over silicon.

Magnetically Enhanced Reactive Ion Etcher

In the magnetically enhanced reactive ion etcher (MERIE), the magnetic field crossed with the electric field reduces electron mobility towards the electrodes and their loss there. Densities of electrons and other species in the plasma are therefore larger in MERIE reactors for the same input power, which enhances the material etch rate. For a given power, higher electron (and ion) densities in MERIE reactors will consume more fractional power and therefore smaller fractional power will be used to accelerate ions in the sheaths. Consequently, ion-bombardment-induced damage on the substrate and electrode surfaces diminishes. Etch uniformity is improved in MERIE reactors by either shaping the applied magnetic field or rotating it physically or electrically. Magnetically enhanced reactive ion etchers have been used extensively for dielectric etching in the semiconductor industry.

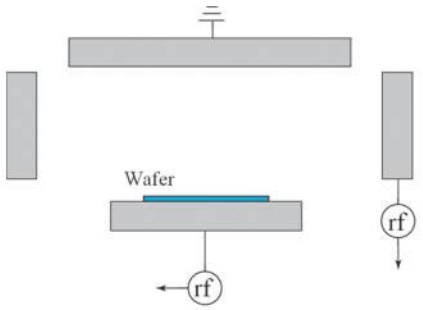

Fig. 23 **Schematic of a triode reactive ion etch reactor with two different radio-frequency power sources.**

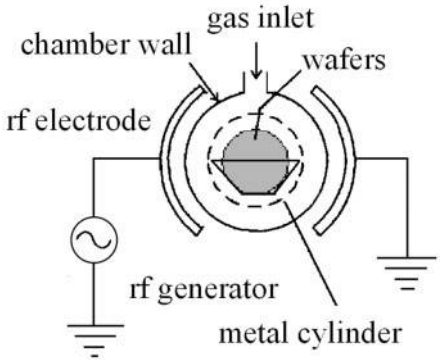

Fig. 24 **Schematic of a typical barrel reactor.**

Triode Reactive Ion Etcher

Another innovation in capacitively coupled plasma etcher design is the use of two (or more) sources at different frequencies as shown in Fig. 23. At the same input power, capacitively coupled plasmas are generated more efficiently at higher frequencies due to higher collision frequencies, and higher electron densities are accumulated at lower frequencies and hence higher self-biases are induced at the cathode. A high-frequency source (25 MHz and above) is therefore used in dual-frequency plasma systems to generate the plasma efficiently, while a low-frequency source (typically a few MHz or lower) accelerates ions. One can therefore obtain a higher plasma density relative to a simpler capacitive plasma system, and independently control ion energy as well.

Barrel Plasma Etcher

The barrel plasma reactor has been used primarily for resist stripping, as discussed in Ch. 12. It is one of the earliest plasma systems. The barrel reactor has a cylindrical design operated at a pressure of about 0.1 to 1 Torr. The power is applied on electrodes placed on both sides of the cylinder. An inner metal cylinder with holes can confine the plasma to the region between the metal cylinder and chamber wall (Fig. 24). The etchant species in the plasma diffuse through holes to etching area, while the energetic ions and electrons of the plasma cannot enter this region. Wafers are placed vertically on a quartz boat with a small separation between wafers, and placed parallel to the electric field to minimize physical etching. The etching is almost purely chemical with isotropic etching and high selectivity.

13.4.4 Inductively Coupled Plasma Etchers

Inductively coupled plasma (ICP) etchers were developed in the early 1990s to address the difficult process requirements of high-aspect-ratio (AR) oxide etch with high selectivity. ICP etchers are operated at lower gas pressure (~3 to 50 mtorr) than capacitively coupled plasma etchers. The lower pressure reduces gas collisions that cause loss of the etching profile. It also increases the mean free path of etchants and etching byproducts, and they can move easily into and out of high-aspect ratio features. However, the lower pressure also reduces the etch rate due

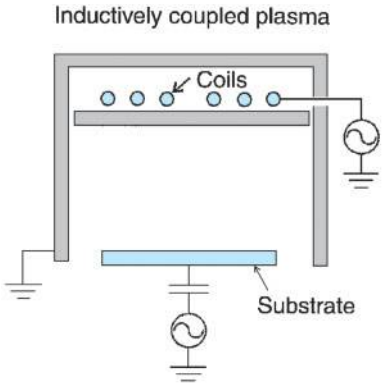

Fig. 25 **Inductively coupled plasma etcher.**

to the reduction in ion density. Therefore, high-density plasma (HDP) is needed to generate sufficient active species for an acceptable etch rate at lower pressures. The gas dissociation rate of HDP can reach about 10% compared with 0.1% of capacitively coupled plasmas etchers.

ICP etchers utilize a set of coils that are physically separated from the gas through a dielectric window as shown in Fig. 25. Radio-frequency current through the coils generates an electromagnetic wave that penetrates the plasma chamber, azimuthally accelerates electrons, and generates the plasma. As most of the input power is consumed by electrons, the electron density is substantially larger ($\sim 10^{11}$- 10^{12} cm^{-3}) in ICP etchers than in capacitively coupled plasmas. Therefore, the ICP etcher is a high-density plasma (HDP) etcher.

In addition, a second source can be used in ICP etchers to separately bias the substrate during etching and impart energy to bombarding ions to enhance the etch rate. As separate sources are used for plasma generation and ion acceleration, high-aspect-ratio oxide etching is possible. Although a higher degree of dissociation enhances etch rate, it has detrimental effects on material selectivity in many cases.

Electron Cyclotron Resonance (ECR) Plasma Etcher

The ECR plasma etcher shown in Fig. 26, which is similar to an ICP etcher, uses resonant wave-plasma interaction. In an ECR etcher, microwave (typically at 2.45 GHz) is launched into a magnetized chamber containing the etchant gas at low pressure (<10 mTorr). Electron cyclotron resonance occurs at spatial locations where the local electron cyclotron frequency (eB/m_e) matches the applied frequency. By carefully designing the magnetic field profile, one can obtain high-density uniform plasma above the substrate surface. Plasma densities in ECR etchers are higher or comparable to ICP reactors. The ECR etcher is also a HDP etcher. Electron cyclotron resonance etchers are also operated at lower gas pressures than capacitively coupled plasma etchers and allow independent biasing of the substrate. Similarly to ICP, ECR etchers are characterized by high degrees of gas dissociation.

Neutral Beam Plasma Etcher

Because of the presence of charged species or ultraviolet radiation in plasma, electrical damage to circuits on the substrate remains a constant concern during plasma etching. To alleviate this problem, plasma etch sources that rely on energetic neutral beams have been developed in recent years. A typical neutral beam source is shown in Fig. 27, and similar designs have been used in the past for ion milling applications. Plasma of the appropriate gas is generated through conventional means and is then allowed to seep through holes in the electrodes. Ions can then be accelerated and neutralized before they bombard the substrate, resulting in energetic neutral-species bombardment on the substrate. Neutral beam sources are under development currently and have not yet been used for high-volume production. Another technique that has been utilized to alleviate plasma charge damage is

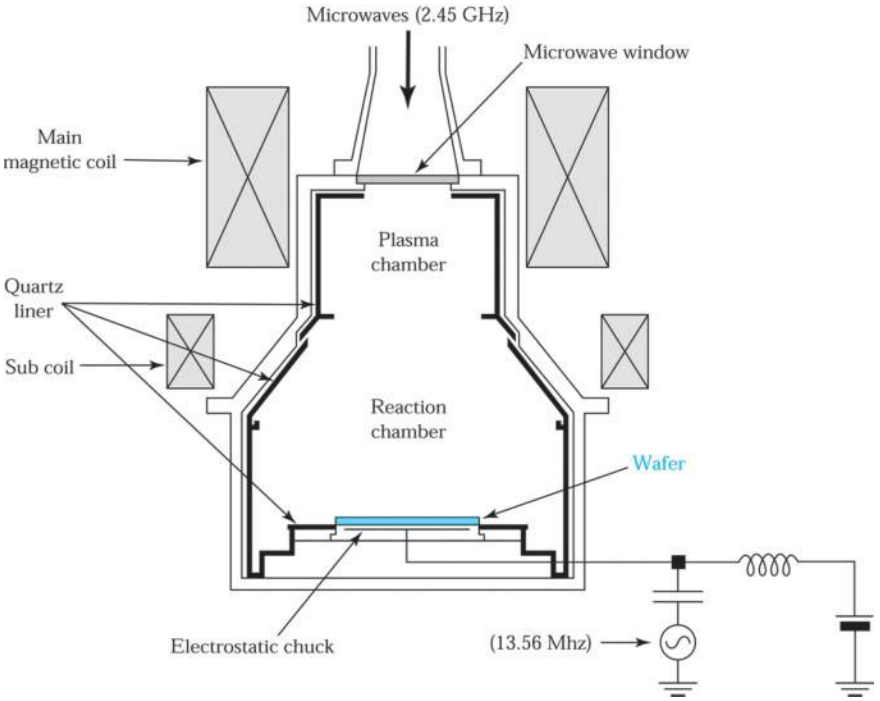

Fig. 26 **Schematic of an electron cyclotron resonance reactor.**[21]

to generate the plasma remotely, i.e., away from the substrate, and transport neutral species to the substrate so that ions are either excluded or neutralized. Remote plasma sources or chemical downstream etchers are used for many plasma cleaning and material treatment applications. These etchers are also useful for high-rate removal of blanket films that do not have any patterned features. Their application for anisotropic etching applications is, however, limited due to the broad angular distribution of neutral etchants.

Single-Wafer Etcher

For modern circuits with nanometer feature sizes, etching processes are more critical. More vertical profiles, better linewidth control, higher selectivity, and better uniformity are necessary. One approach to this problem is to use single-wafer etchers that etch one wafer at a time. Single-wafer etchers can tailor the electrode geometry and gas flow to maximize etch uniformity across the wafer. These machines are easily automated to perform wafer cassette-to-cassette operations so that no operator handling is required. They can incorporate a

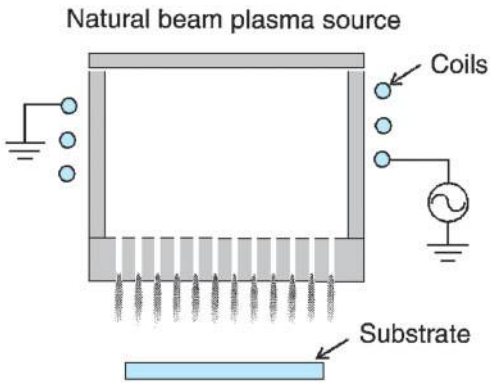

Fig. 27 **Neutral beam plasma etcher.**

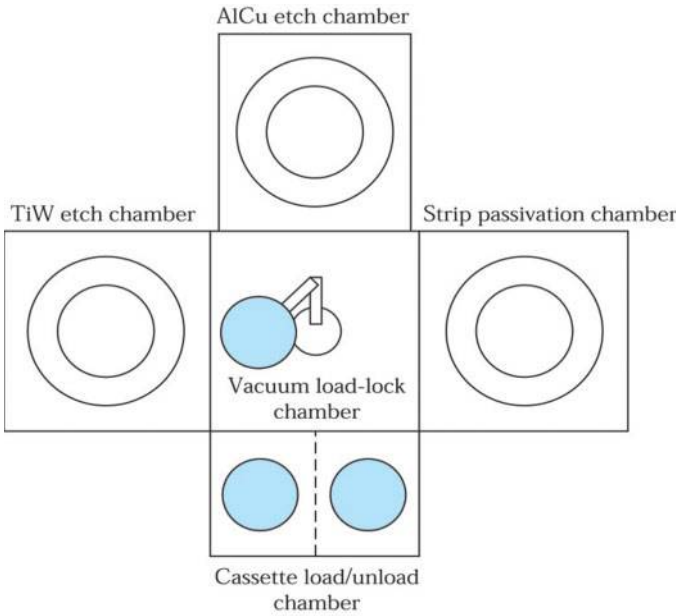

Fig. 28 **Cluster reactive ion etch tool for multilayer metal (TiW/AlCu/TiW) interconnect etching.**[2]

load-locked chamber so that the process chamber need not be vented under normal use. This enhanced uniformity, combined with automatic endpoint detection and microprocessor control, can also provide good process control.

A drawback of single-wafer etchers is that they must etch at higher rates to compete with the throughput of batch etchers. This constraint forces commercial singer-wafer etchers to operate at higher rf power densities and sometimes higher pressures, where process control and selectivity are more difficult to achieve. For this reason, some manufactures offer hybrid reactors that combine a few single-wafer etchers in one machine.

Clustered Plasma Processing

Semiconductor wafers are processed in clean rooms to minimize exposure to ambient particulate contamination. As device dimensions shrink, particulate contamination becomes a more serious problem. To minimize particulate contamination, clustered plasma tools use a wafer handler to pass wafers from one process chamber to another in a vacuum environment. The clustered plasma processing tools can also increase throughput. Figure 28 shows the multilayer metal interconnect (TiW/AlCu/TiW) etching process with clustered tools of an AlCu etch chamber, a TiW etch chamber, and a strip passivation chamber. The clustered tools provide an economic advantage through their high chip yield because the wafer is exposed to less ambient contamination and is handled less.

13.4.5 Plasma Diagnostics and End-Point Control

Plasma Diagnostics

Most processing plasmas emit radiation from infrared to ultraviolet. A simple analytical technique is to measure the intensity of these emissions versus wavelength with the aid of optical emission spectroscopy (OES). Using observed spectral peaks, it is usually possible to determine the presence of neutral and ionic species by correlating these emissions with previously determined spectral series. Relative concentrations of the species can be obtained by correlating changes in intensity with the plasma parameter. The emission signal derived from the primary etchant or byproduct begins to rise or fall at the end of the etch cycle.

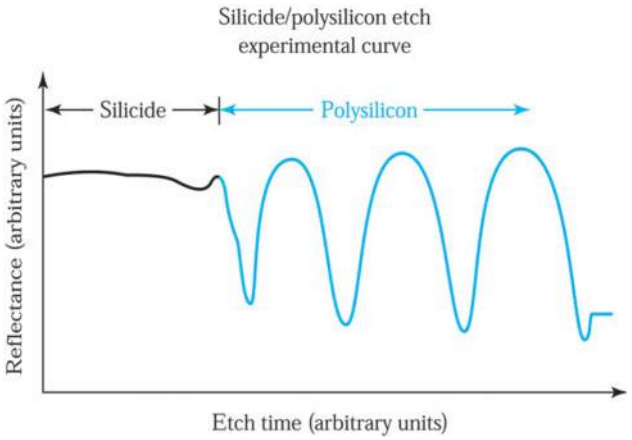

Fig. 29 **The relative reflectance of the etching surface of a composite silicide/poly-Si layer. The end point of the etch is indicated by cessation of the reflective oscillation.**

End-Point Control

Dry etching differs from wet chemical etching in that dry etching does not have enough etch selectivity to the underlying layer. Therefore, the plasma reactor must be equipped with a monitor that indicates when the etching process is to be terminated (i.e., an end point detection system). Laser interferometry of the wafer surface is used to continuously monitor etch rates and to determine the end point. During etching, the intensity of laser light reflected from a thin film surface oscillates because of the phase interference between the light reflected from the outer and inner interfaces of the etching layer. This layer must therefore be optically transparent or semitransparent to observe the oscillation. Figure 29 shows a typical signal from a silicide/polycrystalline Si gate etch. The period of the oscillation is related to the change in film thickness by

$$d \quad / 2\bar{n} \tag{17}$$

where Δd is the change in film thickness for one period of reflected light, λ is the wavelength of the laser light, and $\bar{n}$ is the refractive index of the etching layer. For example, Δd for polysilicon is 80 nm, measured by using a helium-neon laser source for which $\lambda = 632.8$ nm. The end point of the etch is indicated by the cessation of the reflection oscillation.

13.4.6 Etching Chemistries and Applications

Besides the etching equipment, etch chemistry also plays a critical role in the performance of etch processes. Table 2 lists some etch chemistries for different etch processes.

Silicon Trench Etching

As device feature size decreases, a corresponding decrease is needed in the wafer surface area occupied by the isolation between circuit elements and the storage capacitor of a DRAM cell. This surface area can be reduced by etching trenches into the silicon substrate and filling them with suitable dielectric or conductive materials. Deep trenches, usually with depths greater than 5 μm, are used mainly for forming storage capacitors. Shallow trenches, usually with depths less than 1 μm, are often used for isolation.

Chlorine-based and bromine-based chemistries have a high silicon etch rate and high etch selectivity to the silicon dioxide mask. The combination HBr + NF_3 + SF_6 + O_2 gas mixtures is used to form a trench capacitor with a depth of ~7 μm. It is also used for shallow trench isolation etching. Aspect-ratio-dependent

TABLE 2 ETCH CHEMISTRIES OF DIFFERENT ETCH PROCESSES

Material being etched	Etching chemistry
Deep Si trench	$HBr/NF_3/O_2/SF_6$
Shallow Si trench	$HBr/Cl_2/O_2$
Poly Si	$HBr/Cl_2/O_2$, HBr/O_2, BCl_3/Cl_2, SF_6
Al	BCl_3/Cl_2, $SiCl_4/Cl_2$, HBr/Cl_2
AlSiCu	$BCl_3/Cl_2/N_2$
W	SF_6 only NF_3/Cl_2
TiW	SF_6 only
WSi_2, $TiSi_2$, $CoSi_2$	CCl_2F_2/NF_3, CF_4/Cl_2, $Cl_2/N_2/C_2F_6$
SiO_2	$CF_4/CHF_3/Ar$, C_2F_6, C_3F_8, C_4F_8/CO,C_5F_8, CH_2F_2
Si_3N_4	CHF_3/O_2, CH_2F_2, CH_2CHF_2, SF_6/He

etching (i.e., variation in etch rate with aspect ratio) is often observed in submicron-deep silicon trench etching, caused by limited ion and neutral transport within the trench. Trenches with large aspect ratios are etched more slowly than trenches with small aspect ratios.

Polysilicon and Polycide Gate Etching

Polysilicon or polycide (i.e., low-resistance metal silicides over polysilicon) is usually used as a gate material for MOS devices. Anisotropic etching and high etch selectivity to the gate oxide are the most important requirements for gate etching. For example, the selectivity required in 1G DRAM is more than 150 (i.e., the ratio of etch rates for polycide and gate oxide is 150:1). Achieving high selectivity and etch anisotropy at the same time is difficult for most ion-enhanced etching processes. Therefore, multistep processing is used in which different etch steps in the process are optimized for etch anisotropy and selectivity. On the other hand, the trend in plasma technology for anisotropic etching and high selectivity is to utilize a low-pressure, high-density plasma using relatively low power. Most chlorine-based and bromine-based chemistries can be used for gate etching to achieve the required etch anisotropy and selectivity.

Dielectric Etching

The patterning of dielectrics, especially silicon dioxide and silicon nitride, is a key process in the manufacture of modern semiconductor devices. Because of their higher bonding energies, dielectric etching requires aggressive ion-enhanced, fluorine-based plasma chemistry. Vertical profiles are achieved by sidewall passivation as discussed in Section 13.4.2, typically by introducing a carbon-containing fluorine species to the plasma (e.g., CF_4, CHF_3, C_4F_8). High ion-bombardment energies are required to remove this polymer layer from the oxide, as well as to mix the reactive species into the oxide surface to form SiF_x products.

A low-pressure, high-density plasma is advantageous for aspect-ratio-dependent etching. However, the high-density plasma etchers (HDP, e.g., ICP and ECR) generate high-temperature electrons and subsequently produce a high degree of dissociation of ions and radicals, far more active radicals and ions than RIE or MERIE plasmas. In particular, a high F concentration worsens the selectivity to silicon. Various methods have been tried to enhance the selectivity in the high-density plasma. A parent gas with a high C/F ratio, such as C_2H_6, C_4H_8, or C_5H_8, has been successfully tried. Also, other methods to scavenge F radicals have been developed.[22]

Interconnect Metal Etching

Etching of a metallization layer is a very important step in IC fabrication. Aluminum, copper, and tungsten are the most popular materials used for interconnection. These materials usually require anisotropic etching. Chlorine-based (e.g., Cl_2/BCl_3 mixture) chemistry has a very high chemical etch rate with aluminum and tends to produce an

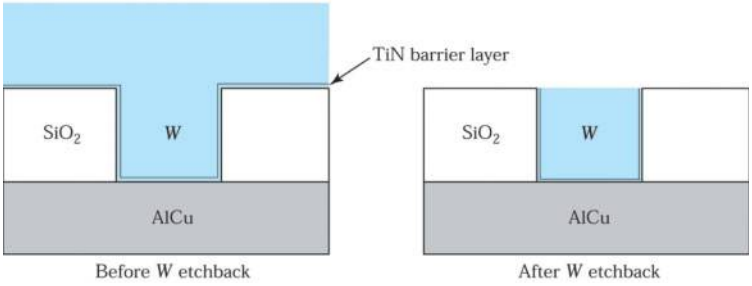

Fig. 30 Formation of tungsten plug in a contact hole by depositing blanket low-pressure chemical-vapor deposition W and then using reaction ion etching etchback.

undercut during etching. Carbon-containing gas (e.g., CHF_3) or N_2 is added to form sidewall passivation during aluminum etching to obtain anisotropic etching.

Copper has attracted much attention because of its low resistivity (~1.7 μohm-cm) and superior resistance to electromigration compared with Al or Al alloys. However, because of the low volatility of copper halides, plasma etching at room temperature is difficult. Process temperatures higher than 200 °C are required to etch copper films. Therefore, the damascene process is used to form Cu interconnection without dry etching. Damascene processing, as discussed in Chapter 12, involves the creation of interconnect lines by first etching a trench or canal in a planar dielectric layer and then filling that trench with metal, such as aluminum or copper. In dual damascene processing shown in Fig. 26 in Section 12.5.4, Chapter 12, a second level is involved where a series of holes (i.e., contacts or vias) are etched and filled in addition to the trench. After filling, the metal and dielectric are planarized by chemical-mechanical processing (CMP). The advantage of damascene processing is that it eliminates the need for metal etch. This is an important concern as the industry moves from aluminum to copper interconnections.

Low-pressure CVD (LPCVD) tungsten (W) has been widely used for filling contact holes and first-level metallization because of its excellent deposition conformability. Both fluorine- and chlorine-based chemistries etch W and form volatile etch products. An important tungsten etch processes is the blanket W etchback to form a W plug. The blanket LPCVD W is deposited on top of a TiN barrier layer, as shown in Fig. 30. A two-step process is usually used. First, 90% of the W is etched at a high etch rate, and then the etch rate is reduced to remove the remaining W with an etchant with a high W-to-TiN selectivity.

▶ SUMMARY

The continued growth of the semiconductor industry is a direct result of the ability to transfer smaller and smaller circuit patterns onto semiconductor wafers. The two major processes for transferring patterns are lithography and etching.

Currently, the vast majority of lithographic equipment is optical systems. The primary factor limiting resolution in optical lithography is diffraction. However, because of advancements in excimer lasers, photoresist chemistry, and resolution enhancement techniques such as the PSM, OPC and immersion technique, optical lithography will remain the mainstream technology, at least to the 32 nm generation.

Electron-beam lithography is the technology of choice for mask making and nanofabrication, in which new device concepts are explored. Other lithographic processing technologies are EUV and ion-beam lithography. Although all these have 100 nm or better resolution, each process has its own limitation: proximity effect in electron-beam lithography, mask blank production difficulties in EUV lithography, and stochastic space charge in ion-beam lithography.

At the present time, no obvious successor to optical lithography can be identified unambiguously. However, a mix-and-match approach can take advantage of the unique features of each lithographic process to improve resolution and to maximize throughput.

Wet chemical etching is used extensively in semiconductor processing. It is particularly suitable for blanket etching. We have discussed wet chemical etching processes for silicon and gallium arsenide, insulators, and metal

interconnections. The undercutting of the layer underneath the mask has resulted in loss of resolution in the etched pattern.

Dry etching methods are used to achieve high-fidelity pattern transfer. We have considered plasma fundamentals and various dry-etching systems, which have grown from relatively simple, parallel-plate configurations to complex chambers with multiple-frequency generators and a variety of process-control sensors.

The challenges for future etching technology are high etch selectivity, better critical-dimension control, high aspect-ratio–dependent etching, and low plasma-induced damage. Low-pressure, high-density plasma reactors are necessary to meet these requirements. As processing evolves from 300 mm to even larger wafers, continued improvements are required for etch uniformity within the wafer. New gas chemistries must be developed to provide the improved selectivity necessary for advanced integration circuits.

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▶ PROBLEMS (* DENOTES DIFFICULT PROBLEMS)

FOR SECTION 13.1 OPTICAL LITHOGRAPHY

1. For a class-100 clean room, find the number of dust particles per cubic meter with particle sizes (a) between 0.5 and 1 μm, (b) between 1 and 2 μm, and (c) above 2 μm.
2. Find the final yield for a nine-mask–level process in which the average fatal defect density per cm^2 is 0.1 for four levels, 0.25 for four levels, and 1.0 for one level. The chip area is 50 mm^2.
3. An optical lithographic system has an exposure power of 0.3 mW/cm^2. The required exposure energy for a positive photoresist is 140 mJ/cm^2 and for a negative photoresist is 9 mJ/cm^2. Assuming negligible times for loading and unloading wafers, compare the wafer throughput for positive photoresist and negative photoresist.
4. (a) For an ArF excimer laser 193 nm optical lithographic system with NA 0.65, k_1 0.60, and k_2 0.50, what are the theoretical resolution and depth of focus for this equipment? (b) What can we do in practice to adjust NA, k_1, and k_2 parameters to improve resolution? (c) What parameter does the phase-shift mask (PSM) technique change to improve resolution?
5. The plots in Fig. 9 are called *response curves* in microlithography. (a) What are the advantages and disadvantages of using resists with high γ values? (b) Conventional resists cannot be used for 248 nm or 193 nm lithography. Why not?

FOR SECTION 13.2 NEXT-GENERATION LITHOGRAPHIC METHODS

6. (a) Explain why a shaped beam promises higher throughput than a Gaussian beam in e-beam lithography. (b) How can alignment be performed for e-beam lithography?
7. Why has the operating mode of optical lithographic systems evolved from proximity printing to 1:1 projection printing and finally to 5:1 projection step-and-repeat?

FOR SECTION 13.3 WET CHEMICAL ETCHING

8. If the mask and the substrate cannot be etched by a particular etchant, sketch the edge profile of an isotropically etched feature in a film of thickness h_f for (a) etching just to completion, (b) 100% overetch, and (c) 200% overetch.

9. A <100>-oriented silicon crystal is etched in a KOH solution through a 1.5 μm × 1.5 μm window defined in silicon dioxide. The etch rate normal to (100)-planes is 0.6 μm/min. The etch rate ratios are 100:16:1 for the (100):(110):(111)-planes. Show the etched profile after 20 seconds, 40 seconds, and 60 seconds.

10. Repeat the previous problem. a $<\bar{1}10>$-oriented silicon is etched with a thin SiO_2 mask in KOH solution. Show the etched pattern profiles on $<\bar{1}10>$-Si.

11. A <100>-oriented silicon wafer 150 mm in diameter is 625 μm thick. The wafer has 1000 μm × 1000 μm ICs on it. The IC chips are to be separated by orientation-dependent etching. Describe two methods for doing this and calculate the fraction of the surface area that is lost in these processes.

FOR SECTION 13.4 DRY ETCHING

***12.** The average distance traveled by particles between collisions is called the mean free path (λ), $\lambda \cong 5 \times 10^{-3}/P$(cm), where P is pressure in Torr. In typical plasmas of interest, the chamber pressure ranges from 1 Pa to 150 Pa. What are the corresponding density of gas molecules (cm^{-3}) and the mean free path?

13. Fluorine (F) atoms etch Si at a rate given
by Etch Rate (nm/min) = $2\,86 \times 10^{-13}\, n_F \times T^{1/2}\, e^{-Ea/RT}$
where n_F is the concentration of F atoms (cm^{-3}), T the temperature (K), and E_a and R the activation energy (2.48 kcal/mol) and gas constant (1.987 cal-K), respectively. If n_F is 3×10^{15}, calculate the etch rate of Si at room temperature.

14. Repeat the previous problem. SiO_2 etched by F atoms can also be expressed by
Etch rate (nm/min) = $0.614 \times 10^{-13}\, n_F \times T^{1/2}\, e^{-Ea/RT}$
where n_F is 3×10^{15} (cm^{-3}) and E_a is 3.76 kcal/mol. Calculate the etch rate of SiO_2 and etch selectivity of SiO_2 over Si at room temperature.

15. A multiple-step etch process is required for etching a polysilicon gate with thin gate oxide. How do you design an etch process that has no micromasking, has an anisotropic etch profile, and is selective to thin gate oxide?

16. Find the etch selectivity required to etch a 400-nm polysilicon layer without removing more than 1 nm of its underlying gate oxide, assuming that the polysilicon is etched with a process having a 10% etch-rate uniformity.

17. A 1 μm Al film is deposited over a flat field oxide region and patterned with photoresist. The metal is then etched with a mixture of BCl_3/Cl_2 gases at a temperature of 70°C in a Helicon etcher. The selectivity of Al over photoresist is maintained at 3. Assuming a 30% overetch, what is the minimum photoresist thickness required to ensure that the top metal surface is not attacked?

18. In an ECR plasma, a static magnetic field B forces electrons to circulate around the magnetic field lines at an angular frequency, ω_e, that is given by

$$\omega_e = qB/m_e,$$

where q is the electronic charge and m_e the electron mass. If the microwave frequency is 2.45 GHz, what is the required magnetic field?

19. What are the major distinctions between the traditional reactive ion etching and high-density plasma etching (ECR, ICP, etc.)?

20. Describe how to eliminate corrosion issues in Al lines after etching with chlorine-based plasma.