

ADD R2, R3, R4:

Signal name	Value	. . . 8 . . . 16 . . . 24 . . . 32 . . .
CLK	1	
PCnext	00000001	
PCout	00000001	
PCplus	00000001	
state	17	
RB	00	
rs1	02	
rs2	00	
rd	03	
sa	zz	
Function	01	
RegWr	1	
JalSig	0	
PCPlusTemp	00000002	
busA	00000002	
busB	00000000	
busW	00000002	
res	00000002	
res_req	00000002	

SUB R2, R3, R4

CLK	0	
PCnext	00000001	
PCout	00000001	
PCplus	00000001	
state	00	
RB	02	
rs1	01	
rs2	02	
rd	01	
sa	00	
busA	zzzzzzz?	
busB	00000005	
busW	FFFFFFFFB	
res	FFFFFFFFB	
res_req	FFFFFFFFB	

AND R2, R3, R4

signal name	value					
CLK	1					39.5
PCnext	00000001			00000001		
PCout	00000001			00000000		
PCplus	00000001			00000001		
state	00	00	01	0A	17	
RB	00	xx		00		
rs1	02	xx		02		
rs2	00	xx		00		
rd	03	xx		03		
sa	zz					
Function	00	xx		00		
RegWr	1					
JalSig	0					

busA	00000002			00000002		
busB	00000000			00000000		
busW	00000000			xxxxxxxx		
res	00000000	xxxxxxxx		00000000		
res_reg	00000000			xxxxxxxx		00000000

CMP R2, R3, R4

signal name	value					
CLK	1					2
PCnext	00000001	xxxxxxxx		00000001		
PCout	00000001			00000000		
PCplus	00000001	xxxxxxxx		00000001		
state	00	00	02	0E		
RB	04	xx		04		
rs1	02	xx		02		
rs2	04	xx		04		
rd	03	xx		03		
sa	zz					
Function	03	xx		03		
RegWr	0					

busA	xxxxxxxx	xxxxxxxx		00000005		
busB	xxxxxxxx	xxxxxxxx		00000005		
busW	xxxxxxxx				xxxxxxxx	

request	0					
WbData	0					
z_falg	1					
ial flan	0					

ANDI R2, R3, 2'b11

Signal name	Value	0	8	16	24	32	40	48
CLK	1 to 0							
PCnext	xxxxxxxx				00000001			
PCout	xxxxxxxx			00000000				0000
PCplus	xxxxxxxx			00000001				
state	00	00		03		10		17
RB	xx	xx		00				
rs1	xx	xx		02				
rs2	xx	xx		00				
rd	xx	xx		03				
JUMP_OUT_reg	00000003		xxxxxxxx			00000003		
Extend_out	00000003			00000003				
Extend_out_reg	00000003		xxxxxxxx			00000003		
InstMemOut_reg	0086001C			0086001C				
BusBReg	00000000		xxxxxxxx			00000000		
BusAReg	00000005		xxxxxxxx			00000005		
res	00000001		xxxxxxxx		00000000		00000001	
res_reg	00000001		xxxxxxxx		00000000		00000001	

ADDI R2, R3, 2'b11

Signal name	Value	0	8	16	24	32	40	48
CLK	1 to 0							
PCnext	xxxxxxxx				00000001			
PCout	xxxxxxxx			00000000				0000
PCplus	xxxxxxxx			00000001				
state	00	00		03		10		17
RB	xx	xx		00				
rs1	xx	xx		02				
rs2	xx	xx		00				
rd	xx	xx		03				
JUMP_OUT_reg	00000003		xxxxxxxx			00000003		
Extend_out	00000003			00000003				
Extend_out_reg	00000003		xxxxxxxx			00000003		
InstMemOut_reg	0086001C			0086001C				

res	xxxxxxx	xxxxxxx	00000000	00000008	
res_reg	xxxxxxx	xxxxxxx	00000000	00000008	

SLLV R2, R3, R4.

CLK	1 to 0	
PCnext	xxxxxxx	00000001
PCout	xxxxxxx	00000000
PCplus	xxxxxxx	00000001
state	00	00 01 00 17 00
RB	xx	xx 04
rs1	xx	xx 02
rs2	xx	xx 04
rd	xx	xx 03
sa	xx	xx 03
Function	xx	xx 02
RegWr	0	
stop_flag	x	
BusBReg	xxxxxxx	xxxxxxx 00000005
BusAReg	xxxxxxx	xxxxxxx 00000005
op1	zzzzzzzz	
busw	xxxxxxx	xxxxxxx 00000000
res	xxxxxxx	xxxxxxx 00000005 000000A0
res_reg	xxxxxxx	xxxxxxx 00000005 000000A0

SLRV R2, R3, R4.

CLK	1 to 0	
PCnext	xxxxxxx	00000001
PCout	xxxxxxx	00000000
PCplus	xxxxxxx	00000001
state	00	00 01 00 17 00
RB	xx	xx 04
rs1	xx	xx 02
rs2	xx	xx 04
rd	xx	xx 03
sa	xx	xx 03
Function	xx	xx 02
RegWr	0	

stop_flag	x				
BusBReg	xxxxxxx	xxxxxxx	00000005		
BusAReg	xxxxxxx	xxxxxxx	00000005		
op1	zzzzzzzz				
busvv	xxxxxxx	xxxxxxx	00000000		
res	xxxxxxx	xxxxxxx	00000005	00000000	
res_reg	xxxxxxx	xxxxxxx	00000005	00000000	

SLL R2, R3, 3.

busW	xxxxxxx	xxxxxxx	00000028		
res	xxxxxxx	xxxxxxx	00000005	00000028	
res_reg	xxxxxxx	xxxxxxx	00000005	00000028	

SLR R2, R3, 3.

busW	xxxxxxx	xxxxxxx	00000000		
res	xxxxxxx	xxxxxxx	00000005	00000000	
res_reg	xxxxxxx	xxxxxxx	00000005	00000000	

J

CLK	1 to 0				
PCnext	xxxxxxx	00000001	00000005	00000006	00000007
PCout	xxxxxxx	00000000	00000004	00000005	00000006
PCplus	xxxxxxx	00000001	00000005	00000006	00000007
state	00	17	08	17	16

BEQ

CLK	1				
PCnext	00000007	00000001		00000003	00000004
PCout	00000006	00000000		00000002	00000003
PCplus	00000007	00000001		00000003	00000004
state	00	17	12	17	17

Jal

