Project: DSP

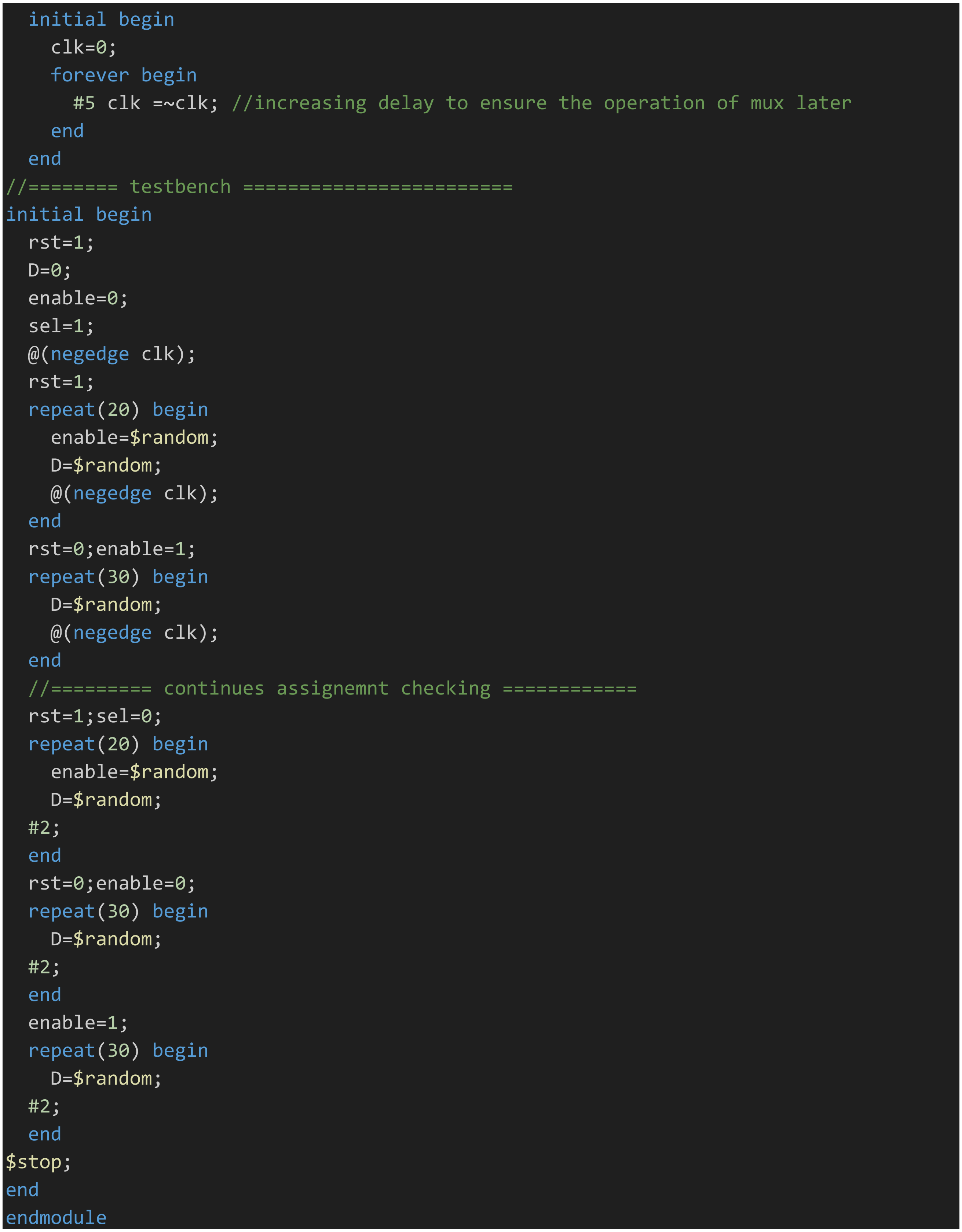
Name: **Osama Mohammed Sultan**

-Flipflop module design Code:

```
module ff_mux (D,clk,rst,enable,Q,sel);
parameter WIDTH =18;
parameter RSTTYPE="SYNC";
input [WIDTH-1:0] D;
output [WIDTH-1:0] Q;
reg[WIDTH-1:0] Q_r;
input rst,clk,enable,sel;
generate
  if (RSTTYPE=="SYNC") begin
    always @(posedge clk) begin
      if (rst) begin
        Q_r<=0;
      end
      else if (enable) begin
        Q_r<=D;
      end
    end
  end
  else if (RSTTYPE=="ASYNC") begin
    always @(posedge clk or posedge rst) begin
      if (rst) begin
        Q_r<=0;
      end
      else if (enable) begin
        Q_r<=D;
      end
    end
  end
endgenerate
assign Q=(sel)?Q_r:D;
endmodule
```

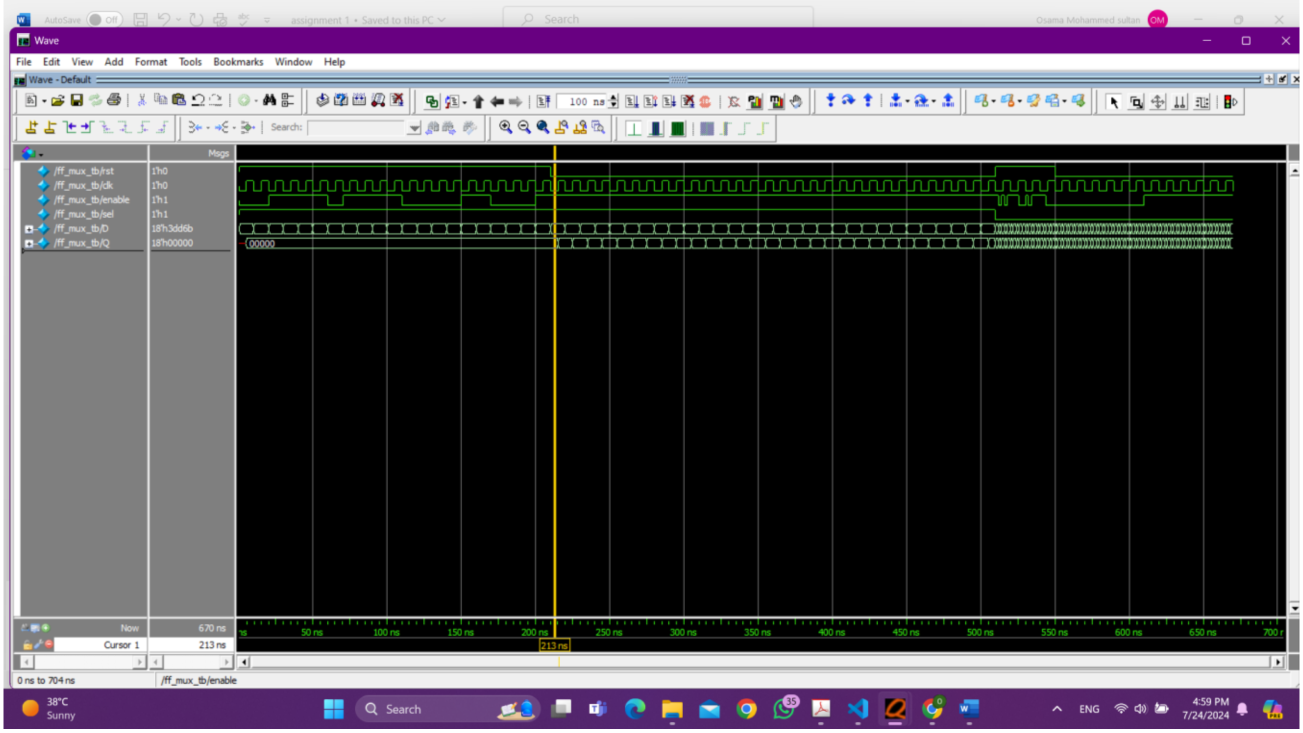
Flipflop module testbench Code:

```
module ff_mux_tb ();
  reg rst,clk,enable,sel;
  reg [17:0] D;
  wire [17:0] Q;
//======== DUT INIT. =======================
  ff_mux dut (.D(D),.rst(rst),.Q(Q),.clk(clk),.enable(enable),.sel(sel));
//========= clock generation ================
```



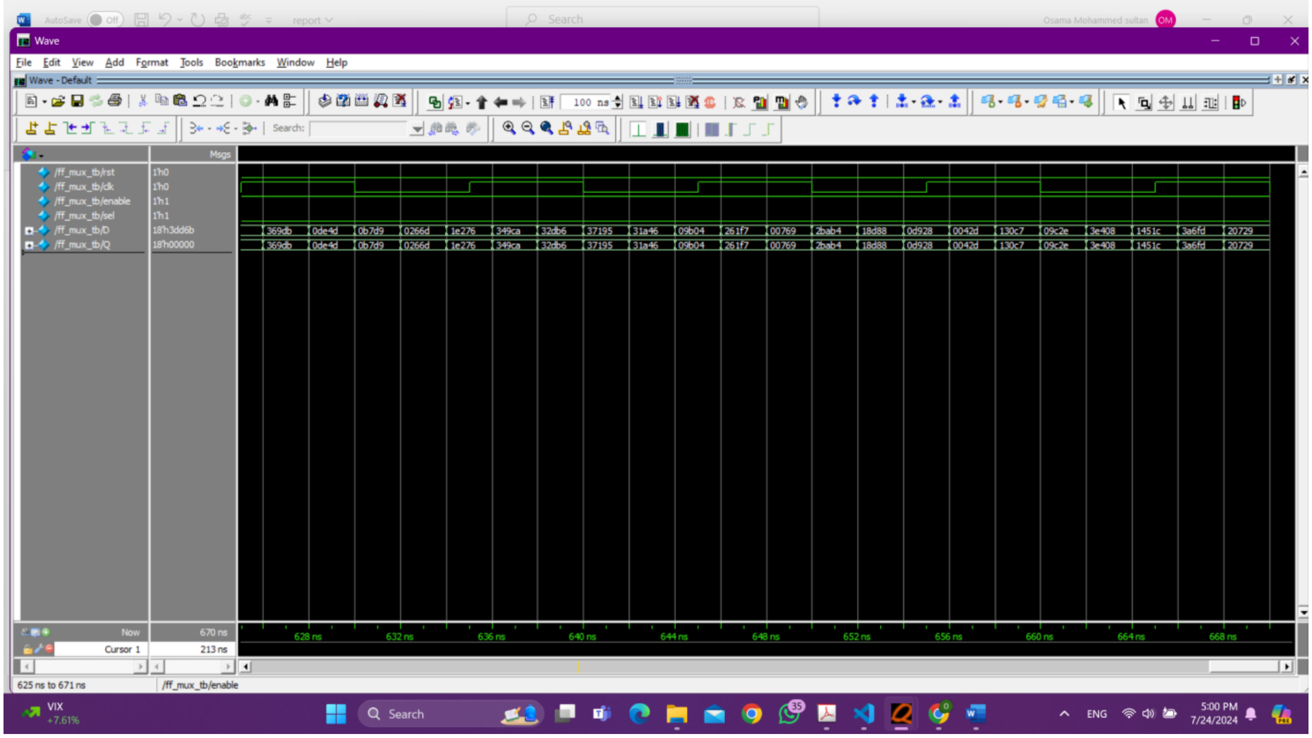
```
  initial begin
    clk=0;
    forever begin
      #5 clk =~clk; //increasing delay to ensure the operation of mux later
    end
  end
//======== testbench ========================
initial begin
  rst=1;
  D=0;
  enable=0;
  sel=1;
  @(negedge clk);
  rst=1;
  repeat(20) begin
    enable=$random;
    D=$random;
    @(negedge clk);
  end
  rst=0;enable=1;
  repeat(30) begin
    D=$random;
    @(negedge clk);
  end
  //========= continues assignemnt checking ============
  rst=1;sel=0;
  repeat(20) begin
    enable=$random;
    D=$random;
  #2;
  end
  rst=0;enable=0;
  repeat(30) begin
    D=$random;
  #2;
  end
  enable=1;
  repeat(30) begin
    D=$random;
  #2;
  end
$stop;
end
endmodule
```

Flipflop module simulation:



Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
00000
Now 670 ns
Cursor 1 213 ns
213 ns
ns 50 ns 100 ns 150 ns 200 ns 250 ns 300 ns 350 ns 400 ns 450 ns 500 ns 550 ns 600 ns 650 ns 700 r
0 ns to 704 ns
/ff_mux_tb/enable
38°C
Sunny
Search
ENG
4:59 PM
7/24/2024

	Msgs
/ff_mux_tb/rst	1'h0
/ff_mux_tb/clk	1'h0
/ff_mux_tb/enable	1'h1
/ff_mux_tb/sel	1'h1
/ff_mux_tb/D	18'h3dd6b
/ff_mux_tb/Q	18'h00000

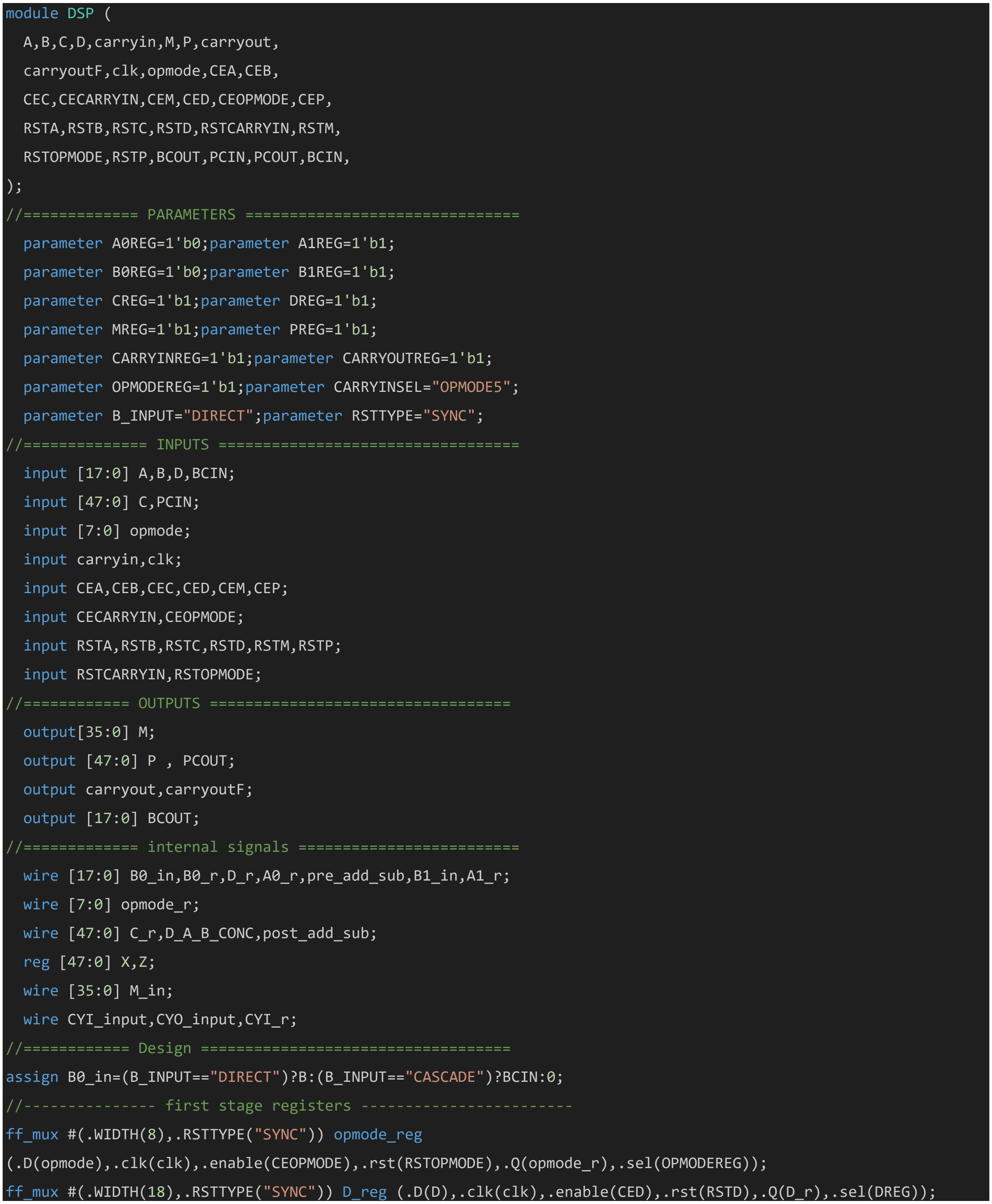


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
Now 670 ns
Cursor 1 213 ns
628 ns 632 ns 636 ns 640 ns 644 ns 648 ns 652 ns 656 ns 660 ns 664 ns 668 ns
625 ns to 671 ns
/ff_mux_tb/enable
VIX
+7.61%
Search
ENG
5:00 PM
7/24/2024

	Msgs
/ff_mux_tb/rst	1'h0
/ff_mux_tb/clk	1'h0
/ff_mux_tb/enable	1'h1
/ff_mux_tb/sel	1'h1
/ff_mux_tb/D	18'h3dd6b
/ff_mux_tb/Q	18'h00000

```
D: 369db 0de4d 0b7d9 0266d 1e276 349ca 32db6 37195 31a46 09b04 261f7 00769 2bab4 18d88 0d928 0042d 130c7 09c2e 3e408 1451c 3a6fd 20729
Q: 369db 0de4d 0b7d9 0266d 1e276 349ca 32db6 37195 31a46 09b04 261f7 00769 2bab4 18d88 0d928 0042d 130c7 09c2e 3e408 1451c 3a6fd 20729
```

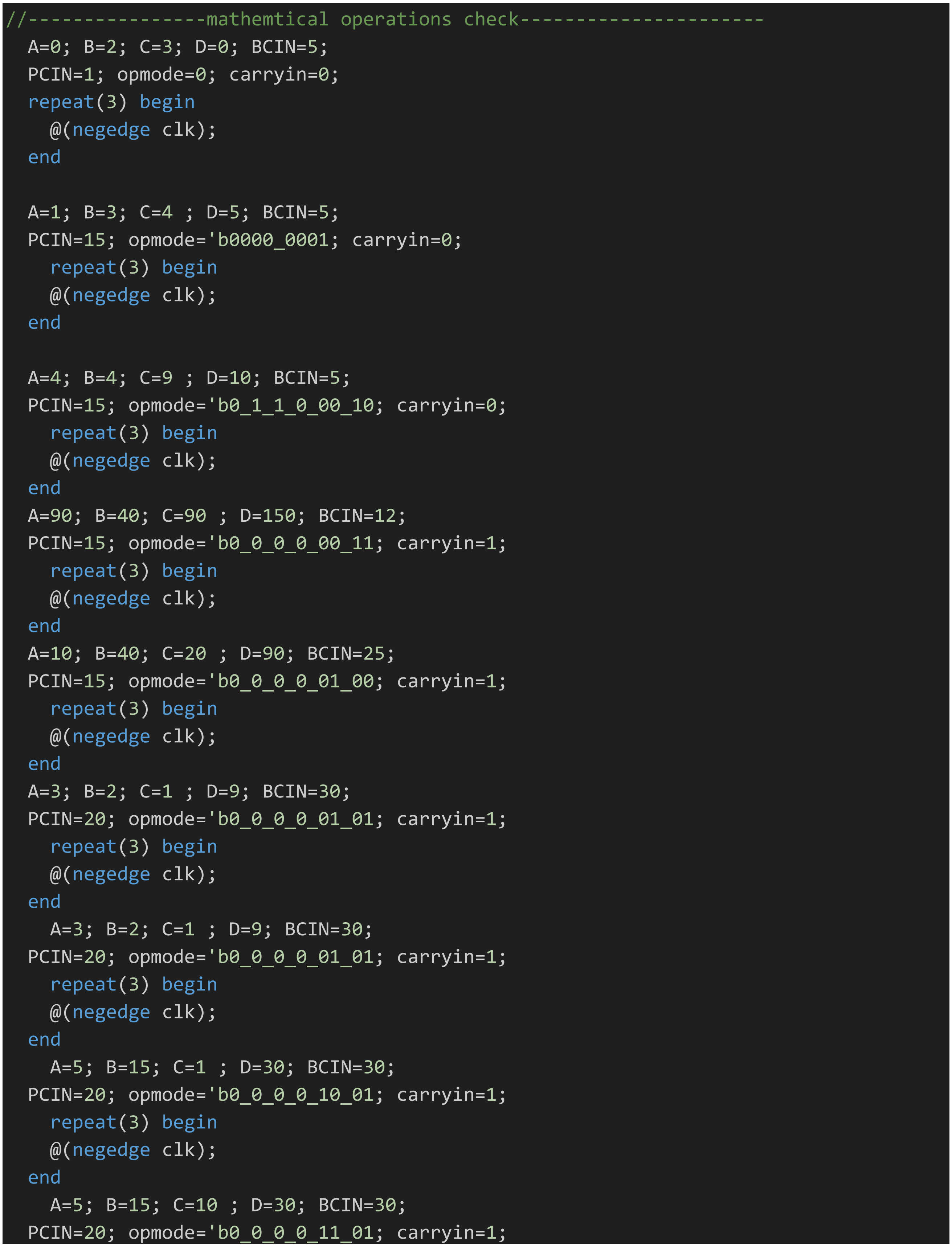
-DSP module design Code:



```
module DSP (
  A,B,C,D,carryin,M,P,carryout,
  carryoutF,clk,opmode,CEA,CEB,
  CEC,CECARRYIN,CEM,CED,CEOPMODE,CEP,
  RSTA,RSTB,RSTC,RSTD,RSTCARRYIN,RSTM,
  RSTOPMODE,RSTP,BCOUT,PCIN,PCOUT,BCIN,
);
//============= PARAMETERS ===============================
  parameter A0REG=1'b0;parameter A1REG=1'b1;
  parameter B0REG=1'b0;parameter B1REG=1'b1;
  parameter CREG=1'b1;parameter DREG=1'b1;
  parameter MREG=1'b1;parameter PREG=1'b1;
  parameter CARRYINREG=1'b1;parameter CARRYOUTREG=1'b1;
  parameter OPMODEREG=1'b1;parameter CARRYINSEL="OPMODE5";
  parameter B_INPUT="DIRECT";parameter RSTTYPE="SYNC";
//============== INPUTS ==================================
  input [17:0] A,B,D,BCIN;
  input [47:0] C,PCIN;
  input [7:0] opmode;
  input carryin,clk;
  input CEA,CEB,CEC,CED,CEM,CEP;
  input CECARRYIN,CEOPMODE;
  input RSTA,RSTB,RSTC,RSTD,RSTM,RSTP;
  input RSTCARRYIN,RSTOPMODE;
//============ OUTPUTS ==================================
  output[35:0] M;
  output [47:0] P , PCOUT;
  output carryout,carryoutF;
  output [17:0] BCOUT;
//============= internal signals =========================
  wire [17:0] B0_in,B0_r,D_r,A0_r,pre_add_sub,B1_in,A1_r;
  wire [7:0] opmode_r;
  wire [47:0] C_r,D_A_B_CONC,post_add_sub;
  reg [47:0] X,Z;
  wire [35:0] M_in;
  wire CYI_input,CYO_input,CYI_r;
//============ Design ==================================
assign B0_in=(B_INPUT=="DIRECT")?B:(B_INPUT=="CASCADE")?BCIN:0;
//--------------- first stage registers ------------------------
ff_mux #(.WIDTH(8),.RSTTYPE("SYNC")) opmode_reg
(.D(opmode),.clk(clk),.enable(CEOPMODE),.rst(RSTOPMODE),.Q(opmode_r),.sel(OPMODEREG));
ff_mux #(.WIDTH(18),.RSTTYPE("SYNC")) D_reg (.D(D),.clk(clk),.enable(CED),.rst(RSTD),.Q(D_r),.sel(DREG));
ff_mux #(.WIDTH(18),.RSTTYPE("SYNC")) B0_reg
(.D(B0_in),.clk(clk),.enable(CEB),.rst(RSTB),.Q(B0_r),.sel(B0REG));
ff_mux #(.WIDTH(48),.RSTTYPE("SYNC")) C_reg (.D(C),.clk(clk),.enable(CEC),.rst(RSTC),.Q(C_r),.sel(CREG));
ff_mux #(.WIDTH(18),.RSTTYPE("SYNC")) A0_reg (.D(A),.clk(clk),.enable(CEA),.rst(RSTA),.Q(A0_r),.sel(A0REG));
assign pre_add_sub=(opmode_r[6]==0)?D_r+B0_r:D_r-B0_r;
assign B1_in=(opmode_r[4]==0)?B0_r:pre_add_sub;
ff_mux #(.WIDTH(18),.RSTTYPE("SYNC")) B1_reg
(.D(B1_in),.clk(clk),.enable(CEB),.rst(RSTB),.Q(BCOUT),.sel(B1REG));
ff_mux #(.WIDTH(18),.RSTTYPE("SYNC")) A1_reg
(.D(A0_r),.clk(clk),.enable(CEA),.rst(RSTA),.Q(A1_r),.sel(A1REG));
//-------------- second stage ----------------------------------
assign M_in=BCOUT*A1_r;
ff_mux #(.WIDTH(36),.RSTTYPE("SYNC")) M_reg (.D(M_in),.clk(clk),.enable(CEM),.rst(RSTM),.Q(M),.sel(MREG));
assign D_A_B_CONC={D_r[11:0],A1_r[17:0],BCOUT[17:0]};
always @(*) begin
//------------ X MULTIPLEXER ------------------------------------
  case (opmode_r[1:0])
    2'b00:X=0;
    2'b01:X=M; //==============>X={11'b000_0000_0000,M}
    2'b10:X=P;
    2'b11:X=D_A_B_CONC;
  endcase
//------------- Z MULTIPLEXER ------------------------------------
  case (opmode_r[3:2])
    2'b00:Z=0;
    2'b01:Z=PCIN;
    2'b10:Z=P;
    2'b11:Z=C_r;
  endcase
end
//--------------- third stage -------------------------------------
assign CYI_input=(CARRYINSEL=="CARRYIN")?carryin:(CARRYINSEL=="OPMODE5")?opmode_r[5]:0;
ff_mux #(.WIDTH(1),.RSTTYPE("SYNC")) CYI_reg
(.D(CYI_input),.clk(clk),.enable(CECARRYIN),.rst(RSTCARRYIN),.Q(CYI_r),.sel(CARRYINREG));
assign {CYO_input,post_add_sub}=(opmode_r[7]==0)?(Z+X+CYI_r):(Z-(X+CYI_r));
ff_mux #(.WIDTH(1),.RSTTYPE("SYNC")) CYO_reg
(.D(CYO_input),.clk(clk),.enable(CECARRYIN),.rst(RSTCARRYIN),.Q(carryout),.sel(CARRYOUTREG));
assign carryoutF=carryout;
ff_mux #(.WIDTH(48),.RSTTYPE("SYNC")) P_reg
(.D(post_add_sub),.clk(clk),.enable(CEP),.rst(RSTP),.Q(P),.sel(PREG));
assign PCOUT=P;
endmodule
```

-DSP module testbench Code:

```
module DSP_tb();
  reg carryin,clk,CEA,CEB,CEC,CED,CEM,CEP;
  reg CECARRYIN,CEOPMODE,RSTA,RSTB,RSTC,RSTD,RSTM;
  reg RSTP,RSTCARRYIN,RSTOPMODE;
  reg [17:0] A,B,D,BCIN;
  reg [47:0] C,PCIN;
  reg [7:0] opmode;
  wire [35:0] M;
  wire [47:0] P , PCOUT;
  wire carryout,carryoutF;
  wire [17:0] BCOUT;
//======= DUT INIT. ======================
  DSP dut (.carryin(carryin),.clk(clk),.CEA(CEA),.CEB(CEB),.CEC(CEC),.CED(CED),
  .CEM(CEM),.CEP(CEP),.CECARRYIN(CECARRYIN),.CEOPMODE(CEOPMODE),.RSTA(RSTA),.RSTB(RS
TB),
  .RSTC(RSTC),.RSTD(RSTD),.RSTM(RSTM),.RSTP(RSTP),.RSTCARRYIN(RSTCARRYIN),.RSTOPMODE
(RSTOPMODE),
  .A(A),.B(B),.D(D),.BCIN(BCIN),.C(C),.PCIN(PCIN),.opmode(opmode),.M(M),.P(P),.PCOUT
(PCOUT),
  .carryout(carryout),.carryoutF(carryoutF),.BCOUT(BCOUT));
//====== clock generation =================
initial begin
  clk=0;
  forever begin
  #1 clk =~clk;
  end
end
//=============== testbench ===============

/*- wait clock cycle for BCOUT
  - wait two clock cycle for M
  - wait one - two - three clock cycles for the output depends on X and Z */


initial begin
  CEA=1; CEB=1; CEC=1; CED=1; CEM=1; CEP=1;
  CECARRYIN=1; CEOPMODE=1; RSTA=1; RSTB=1; RSTC=1; RSTD=1; RSTM=1;
  RSTP=1; RSTCARRYIN=1; RSTOPMODE=1;
  A=0; B=0; C=0; D=0; BCIN=0;
  PCIN=0; opmode=0; carryin=0;
  @(negedge clk);
  RSTA=0; RSTB=0; RSTC=0; RSTD=0; RSTM=0;
  RSTP=0; RSTCARRYIN=0; RSTOPMODE=0;
```



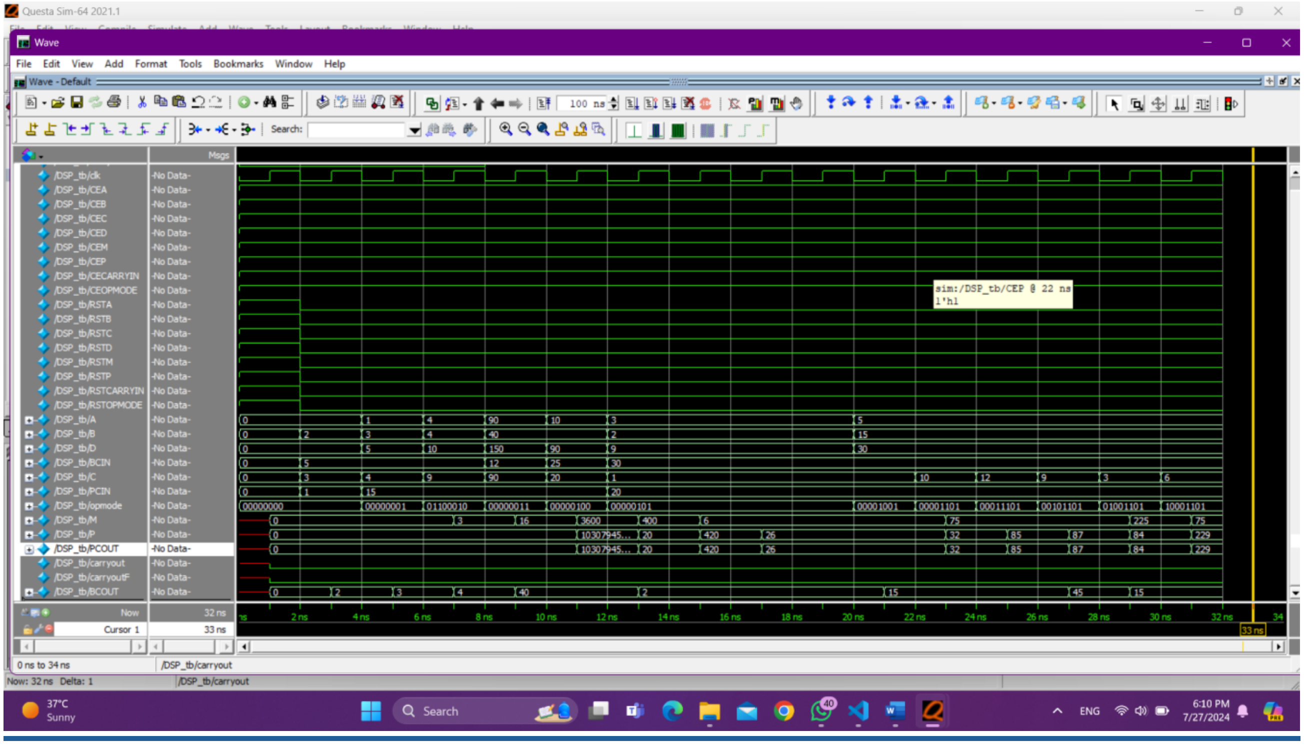
```
//----------------mathemtical operations check----------------------
  A=0; B=2; C=3; D=0; BCIN=5;
  PCIN=1; opmode=0; carryin=0;
  repeat(3) begin
    @(negedge clk);
  end

  A=1; B=3; C=4 ; D=5; BCIN=5;
  PCIN=15; opmode='b0000_0001; carryin=0;
    repeat(3) begin
    @(negedge clk);
  end

  A=4; B=4; C=9 ; D=10; BCIN=5;
  PCIN=15; opmode='b0_1_1_0_00_10; carryin=0;
    repeat(3) begin
    @(negedge clk);
  end
  A=90; B=40; C=90 ; D=150; BCIN=12;
  PCIN=15; opmode='b0_0_0_0_00_11; carryin=1;
    repeat(3) begin
    @(negedge clk);
  end
  A=10; B=40; C=20 ; D=90; BCIN=25;
  PCIN=15; opmode='b0_0_0_0_01_00; carryin=1;
    repeat(3) begin
    @(negedge clk);
  end
  A=3; B=2; C=1 ; D=9; BCIN=30;
  PCIN=20; opmode='b0_0_0_0_01_01; carryin=1;
    repeat(3) begin
    @(negedge clk);
  end
    A=3; B=2; C=1 ; D=9; BCIN=30;
  PCIN=20; opmode='b0_0_0_0_01_01; carryin=1;
    repeat(3) begin
    @(negedge clk);
  end
    A=5; B=15; C=1 ; D=30; BCIN=30;
  PCIN=20; opmode='b0_0_0_0_10_01; carryin=1;
    repeat(3) begin
    @(negedge clk);
  end
    A=5; B=15; C=10 ; D=30; BCIN=30;
  PCIN=20; opmode='b0_0_0_0_11_01; carryin=1;
```

```
    repeat(3) begin
    @(negedge clk);
  end
  A=5; B=15; C=12 ; D=30; BCIN=30;
  PCIN=20; opmode='b0_0_0_1_11_01; carryin=1;
    repeat(3) begin
    @(negedge clk);
  end
  A=5; B=15; C=9 ; D=30; BCIN=30;
  PCIN=20; opmode='b0_0_1_0_11_01; carryin=1;
    repeat(3) begin
    @(negedge clk);
  end
  A=5; B=15; C=3; D=30; BCIN=30;
  PCIN=20; opmode='b0_1_0_0_11_01; carryin=1;
    repeat(3) begin
    @(negedge clk);
  end
  A=5; B=15; C=6 ; D=30; BCIN=30;
  PCIN=20; opmode='b1_0_0_0_11_01; carryin=1;
    repeat(3) begin
    @(negedge clk);
  end
$stop;
end
endmodule
```

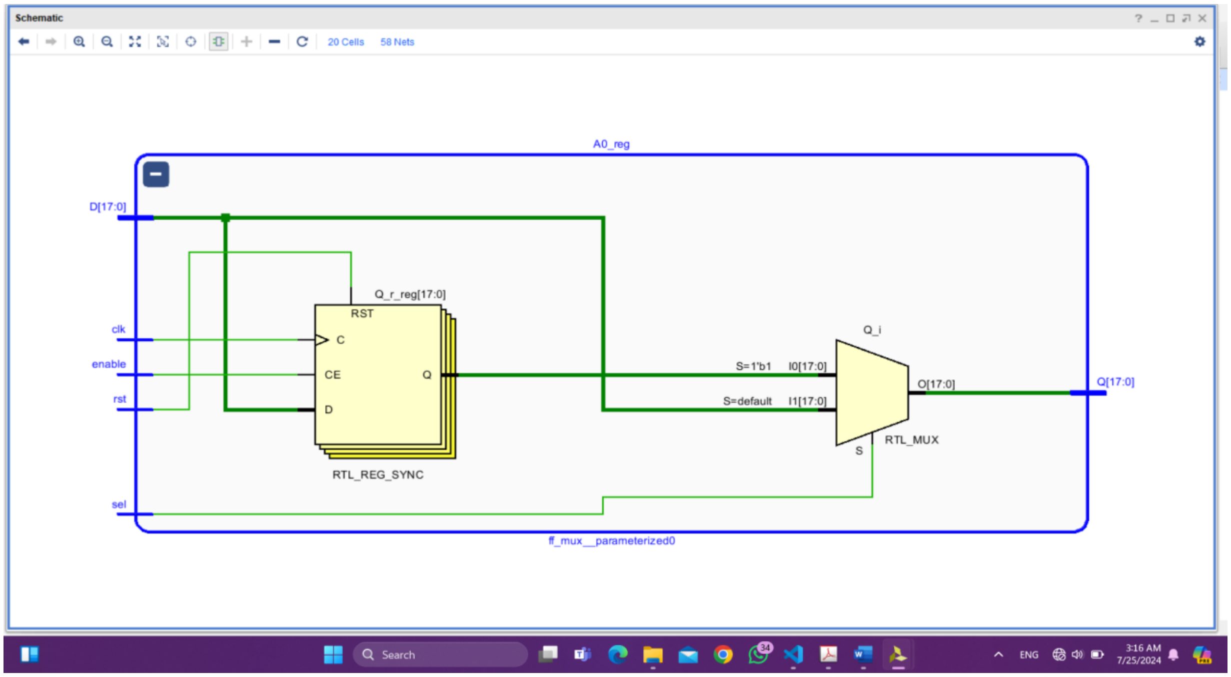
-DO file:

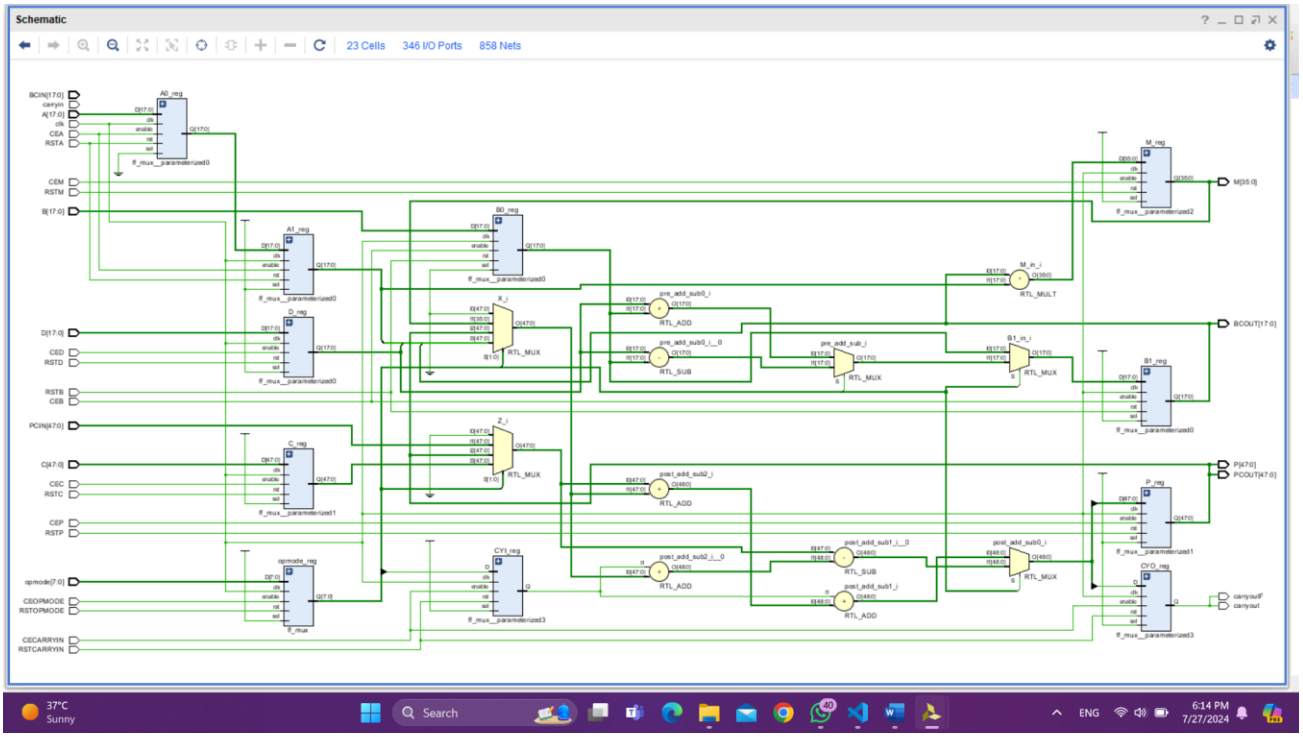
```
vlib work
vlog flipflop.v DSP.v DSP_tb.v
vsim -voptargs=+acc work.DSP_tb
add wave *
run -all
```

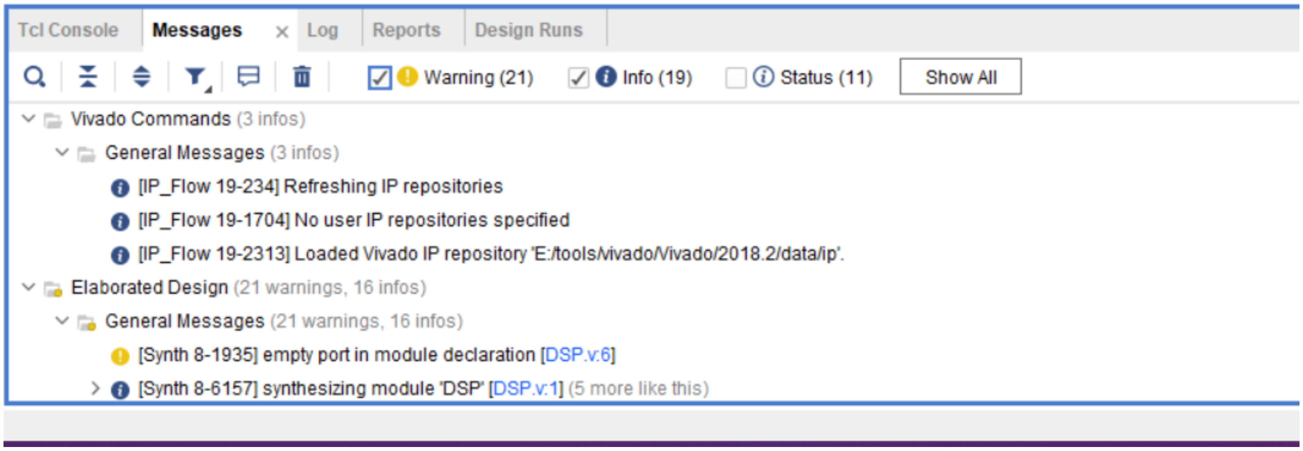
-Simulation:



-Elaboration:

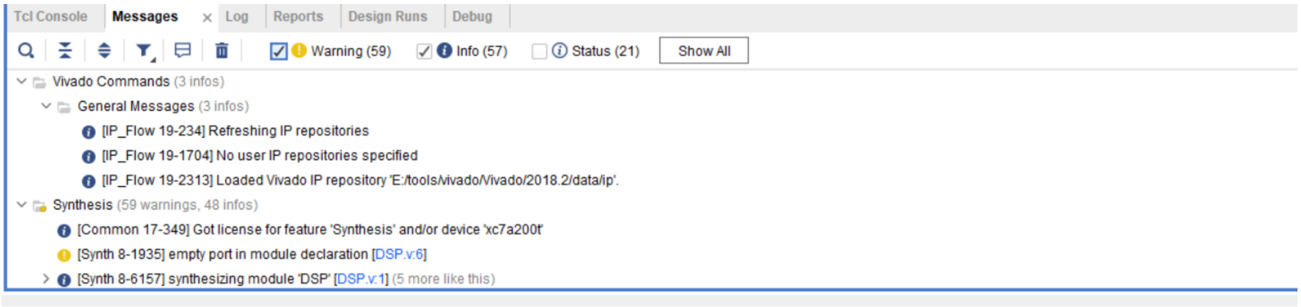




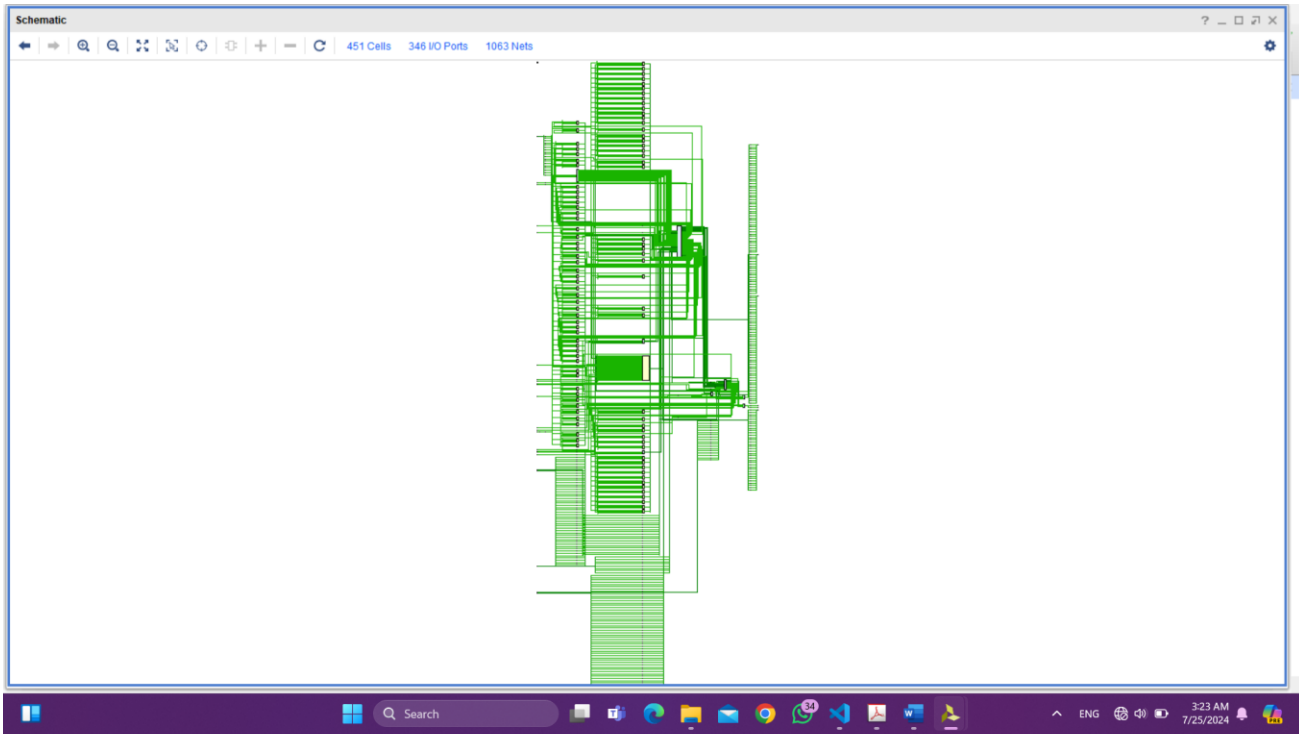


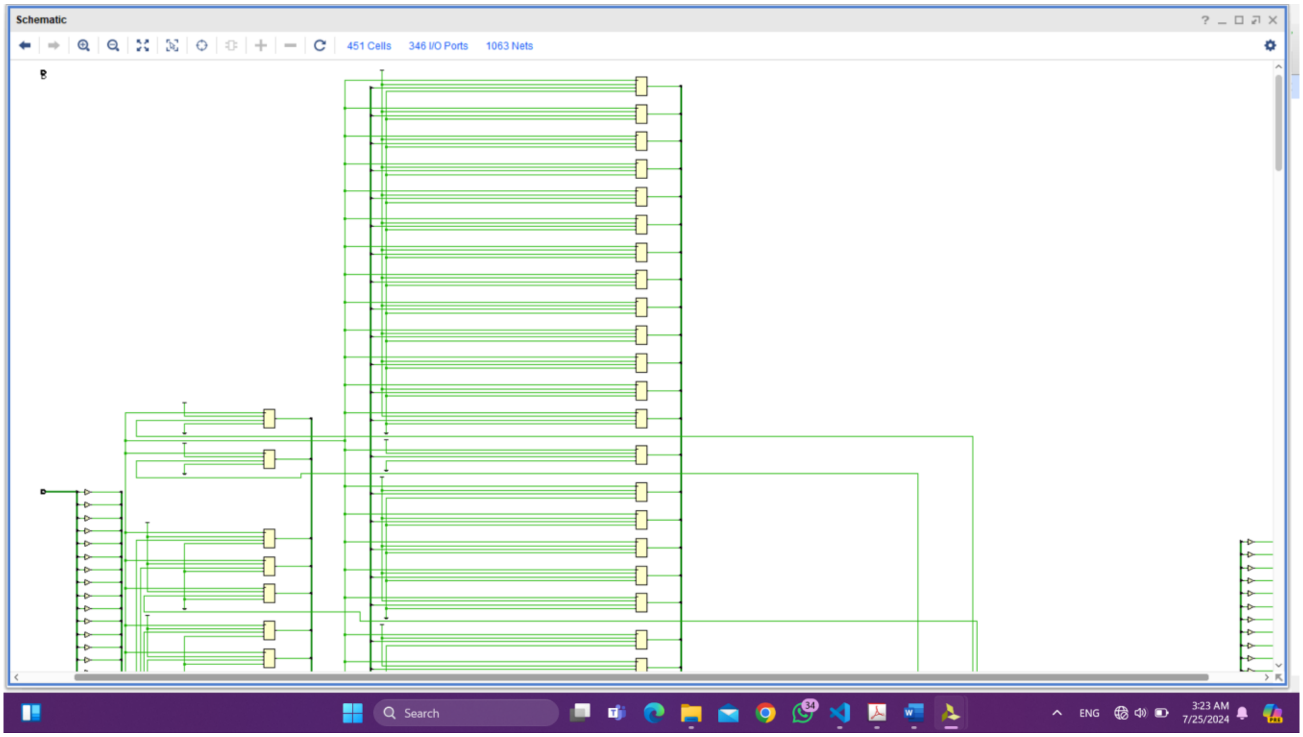
```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'E:/tools/vivado/Vivado/2018.2/data/ip'.
Elaborated Design (21 warnings, 16 infos)
  General Messages (21 warnings, 16 infos)
    [Synth 8-1935] empty port in module declaration [DSP.v:6]
    [Synth 8-6157] synthesizing module 'DSP' [DSP.v:1] (5 more like this)
```

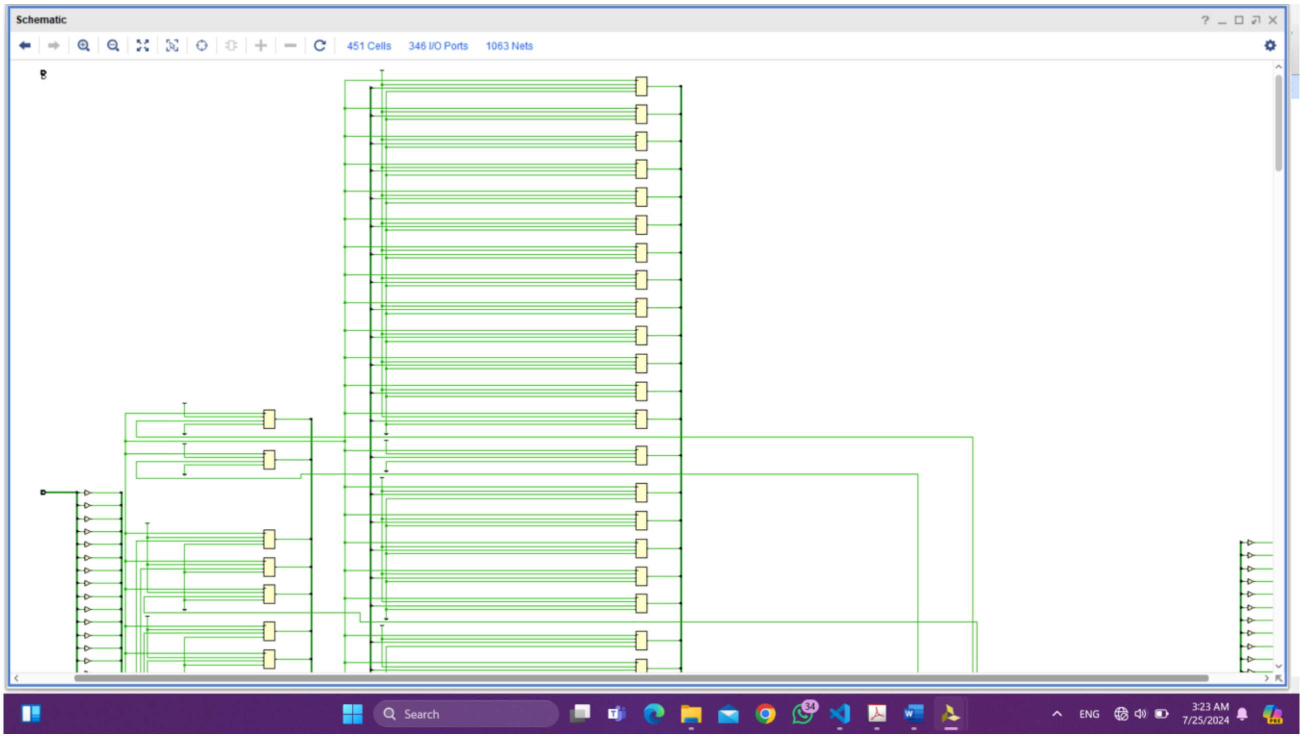
-Synthesis:

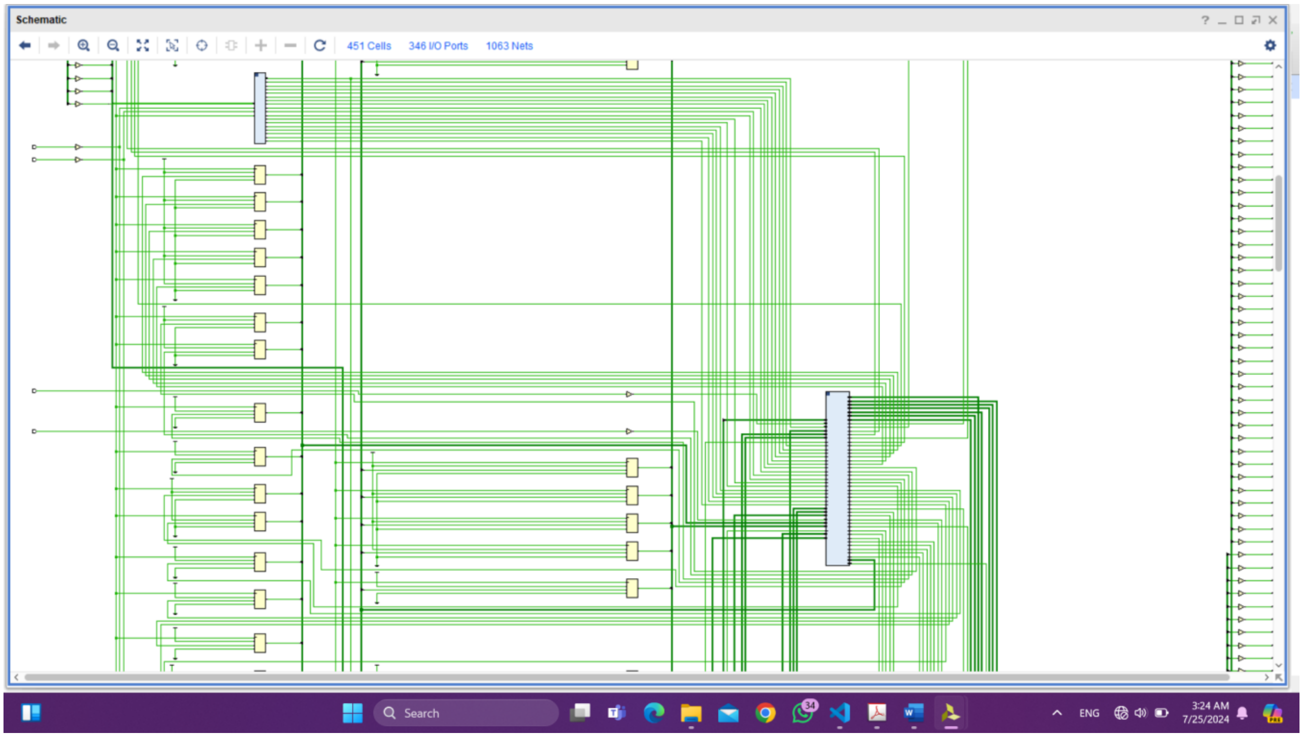


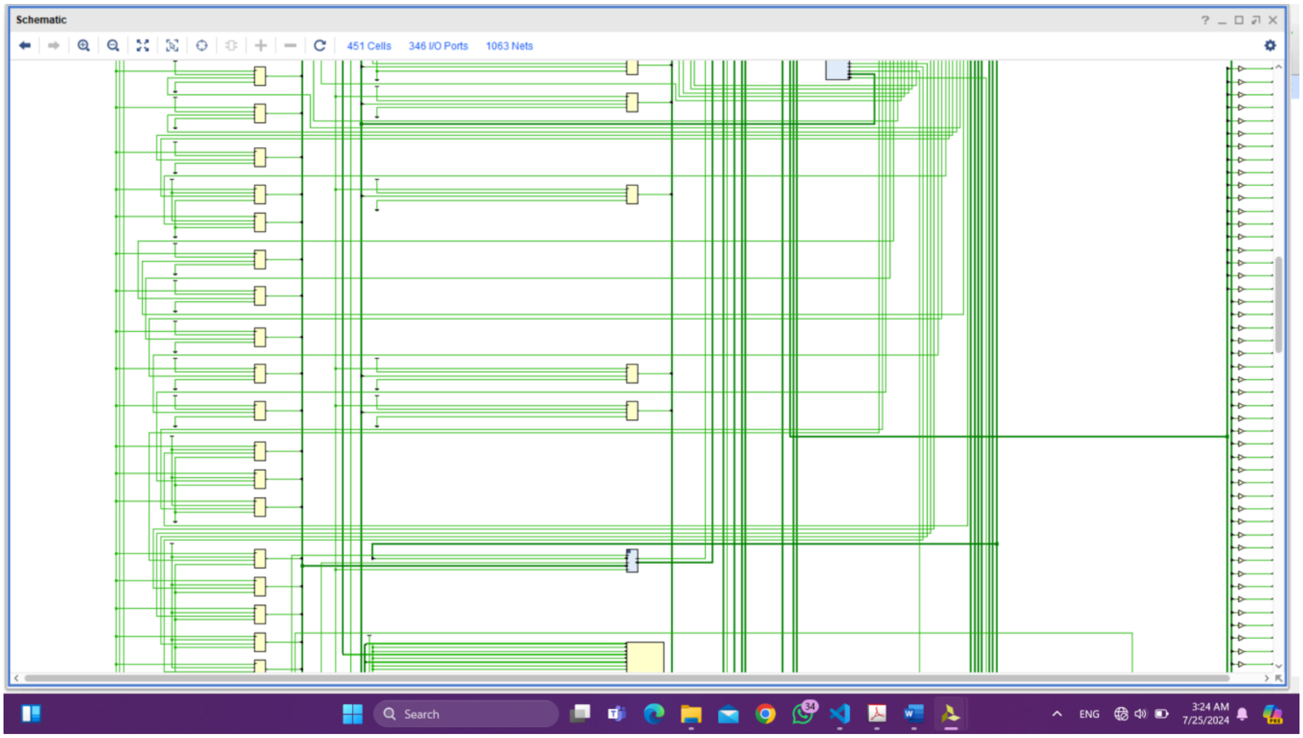
```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'E:/tools/vivado/Vivado/2018.2/data/ip'.
Synthesis (59 warnings, 48 infos)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
  [Synth 8-1935] empty port in module declaration [DSP.v:6]
  [Synth 8-6157] synthesizing module 'DSP' [DSP.v:1] (5 more like this)
```




Schematic
451 Cells
346 I/O Ports
1063 Nets
Search
ENG
3:23 AM
7/25/2024


Schematic
451 Cells
346 I/O Ports
1063 Nets
Search
ENG
3:23 AM
7/25/2024


Schematic
451 Cells
346 I/O Ports
1063 Nets
Search
ENG
3:24 AM
7/25/2024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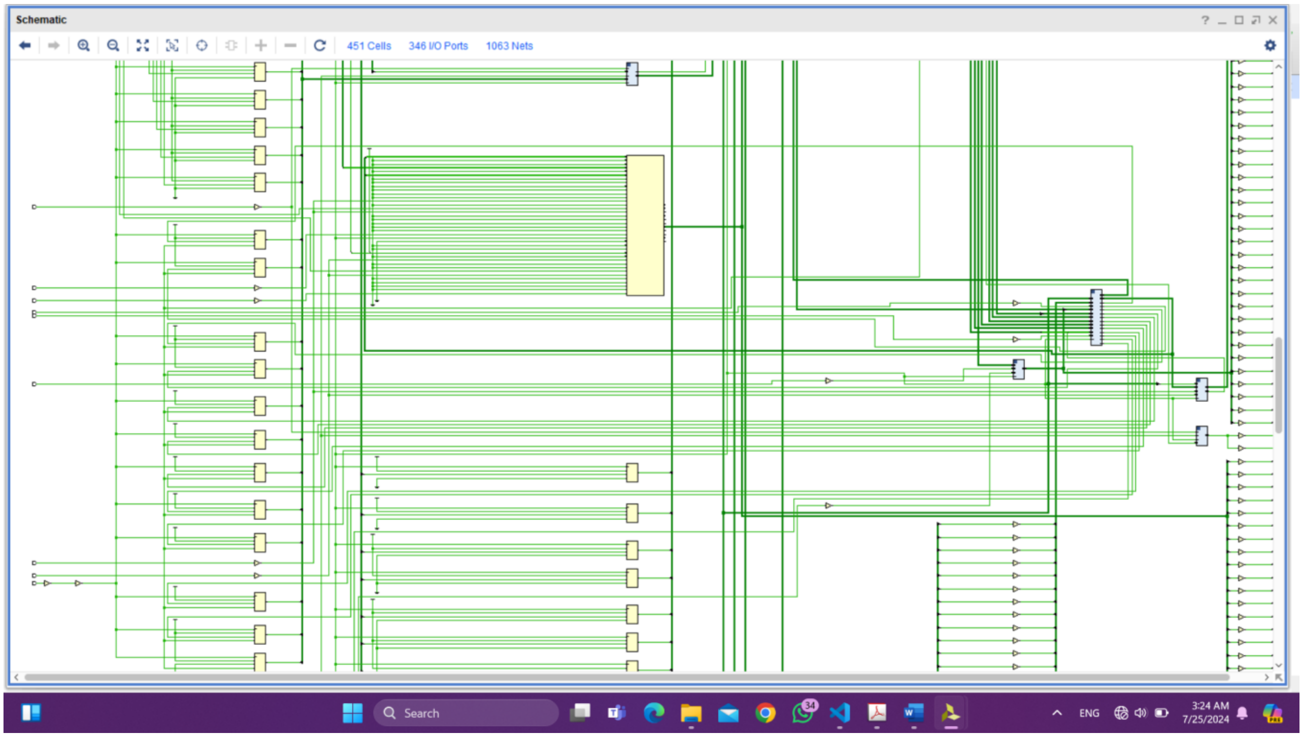
Search
ENG
3:24 AM
7/25/2024


Schematic
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Search
ENG
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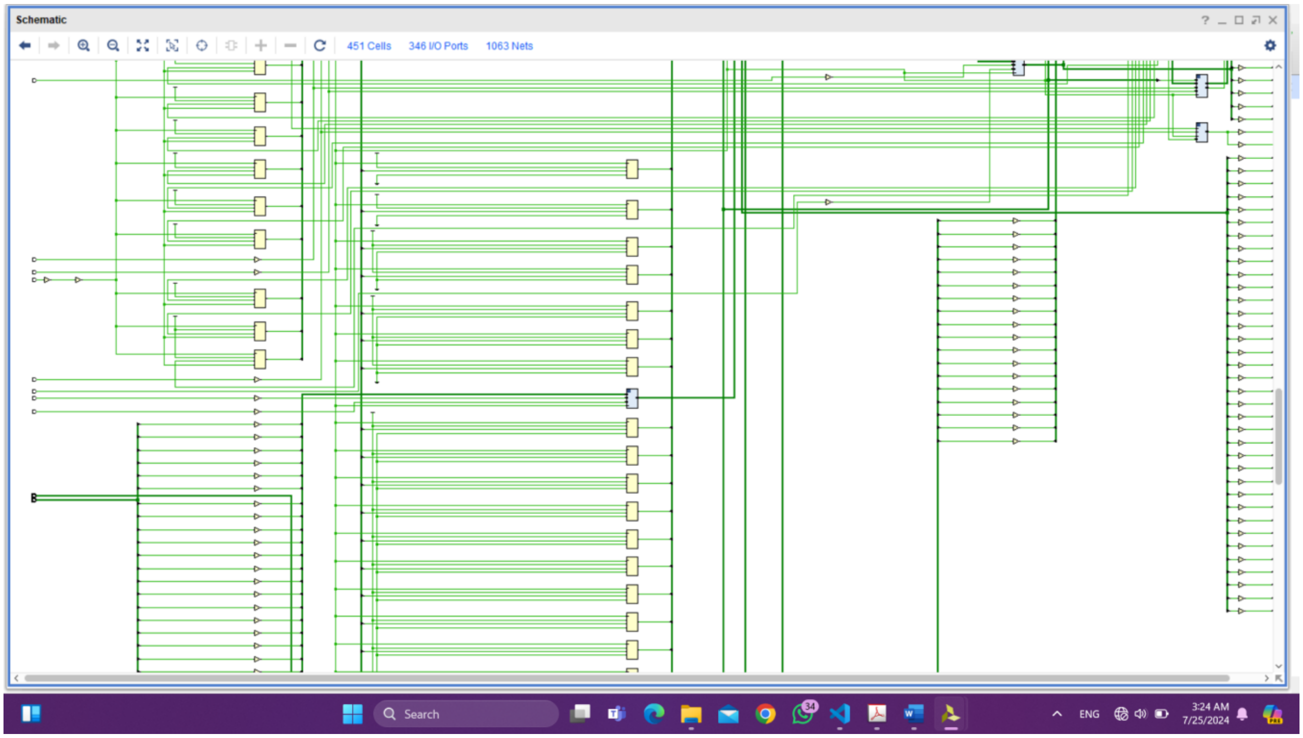
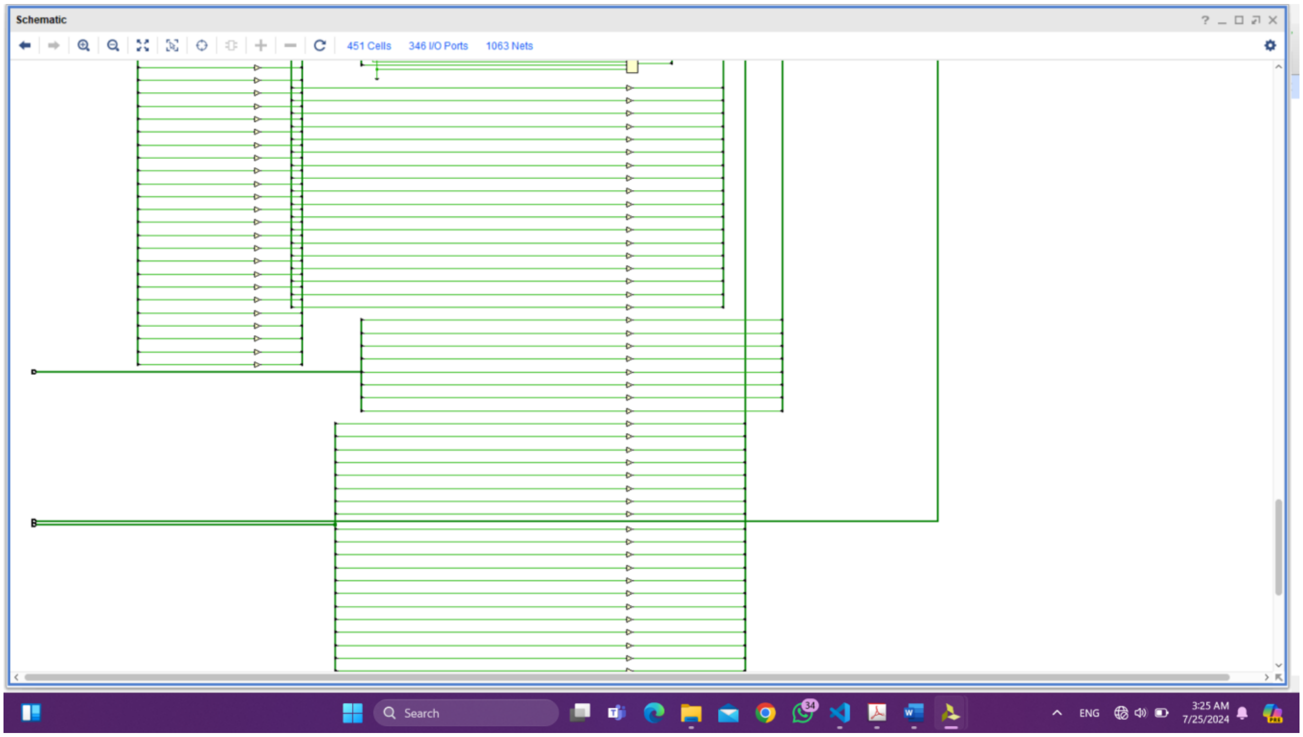
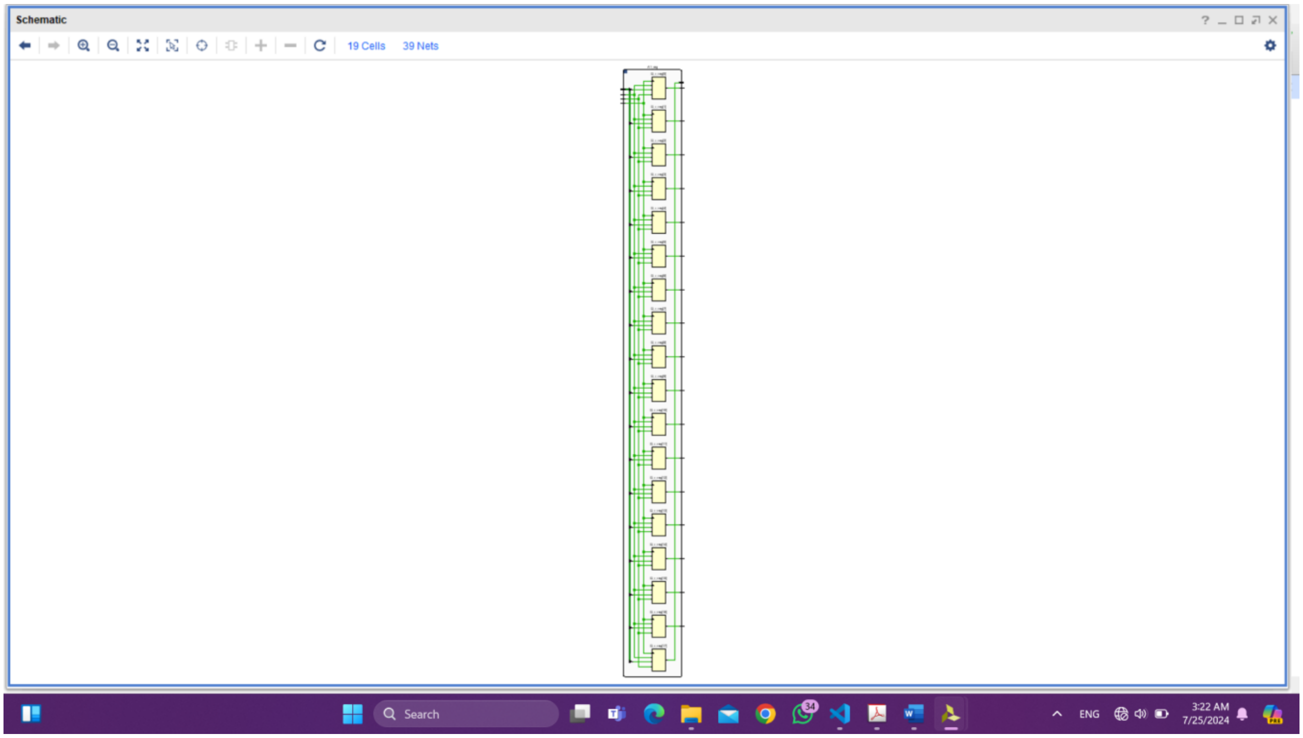
7/25/2024

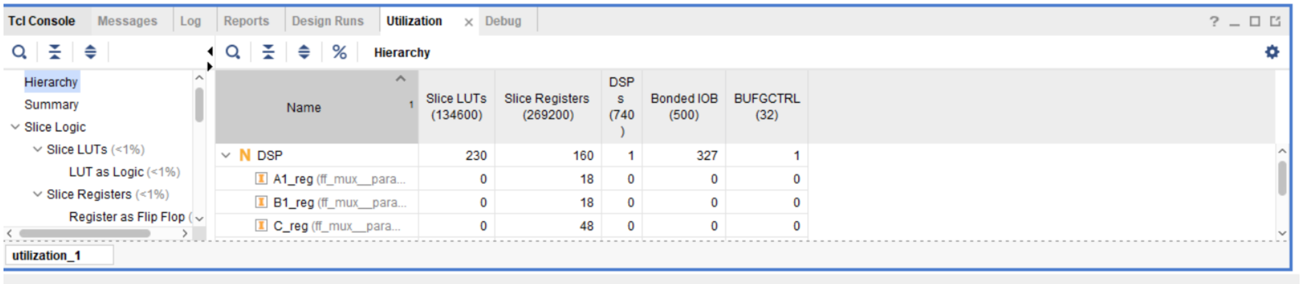

Schematic
451 Cells
346 I/O Ports
1063 Nets
Search
ENG
3:24 AM
7/25/2024



-FF MUX synthesis:

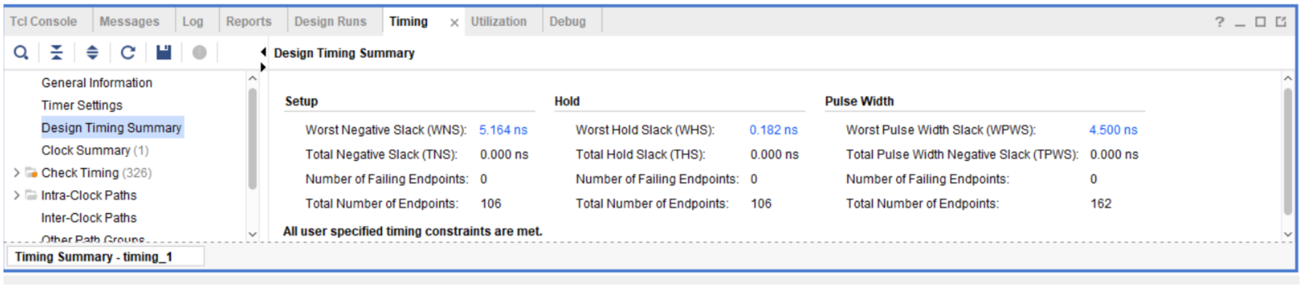


-Utilization report:



Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP	230	160	1	327	1
A1_reg (ff_mux__para...	0	18	0	0	0
B1_reg (ff_mux__para...	0	18	0	0	0
C_reg (ff_mux__para...	0	48	0	0	0

-timing report:

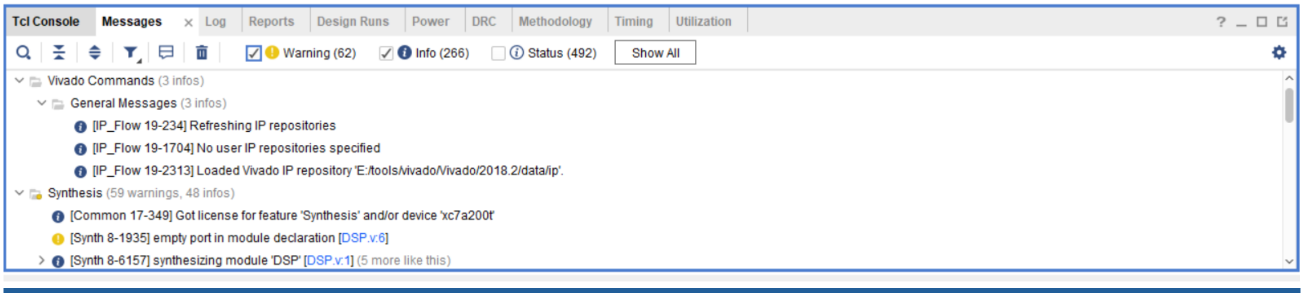


Design Timing Summary

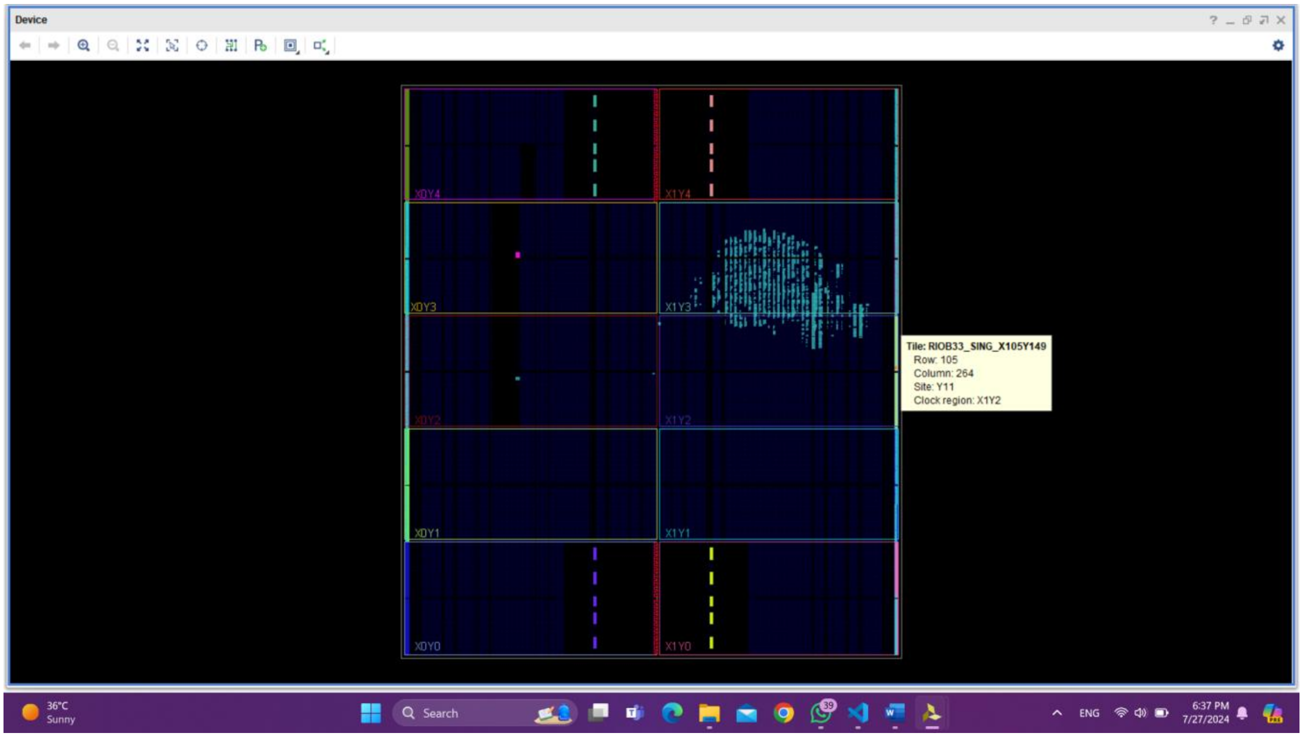
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.164 ns	Worst Hold Slack (WHS):	0.182 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:	162

All user specified timing constraints are met.

-Implementation:

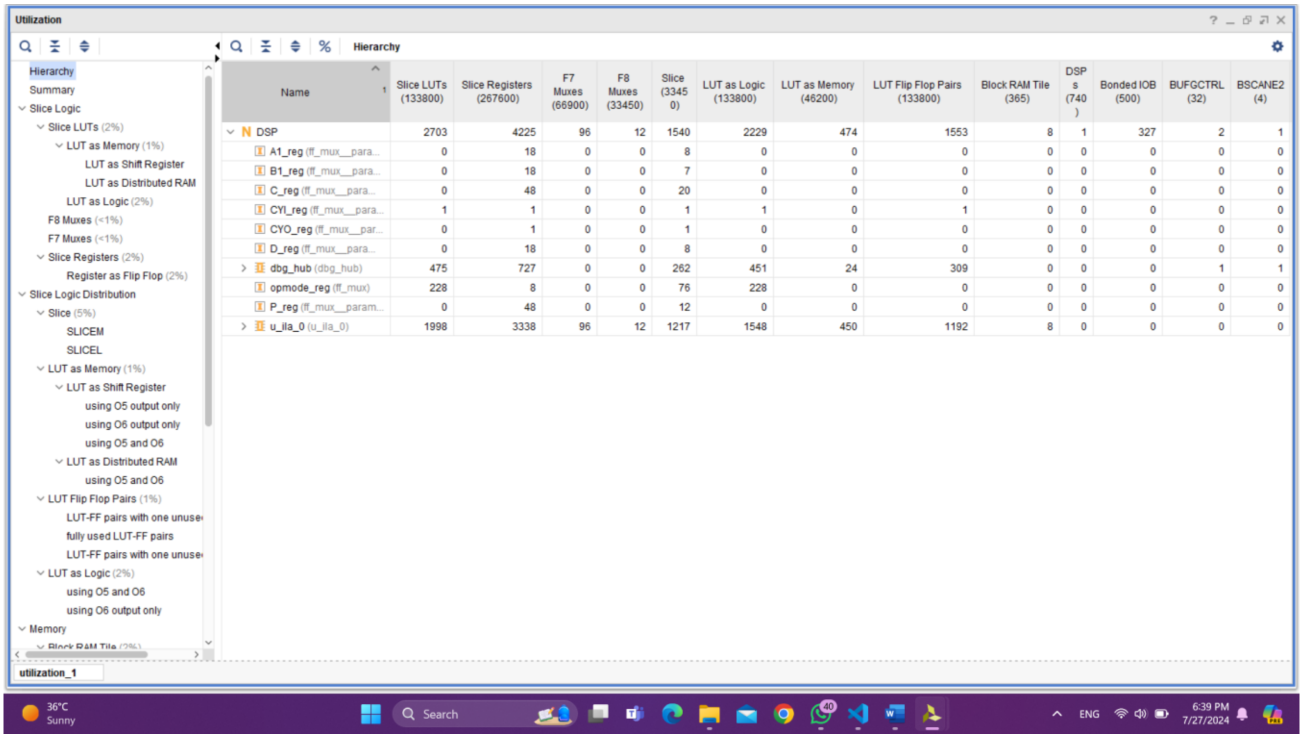


```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'E:/tools/vivado/Vivado/2018.2/data/ip'.
Synthesis (59 warnings, 48 infos)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
  [Synth 8-1935] empty port in module declaration [DSP.v:6]
  [Synth 8-6157] synthesizing module 'DSP' [DSP.v:1] (5 more like this)
```



Tile: RIOB33_SING_X105Y149
Row: 105
Column: 264
Site: Y11
Clock region: X1Y2

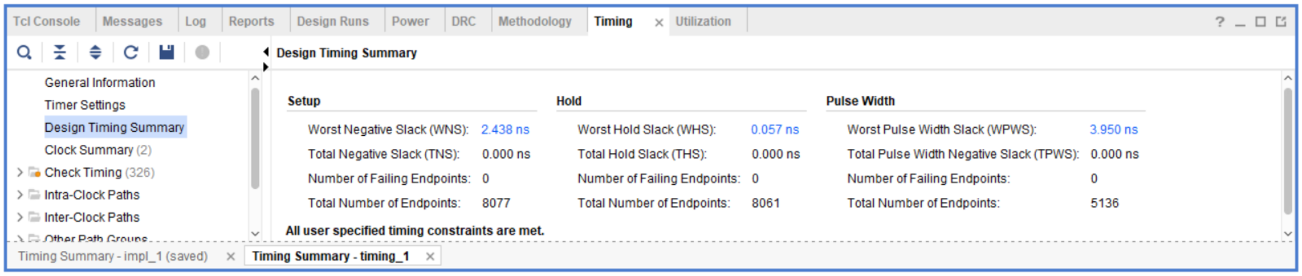
-Utilization report:



- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (2%)
    - LUT as Memory (1%)
      - LUT as Shift Register
      - LUT as Distributed RAM
    - LUT as Logic (2%)
  - F8 Muxes (<1%)
  - F7 Muxes (<1%)
  - Slice Registers (2%)
    - Register as Flip Flop (2%)
- Slice Logic Distribution
  - Slice (5%)
    - SLICEM
    - SLICEL
  - LUT as Memory (1%)
    - LUT as Shift Register
      - using O5 output only
      - using O6 output only
      - using O5 and O6
    - LUT as Distributed RAM
      - using O5 and O6
  - LUT Flip Flop Pairs (1%)
    - LUT-FF pairs with one unuse
    - fully used LUT-FF pairs
    - LUT-FF pairs with one unuse
  - LUT as Logic (2%)
    - using O5 and O6
    - using O6 output only
- Memory
  - Block RAM Tile (2%)

Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	BSCANE2 (4)
N DSP	2703	4225	96	12	1540	2229	474	1553	8	1	327	2	1
A1_reg (ff_mux__para...	0	18	0	0	8	0	0	0	0	0	0	0	0
B1_reg (ff_mux__para...	0	18	0	0	7	0	0	0	0	0	0	0	0
C_reg (ff_mux__para...	0	48	0	0	20	0	0	0	0	0	0	0	0
CYI_reg (ff_mux__para...	1	1	0	0	1	1	0	1	0	0	0	0	0
CYO_reg (ff_mux__par...	0	1	0	0	1	0	0	0	0	0	0	0	0
D_reg (ff_mux__para...	0	18	0	0	8	0	0	0	0	0	0	0	0
dbg_hub (dbg_hub)	475	727	0	0	262	451	24	309	0	0	0	1	1
opmode_reg (ff_mux)	228	8	0	0	76	228	0	0	0	0	0	0	0
P_reg (ff_mux__param...	0	48	0	0	12	0	0	0	0	0	0	0	0
u_ila_0 (u_ila_0)	1998	3338	96	12	1217	1548	450	1192	8	0	0	0	0

-timing report:



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.438 ns	Worst Hold Slack (WHS):	0.057 ns	Worst Pulse Width Slack (WPWS):	3.950 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8077	Total Number of Endpoints:	8061	Total Number of Endpoints:	5136

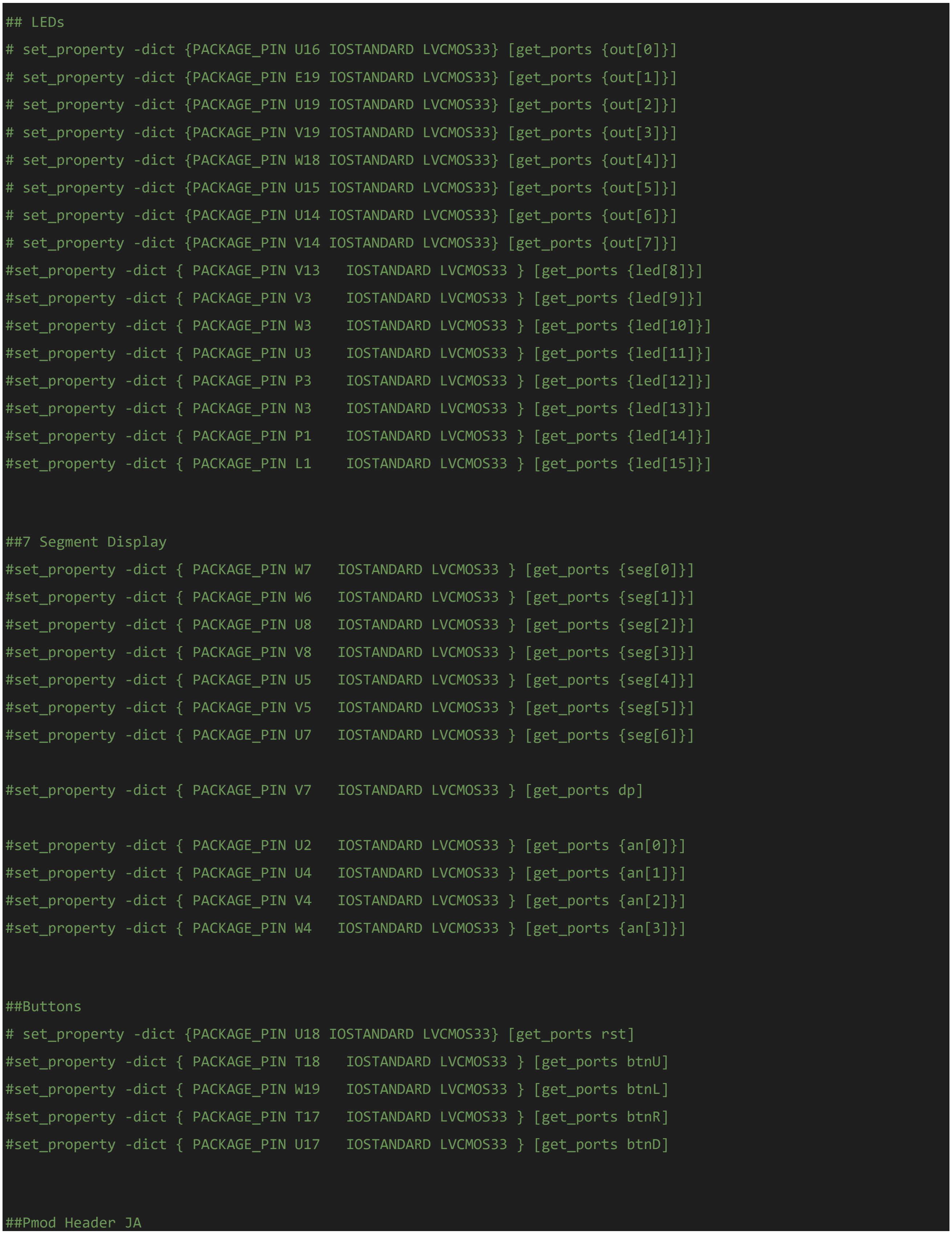
All user specified timing constraints are met.

-Constraints file:

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the
project

## Clock signal
set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports clk]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clk]


## Switches
# set_property -dict {PACKAGE_PIN V17 IOSTANDARD LVCMOS33} [get_ports {a[0]}]
# set_property -dict {PACKAGE_PIN V16 IOSTANDARD LVCMOS33} [get_ports {a[1]}]
# set_property -dict {PACKAGE_PIN W16 IOSTANDARD LVCMOS33} [get_ports {a[2]}]
# set_property -dict {PACKAGE_PIN W17 IOSTANDARD LVCMOS33} [get_ports {a[3]}]
# set_property -dict {PACKAGE_PIN W15 IOSTANDARD LVCMOS33} [get_ports {b[0]}]
# set_property -dict {PACKAGE_PIN V15 IOSTANDARD LVCMOS33} [get_ports {b[1]}]
# set_property -dict {PACKAGE_PIN W14 IOSTANDARD LVCMOS33} [get_ports {b[2]}]
# set_property -dict {PACKAGE_PIN W13 IOSTANDARD LVCMOS33} [get_ports {b[3]}]
# set_property -dict {PACKAGE_PIN V2 IOSTANDARD LVCMOS33} [get_ports {op[0]}]
# set_property -dict {PACKAGE_PIN T3 IOSTANDARD LVCMOS33} [get_ports {op[1]}]
#set_property -dict { PACKAGE_PIN T2    IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
#set_property -dict { PACKAGE_PIN R3    IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
#set_property -dict { PACKAGE_PIN W2    IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
#set_property -dict { PACKAGE_PIN U1    IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
#set_property -dict { PACKAGE_PIN T1    IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
#set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]
```



```
## LEDs
# set_property -dict {PACKAGE_PIN U16 IOSTANDARD LVCMOS33} [get_ports {out[0]}]
# set_property -dict {PACKAGE_PIN E19 IOSTANDARD LVCMOS33} [get_ports {out[1]}]
# set_property -dict {PACKAGE_PIN U19 IOSTANDARD LVCMOS33} [get_ports {out[2]}]
# set_property -dict {PACKAGE_PIN V19 IOSTANDARD LVCMOS33} [get_ports {out[3]}]
# set_property -dict {PACKAGE_PIN W18 IOSTANDARD LVCMOS33} [get_ports {out[4]}]
# set_property -dict {PACKAGE_PIN U15 IOSTANDARD LVCMOS33} [get_ports {out[5]}]
# set_property -dict {PACKAGE_PIN U14 IOSTANDARD LVCMOS33} [get_ports {out[6]}]
# set_property -dict {PACKAGE_PIN V14 IOSTANDARD LVCMOS33} [get_ports {out[7]}]
#set_property -dict { PACKAGE_PIN V13   IOSTANDARD LVCMOS33 } [get_ports {led[8]}]
#set_property -dict { PACKAGE_PIN V3    IOSTANDARD LVCMOS33 } [get_ports {led[9]}]
#set_property -dict { PACKAGE_PIN W3    IOSTANDARD LVCMOS33 } [get_ports {led[10]}]
#set_property -dict { PACKAGE_PIN U3    IOSTANDARD LVCMOS33 } [get_ports {led[11]}]
#set_property -dict { PACKAGE_PIN P3    IOSTANDARD LVCMOS33 } [get_ports {led[12]}]
#set_property -dict { PACKAGE_PIN N3    IOSTANDARD LVCMOS33 } [get_ports {led[13]}]
#set_property -dict { PACKAGE_PIN P1    IOSTANDARD LVCMOS33 } [get_ports {led[14]}]
#set_property -dict { PACKAGE_PIN L1    IOSTANDARD LVCMOS33 } [get_ports {led[15]}]


##7 Segment Display
#set_property -dict { PACKAGE_PIN W7   IOSTANDARD LVCMOS33 } [get_ports {seg[0]}]
#set_property -dict { PACKAGE_PIN W6   IOSTANDARD LVCMOS33 } [get_ports {seg[1]}]
#set_property -dict { PACKAGE_PIN U8   IOSTANDARD LVCMOS33 } [get_ports {seg[2]}]
#set_property -dict { PACKAGE_PIN V8   IOSTANDARD LVCMOS33 } [get_ports {seg[3]}]
#set_property -dict { PACKAGE_PIN U5   IOSTANDARD LVCMOS33 } [get_ports {seg[4]}]
#set_property -dict { PACKAGE_PIN V5   IOSTANDARD LVCMOS33 } [get_ports {seg[5]}]
#set_property -dict { PACKAGE_PIN U7   IOSTANDARD LVCMOS33 } [get_ports {seg[6]}]

#set_property -dict { PACKAGE_PIN V7   IOSTANDARD LVCMOS33 } [get_ports dp]

#set_property -dict { PACKAGE_PIN U2   IOSTANDARD LVCMOS33 } [get_ports {an[0]}]
#set_property -dict { PACKAGE_PIN U4   IOSTANDARD LVCMOS33 } [get_ports {an[1]}]
#set_property -dict { PACKAGE_PIN V4   IOSTANDARD LVCMOS33 } [get_ports {an[2]}]
#set_property -dict { PACKAGE_PIN W4   IOSTANDARD LVCMOS33 } [get_ports {an[3]}]


##Buttons
# set_property -dict {PACKAGE_PIN U18 IOSTANDARD LVCMOS33} [get_ports rst]
#set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports btnU]
#set_property -dict { PACKAGE_PIN W19   IOSTANDARD LVCMOS33 } [get_ports btnL]
#set_property -dict { PACKAGE_PIN T17   IOSTANDARD LVCMOS33 } [get_ports btnR]
#set_property -dict { PACKAGE_PIN U17   IOSTANDARD LVCMOS33 } [get_ports btnD]


##Pmod Header JA
```

```
#set_property -dict { PACKAGE_PIN J1   IOSTANDARD LVCMOS33 } [get_ports {JA[0]}];#Sch name = JA1
#set_property -dict { PACKAGE_PIN L2   IOSTANDARD LVCMOS33 } [get_ports {JA[1]}];#Sch name = JA2
#set_property -dict { PACKAGE_PIN J2   IOSTANDARD LVCMOS33 } [get_ports {JA[2]}];#Sch name = JA3
#set_property -dict { PACKAGE_PIN G2   IOSTANDARD LVCMOS33 } [get_ports {JA[3]}];#Sch name = JA4
#set_property -dict { PACKAGE_PIN H1   IOSTANDARD LVCMOS33 } [get_ports {JA[4]}];#Sch name = JA7
#set_property -dict { PACKAGE_PIN K2   IOSTANDARD LVCMOS33 } [get_ports {JA[5]}];#Sch name = JA8
#set_property -dict { PACKAGE_PIN H2   IOSTANDARD LVCMOS33 } [get_ports {JA[6]}];#Sch name = JA9
#set_property -dict { PACKAGE_PIN G3   IOSTANDARD LVCMOS33 } [get_ports {JA[7]}];#Sch name = JA10

##Pmod Header JB
#set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33 } [get_ports {JB[0]}];#Sch name = JB1
#set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33 } [get_ports {JB[1]}];#Sch name = JB2
#set_property -dict { PACKAGE_PIN B15   IOSTANDARD LVCMOS33 } [get_ports {JB[2]}];#Sch name = JB3
#set_property -dict { PACKAGE_PIN B16   IOSTANDARD LVCMOS33 } [get_ports {JB[3]}];#Sch name = JB4
#set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33 } [get_ports {JB[4]}];#Sch name = JB7
#set_property -dict { PACKAGE_PIN A17   IOSTANDARD LVCMOS33 } [get_ports {JB[5]}];#Sch name = JB8
#set_property -dict { PACKAGE_PIN C15   IOSTANDARD LVCMOS33 } [get_ports {JB[6]}];#Sch name = JB9
#set_property -dict { PACKAGE_PIN C16   IOSTANDARD LVCMOS33 } [get_ports {JB[7]}];#Sch name = JB10

##Pmod Header JC
#set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports {JC[0]}];#Sch name = JC1
#set_property -dict { PACKAGE_PIN M18   IOSTANDARD LVCMOS33 } [get_ports {JC[1]}];#Sch name = JC2
#set_property -dict { PACKAGE_PIN N17   IOSTANDARD LVCMOS33 } [get_ports {JC[2]}];#Sch name = JC3
#set_property -dict { PACKAGE_PIN P18   IOSTANDARD LVCMOS33 } [get_ports {JC[3]}];#Sch name = JC4
#set_property -dict { PACKAGE_PIN L17   IOSTANDARD LVCMOS33 } [get_ports {JC[4]}];#Sch name = JC7
#set_property -dict { PACKAGE_PIN M19   IOSTANDARD LVCMOS33 } [get_ports {JC[5]}];#Sch name = JC8
#set_property -dict { PACKAGE_PIN P17   IOSTANDARD LVCMOS33 } [get_ports {JC[6]}];#Sch name = JC9
#set_property -dict { PACKAGE_PIN R18   IOSTANDARD LVCMOS33 } [get_ports {JC[7]}];#Sch name = JC10

##Pmod Header JXADC
#set_property -dict { PACKAGE_PIN J3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[0]}];#Sch name = XA1_P
#set_property -dict { PACKAGE_PIN L3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[1]}];#Sch name = XA2_P
#set_property -dict { PACKAGE_PIN M2   IOSTANDARD LVCMOS33 } [get_ports {JXADC[2]}];#Sch name = XA3_P
#set_property -dict { PACKAGE_PIN N2   IOSTANDARD LVCMOS33 } [get_ports {JXADC[3]}];#Sch name = XA4_P
#set_property -dict { PACKAGE_PIN K3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[4]}];#Sch name = XA1_N
#set_property -dict { PACKAGE_PIN M3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[5]}];#Sch name = XA2_N
#set_property -dict { PACKAGE_PIN M1   IOSTANDARD LVCMOS33 } [get_ports {JXADC[6]}];#Sch name = XA3_N
#set_property -dict { PACKAGE_PIN N1   IOSTANDARD LVCMOS33 } [get_ports {JXADC[7]}];#Sch name = XA4_N



##VGA Connector
#set_property -dict { PACKAGE_PIN G19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[0]}]
#set_property -dict { PACKAGE_PIN H19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[1]}]
#set_property -dict { PACKAGE_PIN J19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[2]}]
#set_property -dict { PACKAGE_PIN N19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[3]}]
```

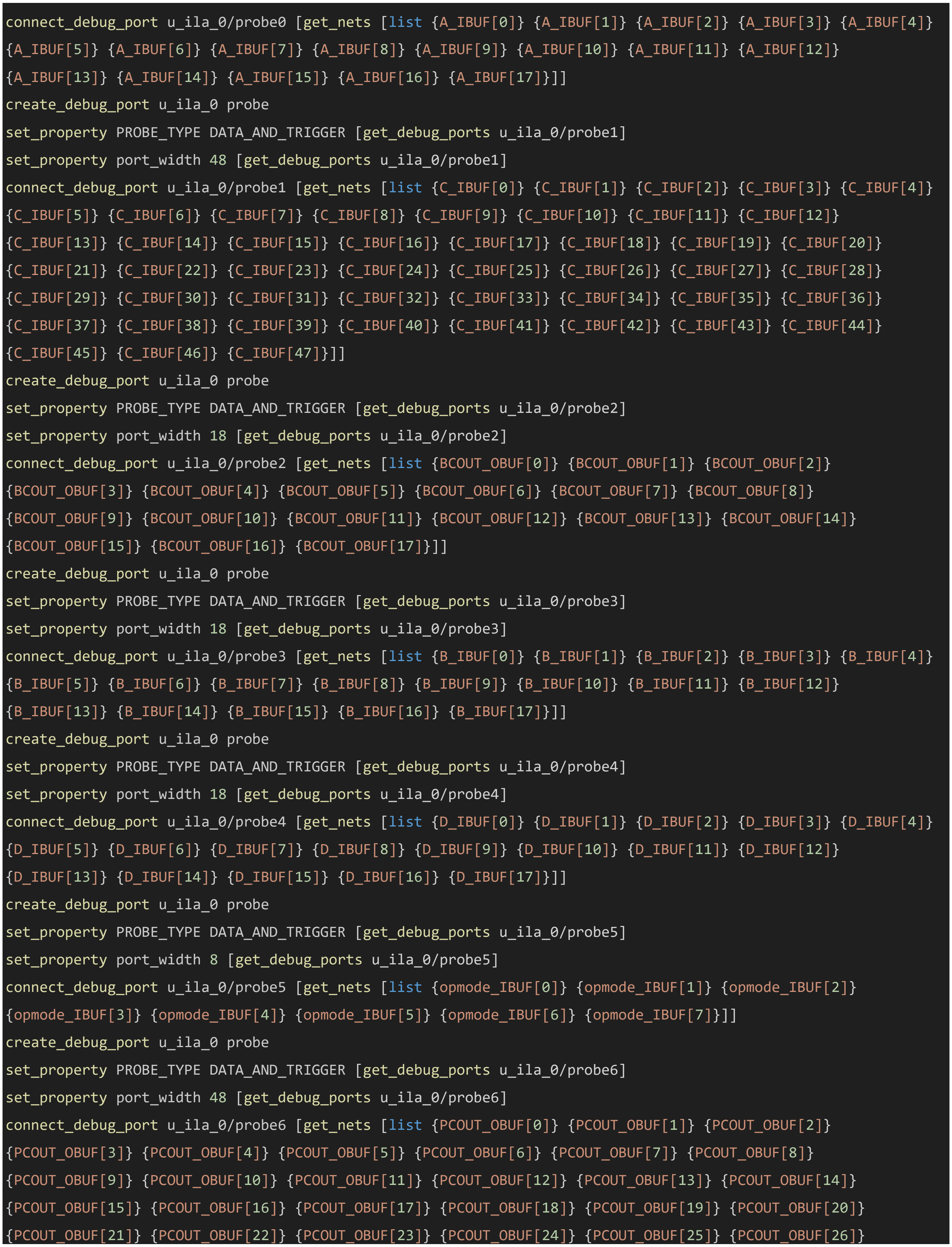
```
#set_property -dict { PACKAGE_PIN N18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[0]}]
#set_property -dict { PACKAGE_PIN L18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[1]}]
#set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[2]}]
#set_property -dict { PACKAGE_PIN J18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[3]}]
#set_property -dict { PACKAGE_PIN J17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[0]}]
#set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[1]}]
#set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[2]}]
#set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[3]}]
#set_property -dict { PACKAGE_PIN P19   IOSTANDARD LVCMOS33 } [get_ports Hsync]
#set_property -dict { PACKAGE_PIN R19   IOSTANDARD LVCMOS33 } [get_ports Vsync]


##USB-RS232 Interface
#set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 } [get_ports RsRx]
#set_property -dict { PACKAGE_PIN A18   IOSTANDARD LVCMOS33 } [get_ports RsTx]


##USB HID (PS/2)
#set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33   PULLUP true } [get_ports PS2Clk]
#set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33   PULLUP true } [get_ports PS2Data]


##Quad SPI Flash
##Note that CCLK_0 cannot be placed in 7 series devices. You can access it using the
##STARTUPE2 primitive.
#set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[0]}]
#set_property -dict { PACKAGE_PIN D19   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[1]}]
#set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[2]}]
#set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[3]}]
#set_property -dict { PACKAGE_PIN K19   IOSTANDARD LVCMOS33 } [get_ports QspiCSn]


create_debug_core u_ila_0 ila
set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
set_property port_width 1 [get_debug_ports u_ila_0/clk]
connect_debug_port u_ila_0/clk [get_nets [list clk_IBUF_BUFG]]
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
set_property port_width 18 [get_debug_ports u_ila_0/probe0]
```



```
connect_debug_port u_ila_0/probe0 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]} {A_IBUF[3]} {A_IBUF[4]}
{A_IBUF[5]} {A_IBUF[6]} {A_IBUF[7]} {A_IBUF[8]} {A_IBUF[9]} {A_IBUF[10]} {A_IBUF[11]} {A_IBUF[12]}
{A_IBUF[13]} {A_IBUF[14]} {A_IBUF[15]} {A_IBUF[16]} {A_IBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
set_property port_width 48 [get_debug_ports u_ila_0/probe1]
connect_debug_port u_ila_0/probe1 [get_nets [list {C_IBUF[0]} {C_IBUF[1]} {C_IBUF[2]} {C_IBUF[3]} {C_IBUF[4]}
{C_IBUF[5]} {C_IBUF[6]} {C_IBUF[7]} {C_IBUF[8]} {C_IBUF[9]} {C_IBUF[10]} {C_IBUF[11]} {C_IBUF[12]}
{C_IBUF[13]} {C_IBUF[14]} {C_IBUF[15]} {C_IBUF[16]} {C_IBUF[17]} {C_IBUF[18]} {C_IBUF[19]} {C_IBUF[20]}
{C_IBUF[21]} {C_IBUF[22]} {C_IBUF[23]} {C_IBUF[24]} {C_IBUF[25]} {C_IBUF[26]} {C_IBUF[27]} {C_IBUF[28]}
{C_IBUF[29]} {C_IBUF[30]} {C_IBUF[31]} {C_IBUF[32]} {C_IBUF[33]} {C_IBUF[34]} {C_IBUF[35]} {C_IBUF[36]}
{C_IBUF[37]} {C_IBUF[38]} {C_IBUF[39]} {C_IBUF[40]} {C_IBUF[41]} {C_IBUF[42]} {C_IBUF[43]} {C_IBUF[44]}
{C_IBUF[45]} {C_IBUF[46]} {C_IBUF[47]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
set_property port_width 18 [get_debug_ports u_ila_0/probe2]
connect_debug_port u_ila_0/probe2 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]} {BCOUT_OBUF[2]}
{BCOUT_OBUF[3]} {BCOUT_OBUF[4]} {BCOUT_OBUF[5]} {BCOUT_OBUF[6]} {BCOUT_OBUF[7]} {BCOUT_OBUF[8]}
{BCOUT_OBUF[9]} {BCOUT_OBUF[10]} {BCOUT_OBUF[11]} {BCOUT_OBUF[12]} {BCOUT_OBUF[13]} {BCOUT_OBUF[14]}
{BCOUT_OBUF[15]} {BCOUT_OBUF[16]} {BCOUT_OBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
set_property port_width 18 [get_debug_ports u_ila_0/probe3]
connect_debug_port u_ila_0/probe3 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]} {B_IBUF[3]} {B_IBUF[4]}
{B_IBUF[5]} {B_IBUF[6]} {B_IBUF[7]} {B_IBUF[8]} {B_IBUF[9]} {B_IBUF[10]} {B_IBUF[11]} {B_IBUF[12]}
{B_IBUF[13]} {B_IBUF[14]} {B_IBUF[15]} {B_IBUF[16]} {B_IBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 18 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list {D_IBUF[0]} {D_IBUF[1]} {D_IBUF[2]} {D_IBUF[3]} {D_IBUF[4]}
{D_IBUF[5]} {D_IBUF[6]} {D_IBUF[7]} {D_IBUF[8]} {D_IBUF[9]} {D_IBUF[10]} {D_IBUF[11]} {D_IBUF[12]}
{D_IBUF[13]} {D_IBUF[14]} {D_IBUF[15]} {D_IBUF[16]} {D_IBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
set_property port_width 8 [get_debug_ports u_ila_0/probe5]
connect_debug_port u_ila_0/probe5 [get_nets [list {opmode_IBUF[0]} {opmode_IBUF[1]} {opmode_IBUF[2]}
{opmode_IBUF[3]} {opmode_IBUF[4]} {opmode_IBUF[5]} {opmode_IBUF[6]} {opmode_IBUF[7]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
set_property port_width 48 [get_debug_ports u_ila_0/probe6]
connect_debug_port u_ila_0/probe6 [get_nets [list {PCOUT_OBUF[0]} {PCOUT_OBUF[1]} {PCOUT_OBUF[2]}
{PCOUT_OBUF[3]} {PCOUT_OBUF[4]} {PCOUT_OBUF[5]} {PCOUT_OBUF[6]} {PCOUT_OBUF[7]} {PCOUT_OBUF[8]}
{PCOUT_OBUF[9]} {PCOUT_OBUF[10]} {PCOUT_OBUF[11]} {PCOUT_OBUF[12]} {PCOUT_OBUF[13]} {PCOUT_OBUF[14]}
{PCOUT_OBUF[15]} {PCOUT_OBUF[16]} {PCOUT_OBUF[17]} {PCOUT_OBUF[18]} {PCOUT_OBUF[19]} {PCOUT_OBUF[20]}
{PCOUT_OBUF[21]} {PCOUT_OBUF[22]} {PCOUT_OBUF[23]} {PCOUT_OBUF[24]} {PCOUT_OBUF[25]} {PCOUT_OBUF[26]}
{PCOUT_OBUF[27]} {PCOUT_OBUF[28]} {PCOUT_OBUF[29]} {PCOUT_OBUF[30]} {PCOUT_OBUF[31]} {PCOUT_OBUF[32]}
{PCOUT_OBUF[33]} {PCOUT_OBUF[34]} {PCOUT_OBUF[35]} {PCOUT_OBUF[36]} {PCOUT_OBUF[37]} {PCOUT_OBUF[38]}
{PCOUT_OBUF[39]} {PCOUT_OBUF[40]} {PCOUT_OBUF[41]} {PCOUT_OBUF[42]} {PCOUT_OBUF[43]} {PCOUT_OBUF[44]}
{PCOUT_OBUF[45]} {PCOUT_OBUF[46]} {PCOUT_OBUF[47]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe7]
set_property port_width 48 [get_debug_ports u_ila_0/probe7]
connect_debug_port u_ila_0/probe7 [get_nets [list {PCIN_IBUF[0]} {PCIN_IBUF[1]} {PCIN_IBUF[2]} {PCIN_IBUF[3]}
{PCIN_IBUF[4]} {PCIN_IBUF[5]} {PCIN_IBUF[6]} {PCIN_IBUF[7]} {PCIN_IBUF[8]} {PCIN_IBUF[9]} {PCIN_IBUF[10]}
{PCIN_IBUF[11]} {PCIN_IBUF[12]} {PCIN_IBUF[13]} {PCIN_IBUF[14]} {PCIN_IBUF[15]} {PCIN_IBUF[16]}
{PCIN_IBUF[17]} {PCIN_IBUF[18]} {PCIN_IBUF[19]} {PCIN_IBUF[20]} {PCIN_IBUF[21]} {PCIN_IBUF[22]}
{PCIN_IBUF[23]} {PCIN_IBUF[24]} {PCIN_IBUF[25]} {PCIN_IBUF[26]} {PCIN_IBUF[27]} {PCIN_IBUF[28]}
{PCIN_IBUF[29]} {PCIN_IBUF[30]} {PCIN_IBUF[31]} {PCIN_IBUF[32]} {PCIN_IBUF[33]} {PCIN_IBUF[34]}
{PCIN_IBUF[35]} {PCIN_IBUF[36]} {PCIN_IBUF[37]} {PCIN_IBUF[38]} {PCIN_IBUF[39]} {PCIN_IBUF[40]}
{PCIN_IBUF[41]} {PCIN_IBUF[42]} {PCIN_IBUF[43]} {PCIN_IBUF[44]} {PCIN_IBUF[45]} {PCIN_IBUF[46]}
{PCIN_IBUF[47]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe8]
set_property port_width 36 [get_debug_ports u_ila_0/probe8]
connect_debug_port u_ila_0/probe8 [get_nets [list {M_OBUF[0]} {M_OBUF[1]} {M_OBUF[2]} {M_OBUF[3]} {M_OBUF[4]}
{M_OBUF[5]} {M_OBUF[6]} {M_OBUF[7]} {M_OBUF[8]} {M_OBUF[9]} {M_OBUF[10]} {M_OBUF[11]} {M_OBUF[12]}
{M_OBUF[13]} {M_OBUF[14]} {M_OBUF[15]} {M_OBUF[16]} {M_OBUF[17]} {M_OBUF[18]} {M_OBUF[19]} {M_OBUF[20]}
{M_OBUF[21]} {M_OBUF[22]} {M_OBUF[23]} {M_OBUF[24]} {M_OBUF[25]} {M_OBUF[26]} {M_OBUF[27]} {M_OBUF[28]}
{M_OBUF[29]} {M_OBUF[30]} {M_OBUF[31]} {M_OBUF[32]} {M_OBUF[33]} {M_OBUF[34]} {M_OBUF[35]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
set_property port_width 1 [get_debug_ports u_ila_0/probe9]
connect_debug_port u_ila_0/probe9 [get_nets [list carryoutF_OBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe10]
set_property port_width 1 [get_debug_ports u_ila_0/probe10]
connect_debug_port u_ila_0/probe10 [get_nets [list CEA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
set_property port_width 1 [get_debug_ports u_ila_0/probe11]
connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
set_property port_width 1 [get_debug_ports u_ila_0/probe12]
connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
set_property port_width 1 [get_debug_ports u_ila_0/probe13]
connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
create_debug_port u_ila_0 probe
```

```
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
set_property port_width 1 [get_debug_ports u_ila_0/probe14]
connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
set_property port_width 1 [get_debug_ports u_ila_0/probe15]
connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
set_property port_width 1 [get_debug_ports u_ila_0/probe16]
connect_debug_port u_ila_0/probe16 [get_nets [list CEOPMODE_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
set_property port_width 1 [get_debug_ports u_ila_0/probe17]
connect_debug_port u_ila_0/probe17 [get_nets [list CEP_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
set_property port_width 1 [get_debug_ports u_ila_0/probe18]
connect_debug_port u_ila_0/probe18 [get_nets [list clk_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
set_property port_width 1 [get_debug_ports u_ila_0/probe19]
connect_debug_port u_ila_0/probe19 [get_nets [list RSTA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
set_property port_width 1 [get_debug_ports u_ila_0/probe20]
connect_debug_port u_ila_0/probe20 [get_nets [list RSTB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
set_property port_width 1 [get_debug_ports u_ila_0/probe21]
connect_debug_port u_ila_0/probe21 [get_nets [list RSTC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
set_property port_width 1 [get_debug_ports u_ila_0/probe22]
connect_debug_port u_ila_0/probe22 [get_nets [list RSTCARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
set_property port_width 1 [get_debug_ports u_ila_0/probe23]
connect_debug_port u_ila_0/probe23 [get_nets [list RSTD_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
set_property port_width 1 [get_debug_ports u_ila_0/probe24]
connect_debug_port u_ila_0/probe24 [get_nets [list RSTM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
set_property port_width 1 [get_debug_ports u_ila_0/probe25]
connect_debug_port u_ila_0/probe25 [get_nets [list RSTOPMODE_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
set_property port_width 1 [get_debug_ports u_ila_0/probe26]
connect_debug_port u_ila_0/probe26 [get_nets [list RSTP_IBUF]]
set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
connect_debug_port dbg_hub/clk [get_nets clk_IBUF_BUFG]
```