EE 254

Electronic Instrumentation

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Lecture Note #11

Content (Brief)

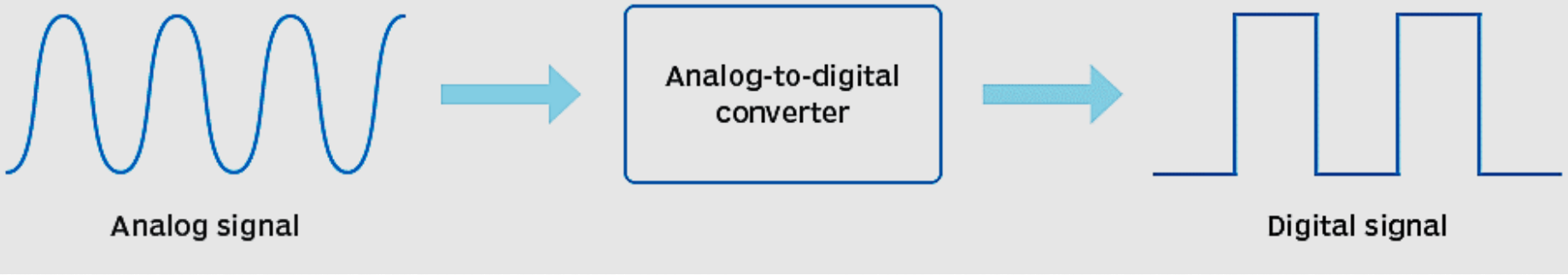
4. Data Converters

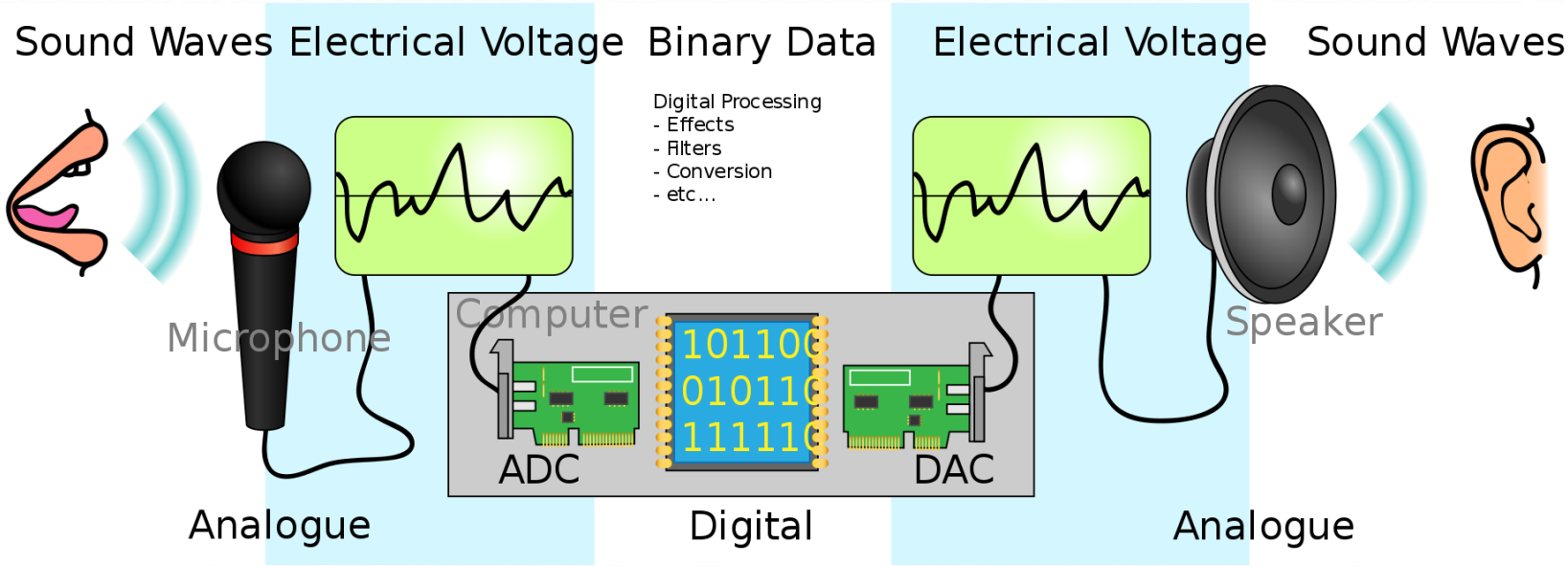
- Analogue to Digital (A/D) Conversion (ADC)
- Digital to Analogue (D/A) Conversion (DAC)
- Sample and Hold Circuit

A/D and D/A Conversion Techniques

What and Why ?

- What is data conversion?
- Why data conversion is needed?





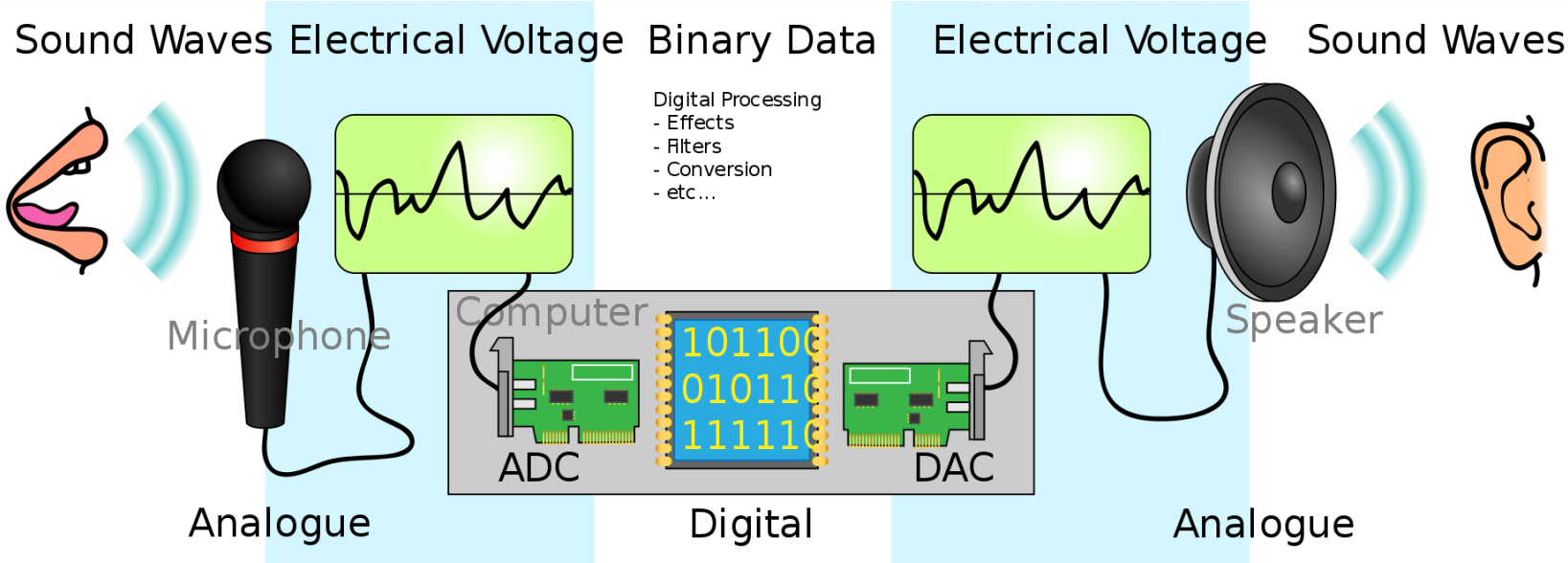
What and Why ?

- **Analogue to Digital Converter (ADC)**

  Converts analogue sound into digital signals that can be stored on a computer

- **Digital to Analogue Converter (DAC)**

  Converts digital signals stored on a computer into analogue sound that can be played through devices such as speakers

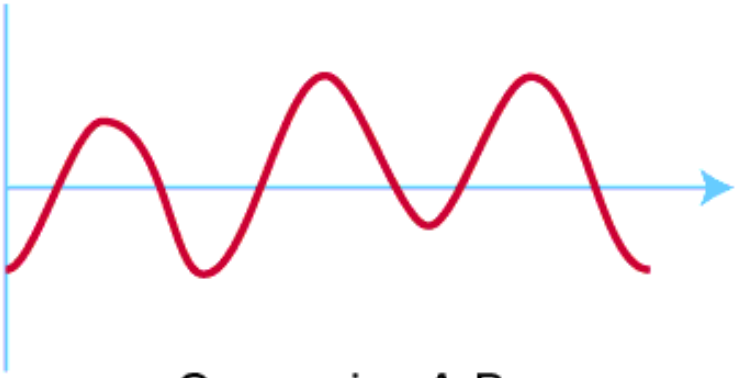


- **fig 1.** The original analogue sound wave is ***a continuous set of points***

- **fig 2.** ADC converts sound into ***digital data***

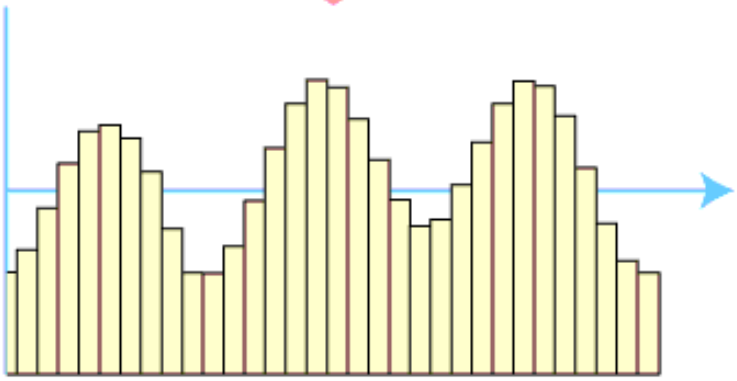
- **fig 3.** DAC converts digital data into ***analogue sound***, the analogue wave produced may differ significantly from the original sound wave

fig. 1



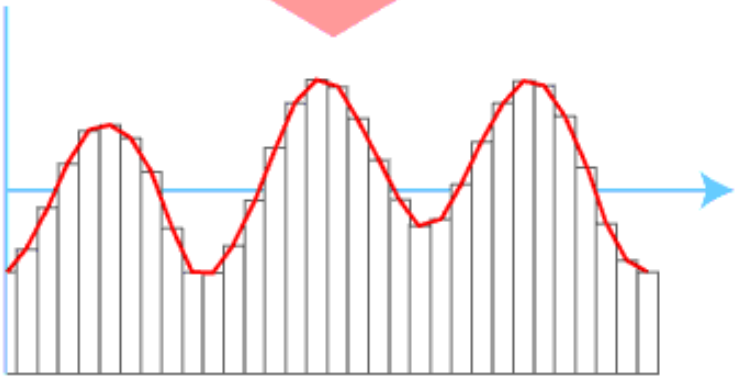
Conversion A-D

fig. 2

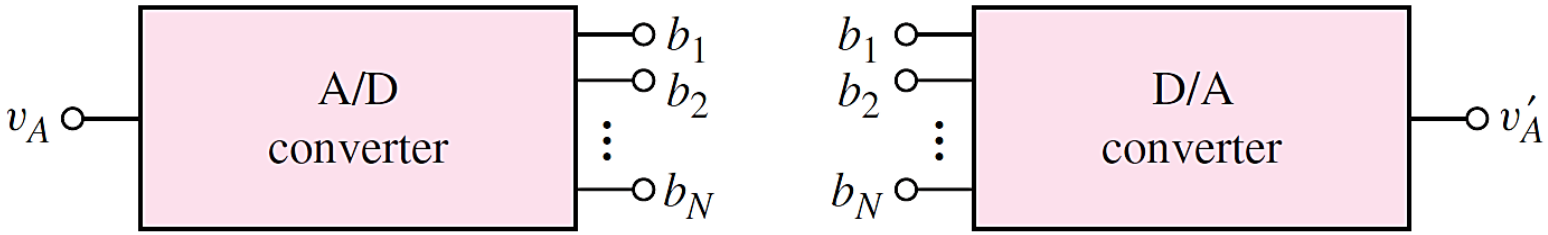


Conversion D-A

fig. 3



Basic A/D and D/A Concepts



Conversion to an N-bit digital signal:

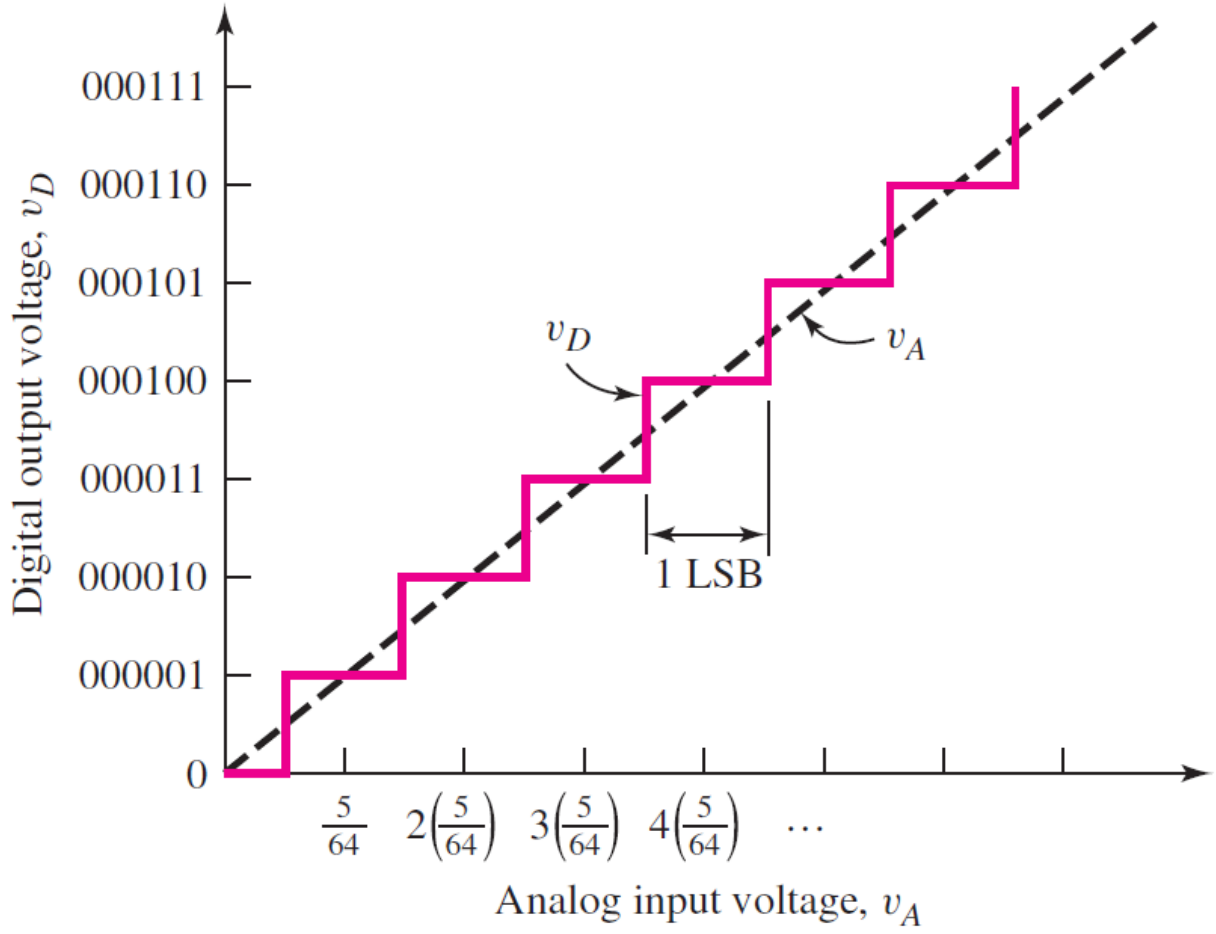
$$v_D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N}$$

where b_1, b_2, etc. are the bit coefficients that are either a 1 or 0. An analog signal v_A is applied to the input of the A/D converter.

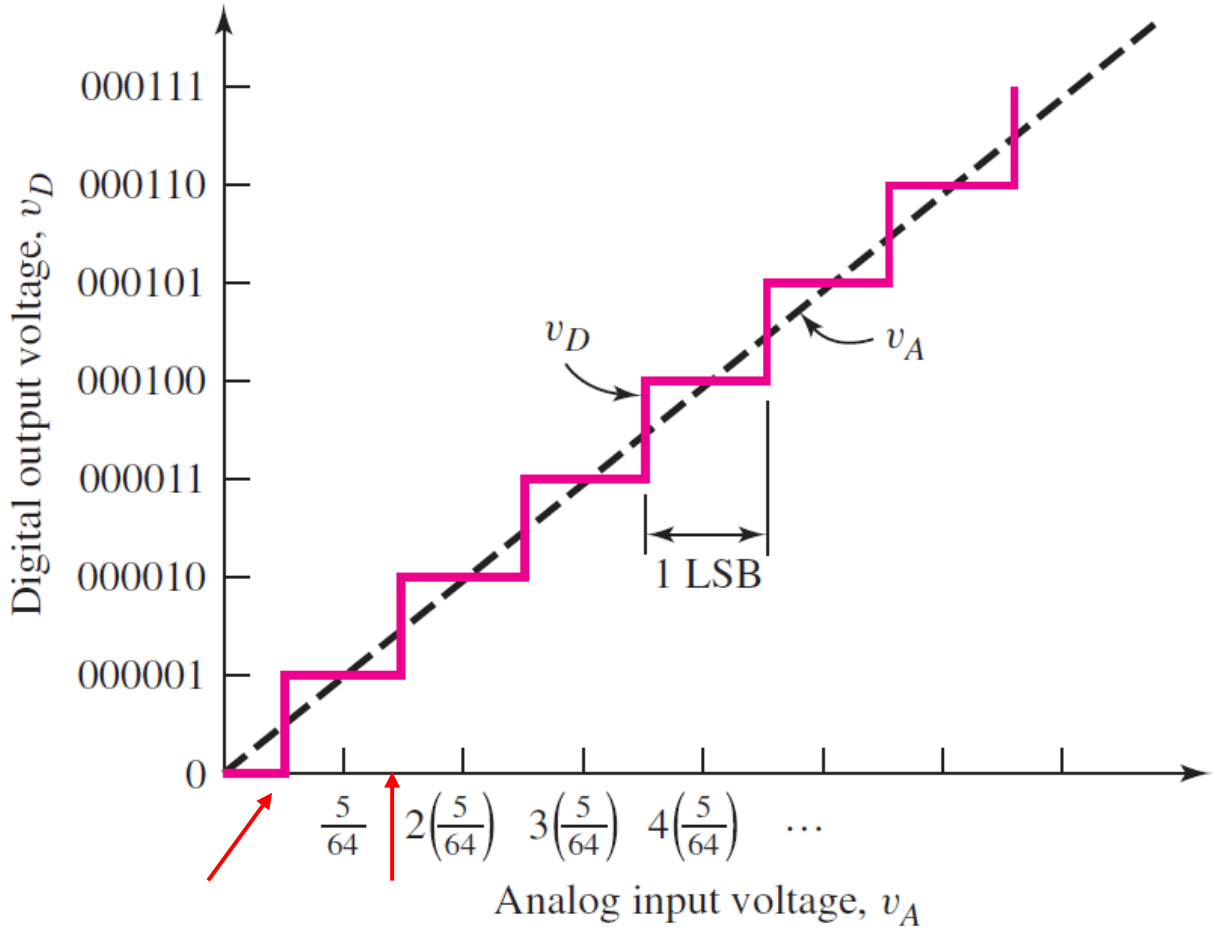
- The bit b_1 is the **most significant bit (MSB)** and the bit b_N is the **least significant bit (LSB)**.

Analog-to-Digital Conversion Concept

- Conversion of an analog signal represented by a voltage in the range $0 \leq v_A \leq 5\,V$ to a 6-bit word digital signal.

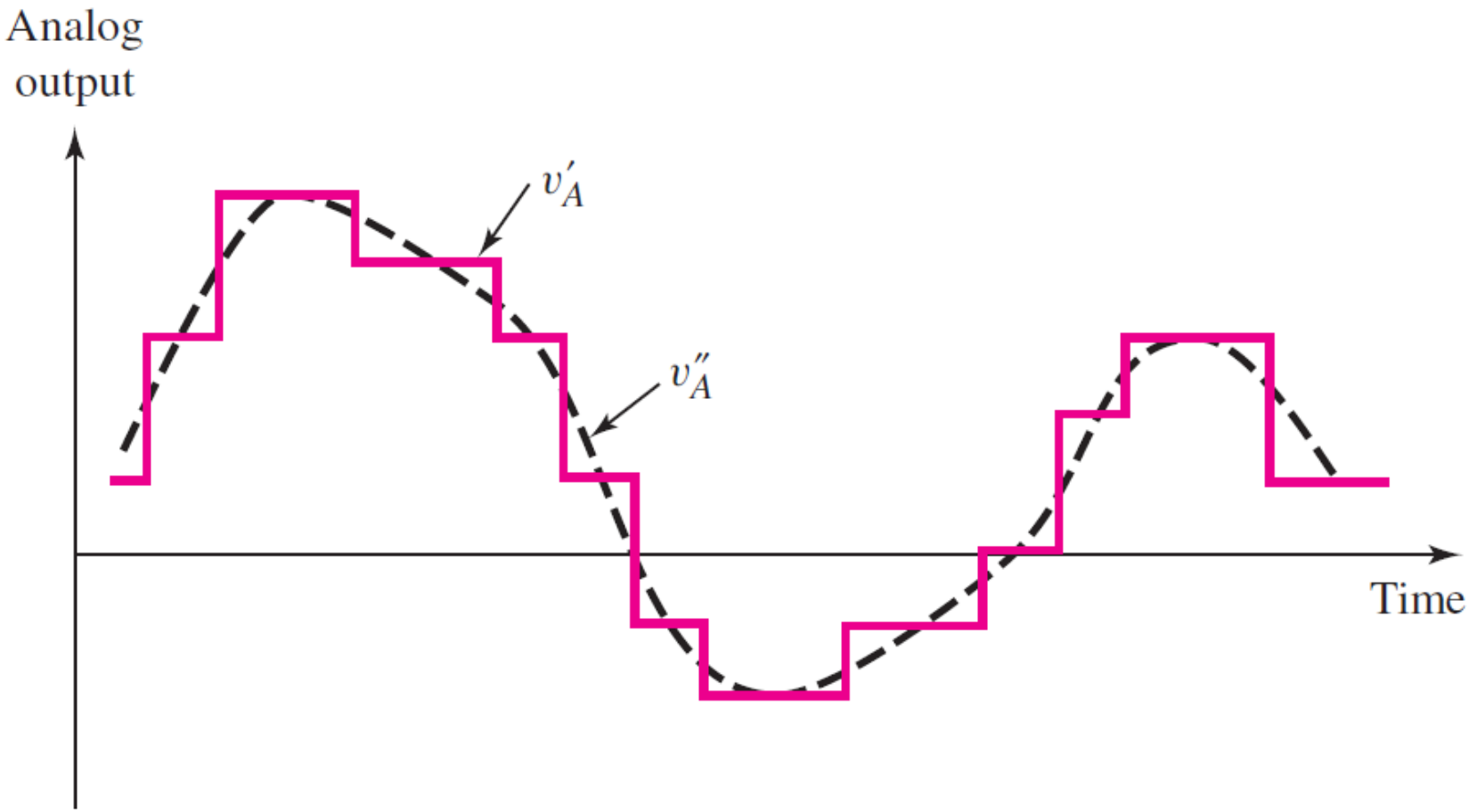


Analog-to-Digital Conversion Concept



- There is an Quantization error in A/D conversion.
- A larger number of bits can reduce it, but requires a more complex circuit.

Digital-to-Analog Conversion Concept



- v'_A is in the form of stair steps.
- Normally, v'_A is fed through a low-pass filter to smooth out the signal to produce the dotted signal v''_A

Analogue-to-Digital Converters

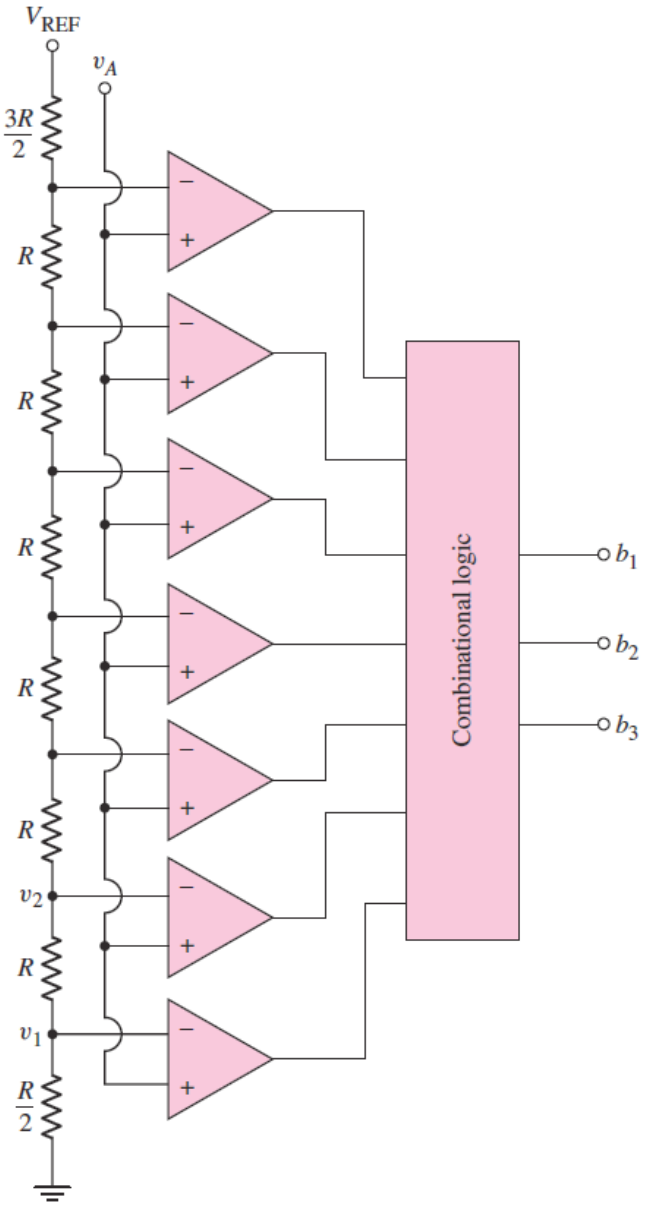
1. Parallel or Flash ADC
2. Counting ADC
3. Dual-Slope ADC
4. Successive Approximation A/D Converter
5. Semi-flash ADC
6. Delta-Sigma ADC
7. Pipelined ADC

Analog-to-Digital Converters

① Parallel or Flash A/D

- Is the simplest in concept.
- The analog input signal v_A is applied to seven comparators at the noninverting terminals.
- A reference voltage is applied to a resistive ladder network.
- The outputs of the ladder network are applied to the inverting terminals of the comparators.

3-bit flash A/D converter



Analog-to-Digital Converters

① Parallel or Flash A/D

- The total resistance in the ladder network is $8R$.
- $V_{REF}/8R$ represents 1 LSB in terms of current.
- **The smallest output voltage:**

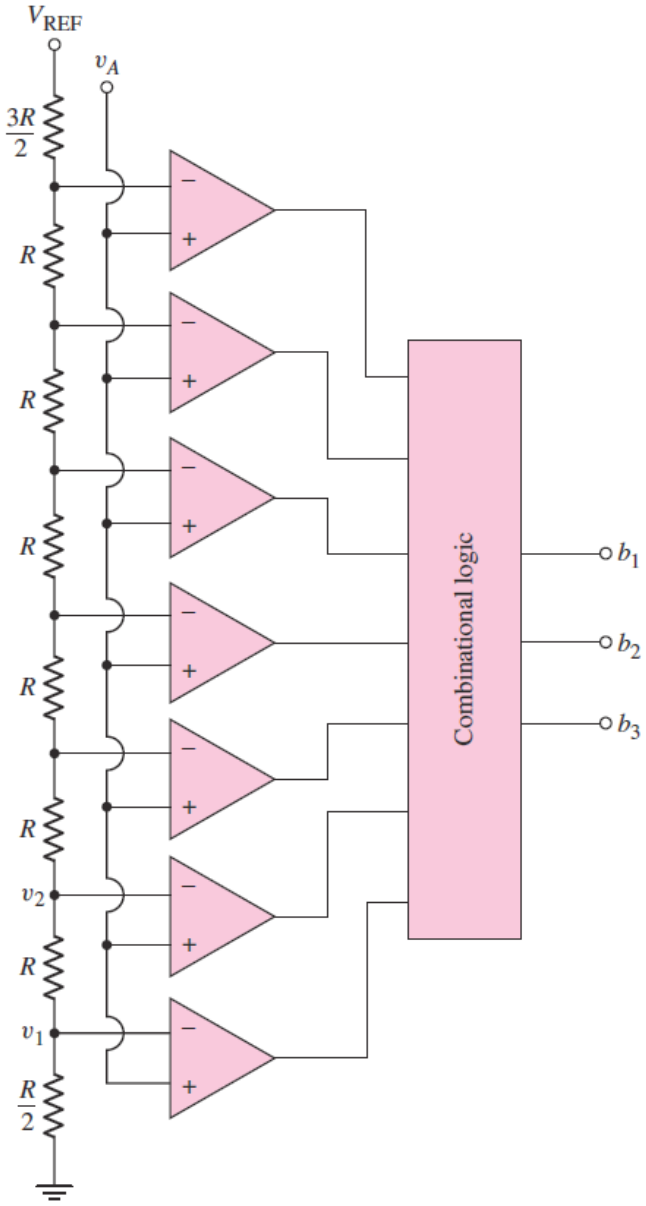
$$v_1 = \frac{V_{\text{REF}}}{8R}\left(\frac{R}{2}\right) = \frac{V_{\text{REF}}}{16}$$

which represents ½ LSB.

- **The second output voltage:**

$$v_2 = \frac{V_{\text{REF}}}{8R}\left(\frac{3R}{2}\right) = 3\left(\frac{V_{\text{REF}}}{16}\right)$$

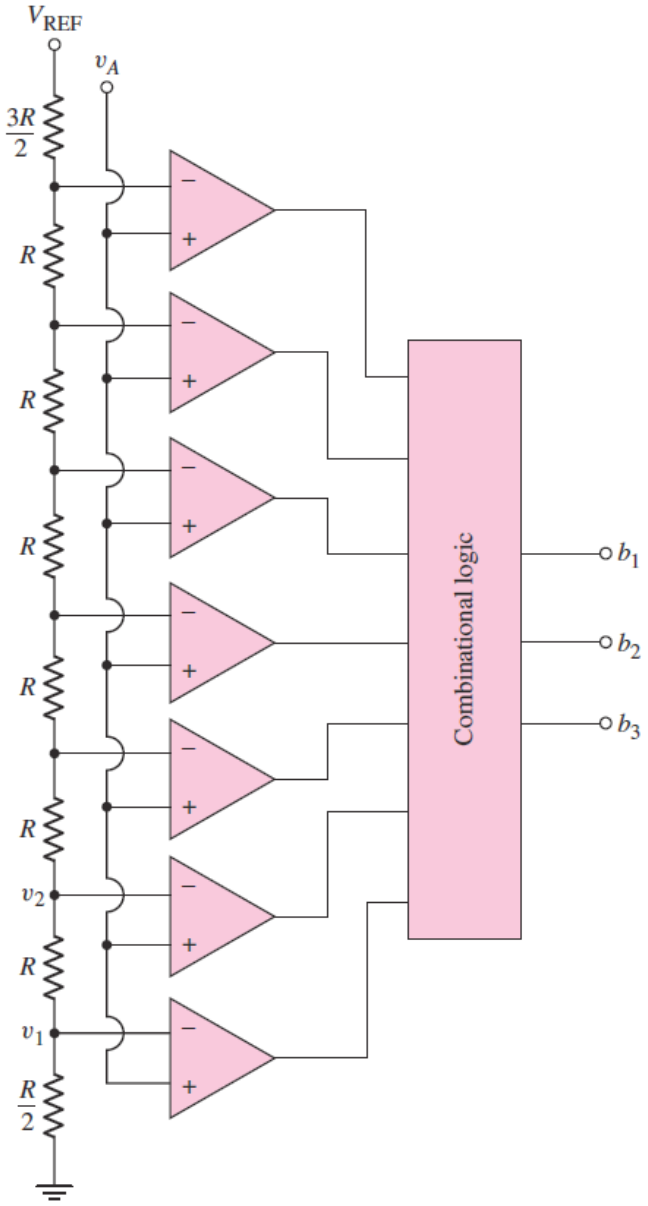
which represents $1\frac{1}{2}$ LSB.



Analog-to-Digital Converters

① Parallel or Flash A/D

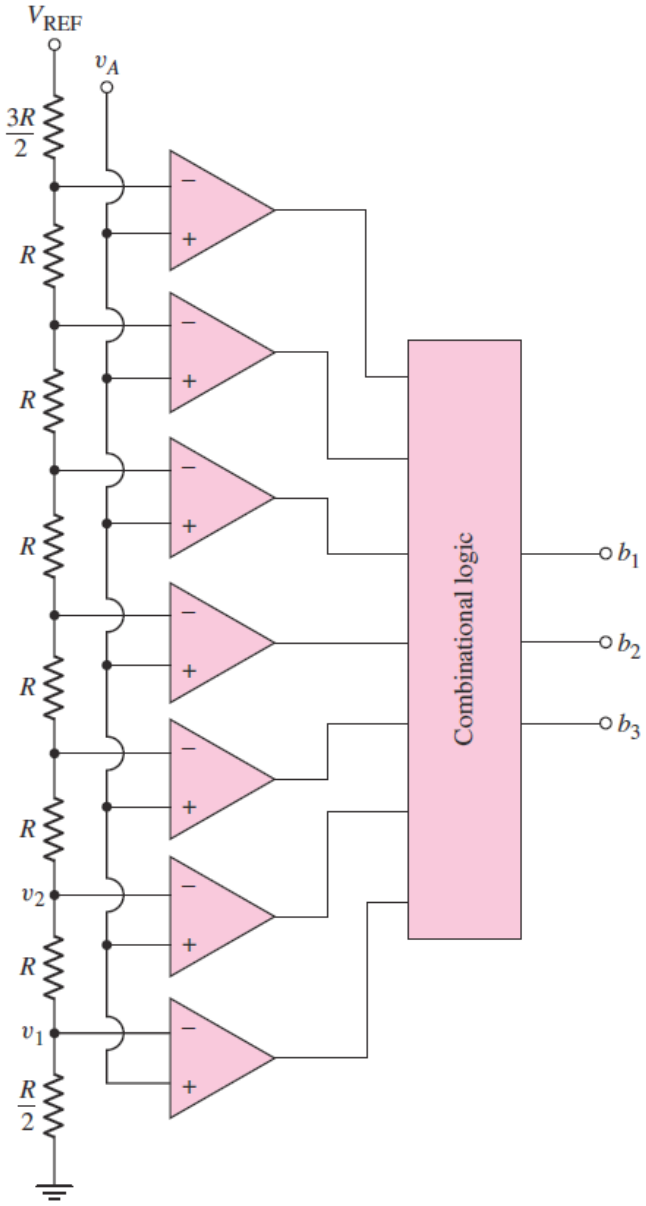
- If the analog input is $v_A < \frac{1}{2}$ LSB, the output of all comparators will be low.
- If the analog input is $\frac{1}{2} LSB < v_A < 1\frac{1}{2}$ LSB, the output of the first comparator goes high.
- As the analog input voltage increases, the outputs of additional comparators go high.
- The combinational logic network then produces the desired 3-bit output word.



Analog-to-Digital Converters

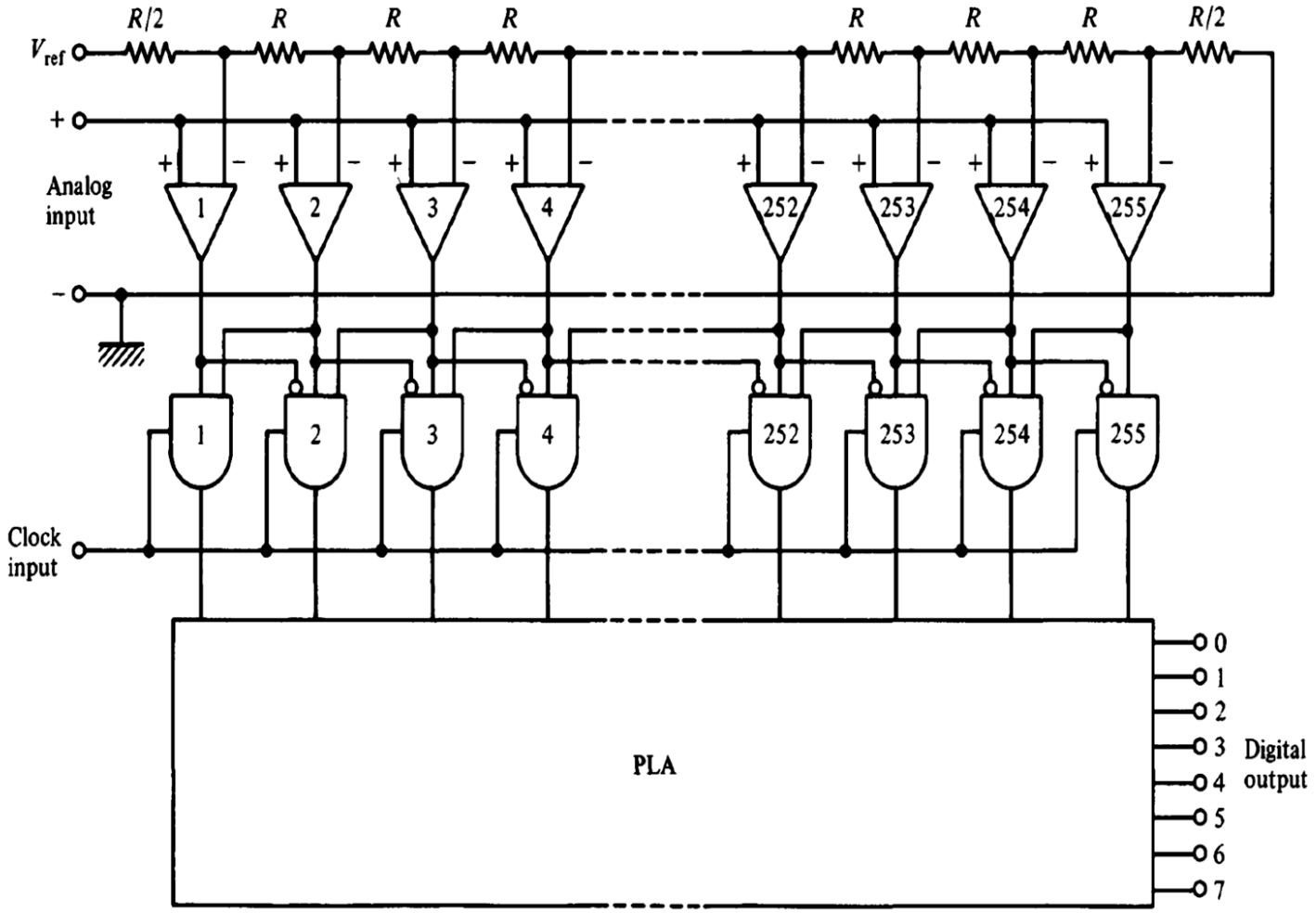
① Parallel or Flash A/D

- One of the disadvantages of the flash A/D converter is that the number of resistors and comparators increases rapidly as the desired number of output bits increases.
- 2^N resistors and $2^N - 1$ comparators are required.
- *Thus, for a 10-bit word, 1024 resistors and 1023 comparators are required.*
- *However, 10-bit resolution A/D flash converters have been fabricated as ICs.*



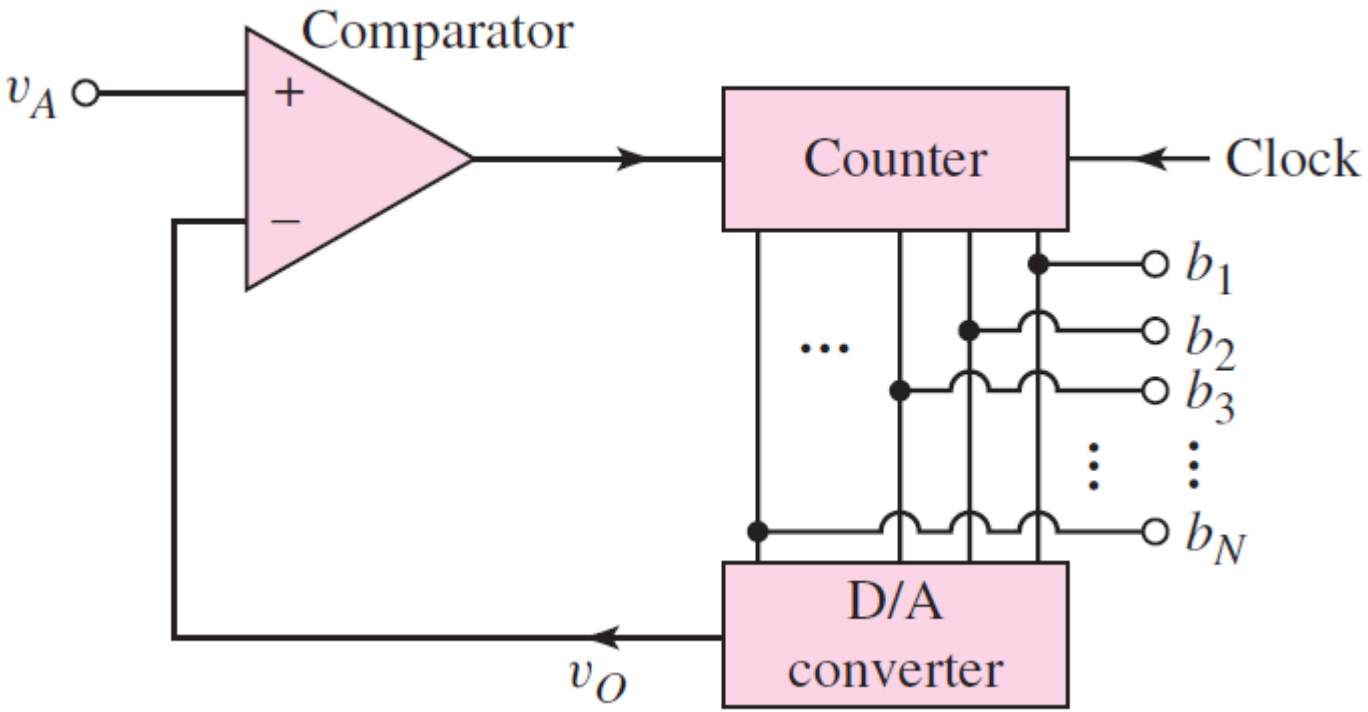
Analog-to-Digital Converters

① Parallel or Flash A/D



Analog-to-Digital Converters

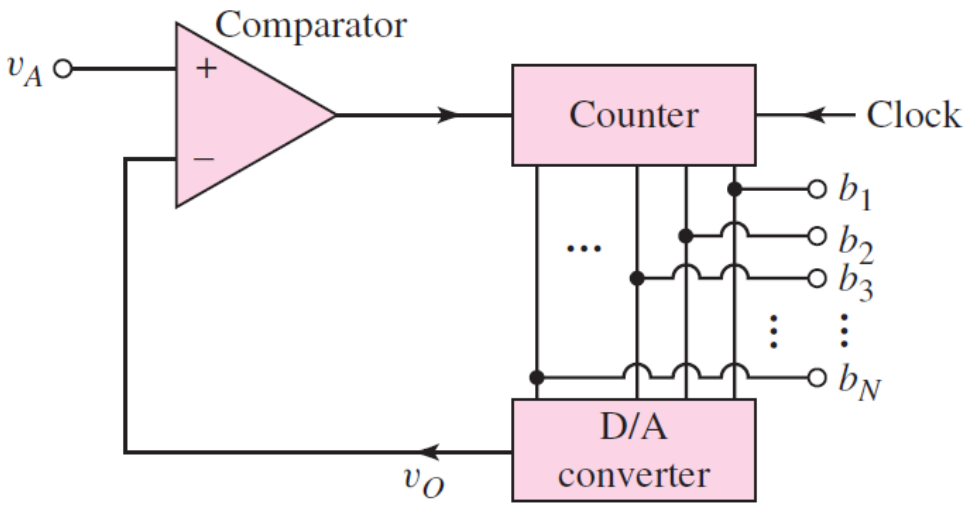
② Counting A/D



- This system contains **a comparator, a counter, and a D/A converter** in a feedback configuration.
- ***There is an additional control circuit which is not shown for simplicity***.

Analog-to-Digital Converters

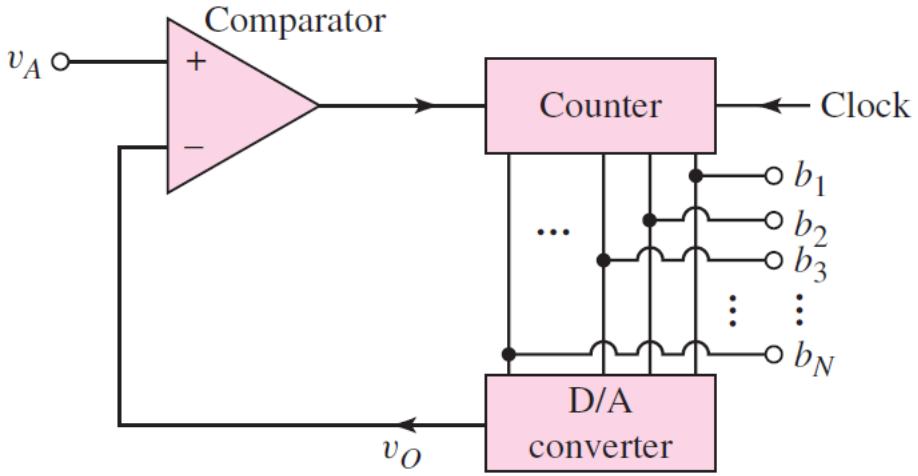
② Counting A/D

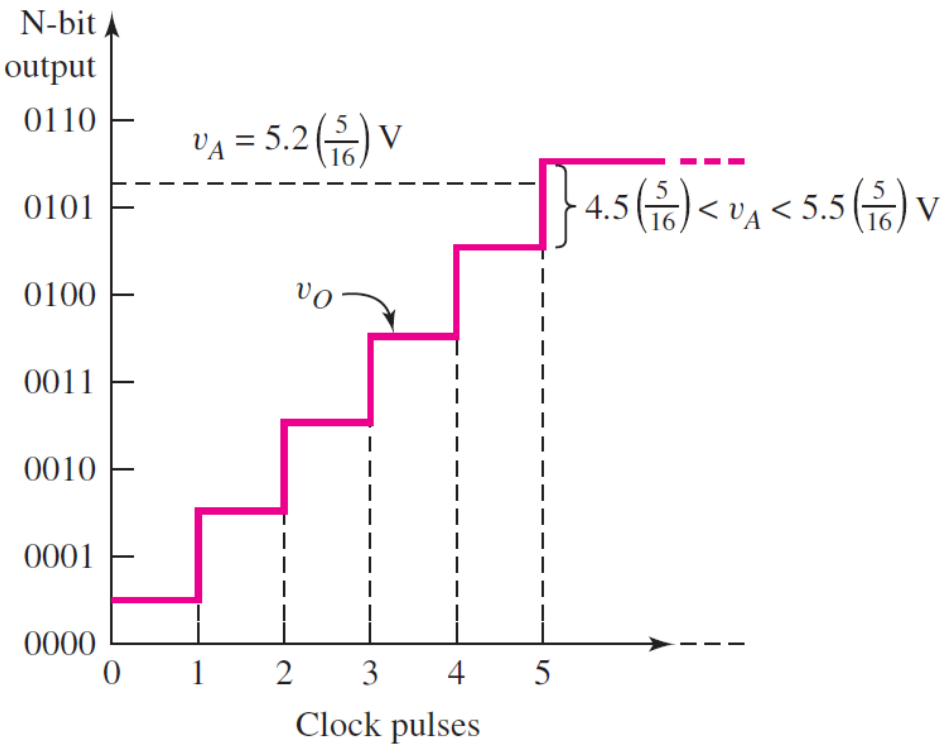


- Initially the output of the counter is set equal to zero and the output of the D/A converter is set to $v_O = \frac{1}{2}\,LSB$.
- When an analog input voltage v_A is applied, the output of the comparator is high (unless $v_A < \frac{1}{2}\,LSB$), which enables the counter.
- Then for each clock pulse, the output of the counter increases by one, producing an N-bit digital output.
- When the output of the D/A becomes just greater than the analog input voltage, the output of the comparator goes low and the counter is disabled.
- The N-bit digital output then corresponds to the analog input signal.

Analog-to-Digital Converters

② Counting A/D





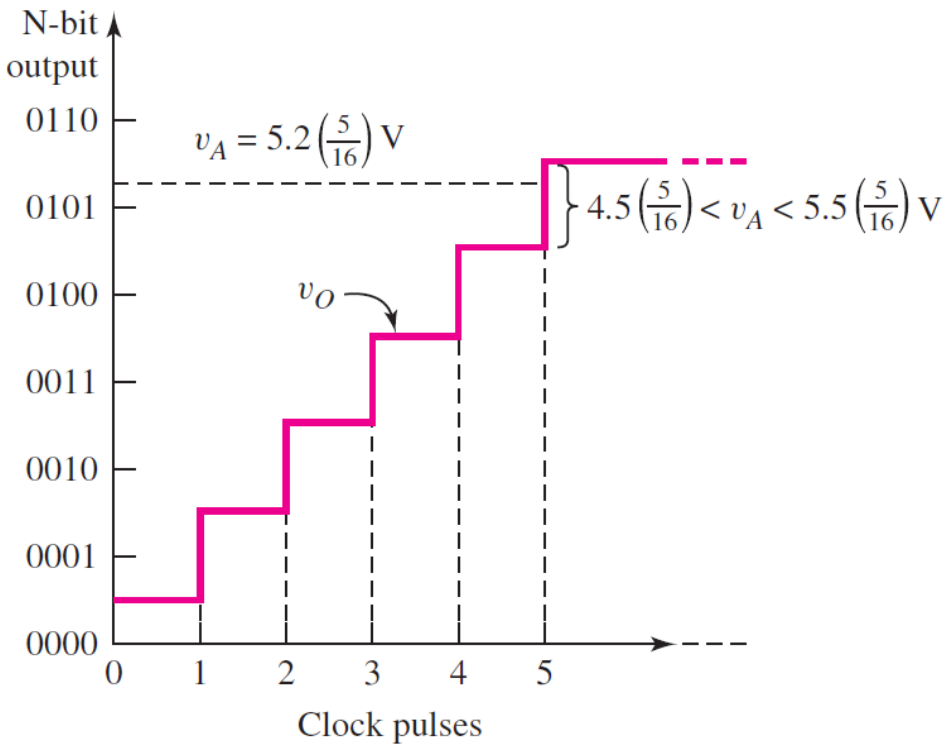
The timing diagram of a counting converter for a 4-bit digital output

- Assume that the analog input signal is in the range $0 \leq v_A \leq 5\ V$.
- A 1 LSB then corresponds to $5/16$ V.

Analog-to-Digital Converters

② Counting A/D

- Assume the analog input signal is $v_A = 5.2(\,5/16\,)\,V$.
- The initial output of the D/A, as mentioned, is a $1/2\ LSB$ ***offset voltage***.
- By including the offset voltage, the maximum quantization error will then be $\pm 1/2\ LSB$.



- After the fifth clock pulse, the output of the D/A:

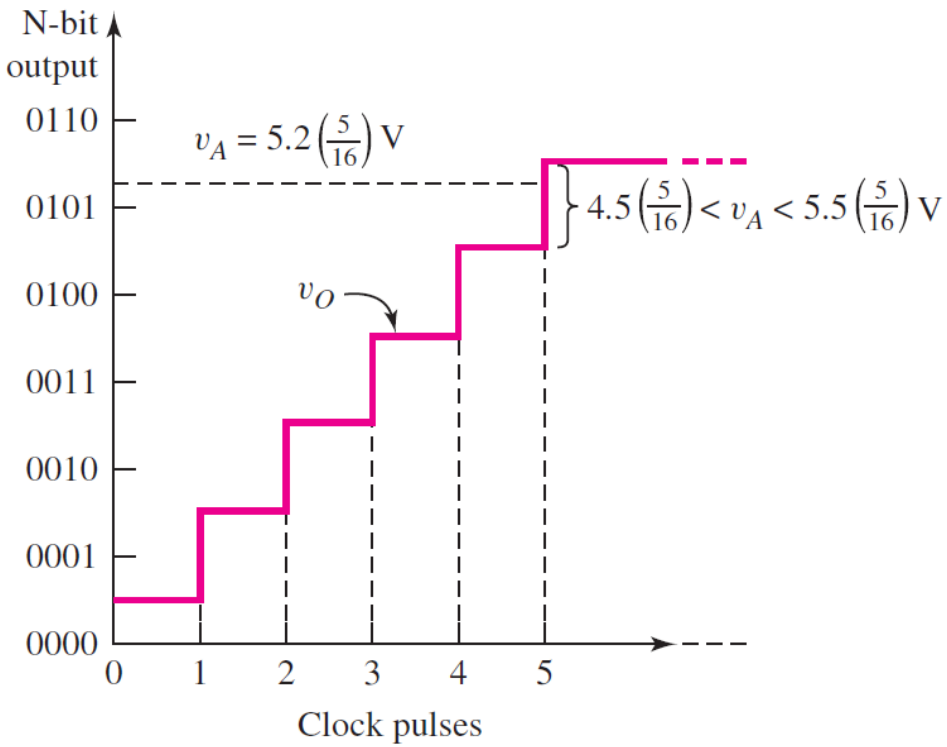
$$v_O = \frac{1}{2}\left(\frac{5}{16}\right) + 5\left(\frac{5}{16}\right) = 5.5\left(\frac{5}{16}\right)\text{V}$$

Analog-to-Digital Converters

② Counting A/D

$$v_O = \frac{1}{2}\left(\frac{5}{16}\right) + 5\left(\frac{5}{16}\right) = 5.5\left(\frac{5}{16}\right) \text{ V}$$

which is larger than v_A.

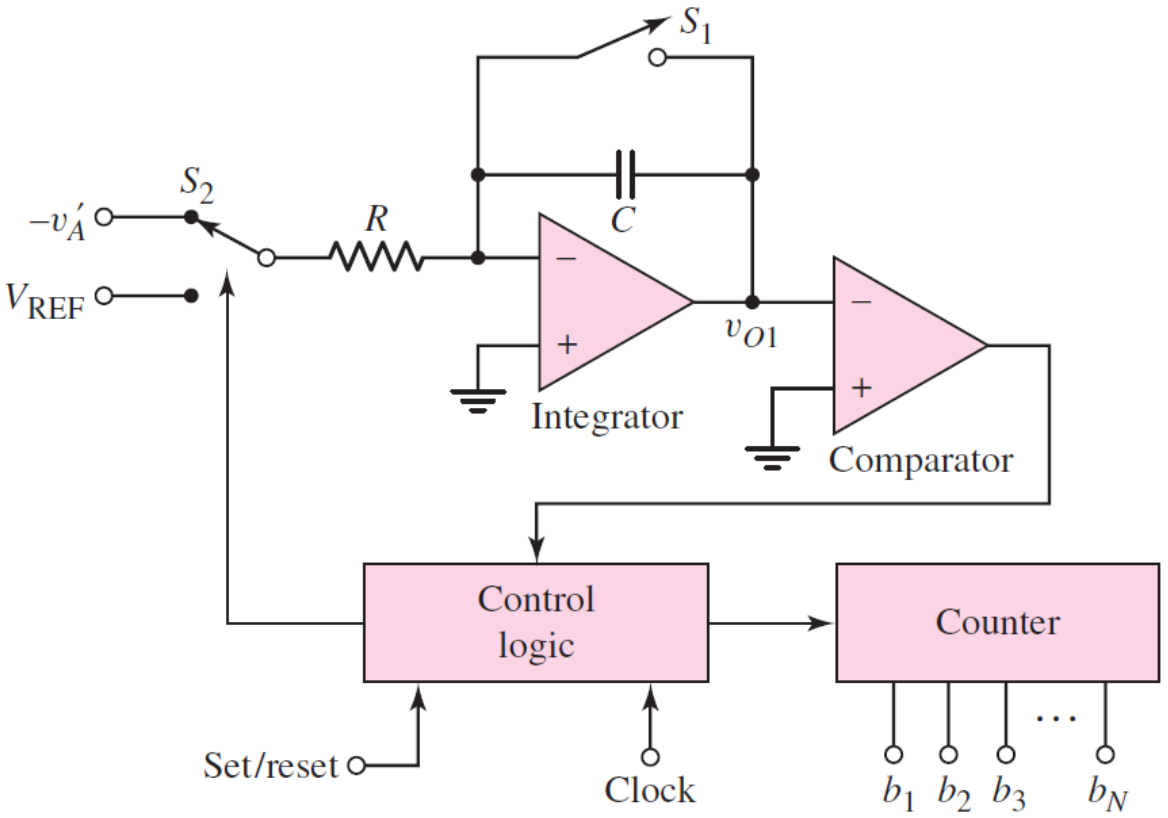


- The counter then stops counting and the digital output is 0101.
- The digital output corresponds to $5(5/16)\,V$, which is within 1/2 LSB of the analog input signal.
- To complete the conversion process, the clock must go through its complete cycle, which for a 4-bit output is 16 clock periods.

Analog-to-Digital Converters

③ Dual-Slope A/D

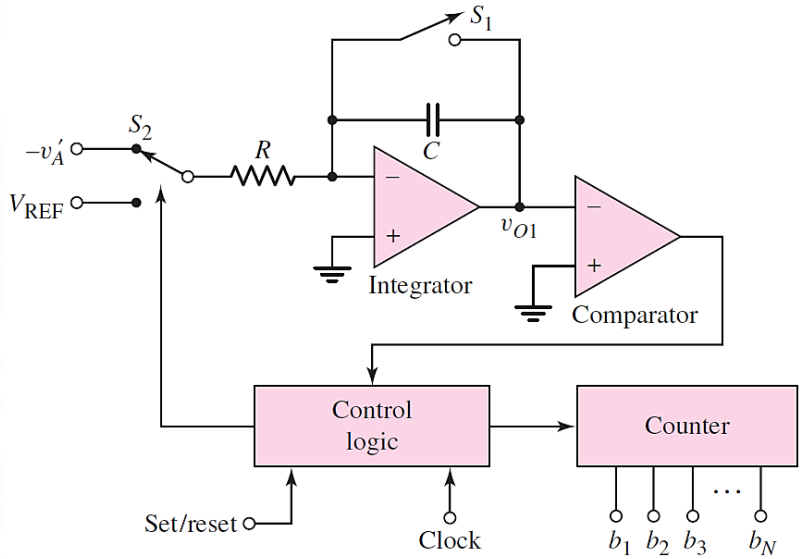
- This type of converter is found in high-resolution data acquisition systems.
- At $t = 0$, the reset switch S_1 opens and a negative input signal ($-v_A'$) is applied to the integrator.

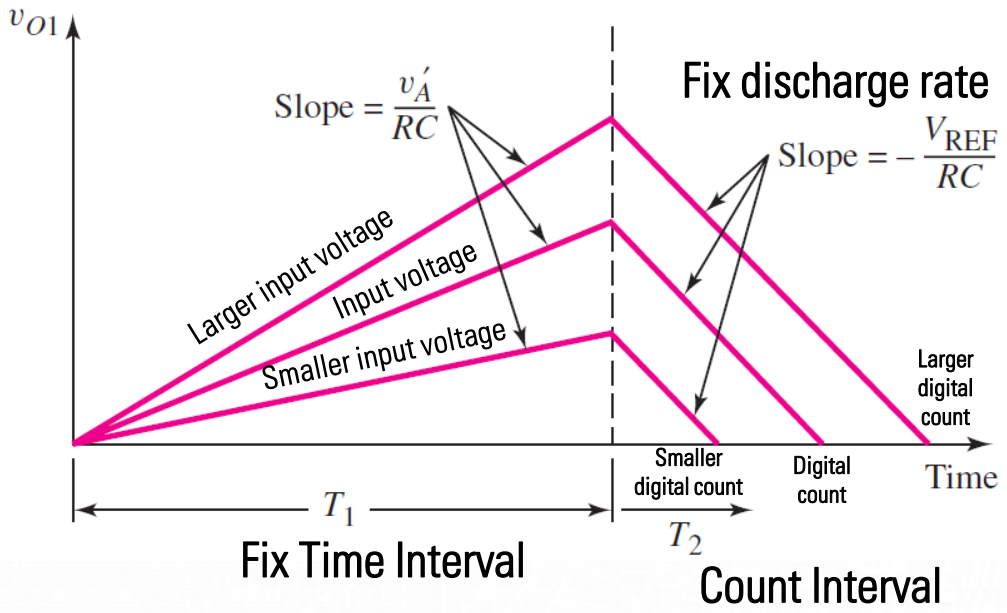


- The input signal v_A' is a sampled portion of the analog signal v_A and hence is a constant during the conversion process.

Analog-to-Digital Converters

③ Dual-Slope A/D

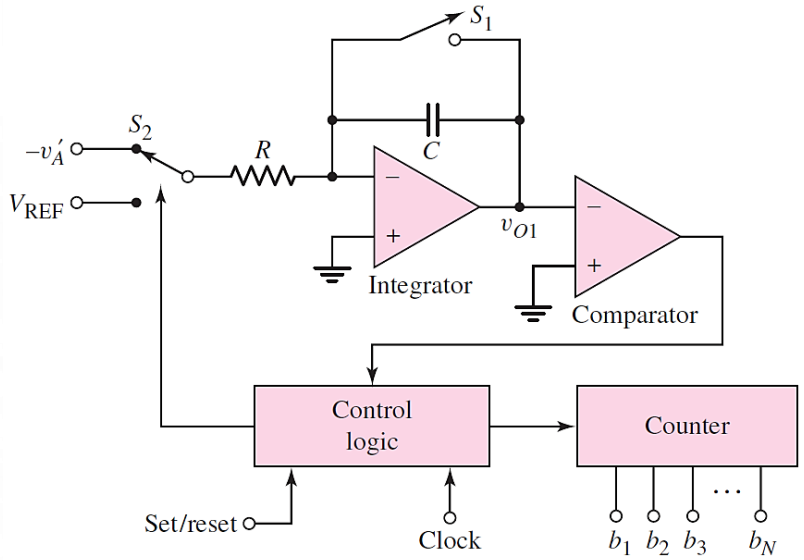


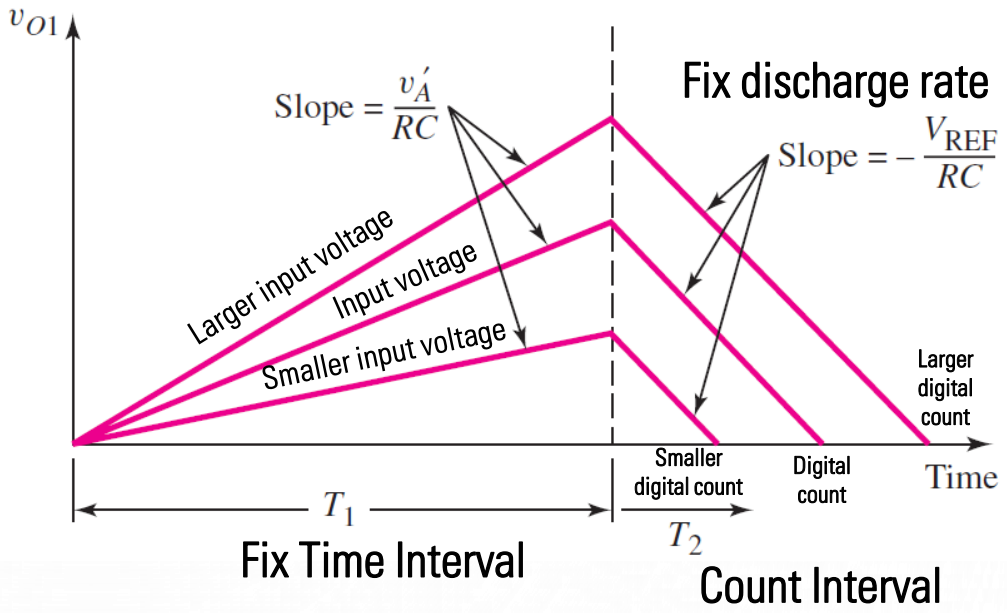


- The output v_{O1} of the integrator is a positive linear signal.
- The slope of the signal is proportional to the value of v_A'.
- This portion of the conversion process continues for a fixed time T_1, at which time the counter has reached its maximum value and overflows.
- At this time, the input switch S_2 changes to a positive input reference voltage V_{REF}.

Analog-to-Digital Converters

③ Dual-Slope A/D

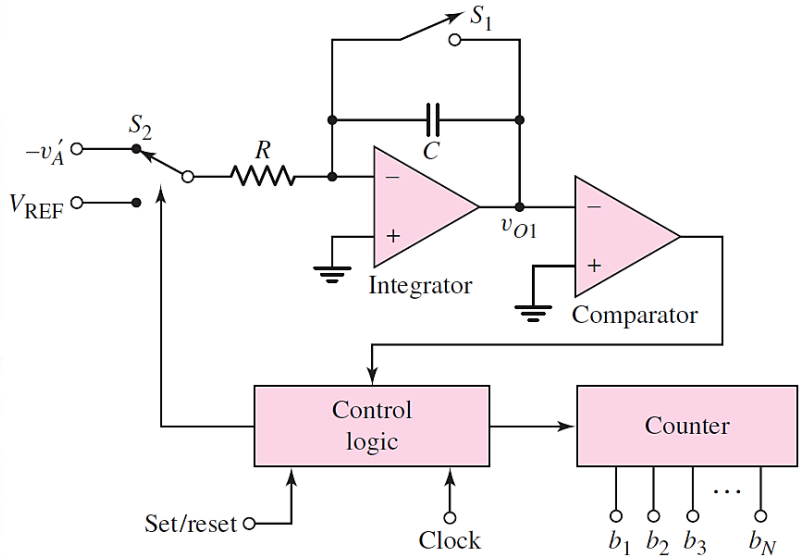


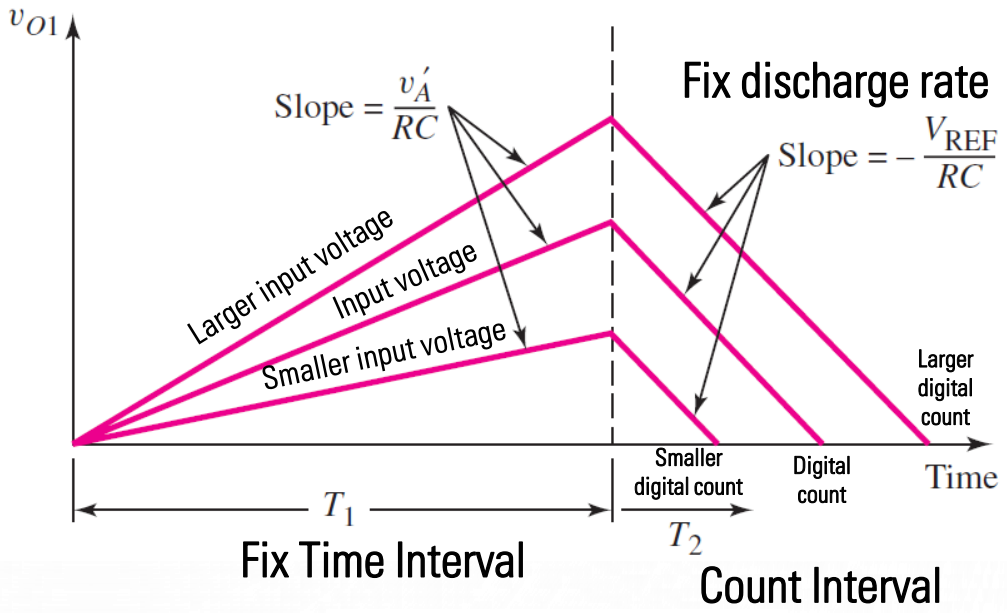


- The output of the integrator starts at the peak output voltage reached at T_1 and now has a negative slope.
- The counter has been reset and is now counting.
- The counting stops when the output voltage v_{O1} reaches zero.

Analog-to-Digital Converters

③ Dual-Slope A/D

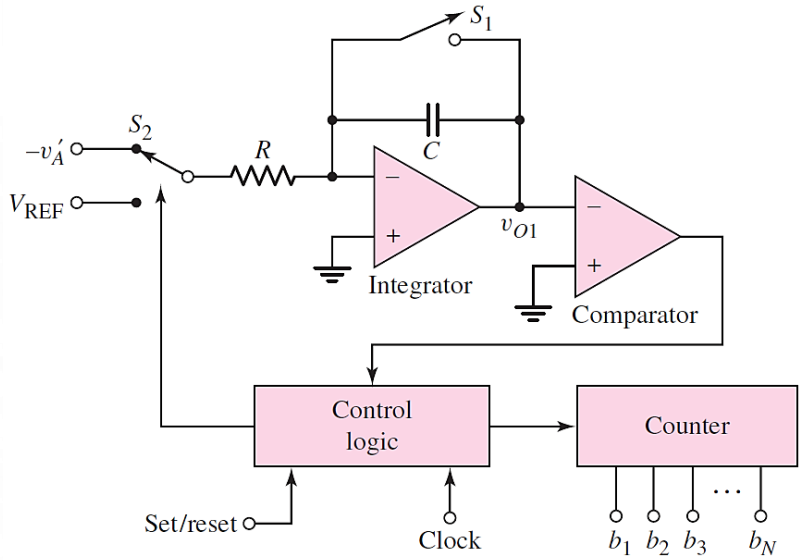


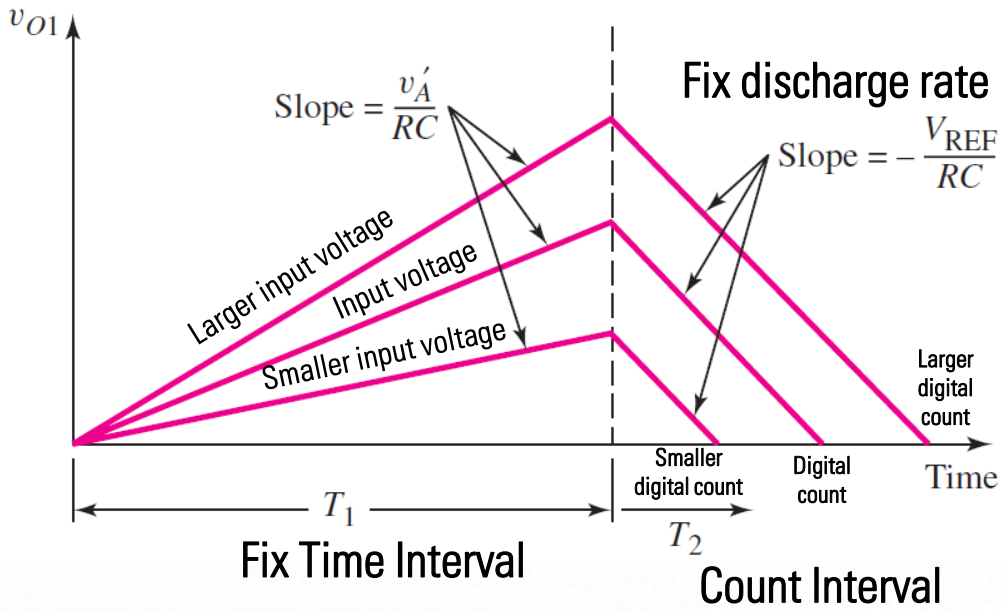


- The time T_2 is related to T_1 and v_A' by: $$T_2 = T_1\left(\frac{v_A'}{V_{\text{REF}}}\right)$$
- The counter reading at T_2 is given by: $$n = 2^N\left(\frac{v_A'}{V_{\text{REF}}}\right)$$
- The output of the counter is then the digital equivalent of v_A' .

Analog-to-Digital Converters

③ Dual-Slope A/D

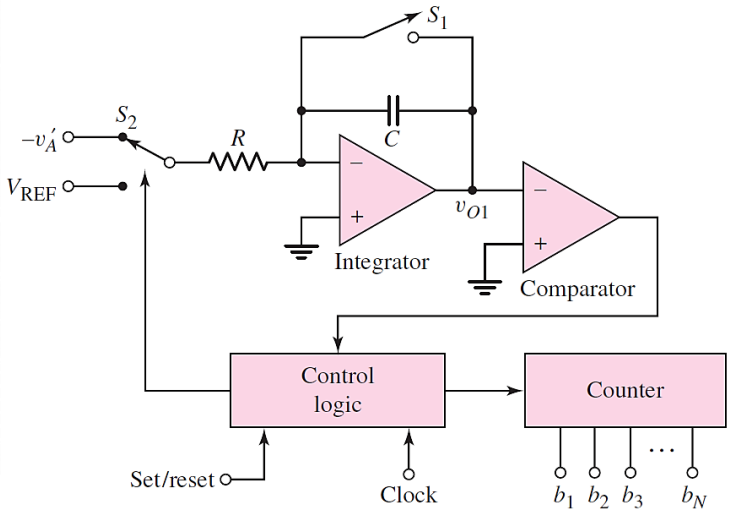


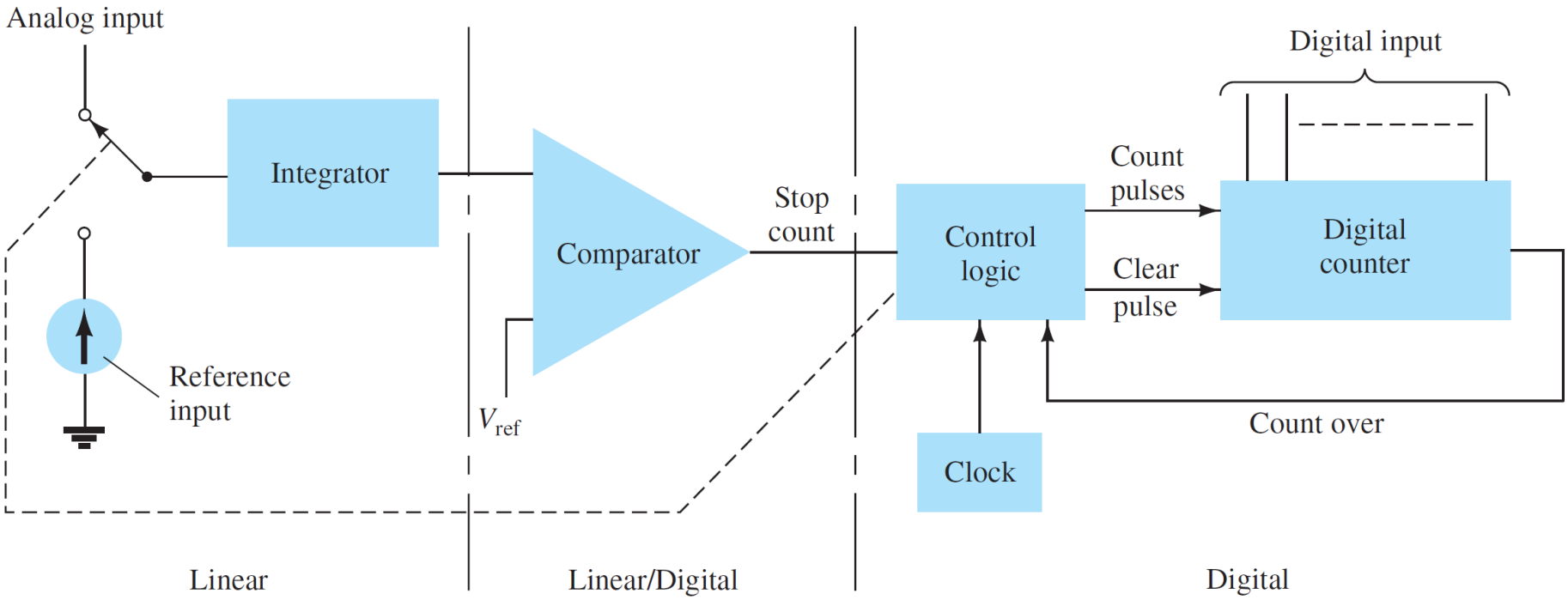


- The output is independent of the actual values of R and C and hence is very accurate.
- The disadvantage of this data converter is that it is a fairly slow system.
- The time T_1 requires 2^N clock pulses and the maximum possible time T_2 would also require 2^N clock pulses.
- For example, a 12-bit A/D converter would require a total of 8192 clock pulses.
- This corresponds to a conversion time of 8.2 ms for a 1 MHz clock.

Analog-to-Digital Converters

③ Dual-Slope A/D Conversion





Analog-to-Digital Converters

1. Parallel or Flash ADC
2. Counting ADC
3. Dual-Slope ADC
4. Successive Approximation A/D Converter
5. Semi-flash ADC
6. Delta-Sigma ADC
7. Pipelined ADC

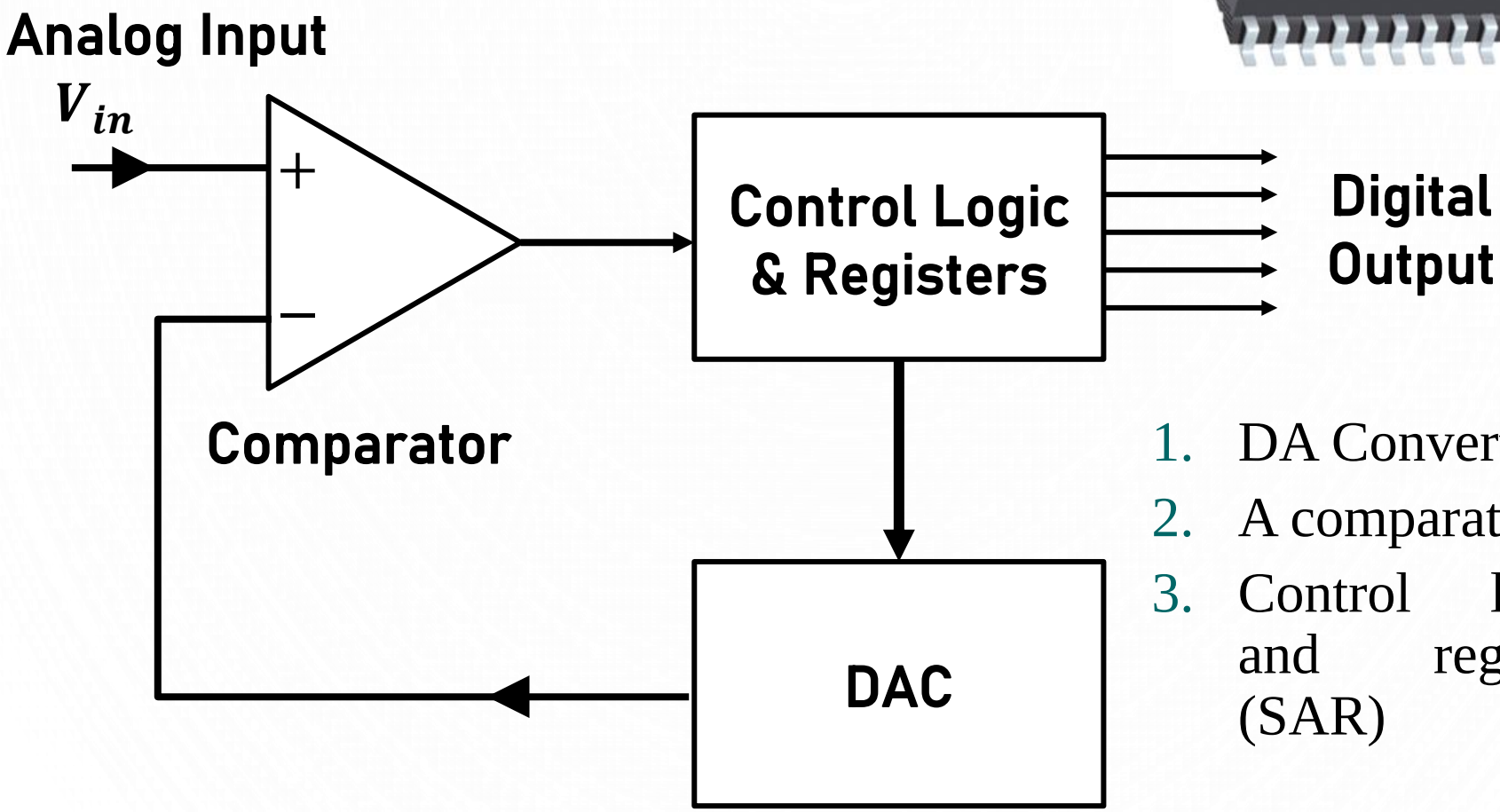
Analog-to-Digital Converters :: Comparison

ADC Type	Pros	Cons	Max Resolution	Max Sampling Rate	Main Applications	Cost	Accuracy
Successive Approximation (SAR)	Good speed/ resolution ratio	No inherent anti-aliasing protection	8-18 bits	10 MHz (2-5 MHz Typical)	Data Acquisition	Low	Medium
Delta-Sigma (ΔΣ)	High dynamic performance, Inherent anti-aliasing protection	Hysteresis on unnatural signals	8-32bits	1 MHz	Data Acquisition, Noise & Vibration, Audio	Low	Low
Dual Slope	Accurate, Inexpensive	Low speed	12-20 bits	100 Hz	Voltmeters	Medium	High
Pipelined	Very fast	Limited resolution	6-16 bits	1 GHz	Oscilloscopes	High	Low
Flash	Fastest	Low bit resolution	4-12 bits	10 GHz	Oscilloscopes	High	Low

Analog-to-Digital Converters

④ Successive Approximation A/D Converter (SAR)

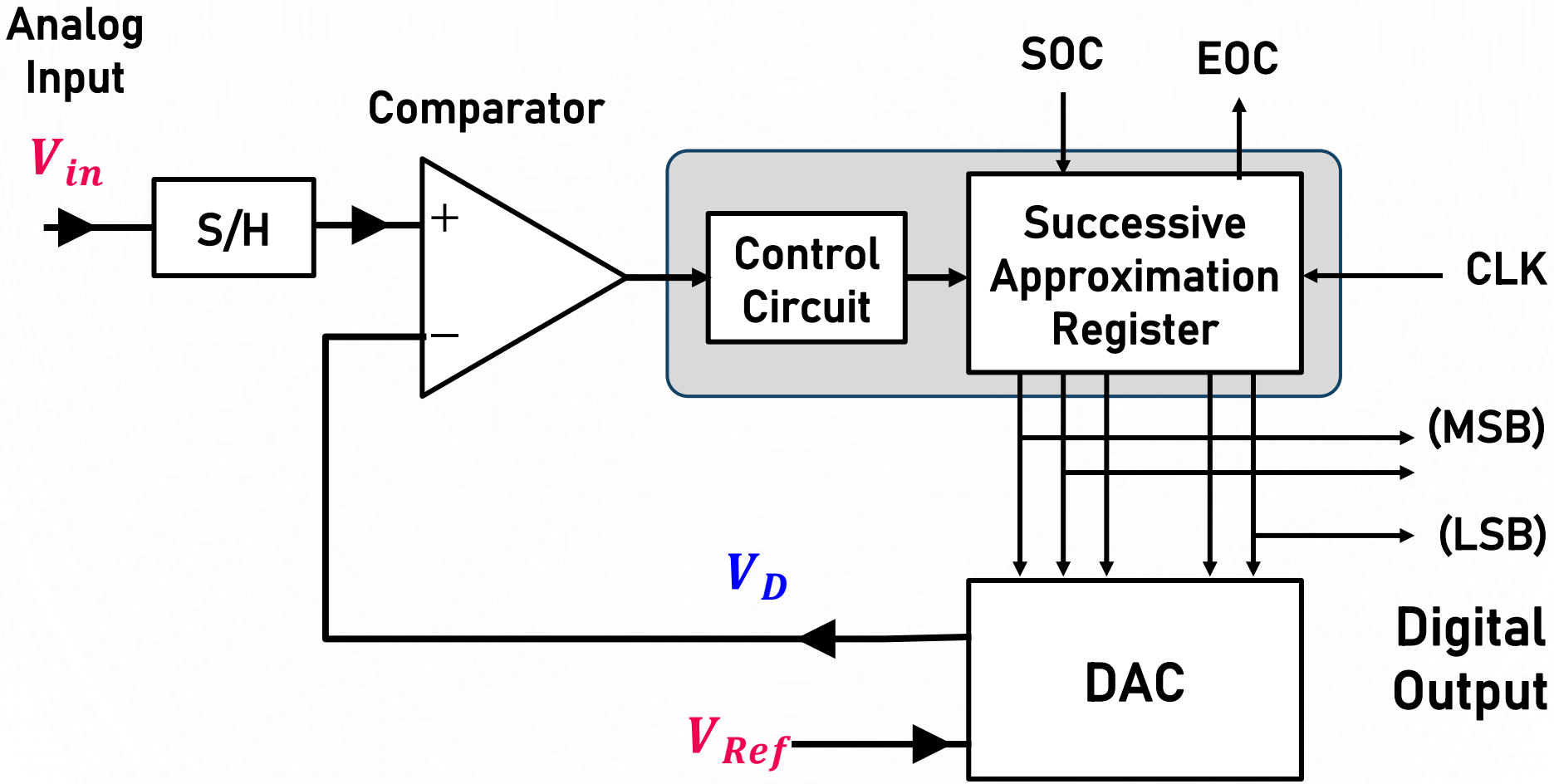
- The basic elements in the architecture



1. DA Converter
2. A comparator
3. Control logics and registers (SAR)

Analog-to-Digital Converters

④ Successive Approximation A/D Converter (SAR)

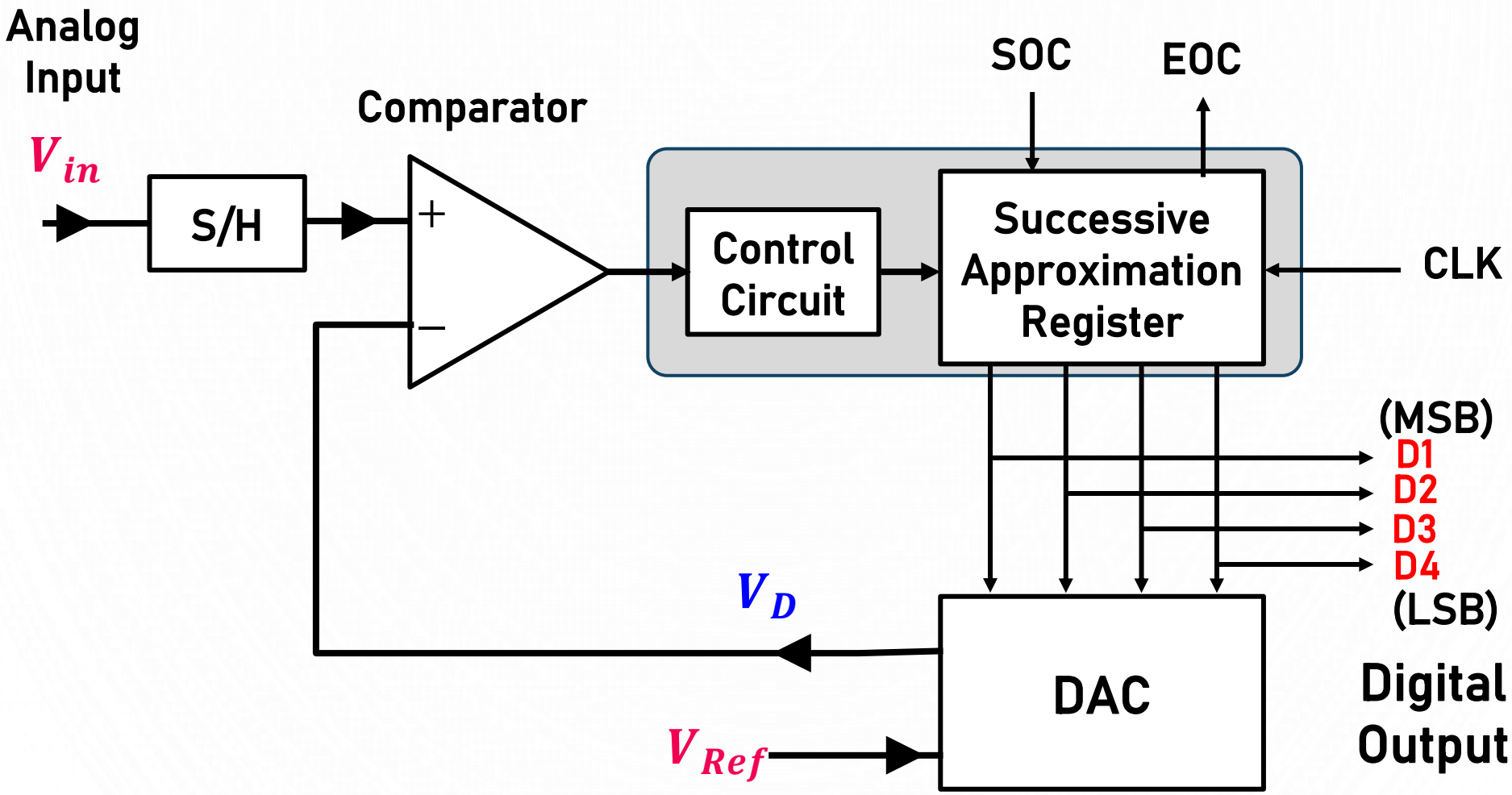


Start of Conversion indicator (SOC), End of Conversion indicator (EOC)

Analog-to-Digital Converters

④ Successive Approximation A/D Converter (SAR)

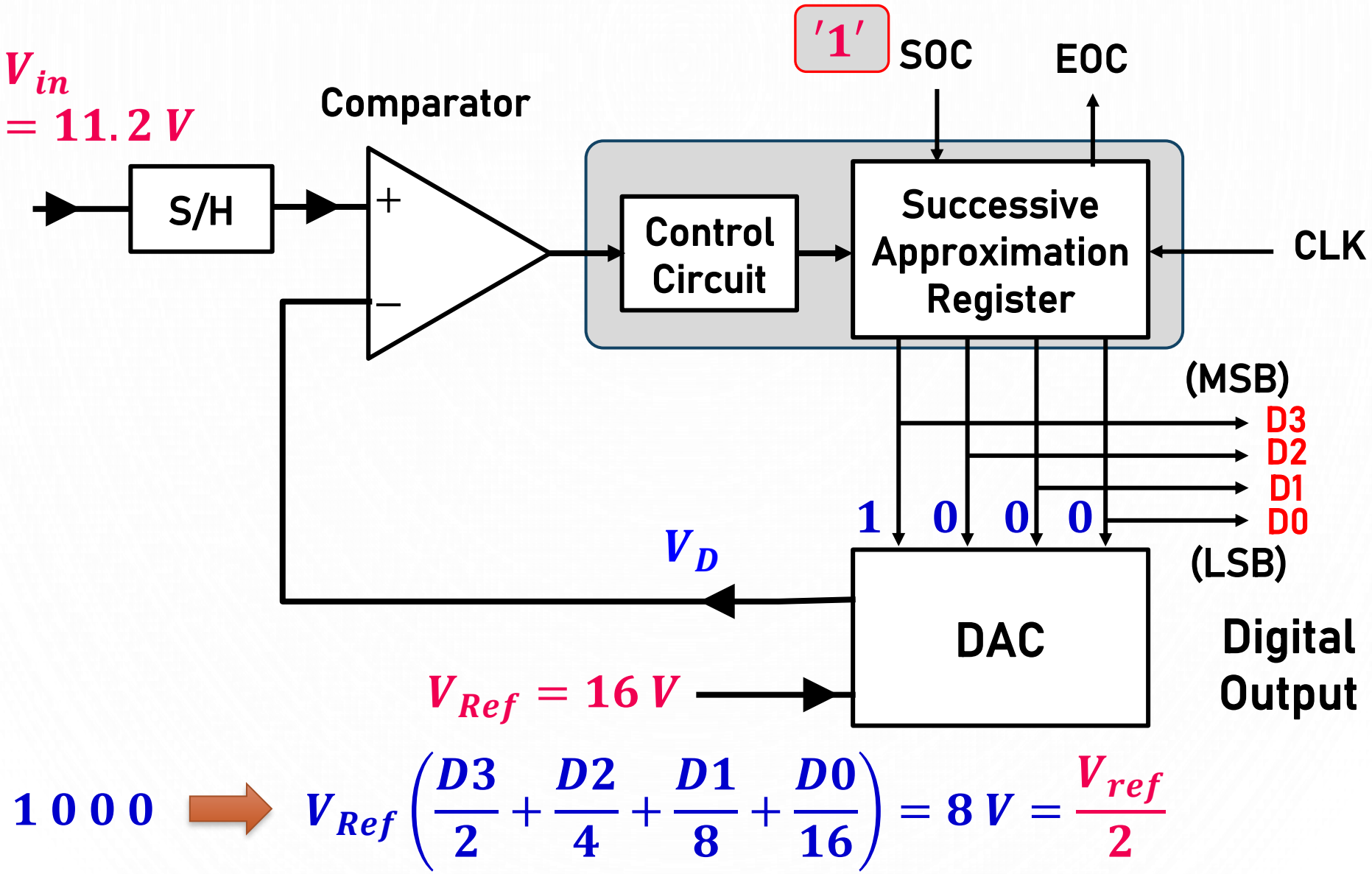
4-bit conversion



Ex. Successive Approximation A/D Converter (SAR)

Convert an analog signal $V_{in} = 11.2\,V$ to digital using 4-bit ADC. The reference voltage of DAC is $V_{Ref} = 16\,V$.

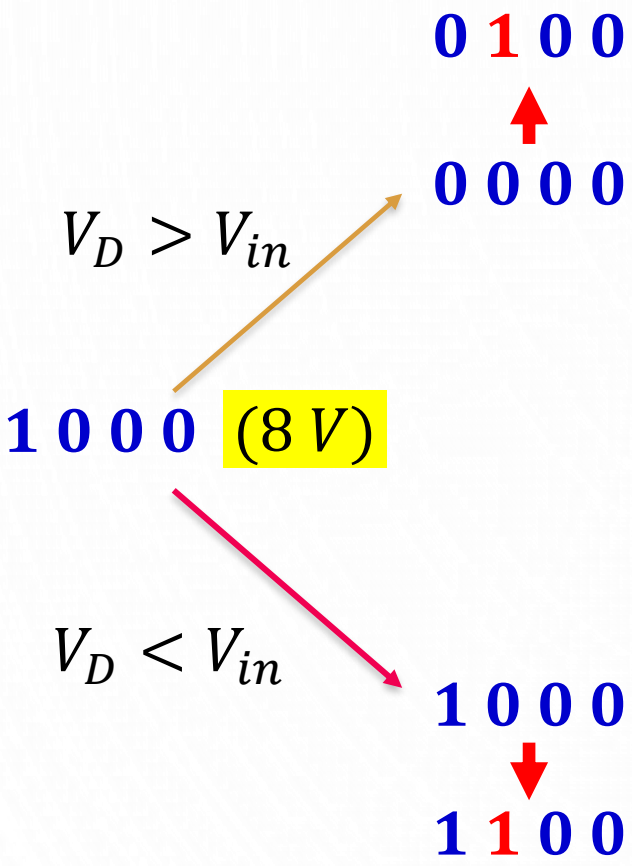
Ex. Successive Approximation A/D Converter (SAR)



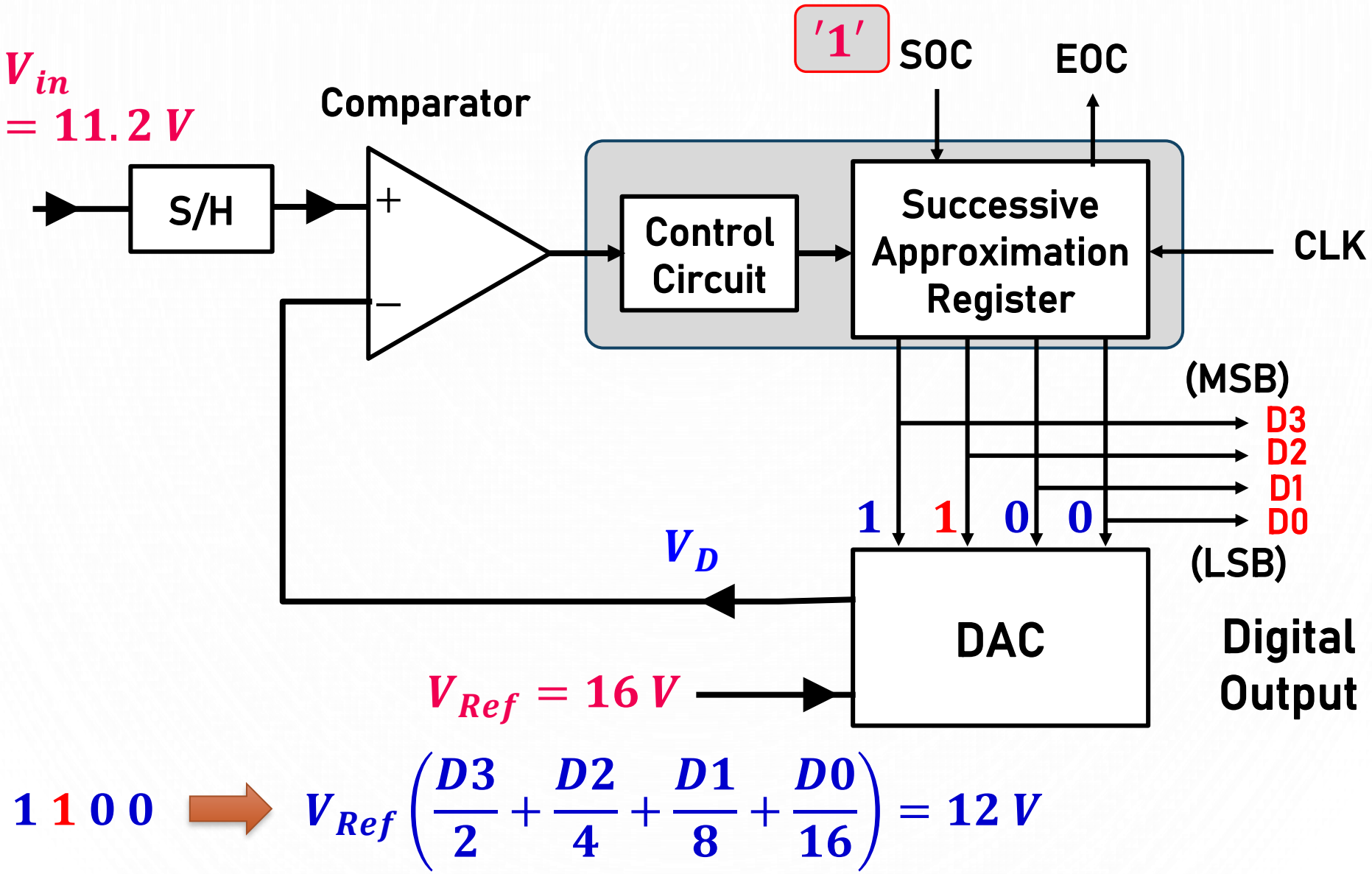
$$1\ 0\ 0\ 0 \Rightarrow V_{Ref}\left(\frac{D3}{2}+\frac{D2}{4}+\frac{D1}{8}+\frac{D0}{16}\right) = 8\ V = \frac{V_{ref}}{2}$$

Ex. Successive Approximation A/D Converter (SAR)

$V_{in} = 11.2\ V$ 4-bit ADC $V_{Ref} = 16\ V$



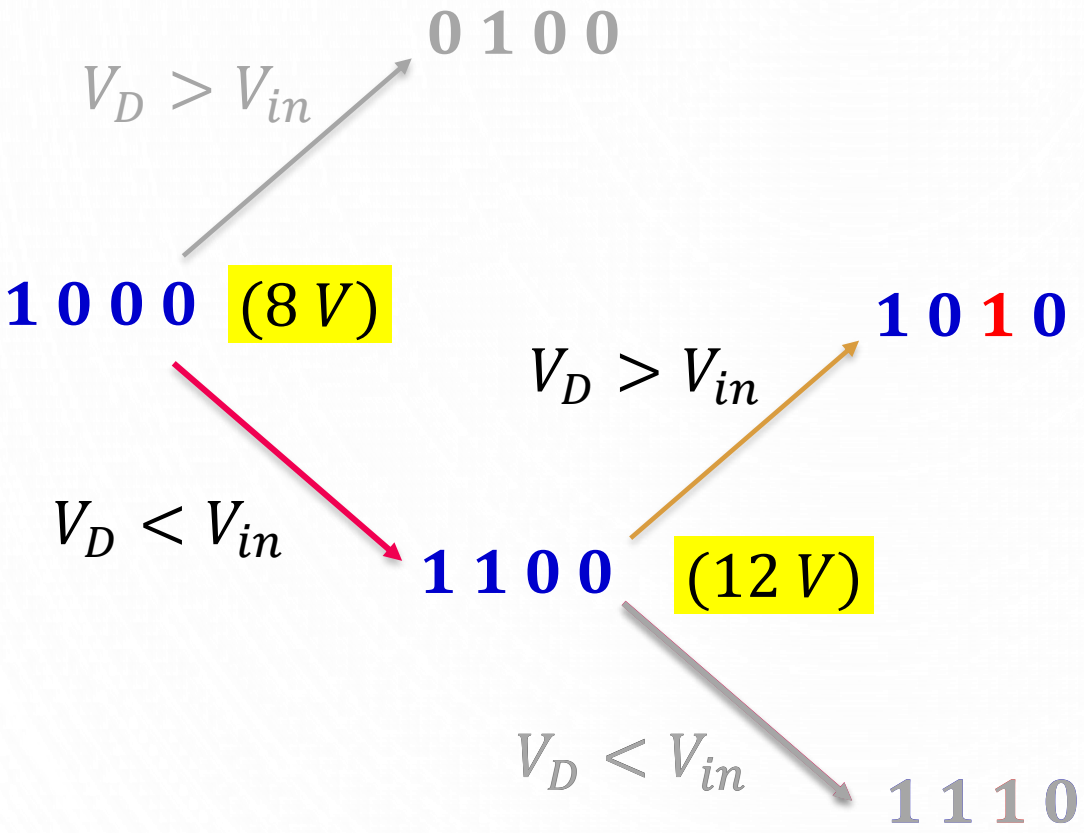
Ex. Successive Approximation A/D Converter (SAR)



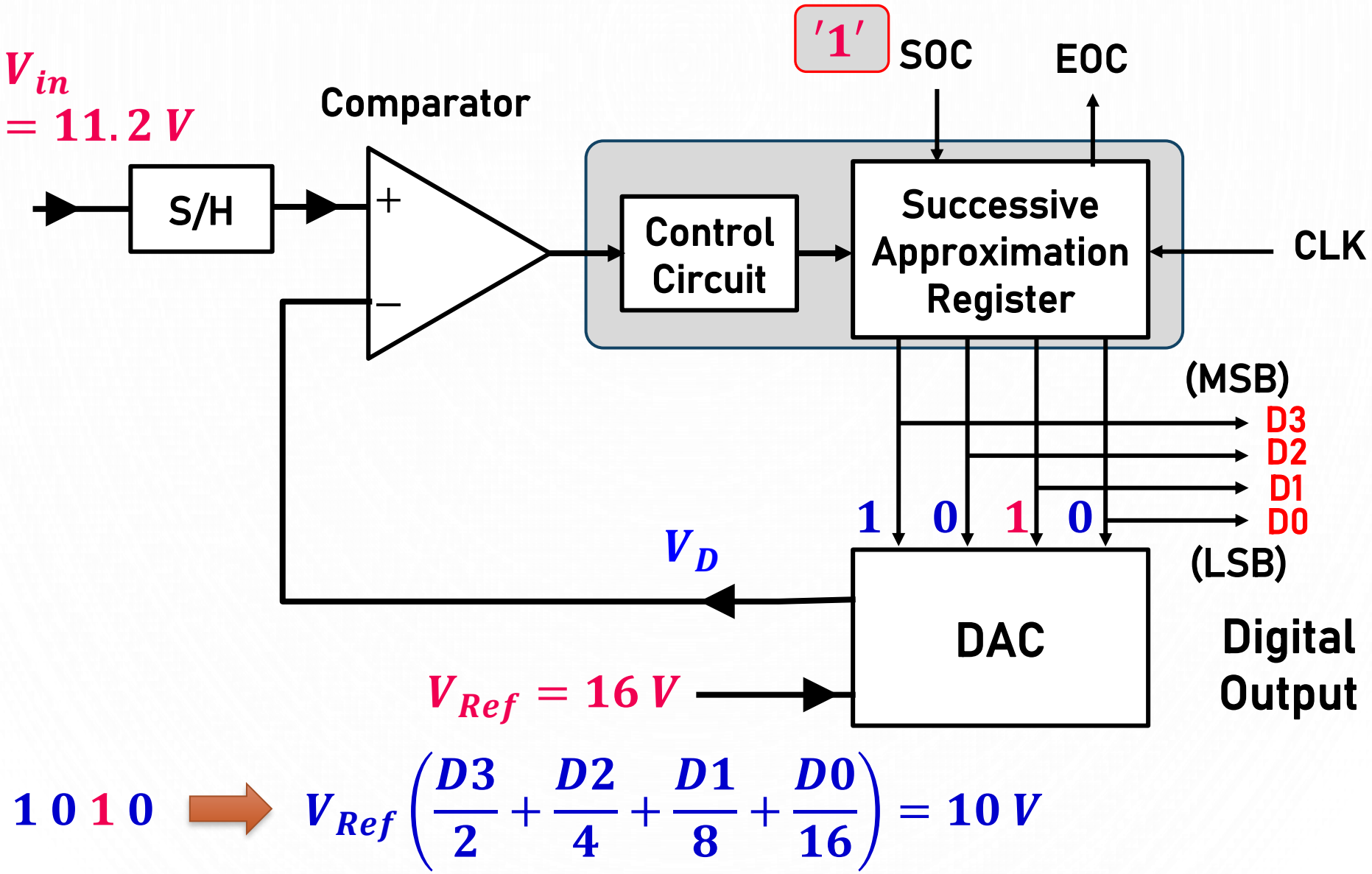
$$1\ 1\ 0\ 0 \Rightarrow V_{Ref}\left(\frac{D3}{2}+\frac{D2}{4}+\frac{D1}{8}+\frac{D0}{16}\right) = 12\ V$$

Ex. Successive Approximation A/D Converter (SAR)

$V_{in} = 11.2\ V$ 4-bit ADC $V_{Ref} = 16\ V$



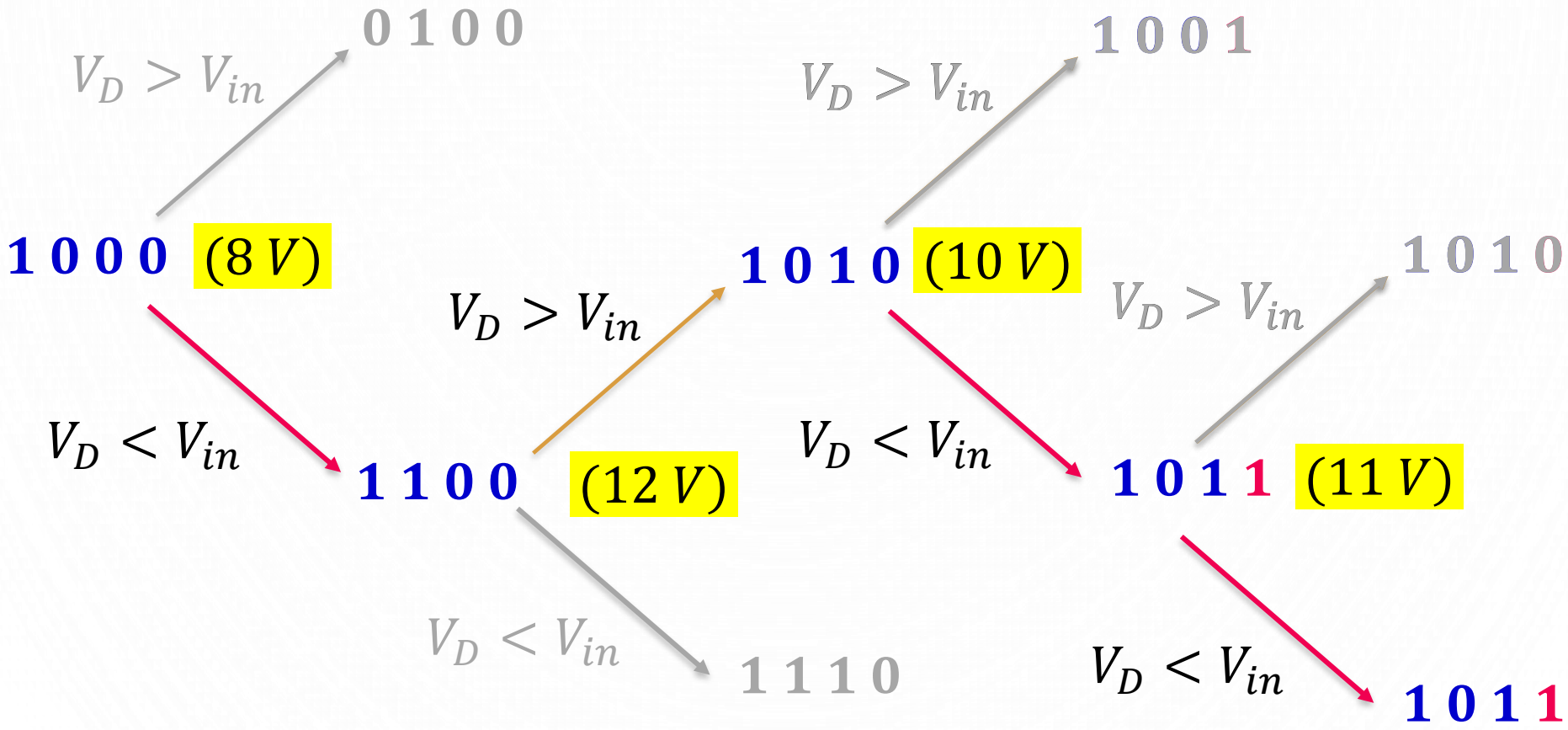
Ex. Successive Approximation A/D Converter (SAR)



$$1\ 0\ 1\ 0 \Rightarrow V_{Ref}\left(\frac{D3}{2} + \frac{D2}{4} + \frac{D1}{8} + \frac{D0}{16}\right) = 10\ V$$

Ex. Successive Approximation A/D Converter (SAR)

$V_{in} = 11.2\ V$ 4-bit ADC $V_{Ref} = 16\ V$



④ Successive Approximation A/D Converter (SAR)

- Conversion time — Independent of the input voltage

$$T_C = N \times T_{CLK}$$