EE 254

Electronic Instrumentation

Dr. Tharindu Weerakoon

Dept. of Electrical and Electronic Engineering

Faculty of Engineering, University of Peradeniya

Lecture Note #12

Content (Brief)

4. Data Converters

- Analogue to Digital (A/D) Conversion (ADC)
- Digital to Analogue (D/A) Conversion (DAC)
- Sample and Hold Circuit

Analogue-to-Digital Converters

1. Parallel or Flash ADC
2. Counting ADC
3. Dual-Slope ADC
4. Successive Approximation A/D Converter
5. Semi-flash ADC
6. Delta-Sigma ADC
7. Pipelined ADC

Digital-to-Analogue Converters

1. Weighted-Resistor DAC
2. R–2R Ladder Network DAC

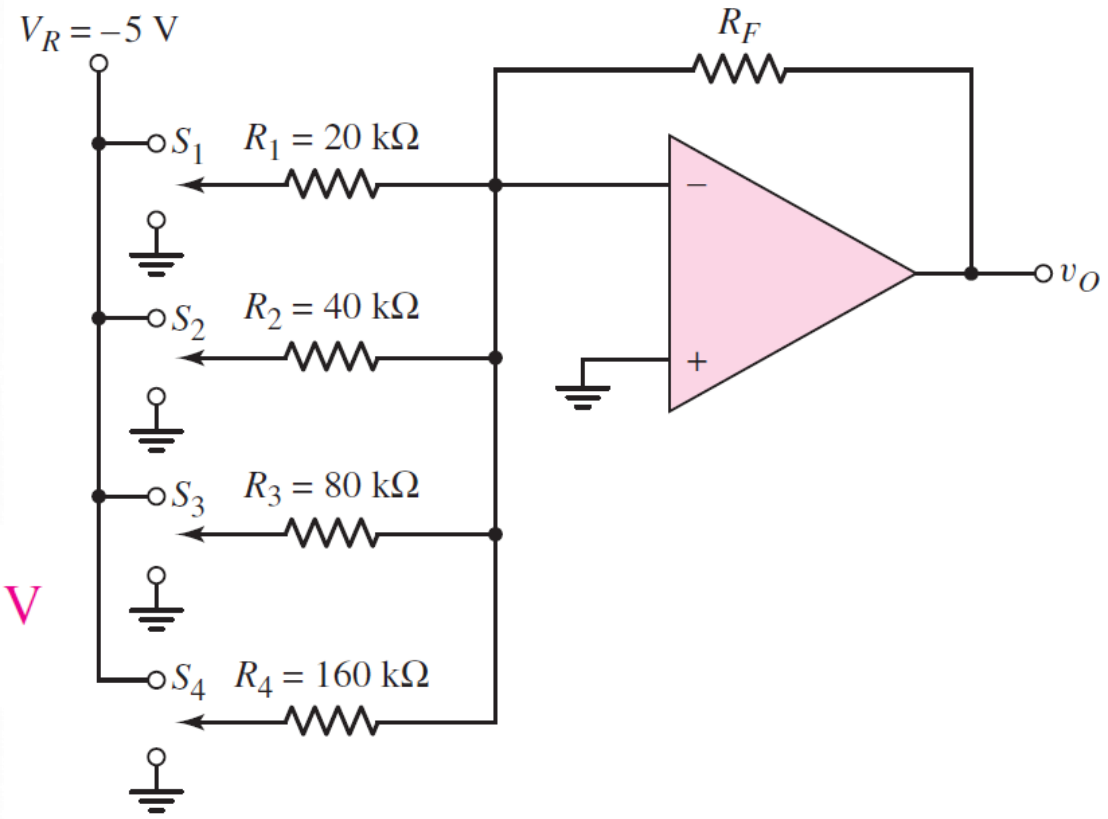
3. Segmented DAC
4. Delta-Sigma DAC

Digital-to-Analog Converters

Weighted-Resistor 4-Bit D/A

- A simple 4-bit D/A converter.
- With $R_F = 10\ k\Omega$, the output voltage:

$$v_O = \left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right)(5)\ \text{V}$$

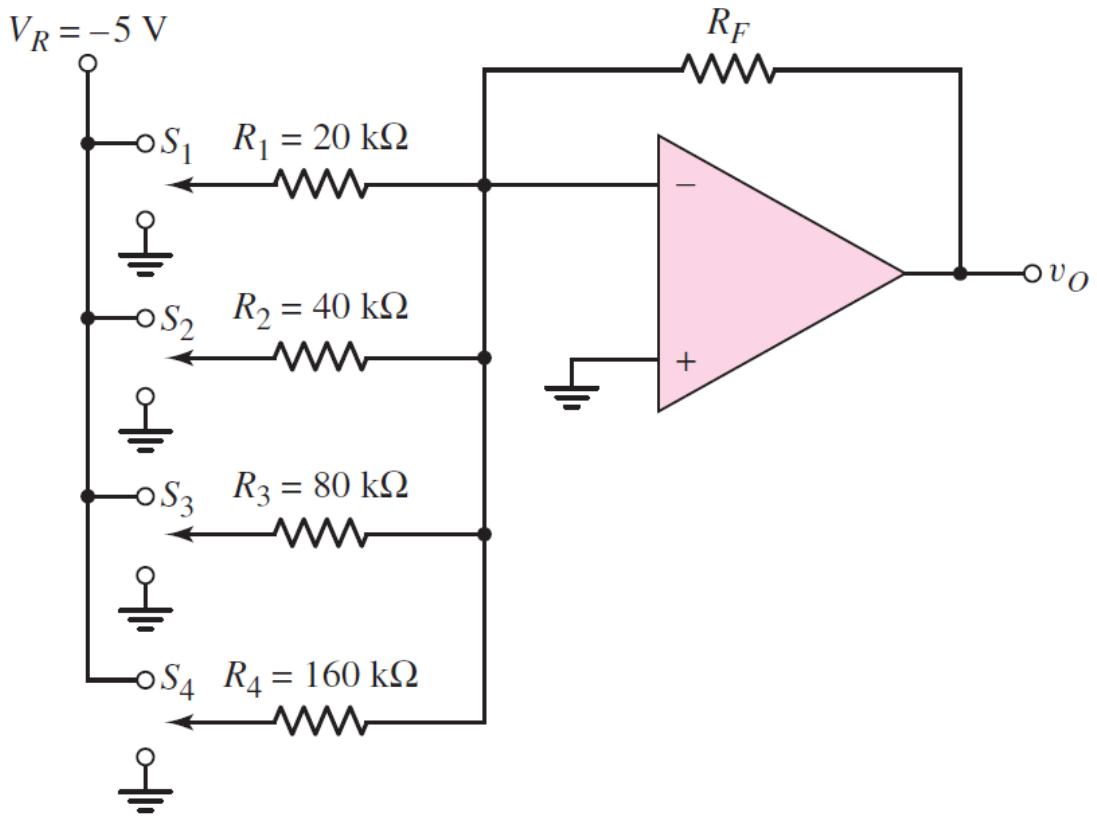


- Accuracy of the circuit can be achieved by the precision of the weighted resistors and the feedback resistor.
- When the N increases, the size of the weighted input resistance increases for lesser significant bits.

Digital-to-Analog Converters

Weighted-Resistor 4-Bit D/A

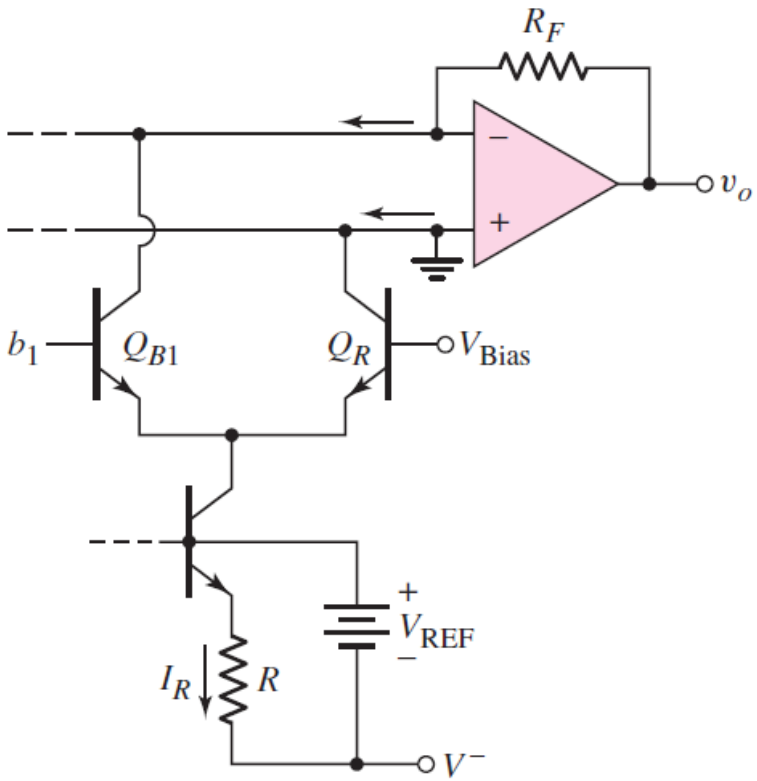
- The accuracy for large resistance values becomes more difficult to maintain.
- The size of this D/A converter is in general limited to a 4-bit input.



- Another factor that determines the **accuracy** of the D/A circuit is the **precision of the switches**.

Digital-to-Analog Converters

Weighted-Resistor 4-Bit D/A

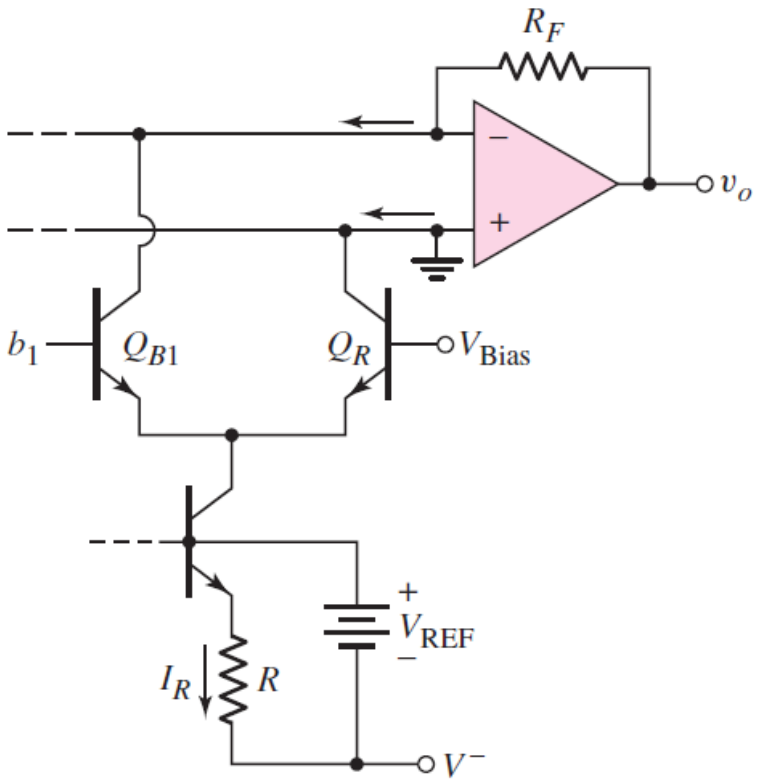


- An example of a current switch, showing only the MSB.
- If the bit b_1 **is a logic 1** ($> V_{Bias}$), then Q_{B1} **is turned on** and Q_R **is turned off** so that the current I_R is switched through Q_{B1}.
- This current becomes a component of the current through the feedback resistor.
- If b_1 **is a logic 0** ($< V_{Bias}$), then Q_{B1} **is turned off** and Q_R **is turned on** so that the current is switched to ground.
- Because of the virtual ground, we may note that the collector voltages of Q_{B1} and Q_R are essentially identical.

Digital-to-Analog Converters

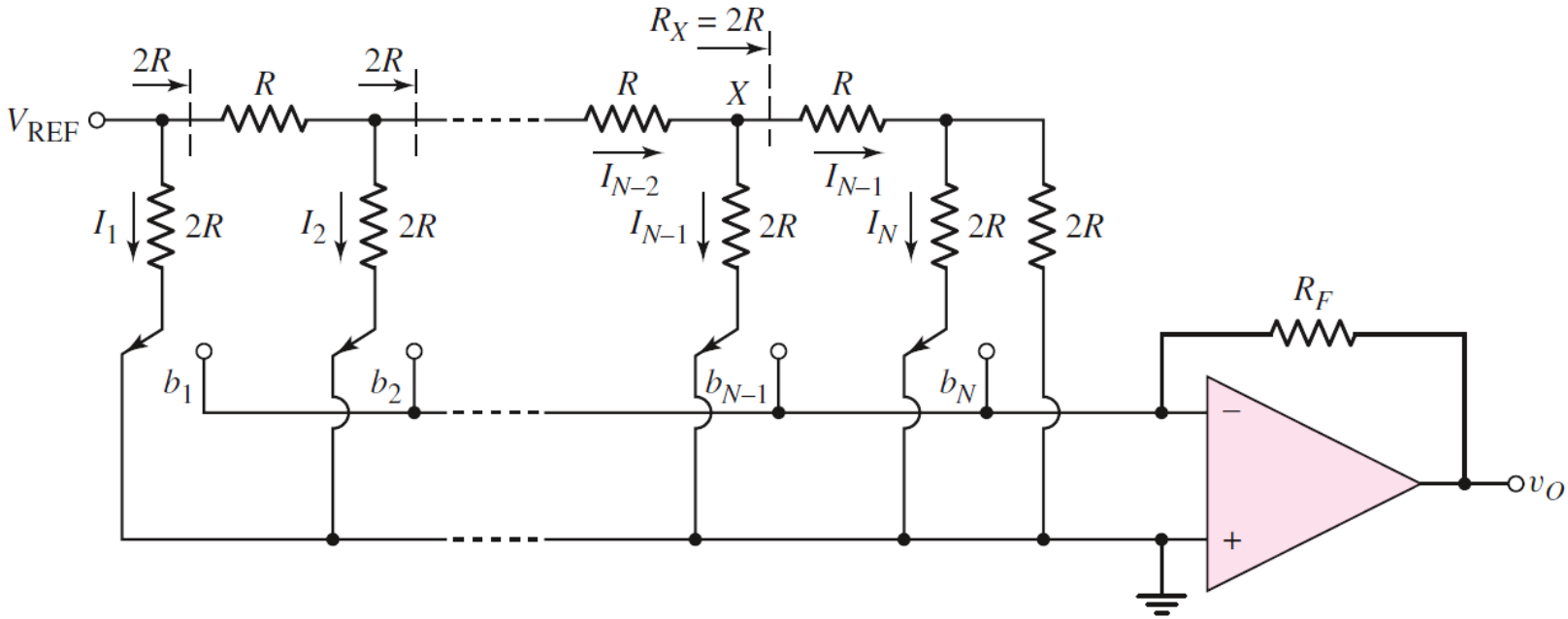
Weighted-Resistor 4-Bit D/A

- For the circuit to operate properly, the base-emitter voltage of all the transistors must be the same.
- Since the currents are smaller for the lesser significant bits, the base–emitter areas must be reduced in order to maintain the same current density.



Digital-to-Analog Converters

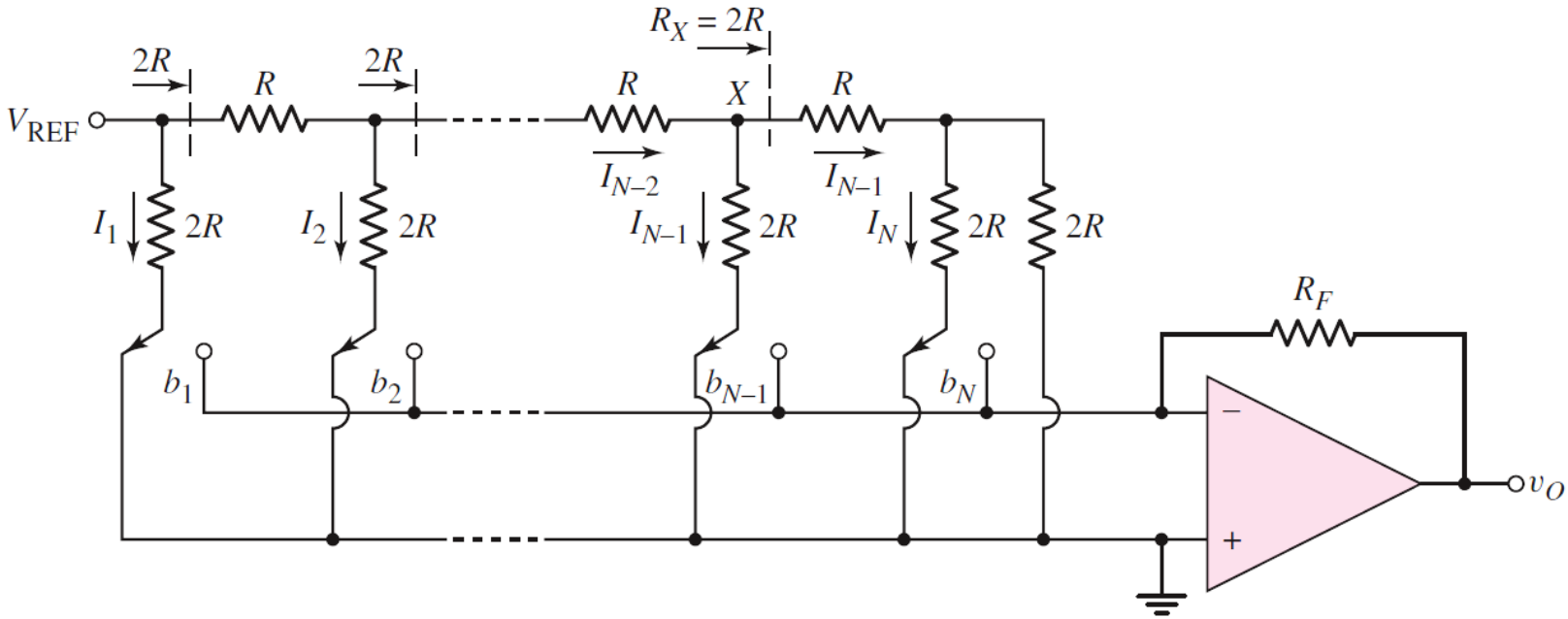
R–2R Ladder Network D/A



- This configuration eliminates the widespread in weighted input resistor values in the previous circuit.
- Assuming the switches are ideal, the current in each resistor is a constant because of the virtual ground concept.

Digital-to-Analog Converters

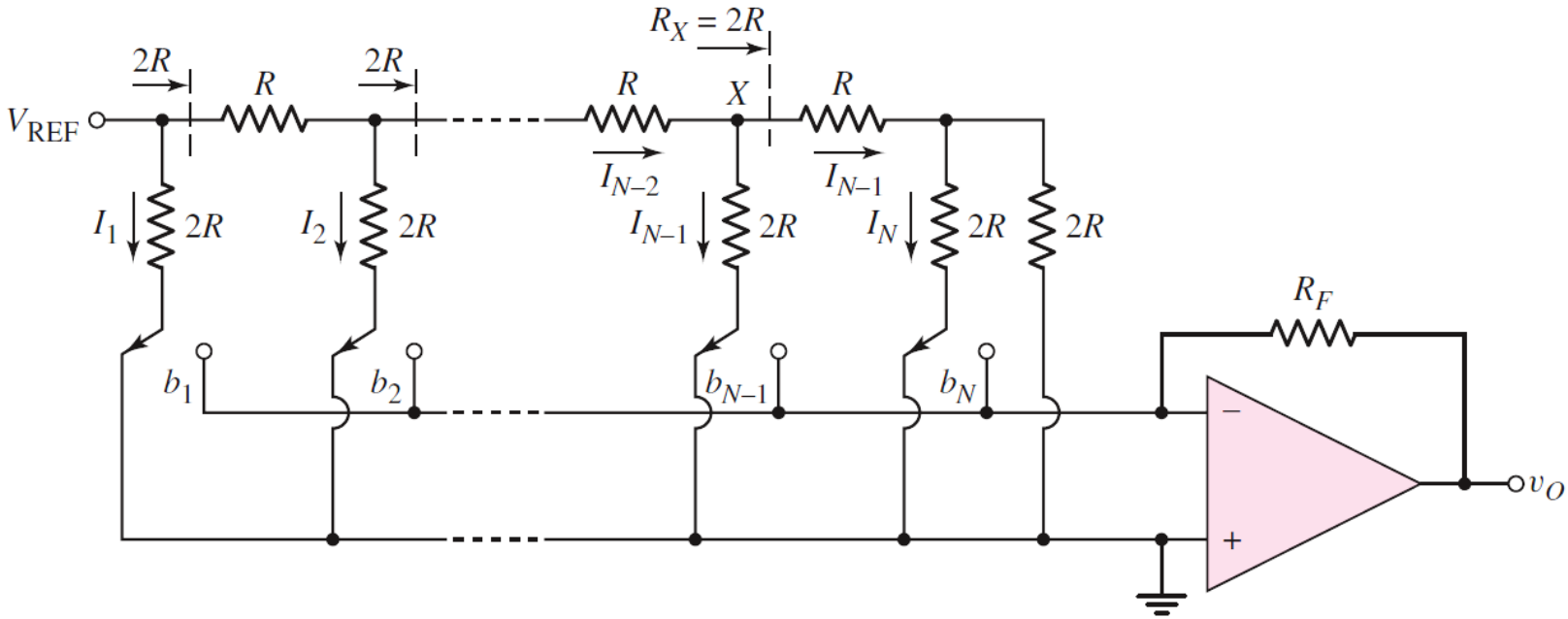
R–2R Ladder Network D/A



- Consider node X, the resistance denoted as R_X is $R_X = 2R$.
- This same resistance occurs at every node in the circuit as indicated.
- Therefore, the current entering each node splits evenly as shown at node X.

Digital-to-Analog Converters

R–2R Ladder Network D/A

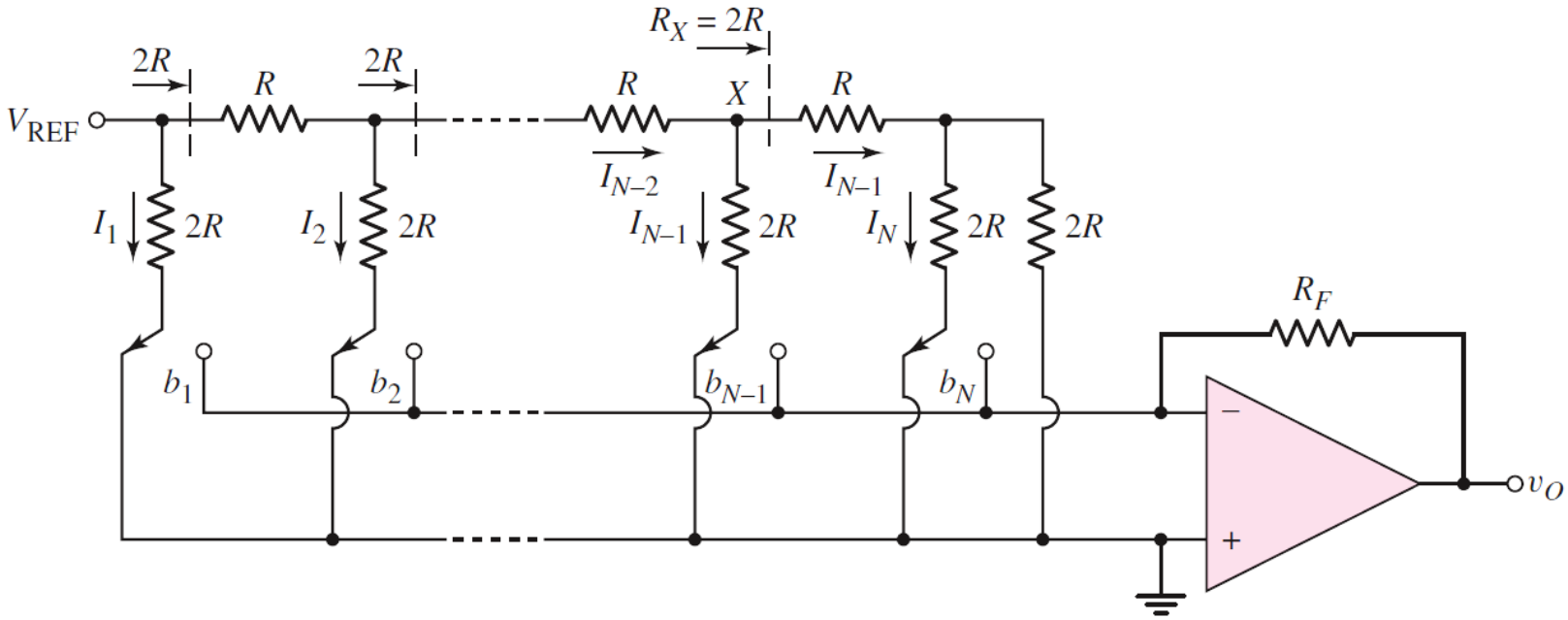


- Then the current entering each node is $I_{N-1} = \frac{1}{2} I_{N-2}$
- This effect again occurs at every node in the circuit. Then,

$$I_1 = 2I_2 = 4I_3 = \cdots = 2^{N-2} I_{N-1} = 2^{N-1} I_N$$

Digital-to-Analog Converters

R–2R Ladder Network D/A



- Setting the feedback resistance to $R_F = R$, we have the output voltage:

$$v_O = (-V_{\text{REF}})\left(\frac{b_1}{2} + \frac{b_2}{4} + \cdots + \frac{b_N}{2^N}\right)$$

Example 01 :: DAC

An analog signal in the range 0 to 5 V is to be converted to a digital signal with a quantization error of less than one percent.

(a) What is the required number of bits?

(b) What input voltage value represents 1 LSB?

(c) What digital output represents an input voltage of 3.5424 V?

Example 02 :: DAC

An analog signal in the range 0 to 3.3 V is to be converted to a digital signal with a quantization error of less than 0.5 percent.

(a) What is the required number of bits?

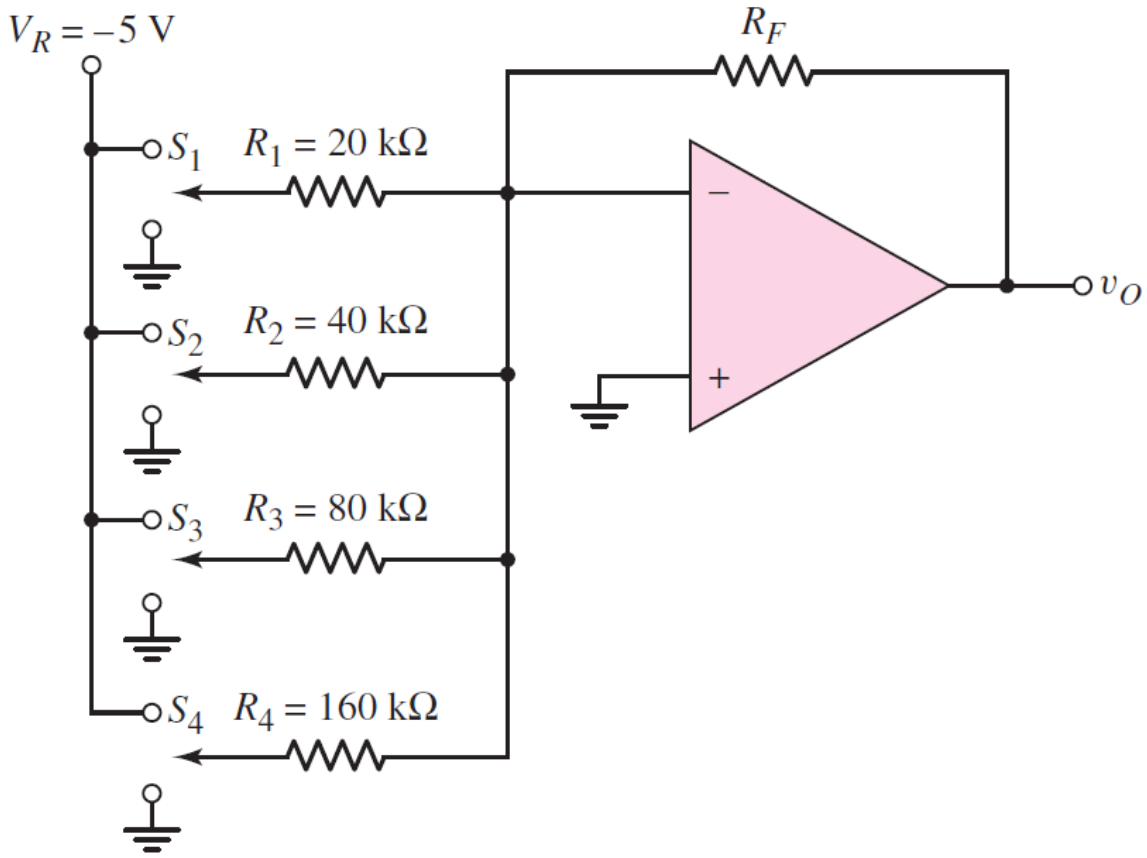
(b) What input voltage value represents 1 LSB?

(c) What digital output represents an input voltage of 2.5321 V?

Example 03 :: DAC

a) What is the output voltage of the 4-bit weighted-resistor D/A in the Figure below if the input is 0110? Assume $R_F = 10k\Omega$.

b) The input signal changes to 1001. What is the output voltage?

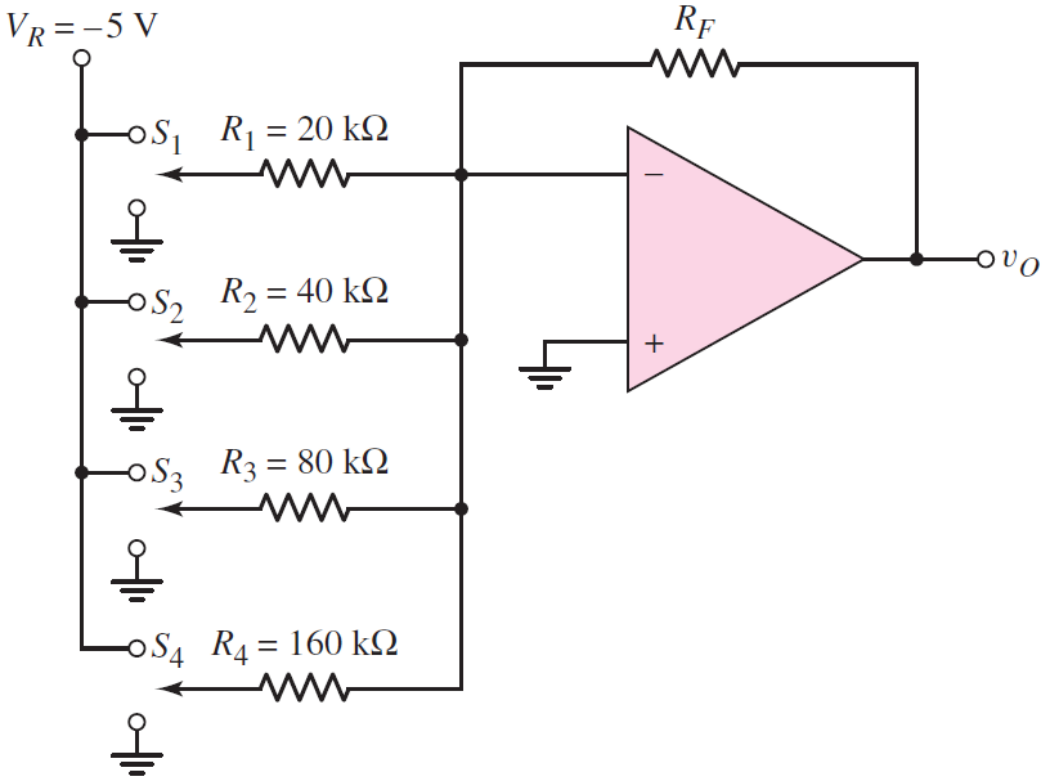


Example 04 :: DAC

Consider the 4-bit weighted-resistor D/A converter in Figure below. Let $R_F = 10k\Omega$

a) What is the maximum allowed tolerance (±percent) in the value of R_1 so that the maximum error in the output is limited to ±1/2 LSB?

b) Repeat part (a) for the resistor R_4.



Example 05 :: DAC

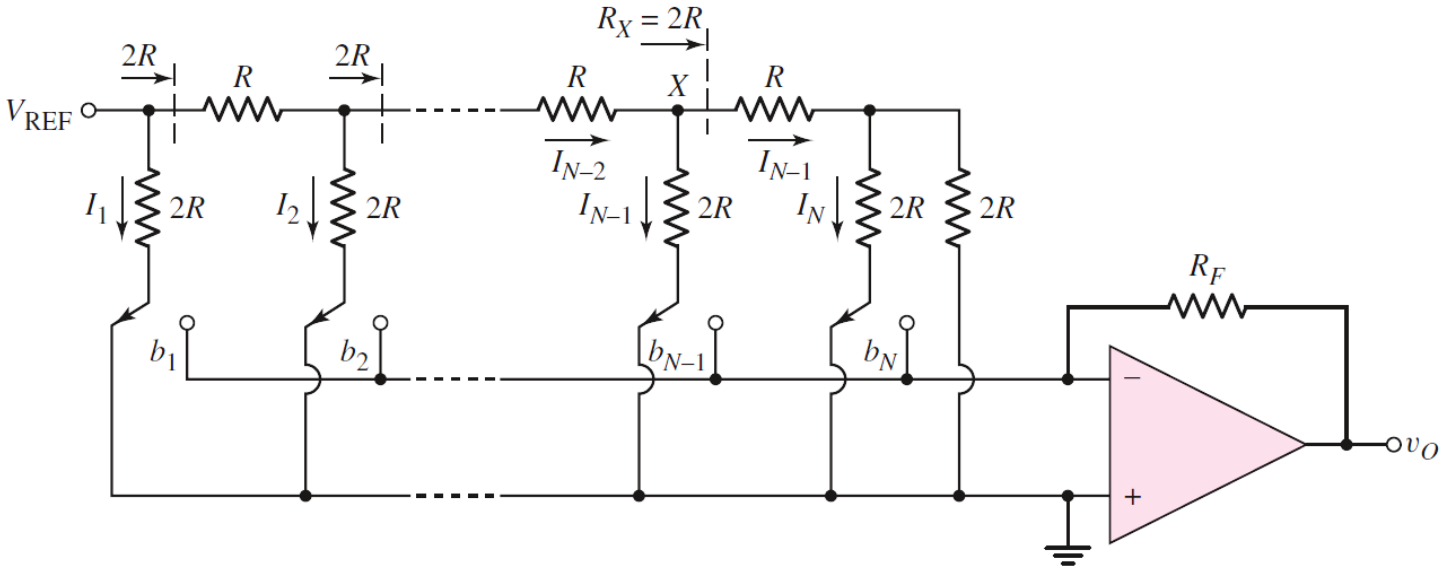
The N-bit D/A converter with an R–2R ladder network in Figure is to be designed as a 6-bit D/A device. Let $V_{REF} = -5.0V$ and $R = R_F = 5.0\ k\Omega$.

a) What are currents I_1, I_2, I_3, I_4, I_5, and I_6?

b) The input changes by 1 LSB. What is the change in the output voltage?

c) What is the output voltage if the input is 010011?

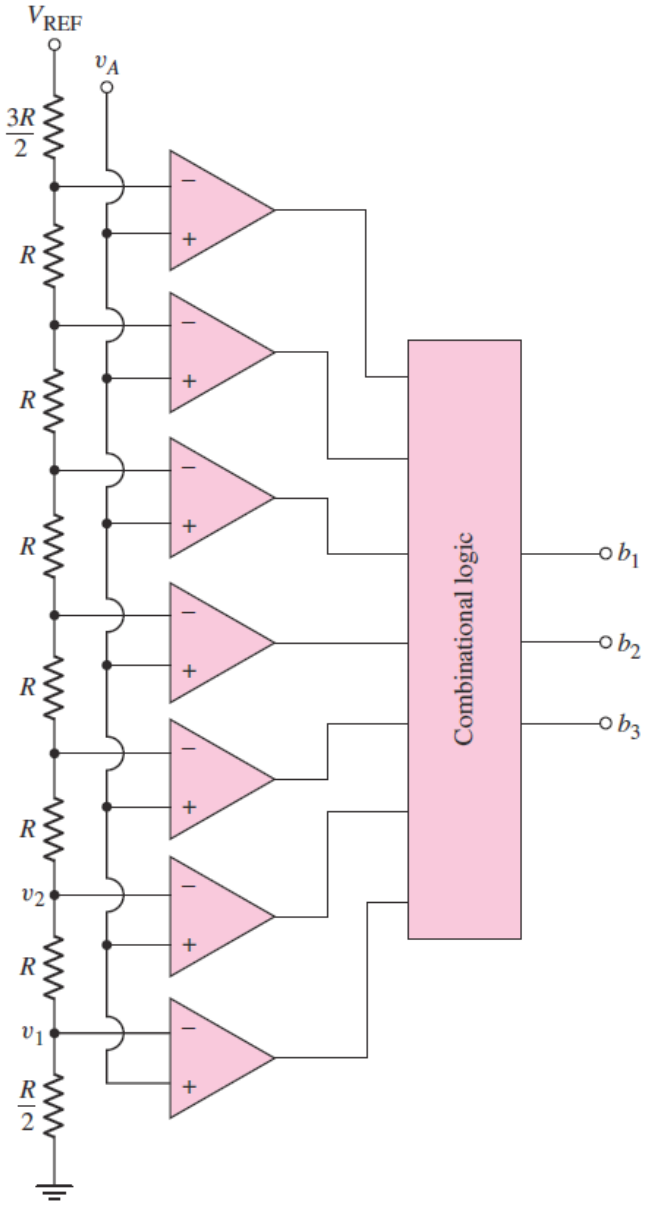
d) What is the change in output voltage if the input changes from 101010 to 010101?



Example 06 :: ADC

The 3-bit flash A/D converter in Figure has a reference voltage of $V_{REF} = 3.3\,V$. The 3-bit output is 101.

What is the range of v_A that produces this output?



Example 07 :: ADC

A 10-bit counting A/D converter has an analog input in the range $0 \leq v_A \leq 5\ V$ and has a clock frequency of $1\ MHz$.

(a) What is the maximum conversion time?

(b) If the output is 0010010010, what is the range of the input signal v_A (assume a quantization error of $\pm 1/2\ LSB$).

(c) How many clock pulses are required to produce an output of 0100100100?