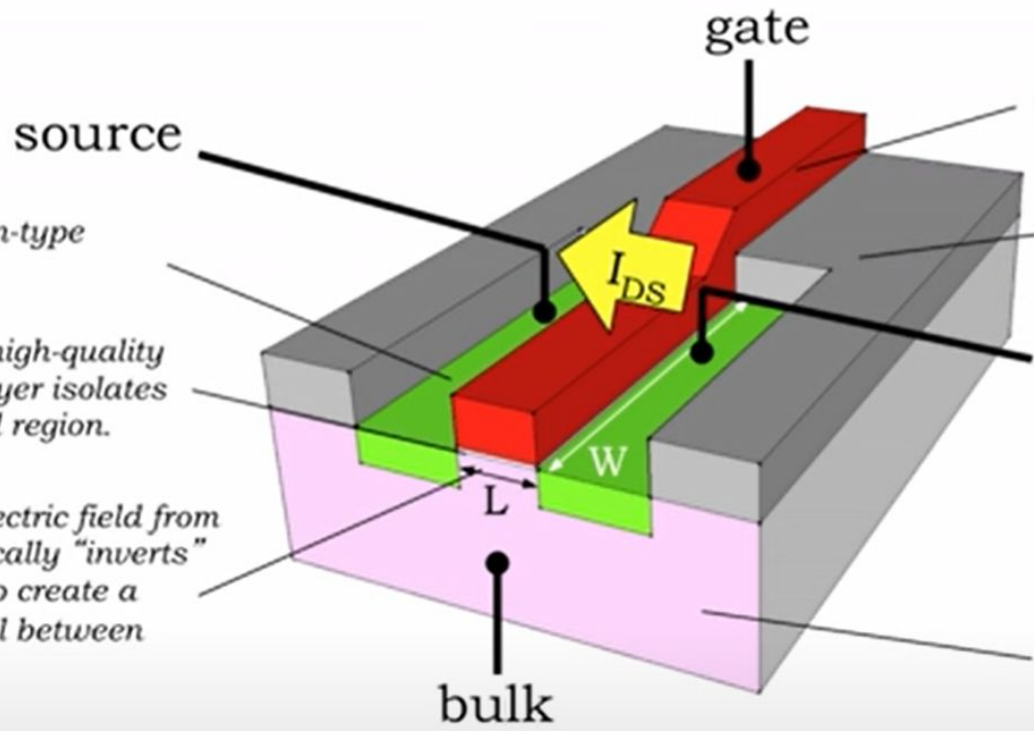
Parasitic effect in Timing analysis

***Objective**: Design a 3 stage (3 inverters) ring oscillator. Find the correlation of the parasitic effect in the oscillation period.*

N-Channel MOSFET: Physical View



Polysilicon wire

Inter-layer SiO_2 insulation

Heavily doped n-type diffusions

Very thin (<20Å) high-quality SiO_2 insulating layer isolates gate from channel region.

Channel region: electric field from charges on gate locally "inverts" type of substrate to create a conducting channel between source and drain.

Doped p-type silicon substrate

$$I_{DS} \propto W/L$$

Device Capacitances of a MOSS

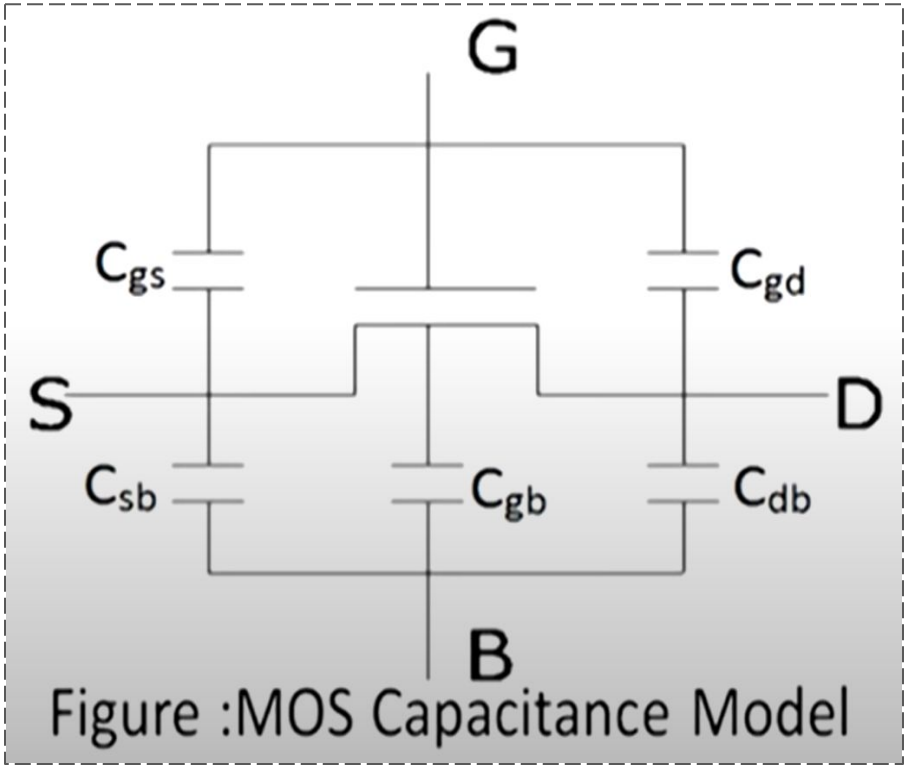
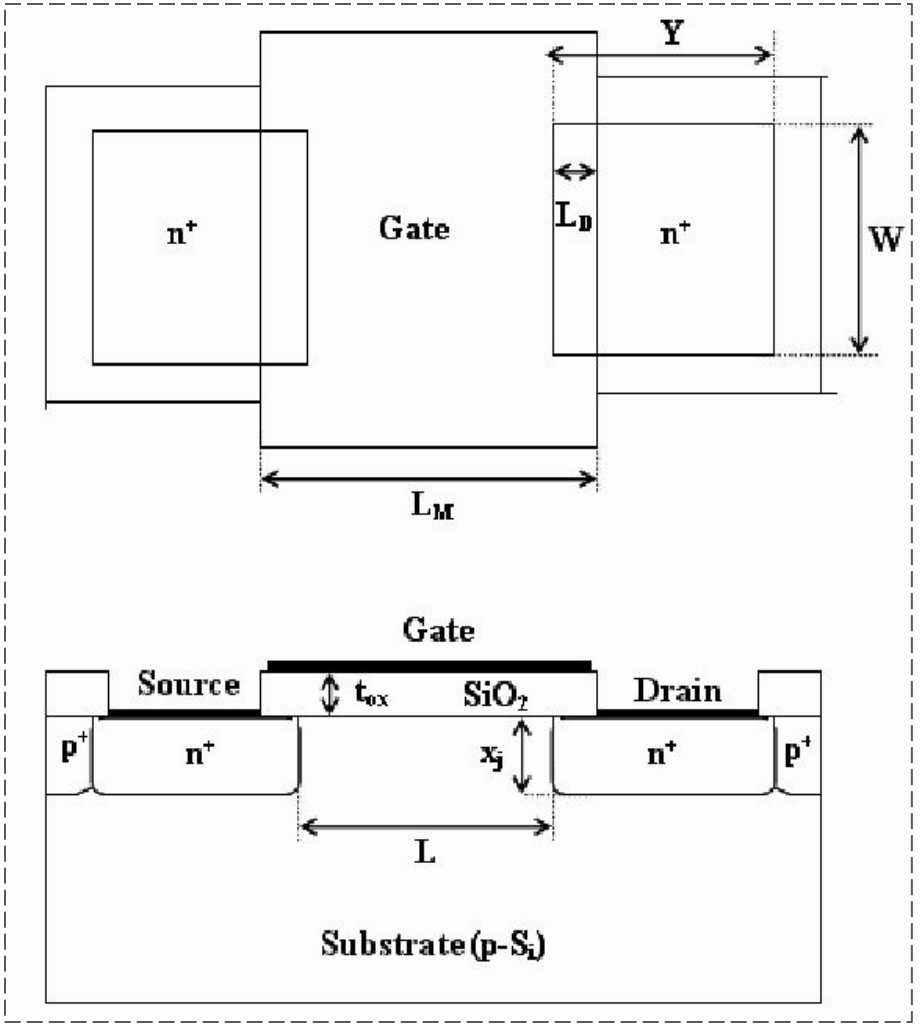
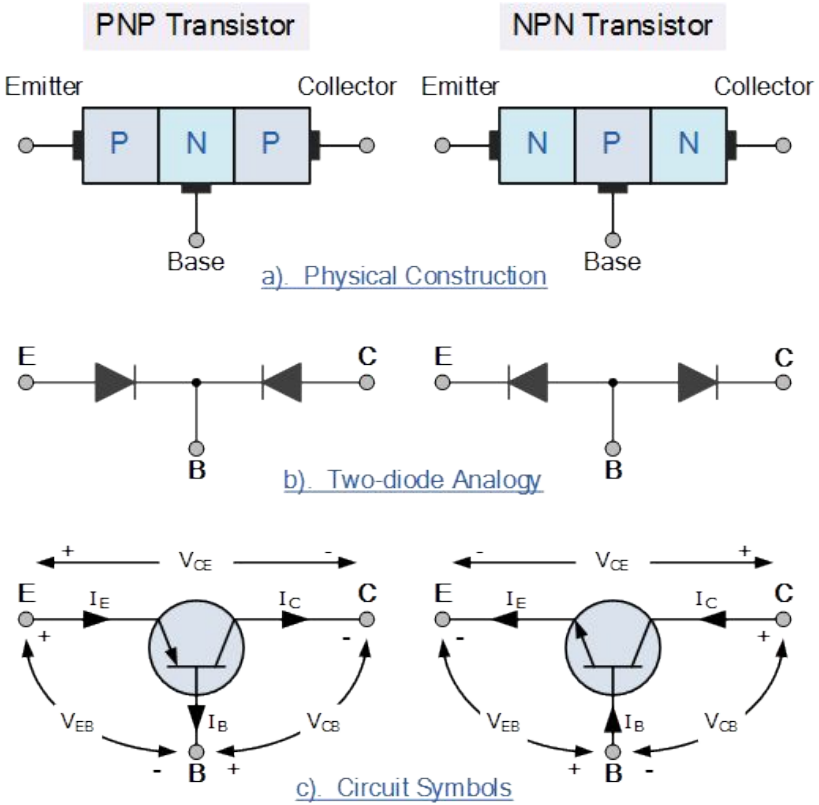


Figure :MOS Capacitance Model



Physical View of BJT Transistor



Active Region – the transistor operates as an amplifier and Ic = β*Ib

Saturation – the transistor is "Fully-ON" operating as a switch and Ic = I(saturation)

Cut-off – the transistor is "Fully-OFF" operating as a switch and Ic = 0