

Circuit 2

- Part 1

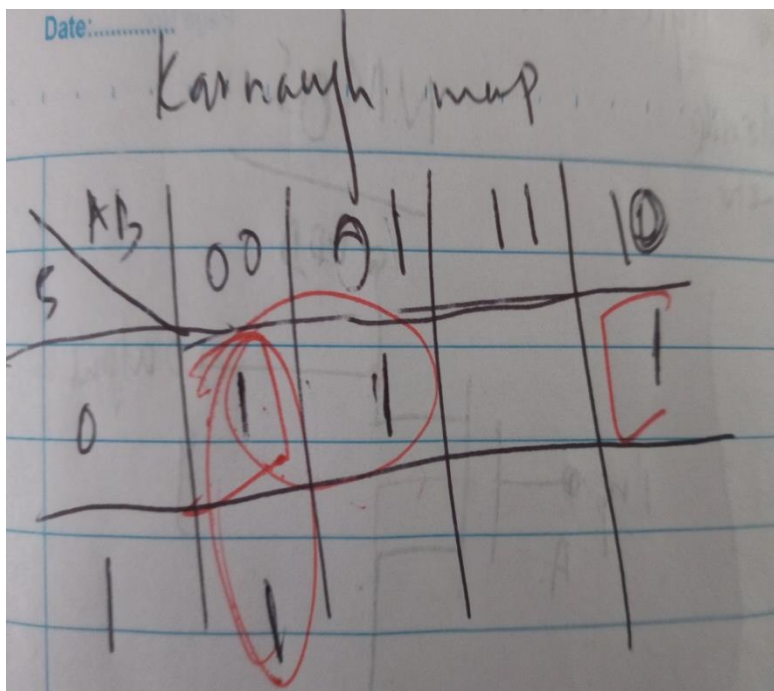
Programmable logic block to configure it as a 'NAND' or a 'NOR' gate using a single selection bit

First I drew a truth table for this part considering a single selection bit (S) with two inputs (A, B) such that S=0 for 'NAND' and S=1 for 'NOR' operations respectively.

S	A	B	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

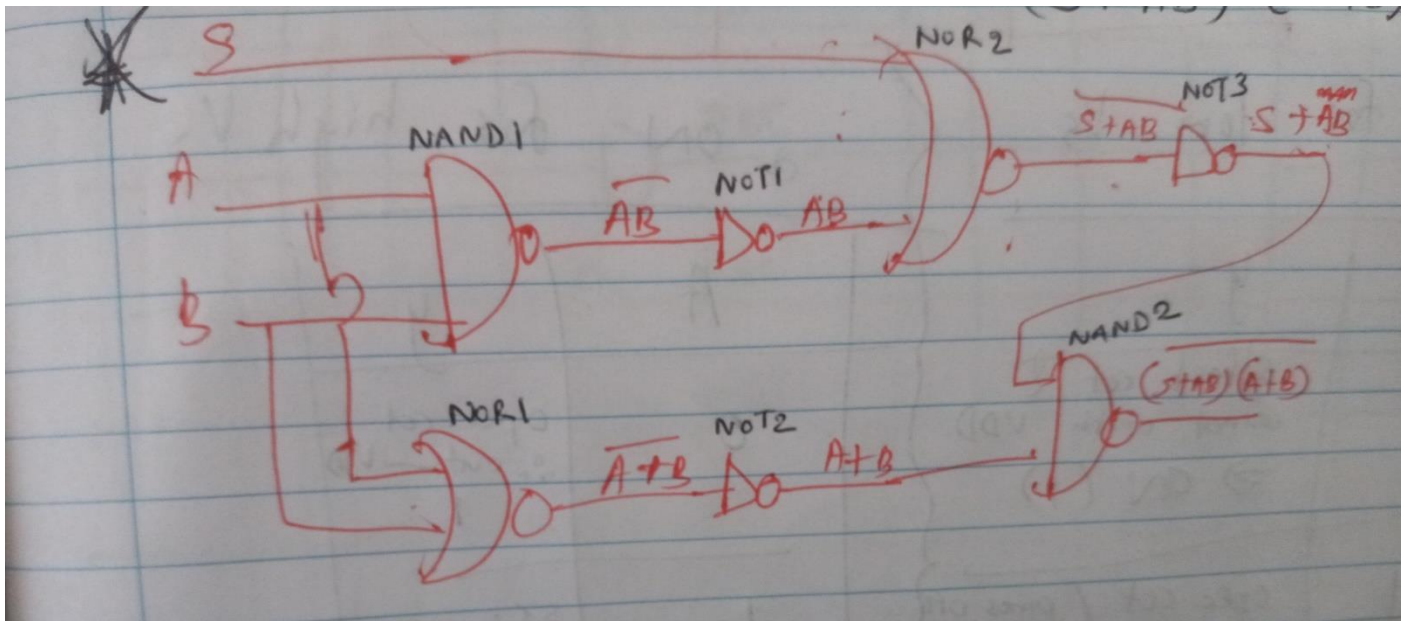
$S=0$ } NAND \Rightarrow
 $S=1$ } NOR \Rightarrow

Then the relevant logic expression was obtained using a karnaugh map and it was further simplified to obtain the combination of 'NAND' and 'NOR' operations.



$$\begin{aligned}
 &\Rightarrow \overline{S}\overline{A} + \overline{S}\overline{B} + \overline{S}\overline{AB} \\
 &\Rightarrow \overline{S}(\overline{A} + \overline{B}) + \overline{AB} \\
 &\Rightarrow \overline{S}(\overline{AB}) + \overline{A} + \overline{B} \\
 &\underline{\underline{S + AB + A + B}} \\
 &\Rightarrow (\overline{S + AB})(\overline{A + B}) \\
 &\Rightarrow (\overline{S + \overline{AB}}) \cdot (\overline{\overline{A} + \overline{B}})
 \end{aligned}$$

So, the resultant combinational logic circuit is as follows. (2 NANDs, 2 NORs, 3 NOTs)



For the implementation of this circuit; 'NOT', 'NAND', and 'NOR' gates were designed using 'NMOS' and 'PMOS' transistors. Their schematics in LTspice are depicted below.

Pdfs- 2part1

NOT – Figure- Schematic of NOT gate

NAND – Figure- Schematic of NAND gate

NOR – Figure- Schematic of NOR gate

Finally, the PLD block is designed using the above gates and the waveforms were obtained.

cct- Figure- Circuit designed using logic blocks

block- Figure- Designed PLD block

wave- Figure- Waveforms for inputs and output of PLD