Department of Electronic and Telecommunication Engineering

University of Moratuwa, Sri Lanka

EN 2110 - Electronics - III

Group Project

Report

Submitted by

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Name	Index	Contribution
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Table 1: Contributions of each member

Contents

1 Parasitic effect in Timing analysis

Objective: *Design a 3 stage (3 inverters) ring oscillator. Find the correlation of the parasitic effect in the oscillation period.*

1.1 System Design

Ring oscillator is a unstable, closed loop device with a negative feedback. It consists of an ***odd number of identical inverters (NOT gates)*** and its output oscillates between ***two voltage levels*** identified as high and low. The period of oscillation(T) of a ring oscillaotr can be expressed as follows where n is the number of cascaded NOT gates and τ_{PD} is the propagation delay of a single inverter.

$$T = 2.n.\tau_{PD}$$

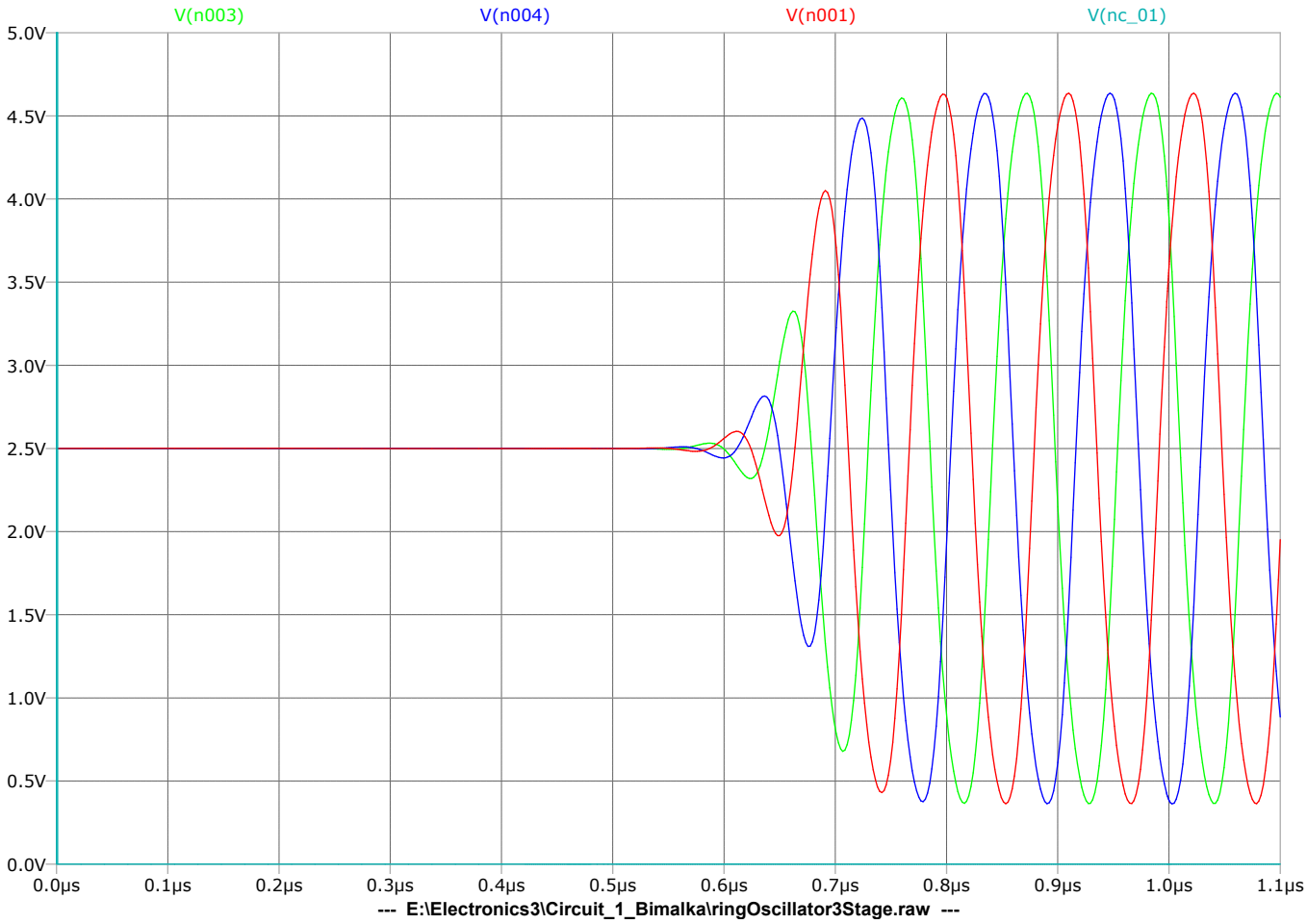

Figure 1: Waveform for Voltage of 3 stages CMOS Ring Oscillator

2 PLD

2.1 Part 1

Objective: *Design a programable logic block to configure it as a 'NAND' or a 'NOR' gate using a single selection bit.*

2.2 Part 2

Objective: *Design a single switch matrix using six pass transistors.*

2.3 Part 3

Objective: *Design a PLD that can be used to design any 3 input combinational circuit.*