- Part 2

Single switch matrix

In this part, the single switch matrix is needed to be designed using six pass transistors. So as the first step, a pass transistor was designed and its performance was checked. Simply an NMOS transistor is fed with a switch could be used for this task.

For signal to travel in both directions (from source to drain and from drain to source) the NMOS has to be symmetric and to have the transistor property, both gate-source and gate-drain of the NMOS should be reverse biased. So body terminal needs to be connected as the lowest voltage in the circuit. So we grounded the body terminal.

So when the switch is on, the input signal will be received at the output. But as we are trying to illustrate a real model, the voltage of the output signal will be somewhat reduced compared with the input signal.

For this task, an NMOS model was chosen and the defined parameters are as follows.

L=0.9u W=1.8u
.MODEL N_1u NMOS LEVEL = 3

+ TOX = 200E-10   NSUB = 1E17   GAMMA = 0.5

+ PHI = 0.7   VTO = 0.8   DELTA = 0.1

+ UO = 650   ETA = 3.0E-6   THETA = 0.1

+ KP = 120E-6   VMAX = 1E5   KAPPA = 0.3

+ RSH = 0   NFS = 1E12   TPG = 1

+ XJ = 500E-9   LD = 100E-9

+ CGDO = 200E-12   CGSO = 200E-12   CGBO = 1E-10

+ CJ = 400E-6   PB = 1   MJ = 0.5

+ CJSW = 300E-12   MJSW = 0.5

So the initially designed pass transistor and its results were obtained as follows.
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without_res_cct– Figure- Schematic diagram of the first designed pass transistor
without_res_wave – Figure- Waveform of the first designed pass transistor

But it was observed that there is a leakage voltage when the NMOS is at the high impedance state. So we used a resistor as a load to pull down the output to zero.
small_res_cct– Figure- Schematic diagram of the second designed pass transistor
small_res_wave – Figure- Waveform of the second designed pass transistor

As observed, the 1kΩ load resistance was not enough to satisfy the necessity. So, we used a larger load instead.
pass_ttr – Figure- Schematic diagram of the finalized pass transistor
pass_wave – Figure- Waveform of the finalized pass transistor

Then using six such transistors, the single switch matrix was designed and the schematic diagram of it is shown below.

   switch_mat – Figure- Schematic diagram of the single switch matrix

   block – Figure- Designed single switch matrix block

Finally the functionality of the circuit was checked by giving pulses to left, right, top, and bottom corners separately and switching on the switches at different periods.

   top – Figure- Waveforms when the top terminal is fed with a pulse

   left – Figure- Waveforms when the left terminal is fed with a pulse

   right – Figure- Waveforms when the right terminal is fed with a pulse

   bottom – Figure- Waveforms when the bottom terminal is fed with a pulse