Influence of MOSFET parameters in its parasitic capacitance and their impact in digital circuits

Article *in* WSEAS Transactions on Circuits and Systems · March 2007

CITATIONS
13

READS
8,173

4 authors:

Nebi Caka
University of Prishtina
111 PUBLICATIONS **173** CITATIONS
SEE PROFILE

Milaim Zabeli
University of Prishtina
26 PUBLICATIONS **78** CITATIONS
SEE PROFILE

Myzafere Limani
Academy of Sciences and Arts of Kosovo
74 PUBLICATIONS **103** CITATIONS
SEE PROFILE

Qamil Kabashi
University of Prishtina
27 PUBLICATIONS **80** CITATIONS
SEE PROFILE

Manuscript received Dec. 20, 2006; revised March. 19, 2007

Influence of MOFSET parameters in its parasitic capacitance and their impact in digital circuits

NEBI CAKA, MILAIM ZABELI, MYZAFERE LIMANI, QAMIL KABASHI
Faculty of Electrical and Computer Engineering
University of Prishtina
10110 Prishtina, Fakulteti Teknik, Kodra e Diellit, p.n.
KOSOVA
nebi.caka@fiek.uni-pr.edu

Abstract: Advanced development of technological processes influenced a wide use of MOSFET transistors in design of integrated digital circuits with high density packages (VLSI). However, in MOSFET transistors parasitic capacitances are present, which will influence on speed of operation in the circuits and dynamic dissipation power. The aim of this paper is to review the influence of channel dimensions, dimensions of source regions, dimensions of drain regions, concentration of impurity (doping concentration) in substrate, concentration of impurity in drain regions (source regions), concentration of impurity sidewalls, level of bias voltage values in particular parasitic capacitance values. Based on the results achieved actions will be determined in order to minimize parasitic capacitance that result in higher speed of operation and lower dynamic power dissipation. Decrease of region dimensions mentioned above depends on technological process capacity for minimal dimensions.

Key words: MOSFET parameters, Parasitic capacitances, Gate capacitive effect, Junction capacitances, Speed of operation, Worst case conditions, Threshold voltage, Propagation delay, Concentration of impurity, Dynamic power dissipation.

1 Introduction

When we analyze MOSFET in its transitive work regime (AC) we should have in mind the parasitic capacitances which influence the speed of operation of the MOSFET device and the MOSFET digital circuits. Considering the MOSFET's structure, these capacitances are distributed and their exact calculation is quite complex. But, by using simple approximation, we can obtain the value of parasitic capacitances which can be used for analyzing the main characteristics of MOSFETs in AC. The Fig. 1 shows the cross-section view and the top view (mask view) of typical n-channel MOSFET (enhancement-type).

Because the gate (L_M) has an extension over the source and drain regions (see Fig. 1), indicated with L_D, the effective channel length is [1, 4, 5]:

$$L = L_M - 2L_D \quad (1)$$

Note that the source and drain overlap region lengths are usually equal to each other because of the symmetry of the MOSFET structure. Typical values of L_D are from $0.05L$ to $0.1L$. Drain and source typical diffusion regions have a width denoted with W, length is denoted by Y and depth is denoted with x_j. Both drain and source regions are surrounded by p^+ in three sides with the purpose of preventing the formation of any unwanted channels between two neighboring n^+ diffusion regions, i.e. to ensure that the surface between two such regions cannot be inverted (as in the case of integrated circuits).

Based on physical structure of MOSFET, its parasitic capacitances can be classified into two major groups:

– the gate capacitive effect (indicated by C_{ox}) and
– junction capacitances *drain-body* and *source-body*.

These two capacitive effects can be modeled by including capacitances in the MOSFET model between its four terminals, G, D, S, and B as shown in Fig. 2. There will be five capacitances: C_{gs}, C_{gd}, C_{gb}, C_{sb} and C_{db} where the subscripts indicate the terminals [2, 3, 5, 6].

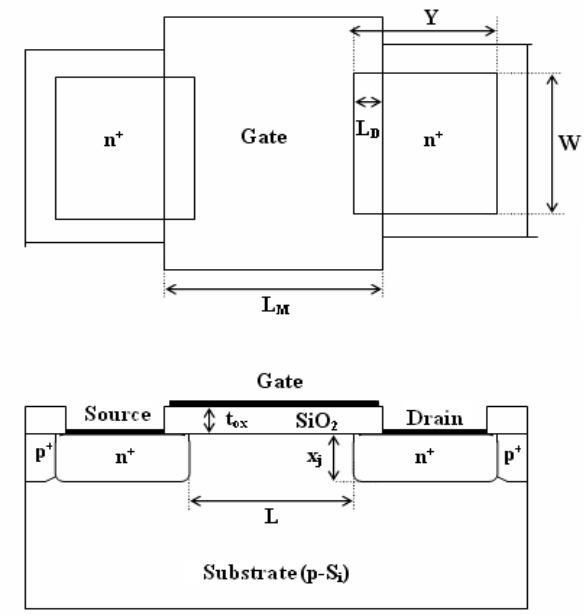

Fig. 1 Cross-section view and the top view of typical n-channel MOSFET.

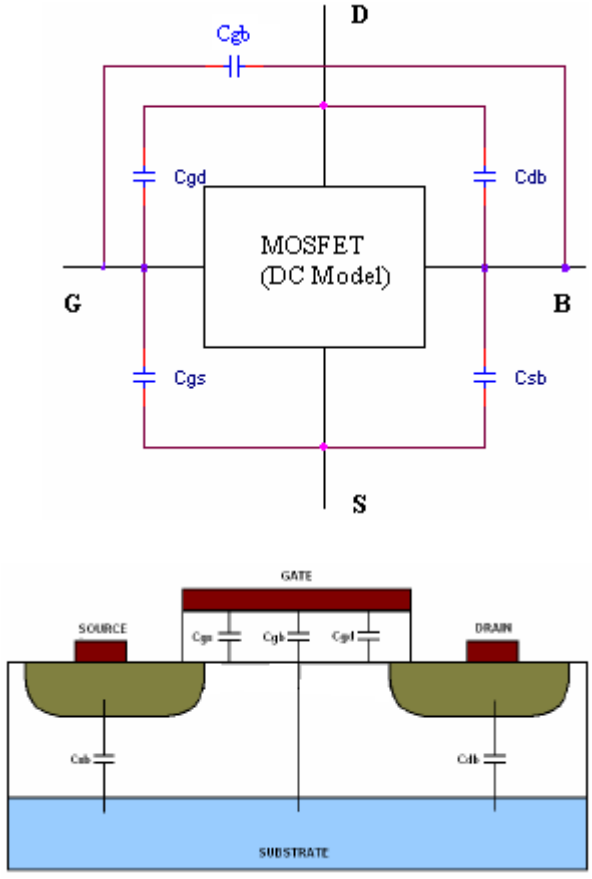

Fig. 2 Lumped representation of the parasitic MOSFET capacitances.

2 Calculation of parasitic capacitances

2.1 The gate capacitive effect

The gate capacitive effect can be modeled by overlapping capacitances C_{GSov}, C_{GDov} and capacitances which are result of interaction between electrodes C_{gs}, C_{gd} and C_{gb} when MOSFET is operating in different work regions [2, 3, 5, 6].

Assuming that both the source and the drain diffusion regions are identically, the overlap capacitances can be calculated as:

$$C_{GSov} = C_{ox}WL_D \quad (2)$$

$$C_{GDov} = C_{ox}WL_D \quad (3)$$

where C_{ox} indicates the value per unit gate area:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (4)$$

ε_{ox} – dielectric constant of S_iO_2, where $\varepsilon_{ox} = 3.97\ \varepsilon_o$ (ε_o – dielectric constant of vacuum), and

t_{ox} – thickness of oxide layer.

Overlapping parasitic capacitances do not depend on the bias conditions (they are voltage-independent). Overlapping capacitances gate-body will not be considered because their values are very small, to compensate this we assume that effective width of channel is W.

Parasitic capacitances C_{gs}, C_{gd}, C_{gb} depend on bias conditions (they are voltage-dependent) as:

– when MOSFET is operating in triode region, channel is considered to be uniform from the source to the drain. The channel on the surface effectively shields the substrate from the gate electric field. Therefore, in this case the gate-channel capacitance will be WLC_{0x} and can be modeled:

$$C_{gs} = C_{gd} = \frac{1}{2}WLC_{ox} \quad \text{and} \quad C_{gb} \approx 0 \quad (5)$$

– when MOSFET is operating in saturation mode, the channel has tapered shape and is pinched off at or near the drain end, thus the channel will not be uniform. In this case the gate-channel capacitance will be approximately $2/3 \cdot WLC_{0x}$ and can be modeled as:

$$C_{gs} \approx \frac{2}{3}WLC_{ox},\ C_{gd} = 0, \text{ and } C_{gb} = 0 \quad (6)$$

– when MOSFET is in cut-off mode, channel is not inducted, thus in this case capacitive effect can be modeled as:

$$C_{gs} = C_{gd} = 0 \text{ and } C_{gb} = WLC_{ox} \quad (7)$$

As we can see from what we said above, the sum of three parasitic capacitances is dependent of gate voltage. This sum has maximal value $C_{ox}WL$ (in the

cut-off and triode region) and minimal value is $0.66 \cdot C_{0x}WL$ (in saturation mode).

Gate capacitive effects in three operating regions of MOSFET including overlapping capacitances are presented as in Table 1.

Tabele 1.

Capa-citance	Cut-off	Linear	Saturation
C_{gbt} C_{gdt} C_{gst}	$C_{ox}WL$ $C_{ox}WL_D$ $C_{ox}WL_D$	0 $1/2C_{ox}WL+C_{ox}WL_D$ $1/2C_{ox}WL+C_{ox}WL_D$	0 $C_{ox}WL_D$ $2/3C_{ox}WL+C_{ox}WL_D$

2.2 Junction capacitances

Parasitic capacitances formed between the source-body and drain-body regions, as a result of reversed polarization during normal operating region of MOSFET, will be in function with reversed polarization voltage. Three dimensional shape of n^+ will form five planer pn-junctions with the surrounding p-type substrate indicated with numbers from 1 to 5. In advanced MOSFETs these parasitic capacitances are calculated separately according to their specific junctions and lumped together in the end. Fig. 4 shows a simpler geometrical shape of MOSFET, focusing n^+ diffusion regions (source) inside body (substrate).

In order to simplify calculation of parasitic capacitances assume that n^+ is rectangular box with dimensions: width *W*, length *Y*, depth x_j. Abrupt (step) pn-junction profiles will be assumed for all junctions for simplicity. In table 2 are shown types and region junctions from Fig. 4.

In the sidewalls 2, 3 and 4 p^+ regions we usually have density about $10N_A$. In practice the actual region shape is quite complicated and impurity concentration is not uniform.

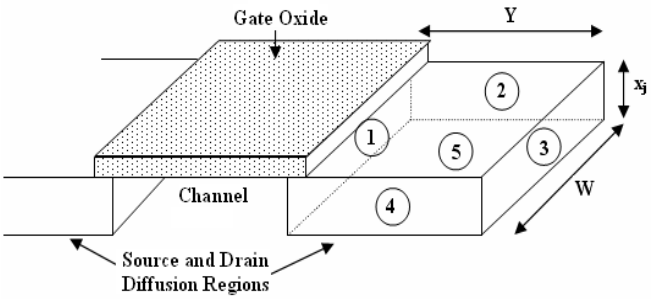

Fig. 3 Three-dimensional view of the n^+ diffusion regions within the p-type substrate.

Table 2. Types and areas of the pn-junctions

Junction	Area	Type
1	$W*x_j$	n^+/p
2	$Y*x_j$	n^+/p^+
3	$W*x_j$	n^+/p^+
4	$Y*x_j$	n^+/p^+
5	W*Y	n^+/p

To calculate the depletion capacitance of a reverse-biased abrupt pn-junction, firstly we consider the depletion region thickness, which is x_d. Assuming that the n-type and p-type doping densities are given by N_D and N_A, respectively, and that reverse bias voltage is given by *V* (negative), the depletion region thickness can be calculated as [3, 5]:

$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{q} \cdot \frac{N_A + N_D}{N_A N_D} \cdot (\phi_0 - V)} \tag{8}$$

where the built-in junction potential is calculated as:

$$\phi_0 = \frac{kT}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) \tag{9}$$

k – Boltzmann's constant, *T* – temperature in Kelvin, *q* – electron charge and n_i – intrinsic carrier concentration in Si.

In normal operating region *pn*-junctions are reverse-biased, therefore amount of electric charge which is stored in depletion region is found by:

$$Q_j = A \cdot q \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D}\right) \cdot x_d = A\sqrt{2\varepsilon_{Si} \cdot q \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D}\right) \cdot (\phi_0 - V)} \tag{10}$$

A – indicates junction area.

The junction capacitances associated with the depletion region are defined as:

$$C_j = \left|\frac{dQ_j}{dV}\right| \tag{11}$$

After differentiating (10) by voltage *V*, we can obtain the expression for pn-junction capacitances:

$$C_j(V) = A \cdot \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D}\right)} \cdot \frac{1}{\sqrt{\phi_0 - V}} \tag{12}$$

This expression can be rewritten in general form by considering the junction grading.

$$C_j(V) = \frac{A \cdot C_{j0}}{\left(1 - \frac{V}{\phi_0}\right)^m} \tag{13}$$

The parameter m in expression (13) is called the grading coefficient. Its value is equal to 1/2 for a step (abrupt) junction profile and 1/3 for a linearly graded junction profile. The zero-bias junction capacitance per unit area C_{j0} is defined as:

$$C_{j0} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\phi_0}} \tag{14}$$

From expression (13) it is obvious that junction capacitance value C_j depends from the external voltage which operates in *pn*-junction. Since the terminal voltage of a MOSFET will change during dynamic operation, exact calculation of junction capacitances under transient conditions is quite complicated. Calculation of junction capacitances by (13) is valid only in the case of small-signal operation. The problem of calculating the junction capacitances value under changing bias conditions can be simplified if we calculate a large-signal average junction capacitance as in the case of logic circuits. This equivalent large-signal capacitance can be defines as [3]:

$$\begin{aligned} C_{eq} &= \frac{\Delta Q}{\Delta V} = \frac{Q_j(V_2) - Q_j(V_1)}{V_2 - V_1} \\ &= \frac{1}{V_2 - V_1} \cdot \int_{V_1}^{V_2} C_j(V) dV \end{aligned} \tag{15}$$

The reverse bias voltage across the pn-junction is assumed to change from V_1 to V_2. The equivalent capacitance is obtained by substituting (13) into (15):

$$C_{eq} = -\frac{A \cdot C_{j0} \cdot \phi_0}{(V_2 - V_1) \cdot (1-m)} \cdot \left[\left(1 - \frac{V_2}{\phi_0} \right)^{1-m} - \left(1 - \frac{V_1}{\phi_0} \right)^{1-m} \right] \tag{16}$$

In the case when m = 1/2 will have:

$$C_{eq} = -\frac{2 \cdot C_{j0} \cdot \phi_0}{(V_2 - V_1)} \left[\sqrt{1 - \frac{V_2}{V_0}} - \sqrt{1 - \frac{V_1}{V_0}} \right] \tag{17}$$

The equation (17) can be rewritten in simpler form by defining a dimensionless coefficient K_{eq}, as follows:

$$K_{eq} = -\frac{2\sqrt{\phi_0}}{V_2 - V_1} \cdot \left(\sqrt{\phi_0 - V_2} - \sqrt{\phi_0 - V_1} \right) \tag{18}$$

$$C_{eq} = A \cdot C_{j0} \cdot K_{eq} \tag{19}$$

K_{eq} – is called the voltage equivalence factor ($0 < K_{eq} < 1$).

The accuracy of calculated values by expressions (18) and (19) is usually sufficient.

From Fig. 1 and Fig. 2 in three junction sidewalls (2, 3 and 4) of MOSFET, source and drain regions are surrounded by p^+ region, with higher doping density then substrate. Consequently, the sidewall zero-bias capacitance C_{j0sw}, as well as the sidewall voltage equivalence factor $K_{eq}(sw)$ will by different from those of the bottom junction (junction 5) and sidewall junction from channel (junction 1).

Assuming that the sidewall doping density in p^+ is $N_A(sw)$, then we will have:

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A(sw) \cdot N_D}{N_A(sw) + N_D} \right) \cdot \frac{1}{\phi_{0sw}}} \tag{20}$$

where ϕ_{0sw} -is the build-in potential of the p^+ sidewall junctions with drain or source regions.

$$\phi_{0sw} = \frac{kT}{q} \cdot \ln \left(\frac{N_A(sw) \cdot N_D}{n_i^2} \right) \tag{21}$$

Since all sidewalls regions p^+ have approximately same depth of x_j, we can define a zero-bias sidewall junction capacitance per unit length.

$$C_{jsw} = C_{j0sw} \cdot x_j \tag{22}$$

The sidewall voltage factor for a voltage swing between V_1 and V_2 is defined as follows:

$$K_{eq}(sw) = -\frac{2\sqrt{\phi_{0sw}}}{V_2 - V_1} \cdot \left(\sqrt{\phi_{0sw} - V_2} - \sqrt{\phi_{0sw} - V_1} \right) \tag{23}$$

Combining the equation (20) through (22), the equivalent large-signal junction capacitance $C_{eq}(sw)$ for sidewall of length (perimeter) P can be calculated as:

$$C_{eq}(sw) = P \cdot C_{jsw} \cdot K_{eq}(sw) \tag{24}$$

Combining the equivalent junction capacitances we can find the equivalent junction capacitance of drain-body or source-body using expressions:

$$C_{db} = C_{sb} = A_t \cdot C_{j0} \cdot K_{eq} + P_t \cdot C_{jsw} \cdot K_{eq}(sw) \tag{25}$$

A_t – total area of the n^+/p junctions (sum of the bottom area and the sidewall area facing the channel region).

P_t – length of the n^+/p^+ junction perimeter (sum of three sides of the drain diffusion area).

Calculation of the equivalent junction source-body parasitic capacitance C_{sb}, proceed in the same way as junction drain – body.

3. Results and discussion

Effects of channel dimensions, drain and source dimensions of regions, concentration impurity in MOSFET capacitances may be achieved by using MOSFET parasitic capacitance expressions.

In Fig. 4 is shown the dependence of gate capacitive effect in the so-called "worst case" conditions on area *S* (product between width and length channel), for parametric values of thickness of oxide layers (t_{ox}). With the so-called "worst case" we understand the case when gate capacitive effect reaches its maximal value.

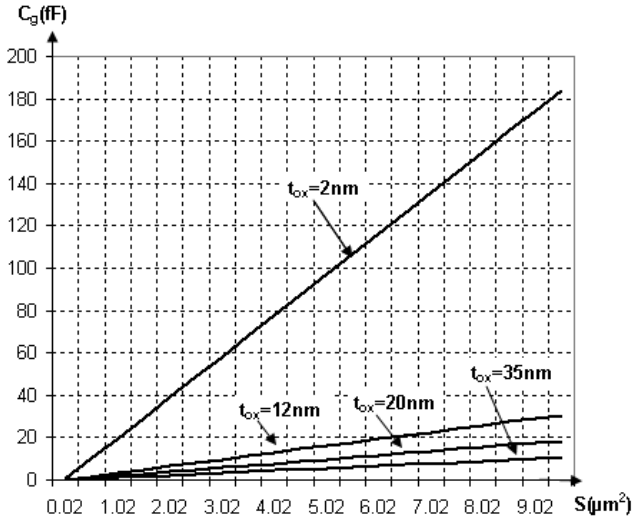

Fig. 4 The dependence of gate capacitive effect on area S for the different values of parameter t_{ox}.

From fig. 4, based on acquired values, we can conclude that gate capacitive effect is in direct proportion with the size of the area *S* but in indirect proportion with thickness of oxide layer. Therefore, minimal capacitive values are gained when *S* (*W*L)* is lower and thickness gains higher values.

The thickness has effect in the threshold voltage [3]. Dependence of threshold voltage (V_{t0}) by thickness is shown in fig. 5, when V_{SB} = 0 V and the MOSFET is defined with long-channel ($L >> x_j$).

Dependence of threshold voltage against the oxide layer thickness is taken for an ideal case, yet it can be a reference for the typical values of threshold voltage. Threshold voltage V_{t0} can be adjusted by selective dopant ion implantation into the channel region of the MOSFET during fabrication process [3].

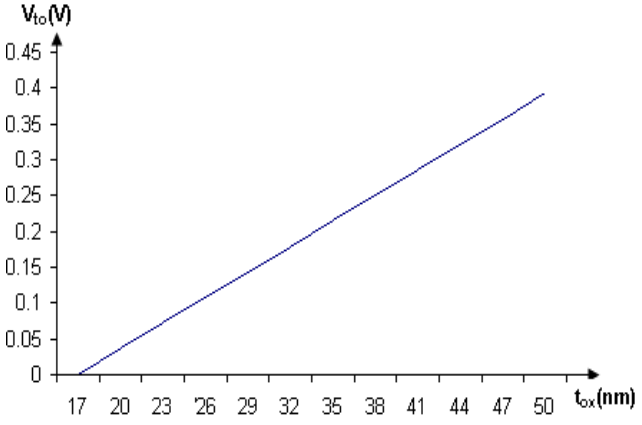

Fig. 5 The dependence of threshold voltage on thickness of oxide layer *tox*, when $N_A = 10^{16}$ cm^{-3} and $N_{ox} = 4 \cdot 10^{10}$ cm^{-3}.

Fig. 6, 7 and 8 shows the dependence of equivalent parasitic capacitance C_{db} from the width of drain regions (*W*) for parametrical length value(*Y*) of drain, when junction depth x_j takes different value.

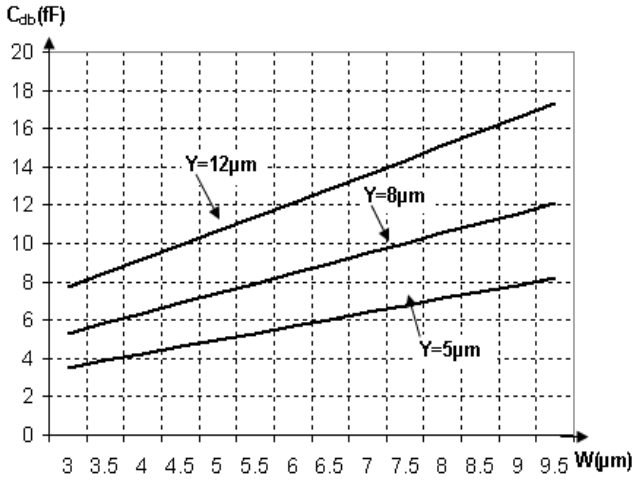

Fig. 6 Dependence of junction capacitance drain-body C_{db} and *W* on parametrical values of *Y* of drain region, for: x_j = 0.4 μm, $N_A = 4 \cdot 10^{15}$ cm^{-3}, $N_D = 2 \cdot 10^{19}$ cm^{-3}, N_A (*sw*) = $4 \cdot 10^{16}$ cm^{-3}; V_1 = 0 V and V_2 = – 5 V.

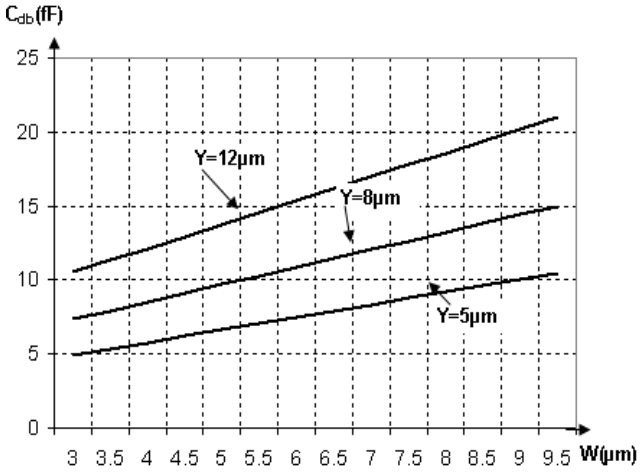

Fig. 7 Dependence of junction capacitance drain-body C_{db} and W on parametrical values of Y of drain region, for x_j = 0.8 µm, $N_A = 4 \cdot 10^{15}$ cm^{-3}, $N_D = 2 \cdot 10^{19}$ cm^{-3}, N_A (sw) = $4 \cdot 10^{16}$ cm^{-3}; V_1 = 0 V and V_2 = – 5 V.

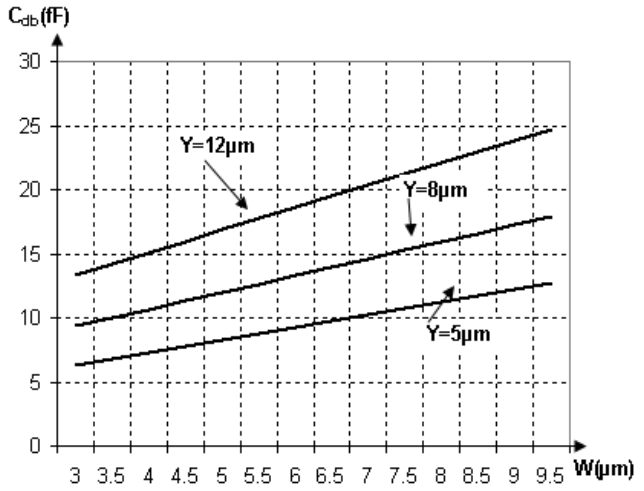

Fig. 8 Dependence of junction capacitance drain-body C_{db} and W on parametrical values of Y of drain region, for x_j = 1µm, $N_A = 4 \cdot 10^{15}$ cm^{-3}, $N_D = 2 \cdot 10^{19}$ cm^{-3}, N_A (sw) = $4 \cdot 10^{16}$ cm^{-3}; V_1 = 0V and V_2 = – 5 V.

Results from fig. 6, 7 and 8 show influence of particular dimensions of drain regions on parasitic capacitance values C_{db}, together with respective capacitance value in fF based on dimensions values. These figures prove that for higher values of any dimensions W, Y or x_i higher values of parasitic capacitance C_{db} will be achieved.

Impact of impurity concentration in substrate (N_A) and drain sidewalls (N_{sw}) on the capacitance value C_{db}, when concentration on the drain region (N_D) remains unchanged is shown in Fig 9.

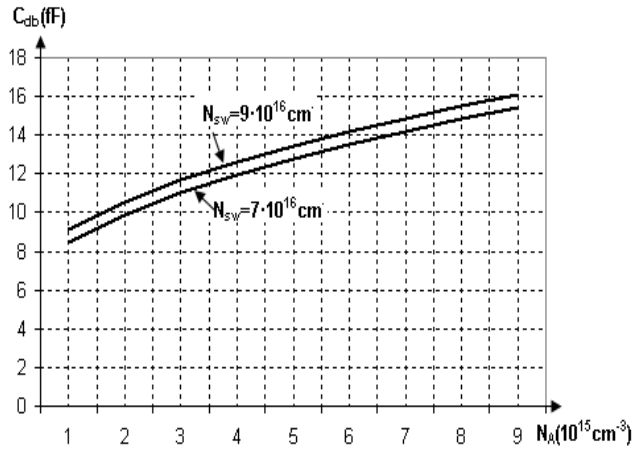

Fig. 9 Dependence of junction capacitance drain-body C_{db} and N_A on parametrical values of N_{sw}, for: x_j = 0.5 µm, $N_D = 2 \cdot 10^{19}$ cm^{-3}, W = 10 µm, Y = 6 µm, V_1 = 0 V and V_2 = – 5 V.

Results in fig 9, show that concentration of N_A and N_{sw} have impact on capacitance values C_{db}. Therefore for higher concentration values, higher capacitance values C_{db} will be achieved.

Influence of impurity concentration of drain region on junction capacitance values C_{db} when other parametrical are constant is shown in Fig 10.

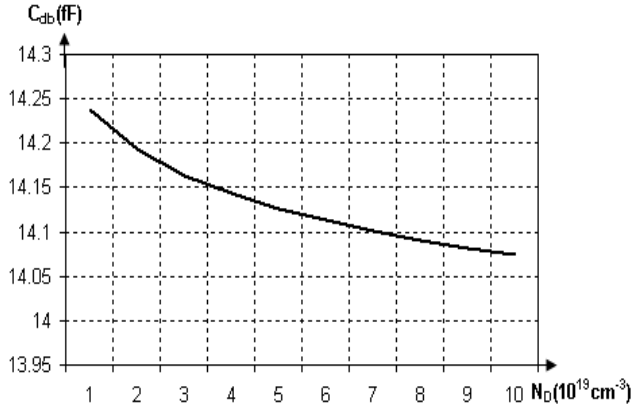

Fig. 10 Dependence of junction capacitance drain-body C_{db} and N_D, for x_j = 0.5 µm, $N_A = 7 \cdot 10^{15}$ cm^{-3}, $N_{sw} = 7 \cdot 10^{16}$ cm^{-3}, W = 10 µm, Y = 6 µm, V_1 = 0V and V_2 = – 5V

Results in Fig. 10 show that increase of impurity concentration in drain region N_D will have a small impact on decrease of C_{db} value.

Impact of bias voltage levels (V_1, V_2) and the difference between them on the capacitance value C_{db} when other parameters are constant is shown in Fig. 11. Smaller difference values of bias voltage will have smaller C_{db} values.

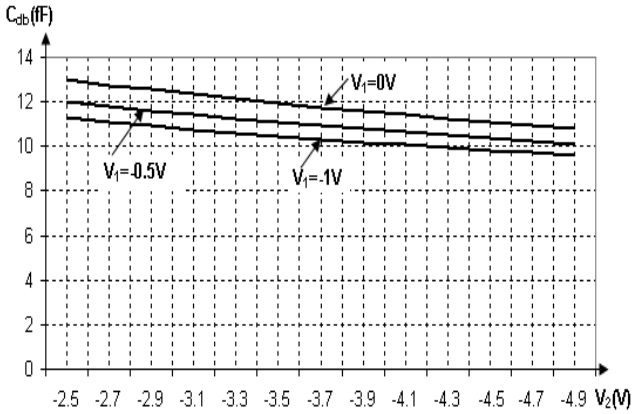

Fig. 11 Dependence of junction capacitance drain - body C_{db} and V_2 on parametrical values of V_1, when x_j = 0.5 µm, $N_A = 4 \cdot 10^{15}$ cm^{-3}, $N_D = 2 \cdot 10^{19}$ cm^{-3}, $N_{sw} = 4 \cdot 10^{16}$ cm^{-3}, W = 10 µm, Y = 6 µm.

Results and discussion for equivalent parasitic capacitance C_{sb} (source- body) are the same as $C_{db.}$

To simplify the problem of MOSFET inverters design, in switched conditions, all parasitic capacitance of MOSFET which influence its parameters will combine into a lumped capacitance C, including load and parasitic capacitances of connection.

Parasitic capacitance C will cause propagation delays t_{PHL} and $t_{PLH,}$ at the output of the inverter. Impact of parasitic capacitance C on CMOS inverter's propagation delays is expressed by [5]:

$$\tau_{PHL} = \frac{1.6C}{k_n'(W/L)_n V_{DD}} \quad (26)$$

$$\tau_{PLH} = \frac{1.6C}{k_p'(W/L)_p V_{DD}} \quad (27)$$

From the propagation delays it may be concluded that for smaller values of parasitic capacitance C, smaller delays will occur. Also propagation delays will determine maximal operation frequency of inverter or circuit designed by MOSFETs [3].

$$f_{max} = 1/(t_{PHL} + t_{PLH}) \quad (28)$$

The value C will influence also the dynamic dissipation power of MOSFET inverter or designed circuits with MOSFET transistors [5]:

$$P_D = f \cdot C \cdot V_{DD}^2 \quad (29)$$

The power-delay is a fundamental parameter for measuring the quality of particular circuit technology [5].

$$DP = P_D \cdot t_P \quad (30)$$

Lower the value of DP the more effective is the circuit's technology.

4 Conclusions

Using achieved results (also graphically presented) it may be concluded that to reduce the gate capacity effect, channel dimensions must be reduced or the thickness of oxide layer must increase. To achieve these nominal values, technological processes capacity for minimal possible dimensions must be taken into account. Final results shows that for the junction capacity values of drain-body, parasitic capacitance values may be reduced for smaller values of drain region dimensions, which are depending on technological process. Impurity concentration will have impact on the junction capacitance values, but still higher impact will have N_A. Smaller values of junction parasitic capacitance will be achieved if voltage bias swing band is smaller. Decreased values of parasitic capacitance will result in propagation delays, higher work speed and lower dynamic dissipation power.

References:

[1] Allen, P. E. and E. Sanchez-Sinencio, *Switched-Capacitor Circuits*, New York: Van Nostrand Reinhold, 1984.

[2] Horenstein, M. N., *Microelectronic Circuit Design*, 2nd edition, New York: McGraw-Hill, 2004.

[3] Kang, S. M. and Y. Leblebici, *CMOS Digital Integrated Circuits*, 3rd edition, McGraw-Hill, 2003

[4] Neamen, D. A. *Electronic Circuit Analysis and Design*, 2nd edition, New York: McGraw-Hill, 2001.

[5] Sedra, A. C. and K. C. Smith, *Microelectronic Circuits*, 5th edition, Oxford University Pres 2004

[6] Tsividis, Y. P., *Operation and Modeling of the MOS Transistor*, New York: Oxford University Press, 1999.

[7] M. G. Anacona, Z. Yu, R. W. Dutton, P. Z. V. Voorde, M Cao, and D Vook, " *Density- Gradient analyses of MOS tunneling", IEEE Trans. Electron Devices* 47, 2310 (2000).

[8] J. Ramirez-Angulo and A. Lopez, "*Mite circuits: The continuous-time counterpart to switched capacitor circuits," IEEE Transactions on Circuits and Systems II*, vol. 48, pp. 45–55, January 2001.