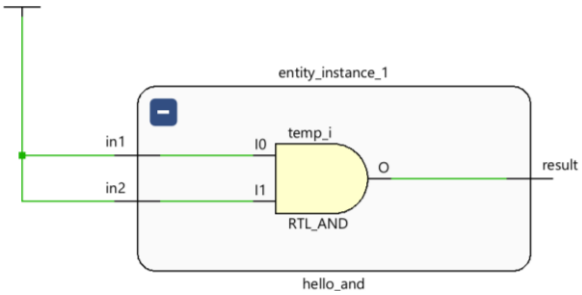
# Group 11 – Lab 1 report

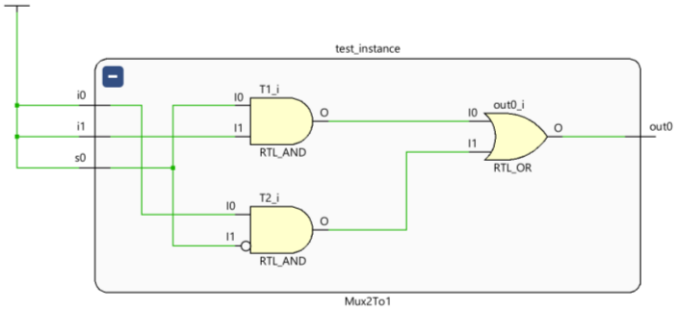
Kim Svedberg (17%), Zebastian Thorsén (17%), Joen Järnkvist (17%),

Sebastian Warzocha (17%), Christian Mokhtar (16%), Majd Sheikh Mahmoud (16%)

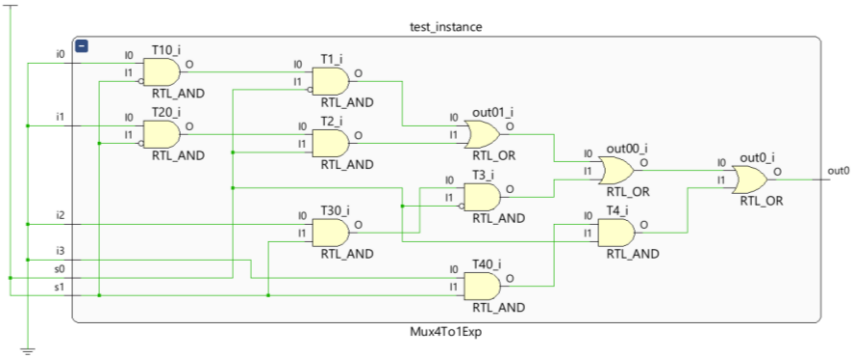
## Block Designs



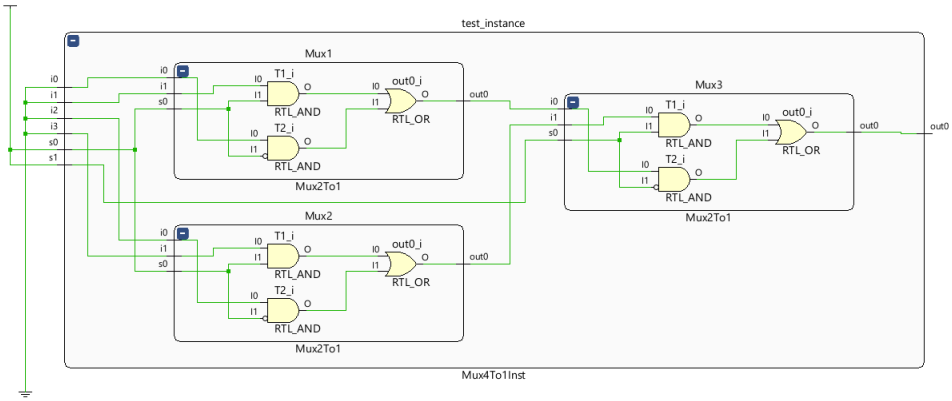

Step 1



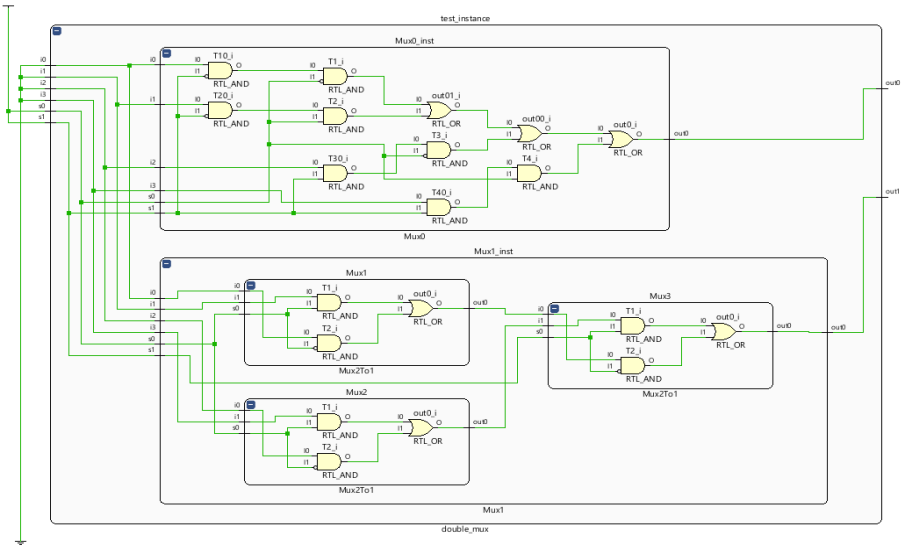

Step 2




Step 3

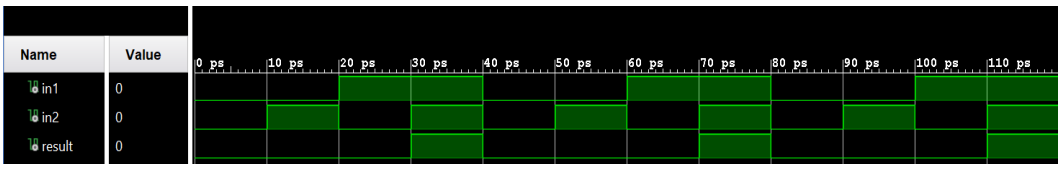



Step 4

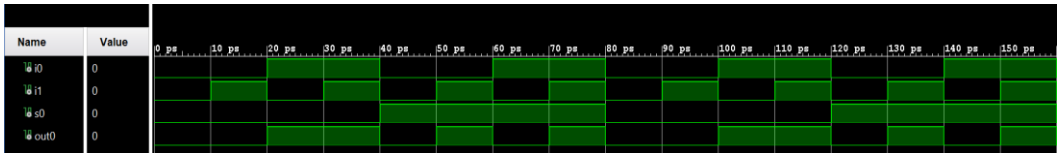



Step 5

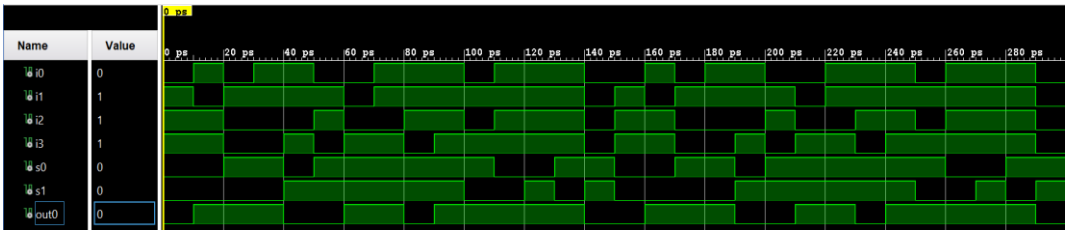
## Simulations



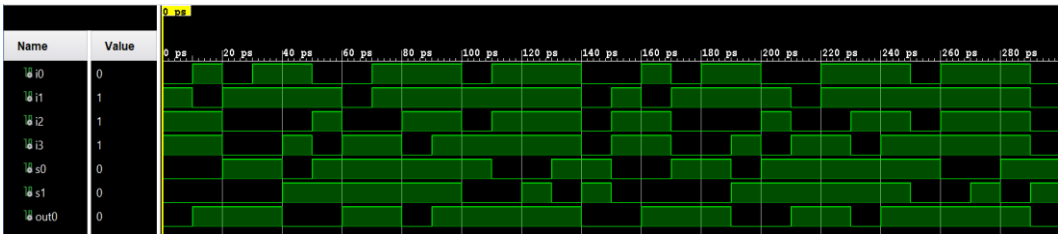

Step 1



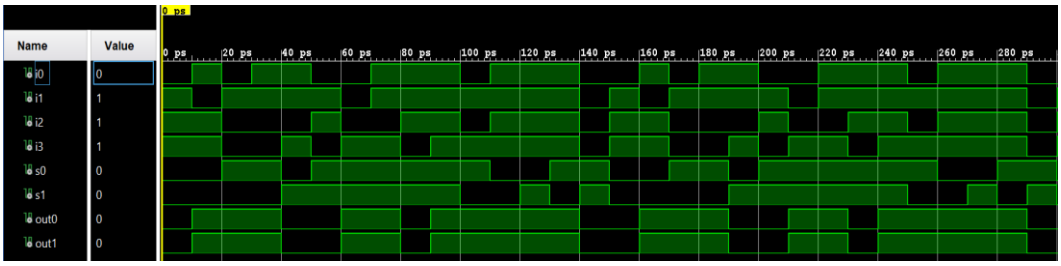

Step 2




Step 3




Step 4




Step 5

## LUT lists

| Site Type | Used | Fixed | Prohibited | Available | Util% |
|---|---|---|---|---|---|
| Slice LUTs* | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Logic | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Memory | 0 | 0 | 0 | 9600 | 0.00 |
| Slice Registers | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Flip Flop | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Latch | 0 | 0 | 0 | 41600 | 0.00 |
| F7 Muxes | 0 | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 0 | 8150 | 0.00 |

Step 1

| Site Type | Used | Fixed | Prohibited | Available | Util% |
|---|---|---|---|---|---|
| Slice LUTs* | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Logic | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Memory | 0 | 0 | 0 | 9600 | 0.00 |
| Slice Registers | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Flip Flop | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Latch | 0 | 0 | 0 | 41600 | 0.00 |
| F7 Muxes | 0 | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 0 | 8150 | 0.00 |

Step 2

| Site Type | Used | Fixed | Prohibited | Available | Util% |
|---|---|---|---|---|---|
| Slice LUTs* | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Logic | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Memory | 0 | 0 | 0 | 9600 | 0.00 |
| Slice Registers | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Flip Flop | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Latch | 0 | 0 | 0 | 41600 | 0.00 |
| F7 Muxes | 0 | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 0 | 8150 | 0.00 |

Step 3

| Site Type | Used | Fixed | Prohibited | Available | Util% |
|---|---|---|---|---|---|
| Slice LUTs* | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Logic | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Memory | 0 | 0 | 0 | 9600 | 0.00 |
| Slice Registers | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Flip Flop | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Latch | 0 | 0 | 0 | 41600 | 0.00 |
| F7 Muxes | 0 | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 0 | 8150 | 0.00 |

Step 4

| Site Type | Used | Fixed | Prohibited | Available | Util% |
|---|---|---|---|---|---|
| Slice LUTs* | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Logic | 0 | 0 | 0 | 20800 | 0.00 |
| LUT as Memory | 0 | 0 | 0 | 9600 | 0.00 |
| Slice Registers | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Flip Flop | 0 | 0 | 0 | 41600 | 0.00 |
| Register as Latch | 0 | 0 | 0 | 41600 | 0.00 |
| F7 Muxes | 0 | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 0 | 8150 | 0.00 |

Step 5