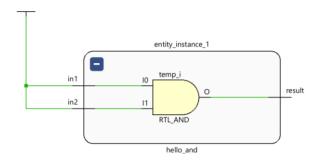
Group 11 – Lab 1 report

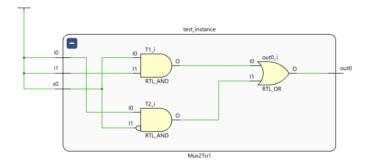
Kim Svedberg (17%), Zebastian Thorsén (17%), Joen Järnkvist (17%),

Sebastian Warzocha (17%), Christian Mokhtar (16%), Majd Sheikh Mahmoud (16%)

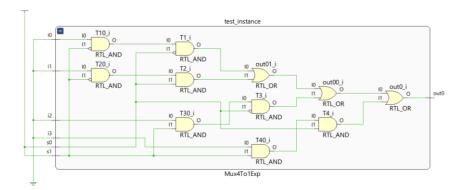
Block Designs



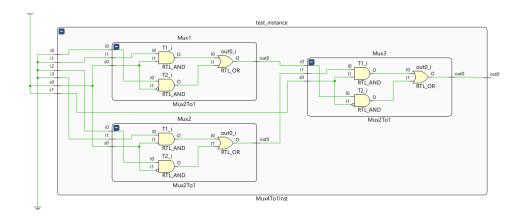
Step 1



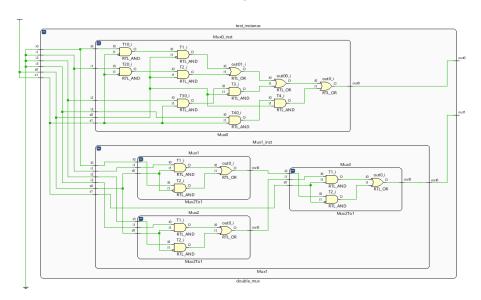
Step 2



Step 3

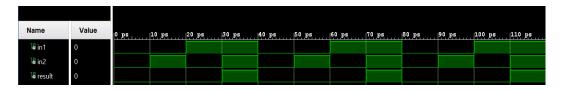


Step 4



Step 5

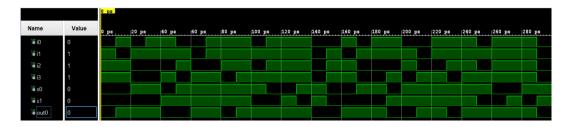
Simulations



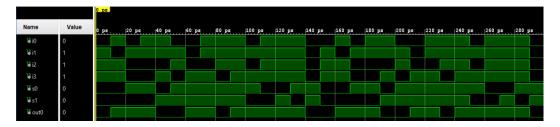
Step 1



Step 2



Step 3



Step 4



Step 5

LUT lists

+	-+		+-		+-		+		+-		+
Site Type		Used				Prohibited					Ţ
·	-+		_		+		ı		-		_
Slice LUTs*		0		0		0	ı	20800		0.00	
LUT as Logic	-	0		0	I	0	I	20800	I	0.00	1
LUT as Memory	-	0		0	I	0	I	9600	l	0.00	1
Slice Registers	-	0		0	Ī	0	Ī	41600	Ī	0.00	1
Register as Flip Flop	1	0	I	0	Ī	0	Ī	41600	ĺ	0.00	Ī
Register as Latch	1	0	1	0	Ī	0	Ī	41600	Ī	0.00	Ī
F7 Muxes	-	0	I	0	Ī	0	Ī	16300	ĺ	0.00	Ī
F8 Muxes	-	0	I	0	Ī	0	Ī	8150	ĺ	0.00	1
+	-+		+-		4.		+		+-		+

Step 1

+	+		+		+	+	++
Site Type					Prohibited	•	
Slice LUTs*	1	0	+	0	l 0	20800	0.00
LUT as Logic	1	0	1	0	0	20800	0.00
LUT as Memory	1	0	L	0	0	9600	0.00
Slice Registers	1	0		0	0	41600	0.00
Register as Flip Flop	I	0	L	0	0	41600	0.00
Register as Latch	1	0	L	0	1 0	41600	0.00
F7 Muxes	1	0	L	0	0	16300	0.00
F8 Muxes	I	0	L	0	0	8150	0.00
+	+		+		+	+	

Step 2

+	-+-		+-		+	+-		+-		+
Site Type	Ţ	Used	Ī	Fixed	Prohibited					
Slice LUTs*		0	+- 	0	 0		20800	1	0.00	
LUT as Logic	1	0	Ī	0	0	Ī	20800	Ī	0.00	1
LUT as Memory	1	0	I	0	0	I	9600	Ī	0.00	1
Slice Registers	1	0	I	0	0	I	41600	1	0.00	1
Register as Flip Flop	1	0	I	0	0	I	41600	I	0.00	1
Register as Latch	1	0		0	0		41600	1	0.00	1
F7 Muxes	1	0		0	0	I	16300	I	0.00	1
F8 Muxes	1	0	I	0	0	I	8150	I	0.00	1
+	-4-		+-		+	4.		4-		-+-

Step 3

Site Type	1 1	Used	İ	Fixed	İ	Prohibited	ĺ	Available	ĺ	Util%
Slice LUTs*	i	0	i		i	0		20800	i	0.00
LUT as Logic	1	0	Ī	0	Ī	0	I	20800	I	0.00
LUT as Memory	1	0	I	0	I	0	I	9600	I	0.00
Slice Registers	1	0	I	0	I	0	I	41600	I	0.00
Register as Flip Flop	1	0	I	0	T	0	1	41600	L	0.00
Register as Latch	1	0	I	0	T	0	1	41600	L	0.00
F7 Muxes	1	0	I	0	Ī	0	I	16300	I	0.00
F8 Muxes	1	0	I	0	I	0		8150	I	0.00
+	+-		+-		+-		+		+-	+

Step 4

+	-+-		+-		+	+-		+-		-+
Site Type	1	Used	I	Fixed	Prohibited	Ĺ	Available	Ī	Util%	1
+	-+-		+-		+	+-		+-		+
Slice LUTs*	1	0	I	0	0	Ī	20800	Ī	0.00	1
LUT as Logic	1	0	I	0	0	Ī	20800	I	0.00	1
LUT as Memory	1	0	I	0	0	Ī	9600	I	0.00	1
Slice Registers		0	I	0	0		41600	I	0.00	-
Register as Flip Flop	1	0		0	0	ľ	41600	I	0.00	1
Register as Latch	1	0	I	0	0		41600	I	0.00	1
F7 Muxes	-	0		0	0	I	16300	I	0.00	1
F8 Muxes	-	0		0	0	ľ	8150	I	0.00	1
						4.		1		

Step 5