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CITY UNIVERSITY OF HONG KONG
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Active EMI Filtering Technology for Power
Electronic Systems

抑制電力電子系統電磁干擾的有源濾波技術

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Department of Electrical Engineering
電機工程學系

in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy
哲學博士學位

by

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August 2022
二零二二年八月

ABSTRACT

In a power electronic system, semiconductor devices work in switched mode to pursue high efficiency and flexible yet stable output. The fast switching transition generates electromagnetic interference (EMI), comprising differential-mode (DM) and common-mode (CM) emissions. Passive EMI filters are widely used to attenuate EMI. However, the bulky volume of passive filters becomes a bottleneck in increasing the power density of the entire system. Active EMI filters are thereby proposed to use active components to replace part of the passive components for volume reduction. This thesis is devoted to developing the active EMI filtering technology for power electronic systems in three aspects: DM filter, input CM filter, and output CM filter.

The first work has advanced the power semiconductor filter (PSF), which is an active DM filter. The concept of the PSF is based on utilizing a series pass device (SPD) operated in linear mode to regulate the input current of switching converters. A fixed-frequency dynamic ramp modulator is proposed to avoid input current oscillation and reduce power dissipation of the SPD. An optimized fast-current regulation circuit is designed to achieve high DM EMI attenuation. A method to predict the EMI suppression performance of the PSF is proposed. Furthermore, the ground loop inductance in the fast-current regulation circuit is shown to significantly impair the filtering performance, and PCB layout guidelines are given to mitigate this adverse effect. A 100W buck-boost PFC prototype with the PSF satisfies EMC standard EN55015 class B in the whole range of 150kHz to 30MHz.

The second work has proposed an advanced input active CM filter (ACF). It has the merits of wide bandwidth, high attenuation, and general multistage structure. The working bandwidth of the ACF ranges from 150kHz to 30MHz. By cascading several ACF sections, a multistage structure that exhibits higher filtering attenuation can be designed. The number of cascaded sections is optimized by considering the required filtering attenuation. The performance of single-stage and multistage ACFs is evaluated on two commercial power supplies with rated power of 90W and 1000W, respectively.

Experimental results show that the physical volume of the ACF is significantly smaller than that of the passive filter, and the power dissipation of the ACF is similar to its passive counterpart.

The third work has proposed a new active filtering architecture for PWM inverter-fed motor drive systems. The stepwise CM voltage at the output of inverters causes EMI and damage to motor bearings. A new output ACF is proposed to compensate for the steep rising/falling edges of CM voltage for EMI reduction and bearing protection. An input ACF is also necessary to attenuate the CM noise injected into the grid. Hence, a holistic assessment of this new active filtering architecture, comprising input and output ACFs, is demonstrated. Moreover, ferrite materials and the winding configuration of the CM transformer used in the output ACF are investigated. The relationship between the input and output ACFs is also discussed. This work aims to provide new perspectives and implementation guidelines for the ACFs in motor drive systems.

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Chapter 1

INTRODUCTION

1.1. Electromagnetic Interference and Its Regulations

In 1865, for the first time, Maxwell systematically described the properties of electric and magnetic fields and their interactions. From 1887 to 1888, Hertz designed ingenious experiments that proved the existence of electromagnetic waves. Since then, extensive works have been devoted to the analysis and application of electromagnetic waves. The widespread use of electromagnetic waves has driven developments in numerous fields; however, they cause electromagnetic interference (EMI). To regulate EMI, the International Committee for Radio Interference (CISPR) was established in 1933. CISPR specifies the EMI measuring apparatus and methods to be employed. The maximum acceptable EMI levels in different applications have also been stipulated.

With the development of power electronics, switched-mode power supplies (SMPS), with various topologies, have been applied to numerous applications to meet the demand for power conversion [1]. The rapid switching transitions generate EMI. Due to the latest advances in semiconductor technology, the operating frequency of power switching devices continues to increase, making EMI a critical issue [2], [3].

As specified by CISPR, a line impedance stabilization network (LISN) is used to measure the EMI generated by switching networks [4]. The LISN provides a standard grid impedance so that the measured EMI is repeatable and comparable; it also blocks the interference of grid-side noise. According to the noise propagation path, EMI can be classified into differential-mode (DM) and common-mode (CM) emission [5]. The propagation paths of DM and CM noise of a general switching converter is shown in Fig. 1.1. A CM/DM noise separator can distinguish CM and DM noise from the overall EMI. It facilitates the analysis and design of EMI filters since CM and DM noise mechanisms are different.

Fig. 1.2 illustrates the noise spectrum and corresponding regulations. Noise below the 50th order of fundamental frequency (50 Hz/60 Hz) is considered as harmonics. There is no regulation for the frequency range of 3-9 kHz, and regulations for 9-150 kHz are only applicable to a few specific applications. Conducted EMI from 150 kHz to 30 MHz is tightly regulated by CISPR. Noise above 30 MHz is defined as radiated EMI. This thesis will focus on conducted EMI from 150 kHz to 30 MHz.

1.2. Review of EMI Mitigation Methods

Classification of conducted EMI mitigation methods is shown in Fig. 1.3. EMI mitigation methods can be classified into two main types: attenuation at noise sources and attenuation along propagation paths. Among these filtering techniques, active EMI filters are promising in regard to achieving high attenuation with a compact size. The shaded blocks in Fig. 1.3 represent the works presented in this thesis to develop the active EMI filtering technology.

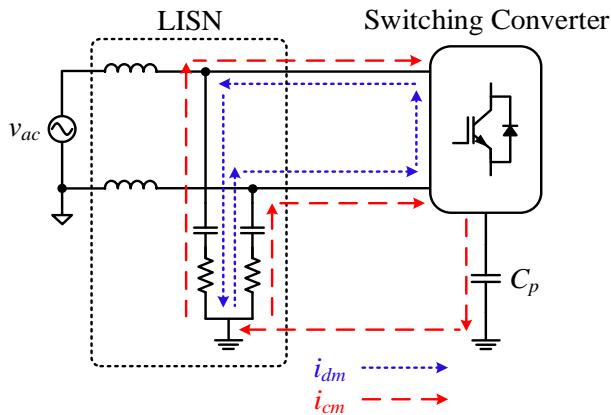


Fig. 1.1. Propagation paths of DM and CM noise.

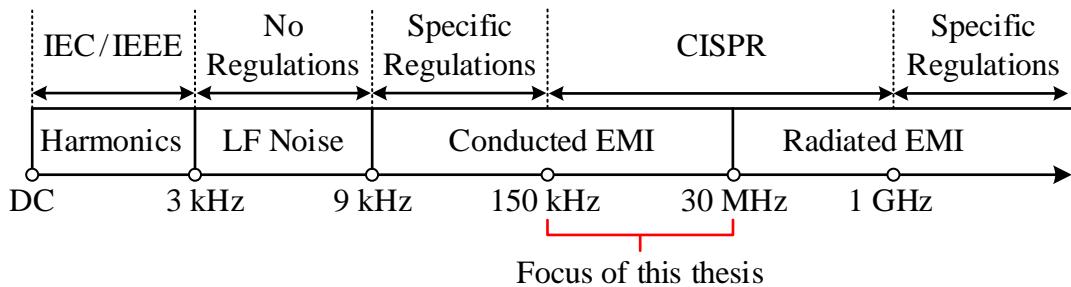


Fig. 1.2. Noise spectrum and regulations.

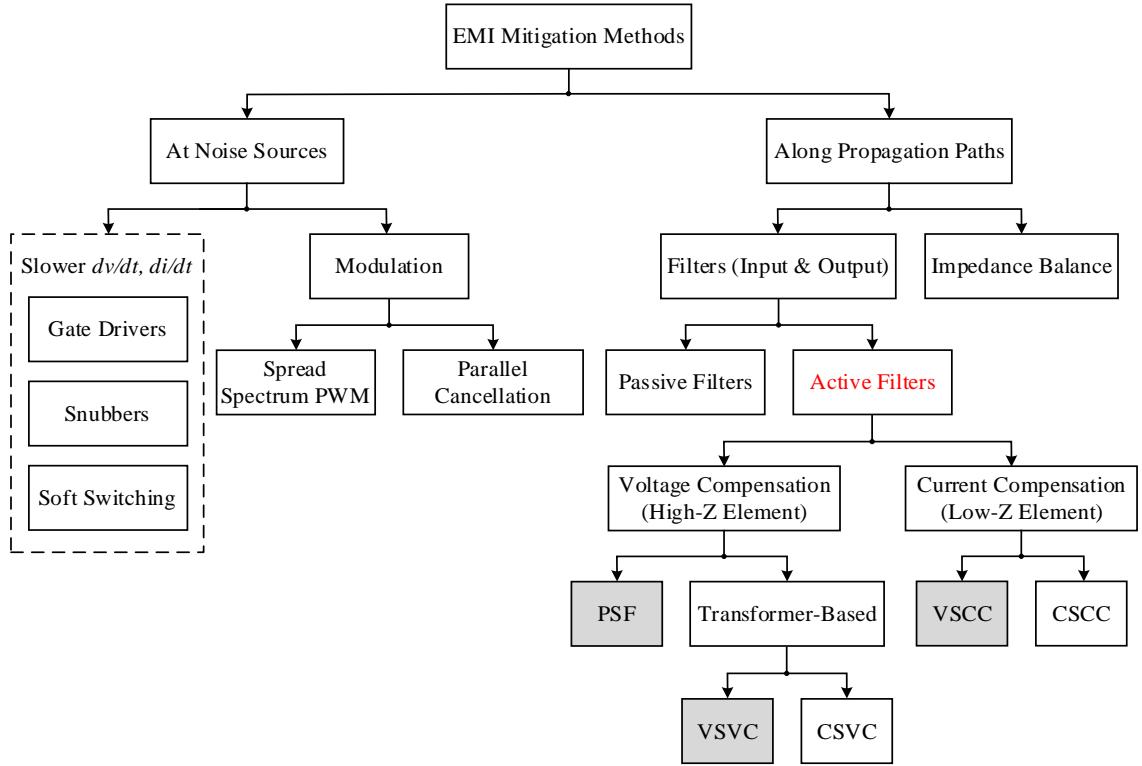


Fig. 1.3. Classification of conducted EMI mitigation methods.

1.2.1. EMI Attenuation at Noise Sources

Since EMI is caused by rapid switching transitions, it will be alleviated if the transitions are slowed down. A conventional approach is to use increased gate resistance to drive the switching device. However, this practice incurs higher switching loss. Considering that EMI is dominated by turn-on transitions while power efficiency mainly depends on turn-off transitions for flyback converters, separated turn-on and turn-off gate resistors are used [6]. In order to better balance the trade-off between power loss and EMI, active gate drivers are proposed to dynamically control the gate-source signal and shape the resulting switching waveforms [7], [8]. Since switching transitions are smoothed but not eliminated, this method is most effective in the high-frequency range.

Snubbers connected across switching devices are effective in dampening overshoots and oscillation; high-frequency EMI is thus reduced at the cost of increased power loss [9].

There is a common belief that the soft-switching technique reduces both switching losses and EMI since soft-switching converters have lower dv/dt and di/dt than their hard-switching counterparts [10]-[12]. The soft-switching technique mitigates the reverse recovery transient of diodes, which is a culprit of DM emission; thus, DM noise in the high-frequency range is reduced. Although the main switches use the soft-switching technique, the auxiliary switches are still in the hard-switching mode. Hence, the reduction of CM emission is not significant. Moreover, the EMI performance is sensitive to the layout of soft-switching-related components. An improper layout can result in strong resonances [13].

EMI can also be mitigated by using sophisticated modulation schemes. Instead of a fixed switching frequency, the switching frequency varies in random, periodic, programmed, or chaotic manners [14]-[17]. EMI noise is thus spread over a wider frequency band to reduce the spectral peaks, as illustrated in Fig. 1.4. In practice, noise reduction can be achieved only when the switching frequency variation is several times higher than the resolution bandwidth (RBW) of the EMI receiver [17]. Although lower EMI peaks are obtained, low-frequency harmonics might be introduced [18]. Another approach is zero CM voltage modulation [19]-[21]. It makes the CM voltages of parallel inverters cancel each other out. CM voltages can be cancelled because they share the same ground, either the protective earth or the neutral point of the DC link voltage. Since each inverter has its individual DM noise propagation path, DM voltage cancellation modulation schemes have not been proposed yet.

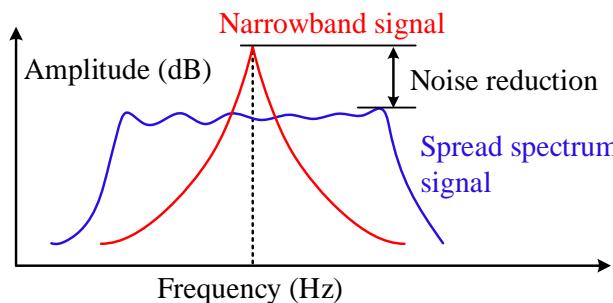


Fig. 1.4. Spectrum spreading for noise reduction [16].

1.2.2. Impedance Balance Technique

Using the concept of the Wheatstone bridge, the impedance balance technique can mitigate the CM noise injected into the grid without suppressing the noise source [22]-[26], as shown in Fig. 1.5. Since DM currents contain the load current and unwanted DM noise, this technique cannot attenuate DM noise without affecting the load current. Hence, this method has achieved good CM filtering performance but is currently not applicable for DM attenuation.

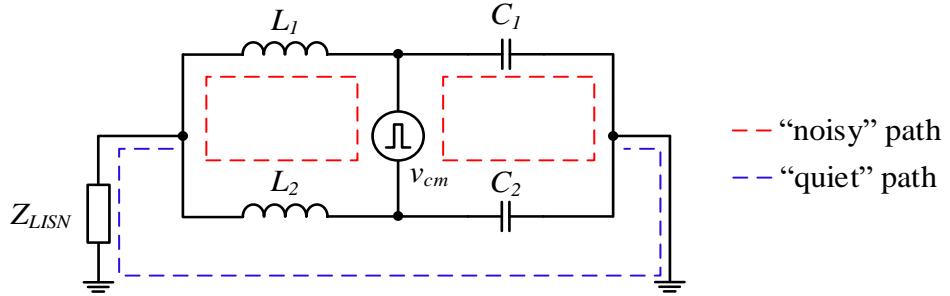


Fig. 1.5. Equivalent CM circuit with the impedance balance technique.

1.2.3. EMI Filters

The sections above introduce the methods to attenuate EMI at noise sources and along propagation paths using the impedance balance technique. They are effective in the high-frequency range and specific applications. However, they cannot suppress the whole spectrum of conducted EMI below the limit stipulated by EMC standards. EMI filters are most widely used due to their generality and flexibility.

1.2.3.1. Passive EMI Filters

Passive EMI filters, including DM and CM filters, are constructed by passive components – inductors and capacitors [27]-[29], as shown in Fig. 1.6. The inductor volume can hardly be reduced due to the limitation of magnetic materials. The attempt to reduce the inductance, in turn, leads to increased capacitor volume. The capacitance in a filter also has restrictions. The DM capacitance in a power factor corrector (PFC) is restricted to maintain a high power factor. For safety considerations, the total Y-

capacitance of a CM filter is limited to avoid high leakage current [30]; a large CM inductor, therefore, is inevitable. Bulky passive EMI filters become a bottleneck in relation to raising power density and efficiency [31], [32].

The parasitic parameters of passive filters will significantly impair high-frequency filtering performance [33]-[35]. Inductive and capacitive coupling exists among inductors, capacitors, and traces on a printed circuit board (PCB). The layout and orientation of components require careful consideration, which complicates the filter design and enlarges the overall volume of filters. Some parasitic cancellation techniques have been proposed to mitigate this adverse effect [36]-[39].

The permeability of ferrite materials will drop above the cut-off frequency, which is inversely proportional to the initial permeability according to Snoek's Law [40]. The complex permeability curves, denoting the reactive (μ_s') and loss (μ_s'') components, of two ferrite materials (T38 [41] and N30 [42]) are shown in Fig. 1.7. T38 has a higher initial permeability but a lower cut-off frequency. Hence, the attempt to make a compact inductor using high permeability materials will compromise high-frequency performance.

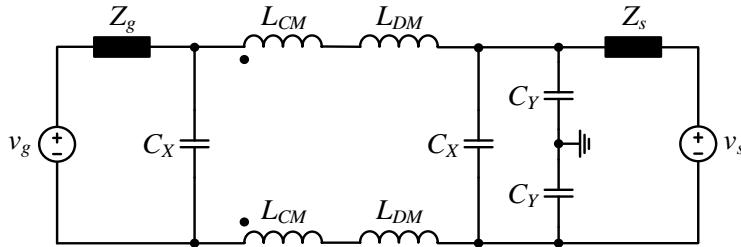


Fig. 1.6. Schematic diagram of a typical passive EMI filter.

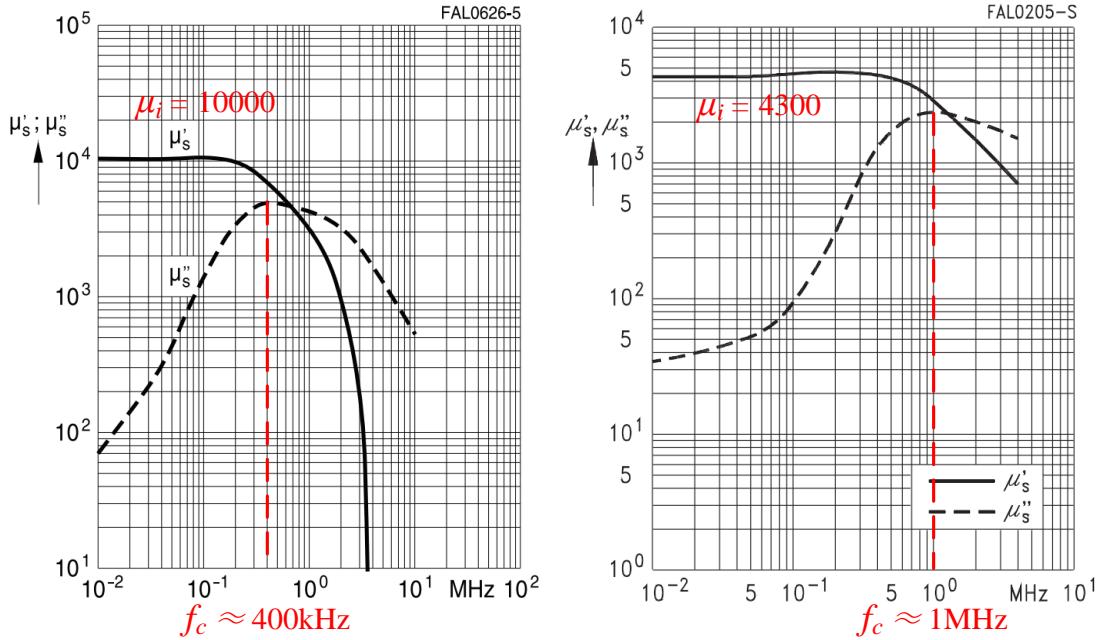


Fig. 1.7. Complex permeability as a function of frequency. (a) T38 [41]. (b) N30 [42].

1.2.3.2. Active EMI Filters

In a passive EMI filter, inductors hinder noise propagation while capacitors shunt noise back to its source. Consequently, noise flowing into the grid is attenuated. Active and passive EMI filters share similar working principles; they have high-impedance elements and low-impedance elements. The voltage-compensation active filter forms a high impedance path in series with noise sources to attenuate the noise, acting as an inductor. The current-compensation active filter creates a low impedance path in parallel with noise sources to circulate high-frequency noise, acting as a capacitor.

An ideal current source has infinite output impedance; it blocks noise in all frequency bands. A metal-oxide field-effect transistor (MOSFET) can be considered as a voltage-controlled current source in its linear region of I-V characteristics, which is shown in Fig. 1.8. This feature inspires the attempt to use the linear characteristics of semiconductors to address EMI caused by switching transitions of semiconductors themselves [43]. It is distinctively different from other active filtering techniques using active components to enhance the performance of passive ones. The power semiconductor

filter (PSF) is proposed to utilize the high output impedance characteristics of a series pass device (SPD) in linear mode [44]-[47]. A fast-current regulation circuit has been devised to significantly increase MOSFETs' intrinsic output impedance; considerable DM attenuation has been achieved [48]. Fig. 1.9 shows a generalized converter's DM noise propagation path with the PSF. In order to attenuate CM noise, a pair of PSFs should be connected to both input power lines. The difficulty in implementing a high-side PSF makes the PSF currently only applicable for DM attenuation. The concept of the PSF can also be applied to active bridge rectifiers [49]. In such active bridge rectifiers, MOSFETs not only perform rectification with a smaller dropout voltage than diodes but also attenuate DM noise. Since no additional MOSFET is introduced into the power circuit, this implementation reduces the volume and power dissipation of the EMI filter.

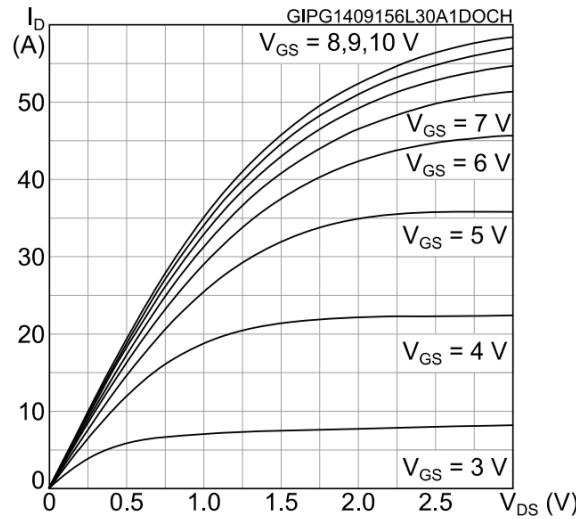


Fig. 1.8. I-V characteristics of MOSFET STD19N3LLH6AG [50].

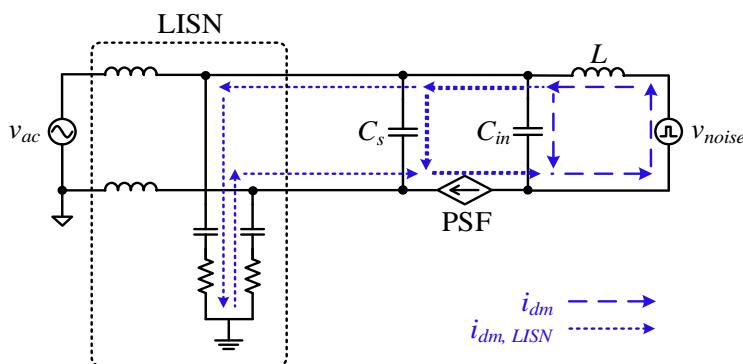
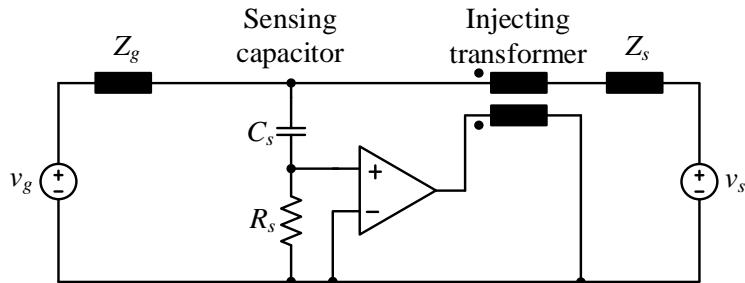


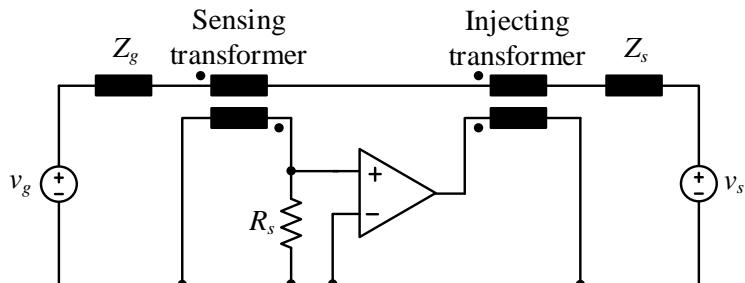
Fig. 1.9. DM EMI propagation path of a generalized converter with the PSF.

Another approach to insert an active high-impedance element into a power circuit is by using a transformer. The noise voltage or current is sensed and amplified by an amplifier. The output voltage of the amplifier is applied to the transformer to realize voltage compensation. According to the sensing stages, there are two implementations: voltage-sensing and voltage-compensation (VSVC) [51]-[54] and current-sensing and voltage-compensation (CSVC) [55], [56], as shown in Fig. 1.10(a) and (b).

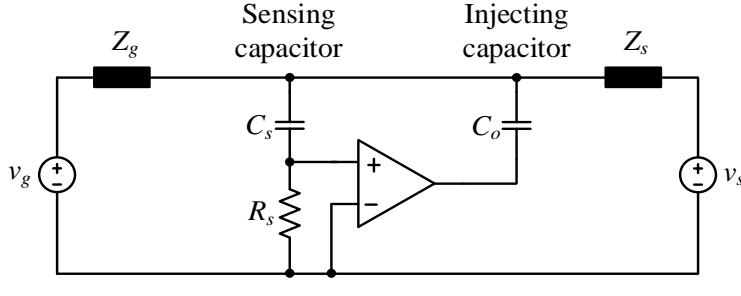
The method of realizing an active low-impedance element is through current compensation. The voltage or current disturbance is sensed and amplified by an amplifier. The output voltage of the amplifier is connected in series with a capacitor. Consequently, the instantaneous rate of capacitor voltage is magnified, and more noise current will circulate through this capacitor. According to the sensing stages, there are two implementations: voltage-sensing and current-compensation (VSCC) [57]-[61] and current-sensing and current-compensation (CSCC) [62]-[68], as shown in Fig. 1.10(c) and (d).



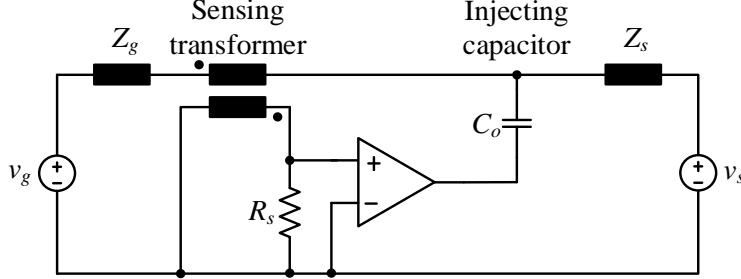
(a)



(b)



(c)



(d)

Fig. 1.10. Four active filter topologies. (a) VSVC. (b) CSVVC. (c) VSCC. (d) CSCC. [69]

1.3. Motivation

Inductors are often concerned with bulkiness, considerable parasitic elements, and reduced permeability at high frequencies. The PSF uses the linear characteristics of semiconductor devices to attenuate their switching noise, which is promising in regard to addressing the issues faced with inductors. Although the PSF has exhibited good DM filtering performance, input current oscillation occurred when using variable-switching frequency in previous works. Fixed-frequency dynamic ramp modulation is thus proposed to set the switching frequency away from the grid-side resonant frequency. Since the noise is concentrated in fixed-frequency operation, resulting in higher spectrum peaks, the DM filtering capability of the PSF is enhanced in this thesis.

The significant DM attenuation achieved by the PSF inspired the author to continue developing active CM filtering techniques. Prior art active CM filters (ACFs) are most effective in regard to low-frequency noise filtering, and their performances are often compromised by stability restrictions or the effect of the parasitic elements. In this

thesis, a high-attenuation and wideband ACF section is proposed. Moreover, the concept of the ACF is extended to multistage configuration to fulfill the requirement of different applications.

The works introduced above have developed the input DM and CM filtering techniques for switching converters. PWM inverter-fed motor drives require an output filter to mitigate CM emission and protect motor bearings. Electric motors account for a considerable part of global power consumption. Hence, it is of great importance to design a low-loss output ACF for motor drives. To this end, this thesis proposes a low-loss output ACF that only compensates for rising/falling edges of CM voltage instead of eliminating CM voltage in the prior art. On top of that, a holistic CM filtering architecture, comprising this new output ACF and the input ACF in the author's second work, is proposed for motor drive systems.

1.4. Thesis Organization

The rest of this thesis is organized as follows:

In Chapter 2, an improved PSF with dynamic ramp modulation for DM attenuation is proposed. Fixed-frequency dynamic ramp modulation avoids input current oscillation and reduces the power dissipation of the PSF. The fast-current regulation circuit in previous work has been optimized to achieve better filtering performance. PCB layout guidelines of the PSF are also provided.

In Chapter 3, a high-attenuation wideband ACF section for input CM EMI filtering is proposed. The general multistage ACF configuration for higher attenuation is demonstrated, and the optimal number of ACF sections at a specific insertion loss is given. The power dissipation of the ACF is comparable with that of conventional passive filters, while the physical volume of the ACF is significantly reduced.

In Chapter 4, a new output ACF is proposed to protect motor bearings and reduce CM noise. A holistic active CM filtering architecture, comprising input and output ACFs, for motor drive systems is assessed. Characteristics and design considerations of the

ACFs for motor drives are also presented.

In Chapter 5, a conclusion of EMI filter design for different applications and the major contributions of this thesis are delineated. In addition, suggestions for future research are discussed.

Chapter 2

ACTIVE DIFFERENTIAL-MODE POWER SEMICONDUCTOR FILTER

2.1. Chapter Introduction

The working principle of the active DM power semiconductor filter (PSF) is based on controlling a series pass device (SPD) operated in linear mode to regulate the input current of switching converters. Continuous work has been done to explore the potential of the PSF in input filtering applications. Reference [45] has presented the concept and analyzed the operating principles of the PSF in filtering out the input current harmonics of the DC-DC buck converter. Reference [46] has applied the PSF to a boost-type PFC to profile the input current. Reference [47] has proposed a series pass module to utilize low voltage rating SPD in high voltage applications to achieve better filtering performance. Although performing well in harmonics filtering, references [45]-[47] have not shown the effectiveness of the PSF in EMI suppression. Started from reference [48], the filtering capability of the PSF has been advanced from low-frequency harmonics to high-frequency EMI noise by thousand times increasing the crossover frequency of the current regulation circuit.

Variable-frequency modulation has been used in converters with the PSF to regulate the SPD voltage in [46]-[48]. Oscillation in the input current is observed if the switching frequency is equal to or close to the grid-side resonant frequency. Traditional front-end passive filters, which are widely used in switching converters, can attenuate harmonics and EMI noise. The reactive elements in the passive filter can decrease the resonant frequency well below the switching frequency. Moreover, passive or active damping is adopted in filter design to avoid resonance. The PSF is proposed to replace conventional passive filters; the input oscillation, therefore, is a critical consideration in variable-frequency operation, where the frequency spectrum is spread. Thus, fixed-frequency modulation is proposed to alleviate such issue by setting the switching frequency away from the grid-side resonant frequency. This is the fundamental difference

in the design consideration of switching converters with passive filters and the PSF.

Reference [48] has demonstrated conducted EMI suppression using the PSF in variable-frequency operation. The EMI noise is spread as switching frequency varying, and the noise peak is thus reduced in variable-frequency operation [16]. In fixed-frequency operation, however, the EMI noise is concentrated on switching frequency and multi-order switching frequencies, resulting in higher EMI noise peaks than these in variable-frequency operation. Hence, better EMI suppression capability of the PSF is required in fixed-frequency operation.

This chapter is devoted to addressing the issues in previous works [45]-[48] in three aspects:

1) Suppression of input current oscillation - A fixed-frequency dynamic ramp modulator is proposed to avoid the oscillation in the input current. It is based on operating the converter at a fixed switching frequency, and the switching frequency is set away from the grid-side resonant frequency.

2) Reduction of the power loss of the SPD - The voltage across the SPD is adaptively regulated at a low level over low-line and high-line conditions by the dynamic ramp modulator. Compared with [48], 48.1% and 19.6% reduction of power dissipation in the SPD has been achieved under full rated power, low-line and high-line conditions, respectively. Due to reduced power dissipation, the heatsink for the SPD can be eliminated, cooling the SPD by the copper plate on PCB. The volume reduction is also realized with power loss reduction.

3) Optimization of the current regulation circuit design - Solving the issues of redundant gain stage design and inadequate capacitive load driving capability in [48], the proposed single-stage amplifier with an RC damping circuit has achieved better EMI suppression performance than that of the configuration of the two-stage amplifiers. The cost and volume of the PSF are also reduced.

The operating principles and design procedures of the dynamic ramp modulator

will be introduced. Modeling and optimization of the fast-current regulation circuit will also be studied. A 100W, 90-264Vac / 200Vdc, buck-boost LED driver is built to validate the operation of the dynamic ramp modulator and EMI suppression performance of the optimized fast-current regulation circuit. Experimental results show the validity of the theoretical analysis.

2.2. Overview of Operating Principles of the PSF

Fig. 2.1 shows the system architecture of a buck-boost LED driver with the PSF. The PSF is connected at the input of the converter. The gate-source voltage of the SPD T_c is continuously regulated by the fast-current controller; hence, the output impedance of T_c is continuously adjusted so that T_c operates as a controlled current source. Ideally, only fundamental frequency current can pass through T_c ; hence, harmonics and high frequencies EMI noise are suppressed. Capacitor C_{in} is connected at the input of the converter, providing a low impedance path for the high-frequency current to circulate back to the power converter stage. Capacitor C_X is used to absorb high-frequency noise caused by the non-ideal characteristics of the diode bridge. Parasitic capacitor C_p provides a path for the CM current; capacitor C_Y is used to absorb CM EMI noise. The EMI noise flowing into the grid side, therefore, is reduced.

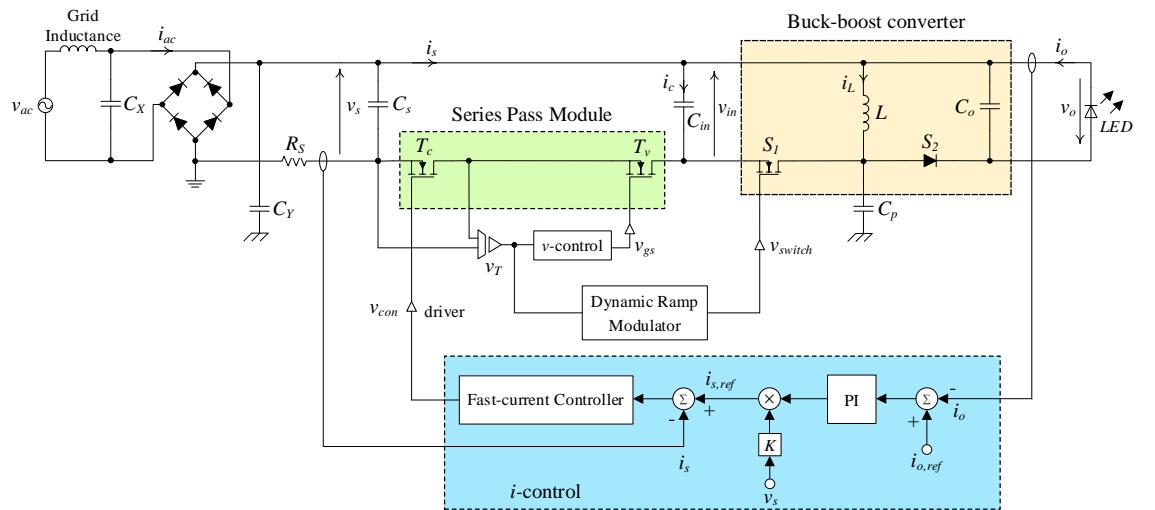


Fig. 2.1. The system architecture of the 100W buck-boost LED driver.

Non-ideal parasitic characteristics of the SPD would degrade its EMI suppression capability. Regarding to this issue, a high-voltage rating MOSFET T_v is used to form a series pass module (SPM), as depicted in [47]. The low-voltage SPD T_c has higher output impedance than T_v ; hence, T_c is used to tightly regulate the current flowing through it. T_v withstands high voltage stress at start-up and around zero-crossing while maintains fully-on during the rest time of a line period. This structure enables designers to utilize low-voltage rating SPD in high-voltage applications.

The difference between the output current i_o and the current reference $i_{o,ref}$ is processed by the PI controller; then, the output of the PI controller is multiplied by the input voltage v_s with a scaler K . The input current reference $i_{s,ref}$, is a rectified waveform of v_{ac} (i.e., v_s) and is in phase with it. The fast-current controller makes the input current i_s tightly follow $i_{s,ref}$. The voltage across T_c , v_T , is sensed and compared with a voltage reference $v_{T,ref}$ to dictate the operating state of the switch S_I through the dynamic ramp modulator. The analysis and design procedures of the dynamic ramp modulator will be demonstrated in Section 2.3.

2.3. Analysis and Design of the Dynamic Ramp Modulator

To minimize the power loss of the SPD, the SPD is regulated to operate around the “knee point” between the ohmic and saturation regions of MOSFET.

2.3.1. Operation Principles of the Dynamic Ramp Modulator

In the ohmic region of the SPD, the variation of the current with v_T is large; valley-voltage mode control [70] is employed to regulate the minimum voltage to avoid the SPD entering this region. Instead of using a fixed reference, the voltage across T_c , v_T is compared with a reference $v_{T,ref}$, which consists of a dynamic ramp V_{ramp} and an offset V_{offset} , as illustrated in Fig. 2.2.

The valley-voltage mode control shares similar characteristics with current-programmed control; they are susceptible to disturbance [70]. A duty cycle smaller than 0.5 would lead to instability in valley-voltage mode control. An artificial ramp V_{ramp} is

necessary to add a step of slope compensation to diminish the perturbation in v_T thereby enhancing the stability of this system. V_{offset} is adopted to ensure T_c always works beyond the ohmic region. The switch S_1 will turn on when v_T decreases below the reference voltage $v_{T,ref}$; it will turn off when v_T goes up higher than $v_{T,ref}$.

A logic circuit is designed to realize fixed-frequency operation, as depicted in Fig. 2.3. The operating states and principles of the logic circuit are tabulated in Table 2.1. The SR latch is reset by the clock signal V_{CLK} at the beginning of each fixed period T_S to turn the switch S_1 off, avoiding v_T to go up too large. During the rest time of a cycle, the state of switch S_1 remains unchanged, unless v_T is smaller than $v_{T,ref}$. Once v_T decreases below $v_{T,ref}$, switch S_1 turns on and then v_T increases until the next reset. The switching frequency is identical to the clock signal; fixed-frequency operation, therefore, is achieved. Two possible waveforms of v_T is shown in Fig. 2.4.

Switching noise or ringing of the switch S_1 may lead to false modulation triggering. The circuit, shown in Fig. 2.3, has the ability of blanking mis-triggering. During the turn-on transition, S_1 cannot be turned off until the next clock appears. The narrow pulse signal V_{CLK} can blank false turn-on during the turn-off transition.

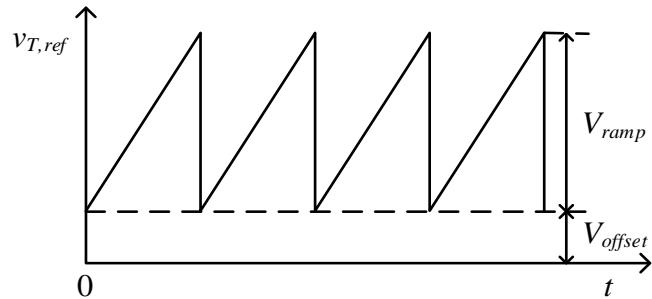


Fig. 2.2. Waveform of the reference voltage.

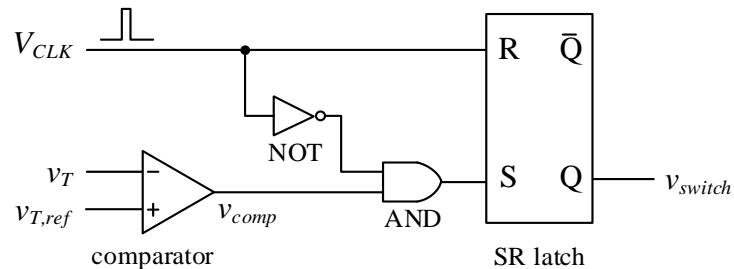


Fig. 2.3. Schematic of the logic circuit.

Table 2.1
Logic Table

V_{CLK}	v_{comp}	R	S	Q
0	0	0	0	$Q_{n+1} = Q_n$
0	1	0	1	1
1	0	1	0	0
1	1	1	0	0

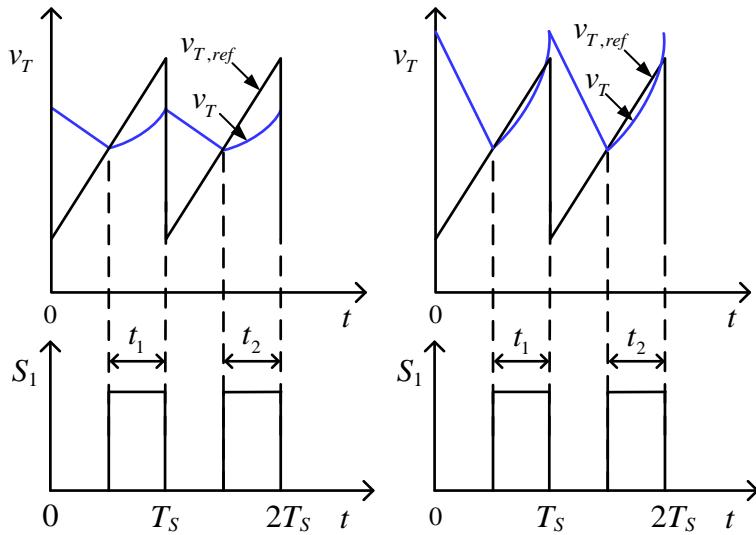


Fig. 2.4. Waveforms of in fixed-frequency operation.

2.3.2. Oscillation in the Input Current

The grid inductor L_g and grid-side capacitor (C_X and C_S) form a resonant path. High-frequency harmonics may enter this resonant path, causing input current oscillation. Based on the characteristics of the PSF, the PSF can be viewed as a controlled current source. Thus, combining the converter part in Fig. 2.1 as a current source of switching frequency and then a simplified oscillation circuit is derived, as shown in Fig. 2.5.

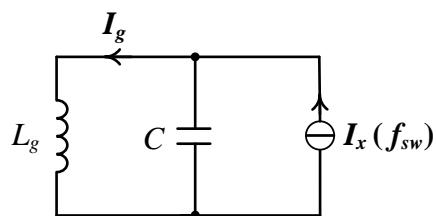


Fig. 2.5. Simplified circuit to describe interaction with the line.

The current through the grid inductance, I_g , is derived from current division between Z_{L_g} and Z_C .

$$I_g = I_x(f_{sw}) \cdot \frac{Z_C}{Z_{L_g} + Z_C} \quad (2.1)$$

where $Z_{L_g} = j\omega_{sw}L_g$, $Z_C = 1/(j\omega_{sw}C)$, and $C = C_X + C_S$.

I_g therefore can be expressed as

$$I_g = \frac{I_x(f_{sw})}{1 - \omega_{sw}^2 L_g C} \quad (2.2)$$

The partial derivate of I_g with respect to ω_{sw} is

$$\begin{aligned} \frac{\partial I_g}{\partial \omega_{sw}} &= \frac{2L_g C \omega_{sw}}{\left(1 - \omega_{sw}^2 L_g C\right)^2} I_x(f_{sw}) \\ &= \frac{2\omega_{sw}/\omega_{res}^2}{\left(1 - \omega_{sw}^2/\omega_{res}^2\right)^2} I_x(f_{sw}) \end{aligned} \quad (2.3)$$

where $\omega_{res} = 1/\sqrt{L_g C}$.

If the switching frequency changes by $\Delta\omega_{sw}$, the current variation ΔI_g is

$$\Delta I_g = \int_{\omega_{sw}}^{\omega_{sw} + \Delta\omega_{sw}} \frac{\partial I_g}{\partial \omega_{sw}} d\omega_{sw} \quad (2.4)$$

The per-unit value of ΔI_{g*} can be derived as

$$\Delta I_{g*} = \frac{\Delta I_g}{I_g} = \frac{\Delta\omega_{sw}^2 + 2\omega_{sw}\Delta\omega_{sw}}{\omega_{res}^2 - (\omega_{sw} + \Delta\omega_{sw})^2} \quad (2.5)$$

Rearranging (2.5) as

$$\Delta I_{g*} = \frac{\Delta\omega_{sw*}^2 + 2\Delta\omega_{sw*}}{\left(\frac{\omega_{res}}{\omega_{sw}}\right)^2 - (1 + \Delta\omega_{sw*})^2} \quad (2.6)$$

where $\Delta\omega_{sw*} = \Delta\omega_{sw}/\omega_{sw}$.

Based on (2.6), the relationship between ΔI_g^* and $\Delta\omega_{sw}^*$ is depicted in Fig. 2.6. The resonant frequency, ω_{res} , is dependent on the circuit parameters. In cases where ω_{res} is smaller than the switching frequency ω_{sw} , the current variation ΔI_g becomes greater along with the reduction of the switching frequency. If the switching frequency ω_{sw} is variable, input current oscillation will appear when ω_{sw} decreases to or close to the resonant frequency ω_{res} . Fixed-frequency dynamic ramp modulation proposed in this chapter can avoid this issue by operating the converter at a fixed switching frequency, and the switching frequency is set away from the grid-side resonant frequency.

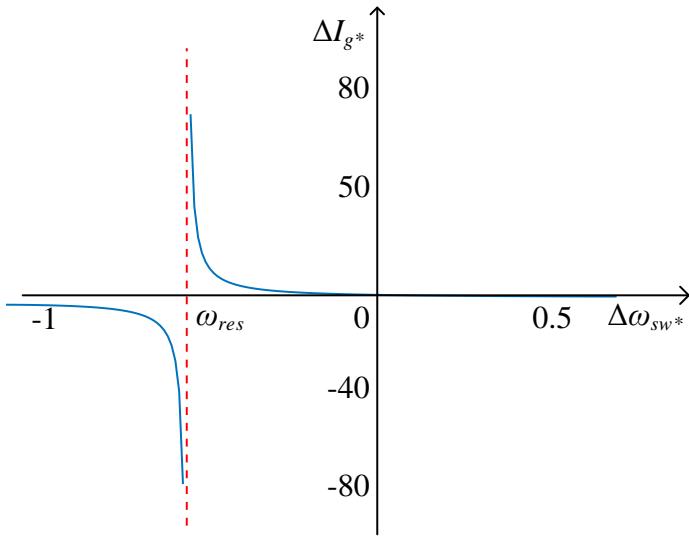


Fig. 2.6. Relationship between ΔI_g^* and $\Delta\omega_{sw}^*$.

2.3.3. Design Procedures of the Dynamic Ramp Modulator

The design procedures and considerations of the dynamic ramp modulator will be described as follows.

1) *Offset Voltage V_{offset}* : Once T_c enters its ohmic region, the current flowing through T_c varies drastically with the fluctuation of v_T . An offset voltage is necessary to avoid v_T from being smaller than the knee point between the saturation and ohmic region. The knee point depends on the type of SPD, and a smaller one is preferable because it means less power dissipation in the SPD. In this thesis, V_{offset} is set at 0.1V.

2) *Ramp Voltage V_{ramp}* : Compared with the hysteresis loop control, single threshold (peak- or valley-mode) control scheme may lose stability in the presence of perturbation. Stable operations can only be maintained when the duty cycle is greater than 0.5 for valley-voltage mode control.

When an artificial ramp is adopted, the above-mentioned unstable situation can be avoided over the whole range of duty cycle. As illustrated in Fig. 2.7, a perturbation $v_{T(0)}^*$ is introduced at the beginning of a switching period. The following equations can be derived.

$$v_{T(0)}^* = (m_a + m_2)\hat{d}T_S \quad (2.7)$$

$$v_{T(T_S)}^* = (m_1 - m_a)\hat{d}T_S \quad (2.8)$$

From (2.7) and (2.8), (2.9) can be derived.

$$v_{T(nT_S)}^* = v_{T(0)}^* \left(\frac{m_1 - m_a}{m_a + m_2} \right)^n \quad (2.9)$$

The relationship between $v_{T(nT_S)}^*$ and $v_{T(0)}^*$ is expressed as

$$v_{T(nT_S)}^* = v_{T(0)}^* \left(\frac{m_1 - m_a}{m_a + m_2} \right)^n = v_{T(0)}^* \alpha^n \quad (2.10)$$

where $\alpha = \frac{m_1 - m_a}{m_a + m_2}$.

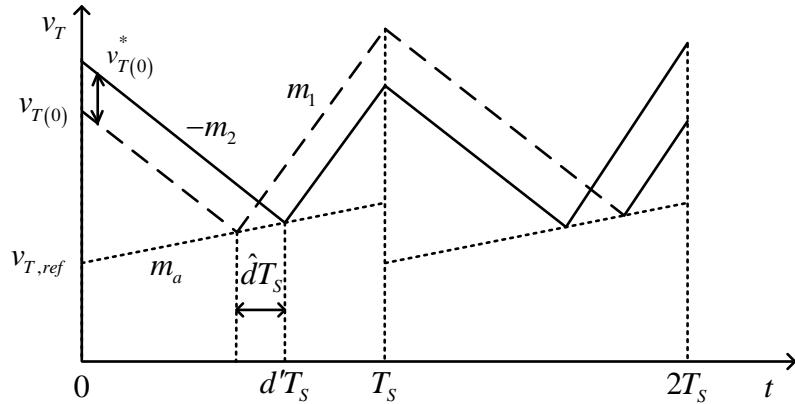


Fig. 2.7. Reference voltage with an artificial ramp.

The slope of the ramp m_a should satisfy the condition of

$$|\alpha| = \left| \frac{m_1 - m_a}{m_a + m_2} \right| < 1 \quad (2.11)$$

Therefore, the value range of m_a can be expressed as

$$m_a > \frac{1}{2}(m_1 - m_2) \quad (2.12)$$

v_T is equal to the difference between v_s and v_{in}

$$v_T = v_s - v_{in} \quad (2.13)$$

Since the switching frequency is much higher than the line frequency, v_s can be regarded as constant over a switching cycle. Thus, the fluctuation of v_T has the same magnitude but opposite phase as that of v_{in}

$$\Delta v_T = -\Delta v_{in} \quad (2.14)$$

The fluctuation in v_{in} is caused by the charging and discharging of the capacitor C_{in} , and the variation rate of v_{in} is related to i_{Cin} and C_{in} .

$$\frac{dv_{in}}{dt} = \frac{i_{C_{in}}}{C_{in}} \quad (2.15)$$

where i_{Cin} is the current flowing through the input capacitor.

During the turn-on time of switch S_I , capacitor C_{in} is discharged and $i_{C_{in}} = -(i_L - i_s)$. During turn-off, capacitor C_{in} is charged and $i_{Cin} = i_s$. Define the amplitude of dv_{in}/dt as the slope of v_T ; the rising slope m_1 and the falling slope m_2 can be expressed as

$$m_1 = \frac{i_L - i_s}{C_{in}} \quad (2.16)$$

$$m_2 = \frac{i_s}{C_{in}} \quad (2.17)$$

To ensure the modulator maintains stable at any condition, the ramp voltage V_{ramp} should satisfy the condition of

$$V_{ramp} > T_s \left[\frac{1}{2C_{in}} (i_L - 2i_s) \right]_{\max} \quad (2.18)$$

The simulated results show V_{ramp} varies from 1.26V to 2.36V for 90-264Vac input voltage by use of (2.18). V_{ramp} will be further processed by amplifiers with the supply voltage of 5V, for power loss reduction, which means that any ramp voltage less than 5V can be implemented. It gives designers the flexibility to increase the computed value when other disturbances exist or having stricter requirements on stability in the implementation. It will be explained that increasing V_{ramp} does not lead to more power dissipation due to the power loss reduction circuit below.

3) *Power Loss Reduction:* The waveform of v_T over two switching periods is illustrated in Fig. 2.8. The source current i_s is nearly constant during a switching period, denoted by I_s . The variation of v_T during a switching period can be expressed as

$$\Delta v_T = \int_0^{dT_S} m_2 dt = \int_0^{dT_S} \frac{i_s}{C_{in}} dt = \frac{I_s}{C_{in}} d'T_S \quad (2.19)$$

Hence, the upper and lower envelopes of v_T are expressed as

$$v_{T,upper} = V_{offset} + d'V_{ramp} + \Delta v_T \quad (2.20)$$

$$v_{T,lower} = V_{offset} + d'V_{ramp} \quad (2.21)$$

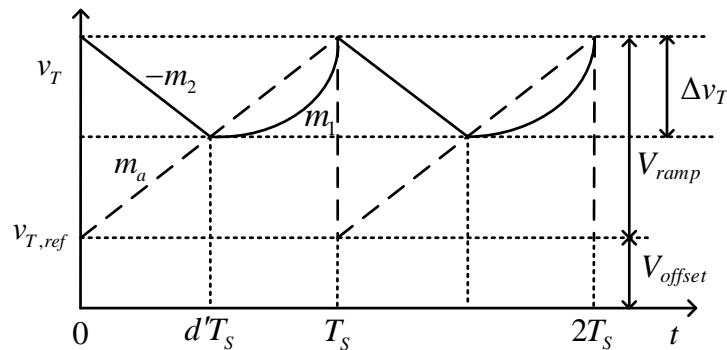


Fig. 2.8. The waveform of v_T over two switching cycles.

Based on (2.20) and (2.21), the waveform of v_T over a line cycle can be drawn in Fig. 2.9(a). If the constant ramp is subtracted by $d'V_{ramp}$, the valley voltage of v_T would be flattened by the dynamic ramp as shown in Fig. 2.9(b). The voltage stress in v_T during zero-crossing is not due to modulation; it is caused by the rising slew rate of v_{in} is smaller than that of v_s during zero-crossing. The voltage difference between v_s and v_{in} is thereby built in v_T .

In continuous conduction mode (CCM), the duty cycle d of buck-boost converters is

$$d = \frac{v_o}{v_{in} + v_o} \quad (2.22)$$

Hence, $d'V_{ramp}$ can be derived as

$$d'V_{ramp} = \frac{v_{in}}{v_{in} + v_o} V_{ramp} \quad (2.23)$$

A microcontroller, STM32F334C8Tx, with a floating-point unit (FPU), is adopted to process the floating-point division. The power loss reduction circuit is illustrated in Fig. 2.10.

Subtracting $d'V_{ramp}$ from $v_{T,ref}$, the average voltage across the SPD will be decreased so that the power loss reduction can be achieved.

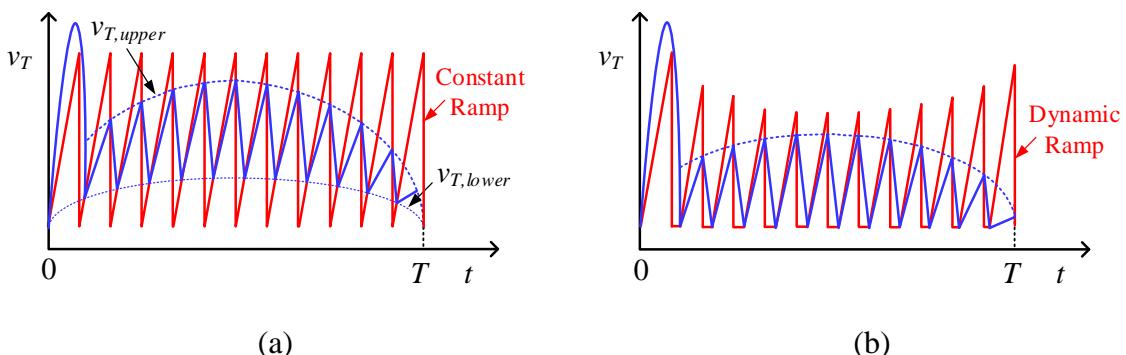


Fig. 2.9. The simplified waveform of v_T over a line cycle. (a) Without power loss reduction. (b) With power loss reduction.

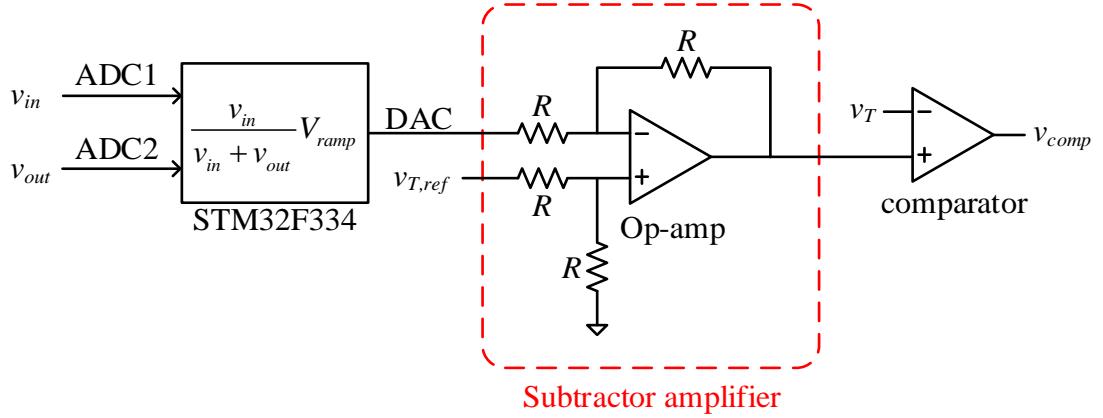


Fig. 2.10. Power loss reduction circuit.

The buck-boost converter may enter the discontinuous conduction mode (DCM) under light load conditions. The duty cycle in DCM, d_{DCM} , is [70]

$$d_{DCM} = \frac{v_o}{v_{in}} \sqrt{\frac{2L}{RT_s}} \quad (2.24)$$

where $L = 200\mu\text{H}$, $R = 400\Omega$, and $T_s = 5\mu\text{s}$.

Based on these parameters, the following inequality can be obtained.

$$d'_{DCM} = 1 - \frac{v_o}{v_{in}} \sqrt{\frac{2L}{RT_s}} > 1 - \frac{v_o}{v_{in} + v_{in}} > d' \quad (2.25)$$

Based on (2.25), the power loss reduction under DCM conditions is not optimized, whereas experimental results show that the prototype can operate without stability issues. The prototype is most often working in rated power condition (CCM); the power loss reduction is therefore optimized during majority working time.

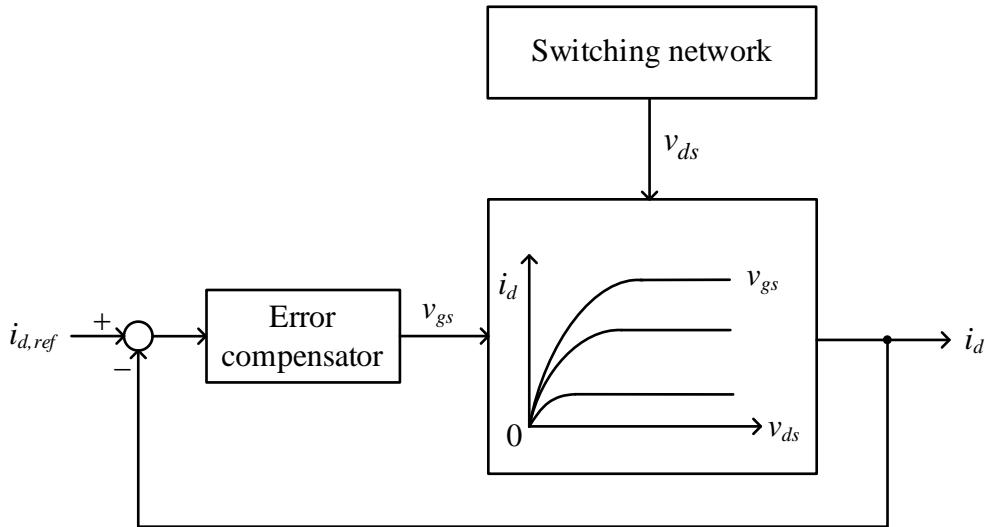
2.4. Analysis of the Fast-Current Regulation Circuit

MOSFET can be viewed as a double-input-single-output nonlinear network. Gate-source voltage v_{gs} and drain-source voltage v_{ds} regulate the drain current i_d flowing through the MOSFET. As discussed in Section 2.3, v_{ds} is determined by the modulator, v_{gs} is the only controllable variable to regulate i_d . Fig. 2.11 (a) illustrates the mechanism of i_d controlled by v_{gs} and v_{ds} .

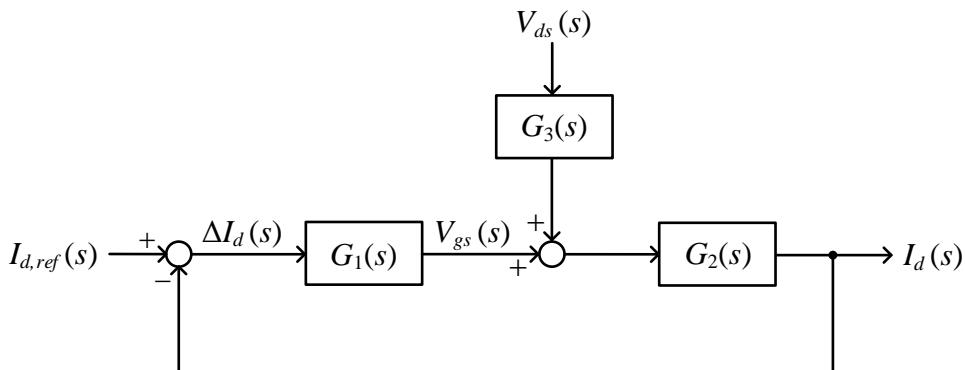
The control block diagram of the fast-current regulation circuit is shown in Fig. 2.11 (b). $G_1(s)$ and $G_2(s)$ are the transfer functions of the error compensation circuit and SPD MOSFET V-I characteristics, respectively. For the sake of simplicity, $G_3(s)$ is introduced to combine the two control variations into a single control signal.

Based on the superposition theorem, firstly let $V_{ds}(s) = 0$, the closed-loop transfer function $G_{gs}(s)$ is

$$G_{gs}(s) = \frac{I_d(s)}{I_{d,ref}(s)} = \frac{G_1(s)G_2(s)}{1 + G_1(s)G_2(s)} \quad (2.26)$$



(a)



(b)

Fig. 2.11. Fast-current regulation circuit. (a) Time-domain model. (b) Control block diagram of the fast-current regulation circuit.

Then, let $I_{d,ref}(s) = 0$, the closed-loop transfer function $G_{ds}(s)$ can be expressed as

$$G_{ds}(s) = \frac{I_d(s)}{V_{ds}(s)} = \frac{G_3(s)G_2(s)}{1+G_1(s)G_2(s)} \quad (2.27)$$

Summing up both inputs of the control block diagram, the total drain current $\sum I_d(s)$ is obtained,

$$\sum I_d(s) = G_{gs}(s)I_{d,ref}(s) + G_{ds}(s)V_{ds}(s) \quad (2.28)$$

$$\sum I_d(s) = \frac{G_1(s)G_2(s)}{1+G_1(s)G_2(s)}I_{d,ref}(s) + \frac{G_3(s)G_2(s)}{1+G_1(s)G_2(s)}V_{ds}(s) \quad (2.29)$$

Considering $G_1(s)G_2(s) \gg 1$ and $G_1(s) \gg G_3(s)$

$$G_{ds}(s)V_{ds}(s) \approx 0 \quad (2.30)$$

$$\sum I_d(s) \approx I_{d,ref}(s) \quad (2.31)$$

Due to the fluctuations of v_{ds} , v_{gs} , and i_d are in a similar magnitude range, $G_2(s)$ and $G_3(s)$ are sufficiently smaller in magnitude than $G_1(s)$. Hence, assumptions $G_1(s)G_2(s) \gg 1$ and $G_1(s) \gg G_3(s)$ can be easily satisfied by the design of $G_1(s)$ with high loop gain.

Above analysis explains why the proposed fast-current regulation circuit can suppress EMI noise and how to realize good suppression of EMI noise. Pursing high loop gains within the frequencies of interest with stability consideration, therefore, is of great importance to achieve good current regulation performance.

2.4.1. Optimization of the Fast-Current Regulation Circuit

The fast-current regulation circuit is designed to diminish error between drain current i_d and reference $i_{d,ref}$. Type-I, Type-II, and Type-III error compensators are available to this application [71]. The slope of the EMI spectrum of switching waveform is approximate -20dB/decade [2], [72]. To ensure stability, the open-loop gain of the fast-current regulation circuit should cross the 0-dB axis with the attention of -20dB/decade [73]. As shown in Fig. 2.12, within the conducted EMI frequency range, i.e., from 150kHz to 30MHz, the loop gain should decrease with a slope of -20dB/decade to maintain

stability and obtain maximum loop gain. Besides, the fast-current regulation circuit also performs PFC and thereby high loop gain at power line frequency is required. Hence, Type-I compensator is the most suitable circuit to filter out EMI noise with the least components cost.

In order to suppress higher EMI noise in fixed-frequency operation, the fast-current regulation circuit proposed in [48] is optimized. Such optimized fast-current regulation circuit has solved two issues in [48]: redundant gain stage design and inadequate capacitive load driving capability. This improvement is realized with considerations of the characteristics of the wideband amplifier in EMI suppression application. The diagram of the optimized closed-loop fast-current regulation circuit is shown in Fig. 2.13.

In [48], the gain stage of the fast-current regulation circuit consists of a pre-amplifier and a high-gain Type-I error amplifier. In addition to providing gain, the pre-amplifier, amplifying v_{Rs} by 10 times, is also used to decrease the effect of the microcontroller output offset on the current regulation. The pre-amplifier provides much smaller gain than the error amplifier; however, it introduces -90° phase shift that reduces phase margin.

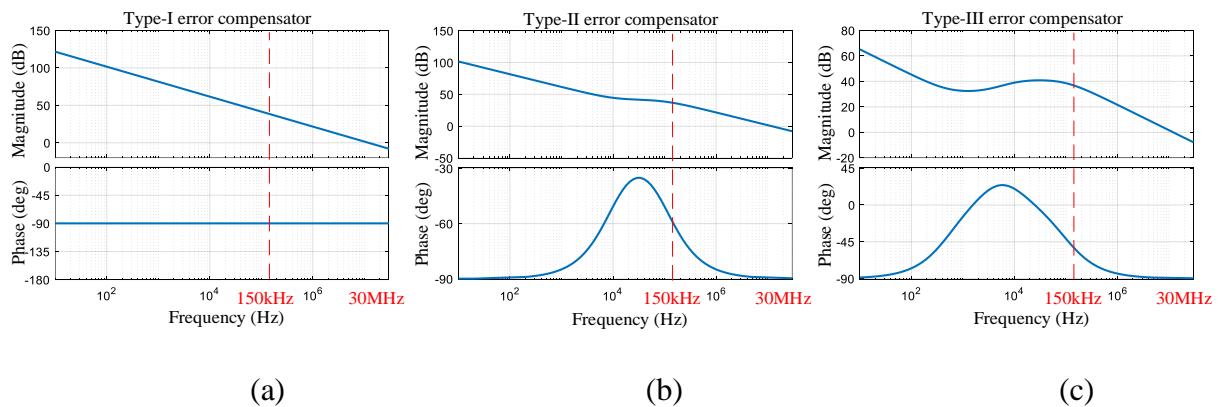


Fig. 2.12. Frequency response of three kinds of error compensators. (a) Type-I error compensator. (b) Type-II error compensator. (c) Type-III error compensator.

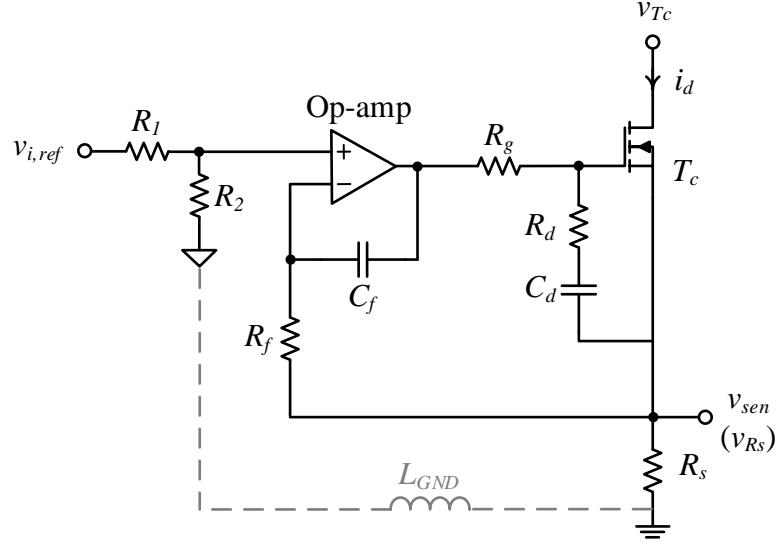


Fig. 2.13. Optimized closed-loop fast-current regulation circuit.

In this chapter, removing the pre-amplifier and using smaller values of feedback parameters (R_f and C_f), higher open-loop gain is obtained with a simpler structure. Since the wideband amplifiers dominate the overall cost, the cost of the fast-current regulation circuit, therefore, is halved.

Due to the very high gain-bandwidth-product, wideband amplifiers have smaller capacitive load driving capability compared with its low-frequency counterparts. Amplifier output ringing will appear when the capacitive load is more than 5pF [74]; however, the input capacitance of T_c is larger than 300pF [50]. An RC damping circuit, constructed by R_d and C_d , is used to mitigate the ringing. This mechanism is explained as follows.

The open-loop gain of the Type-I compensator will cross the 0-dB axis with a slope of -20dB/decade and sufficient phase margin. However, the input capacitance of T_c and the output impedance of the amplifier introduce a pole below the crossover frequency of the current regulation circuit. This additional pole makes the open-loop gain cross the 0-dB axis with a slope of -40dB/decade and phase drop drastically, which converts the system into a second-order one. The step response will then exhibit considerable overshoot and ringing with a small phase margin.

The proposed RC damping circuit provides phase lag compensation. It splits the pole caused by the input capacitance of T_c into a low-frequency pole below crossover frequency and a high-frequency pole that is beyond the crossover and thus has no adverse effect. It also introduces a zero close to the low-frequency pole. This zero cancels the low-frequency pole, which significantly suppresses the overshoot and ringing. Hence, this RC damping circuit is crucial for the design of the fast-current regulation circuit; it advances the capacitive load driving capability of the wideband amplifier.

2.4.2. Stability Analysis of the Fast-Current Regulation Circuit

The small-signal model of the optimized fast-current regulation circuit is illustrated in Fig. 2.14, and the circuit parameters are shown in Table 2.2. The parameters of the operational amplifier and SPD MOSFET are derived from datasheets and measurements. The input impedance of the amplifier Z_i is modeled as a $100\text{ k}\Omega$ resistor in parallel with a 0.1 pF capacitor; the open-loop output impedance $Z_{o,ol}$ is modeled as a 280Ω resistor in parallel with an RC branch, where $R = 20\Omega$ and $C = 26\text{nF}$.

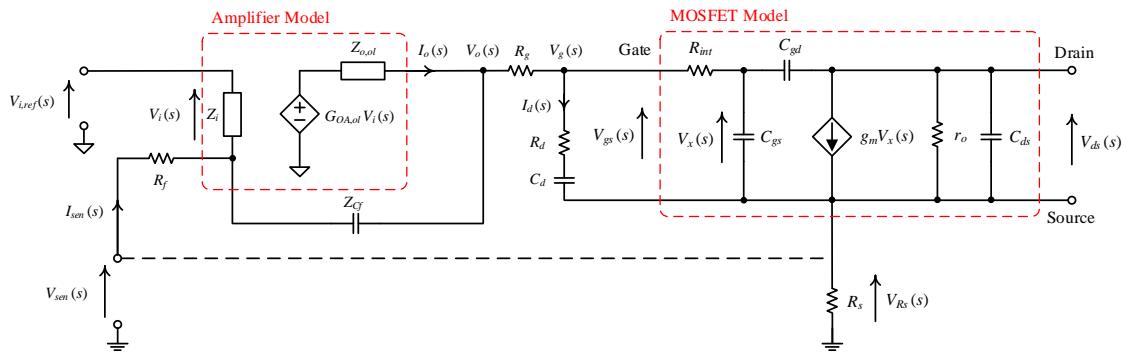


Fig. 2.14. The small-signal model of the optimized fast-current regulation circuit.

Table 2.2
PARAMETERS OF THE OPTIMIZED FAST-CURRENT REGULATION CIRCUIT

Components	Value	Components	Value
R_1	10kΩ	R_2	1kΩ
R_s	0.1Ω	R_g	15Ω
R_f	2Ω	C_f	330pF
R_d	5Ω	C_d	10nF
R_{int}	1.85Ω	C_{gs}	289.7pF
C_{gd}	131pF	C_{ds}	108.8pF
g_m	3.97	r_o	15.56Ω

To derive the input-output relationship of $V_{Rs}(s)$ and $V_{sen}(s)$, set $V_{i,ref}(s)$ and $V_{ds}(s)$ to zero by applying the superposition theorem as follows,

$$I_{sen}(s) = \frac{V_{sen}(s) + V_i(s)}{R_f} \quad (2.32)$$

$$V_o(s) = -V_i(s) - I_{sen}(s)Z_{C_f} \quad (2.33)$$

$$I_o(s) = \frac{G_{OA,ol}(s)V_i(s) - V_o(s)}{Z_{o,ol}} \quad (2.34)$$

$$V_g(s) = V_o(s) - (I_{sen}(s) + I_o(s))R_g \quad (2.35)$$

$$I_d(s) = \frac{V_g(s) - V_{Rs}(s)}{Z_d} \quad (2.36)$$

$$V_g(s) = (I_{sen}(s) + I_o(s) - I_d(s))R_{int} + V_x(s) + V_{Rs}(s) \quad (2.37)$$

$$I_{sen}(s) + I_o(s) - I_d(s) = \frac{V_x(s)}{Z_{C_{iss}}} \quad (2.38)$$

$$V_{Rs}(s) = R_s \left(g_m V_x(s) + \frac{V_x(s)}{Z_{C_{iss}}} + I_d(s) \right) \quad (2.39)$$

where $Z_{C_f} = \frac{1}{sC_f}$, $Z_d = R_d + \frac{1}{sC_d}$, and $Z_{C_{iss}} = \frac{1}{s(C_{gs} + C_{gd})}$.

The open-loop transfer function $G_{OL}(s)$ can be derived by using (2.32) to (2.39)

$$G_{OL}(s) = \frac{V_{Rs}(s)}{V_{sen}(s)} = \frac{R_s m_1(s) (G_{OA,ol}(s) Z_{C_f} - Z_o)}{Z_{C_f} m_2(s) + Z_o m_3(s) + R_f m_4(s)} \quad (2.40)$$

where

$$m_1(s) = R_{int} + Z_d + Z_{C_{iss}} (1 + g_m Z_d) \quad (2.41)$$

$$m_2(s) = m_5(s) + m_6(s) Z_d \quad (2.42)$$

$$m_3(s) = (R_g + R_s + Z_{C_f})(R_{int} + Z_{C_{iss}}) + (m_6(s) + Z_{C_f}) Z_d \quad (2.43)$$

$$m_4(s) = (1 + G_{OA,ol}(s)) (m_5(s) + m_6(s) Z_d) + m_7(s) Z_o \quad (2.44)$$

$$m_5 = (R_g + R_s)(R_{int} + Z_{C_{iss}}) \quad (2.45)$$

$$m_6(s) = R_g + R_{int} + R_s + Z_{C_{iss}} + g_m R_s Z_{C_{iss}} \quad (2.46)$$

$$m_7(s) = (R_{int} + Z_{C_{iss}} + Z_d) Z_o \quad (2.47)$$

The frequency response of the open-loop gain $G_{OL}(s)$ with and without the RC damping circuit is shown in Fig. 2.15. As analyzed in Section 2.4.1, without the RC damping circuit, a pole occurs below the crossover frequency, further adding a slope of -20dB/decade and -90° phase shift. The RC damping circuit provides phase lag compensation, making the open-loop gain cross the 0-dB axis with a slope of -20dB/decade; it slightly decreases the open-loop gain but significantly improves the phase margin. The overshoot and ringing on v_{gs} , therefore, is mitigated. The crossover frequency and phase margin of the optimized fast-current regulation circuit with the RC damping circuit is 12.8MHz and 69.8° , respectively. The stability and EMI suppression capability of the fast-current regulation circuit are both improved.

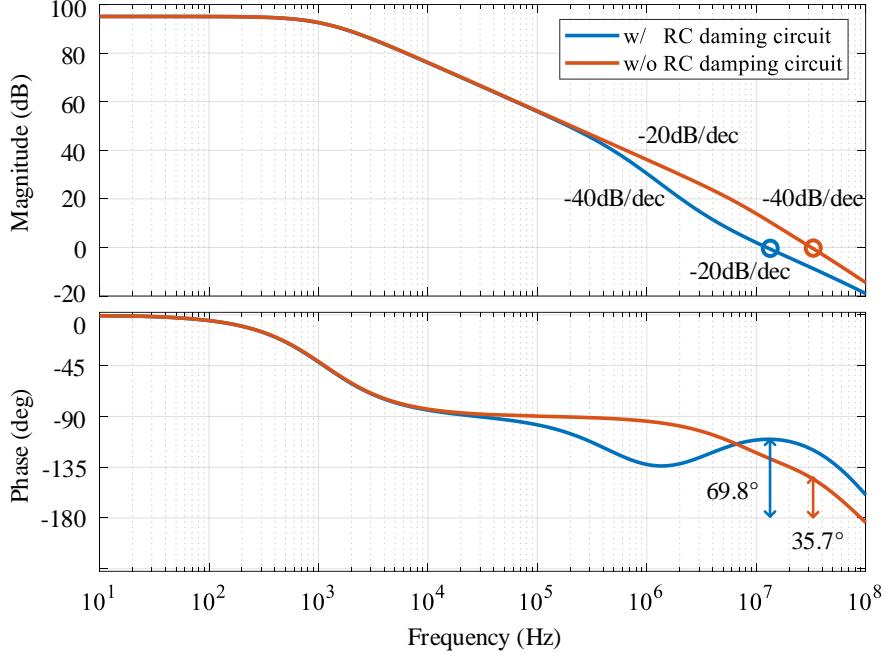


Fig. 2.15. Frequency response of the optimized fast-current regulation circuit.

2.4.3. Analysis and Prediction of EMI Suppression Performance

To achieve good EMI suppression, the current regulation circuit should have fast dynamic response. The PSF is a controlled current source; its EMI suppression performance is quantified by the capability of tracking high-frequency signals.

Combining $G_1(s)$ and $G_2(s)$ as $G_{OL}(s)$, which is calculated in Section 2.4.2, a simplified control block diagram of the fast-current regulation circuit is shown in Fig. 2.16. $R(s)$, $C(s)$, and $E(s)$ denotes the input, output, and error signal, respectively.

The error transfer function $\Phi_e(s)$ is

$$\Phi_e(s) = \frac{E(s)}{R(s)} = \frac{1}{1 + G_{OL}(s)} \quad (2.48)$$

Using a high-frequency signal $r(t) = A\sin(2\pi ft)$ as the input signal, and taking Laplace transformation of $r(t)$

$$R(s) = \frac{2\pi Af}{s^2 + 4\pi^2 f^2} \quad (2.49)$$

where A is the magnitude and f is the frequency of the input signal.

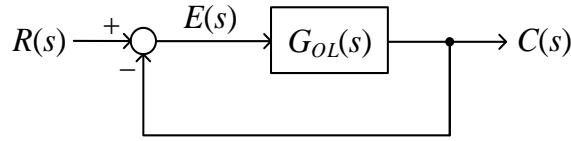


Fig. 2.16. Simplified control block diagram of the optimized fast-current regulation circuit.

$$E(s) = \Phi_e(s)R(s) \quad (2.50)$$

$$E(s) = \frac{1}{1 + G_{OL}(s)} \cdot \frac{2\pi Af}{s^2 + 4\pi^2 f^2} \quad (2.51)$$

The steady-state error signal in time domain, $e_{ss}(t)$, can be derived by taking inverse Laplace transformation of $E(s)$ as

$$e_{ss}(t) = \frac{1}{2\pi j} \int_{\beta-j\infty}^{\beta+j\infty} E(s)e^{st} ds \quad (2.52)$$

EMI noise reduction ratio k can be expressed as the ratio of the amplitude of the error signal, $e_{ss}(t)$, and the input signal, $r(t)$, in logarithmic scale as

$$k = 20 \log \left(\frac{|e_{ss}(t)|_{\max}}{A} \right) \quad (2.53)$$

Based on (2.53), for a given frequency, the EMI noise reduction ratio k is determined by the feedback parameters of the error compensator, i.e., R_f and C_f . This relationship at the fundamental switching frequency is illustrated in Fig. 2.17. According to (2.40), too large open-loop gain would lead to instability. Within satisfaction of stability requirements, the value of $1/(R_f C_f)$ can be increased in order to achieve higher open-loop gain and better EMI suppression performance. When the feedback parameters are determined, the EMI noise suppression capability of the PSF can be calculated from (2.53) by sweeping frequency from 150kHz to 30MHz. The proposed EMI suppression capability prediction method facilitates the analysis and design of the fast-current regulation circuit.

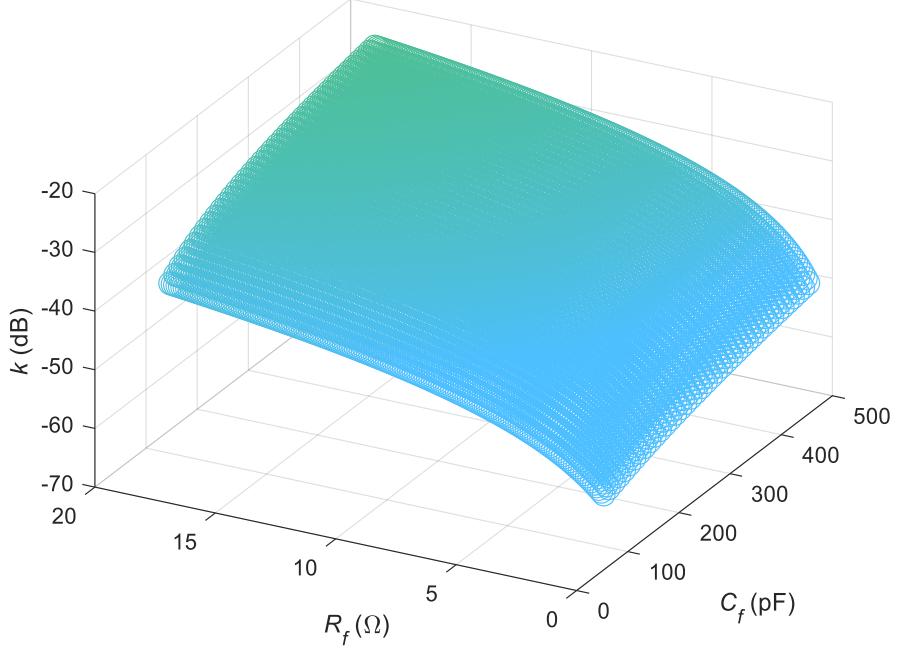


Fig. 2.17. EMI noise reduction ratio k as a function of C_f and R_f .

Under the condition of 115Vdc and 100W rated power, the PSF is removed, and the prototype is operated at fixed duty cycle condition for comparison. The measured peak DM EMI noise levels of the prototype with and without the PSF are shown in Fig. 2.18(a). The computed and measured EMI noise reduction are plotted versus frequency, given $R_f = 2\Omega$ and $C_f = 330\text{pF}$, as shown in Fig. 2.18(b). Affected by parasitic parameters in implementation, the computed and measured results share similar envelope.

The open-loop gain of the fast-current regulation circuit consists of the gain of the amplifier stage and the SPD MOSFET stage. In order to obtain insight and intuition into (2.40), the open-loop gain of the fast-current regulation circuit can be regarded as is controlled and dominated by the amplifier stage. The open-loop gain of the Type-I error amplifier is approximately equal to $1/(sR_fC_f)$. Taking the ten times gain pre-amplifier in [48] into account, the open-loop gain in this thesis is enlarged by $[1/(2\Omega \cdot 330\text{pF})]/[10/(109\Omega \cdot 220\text{pF})]$, which is 11.2dB. Besides, the phase margin is improved by the RC damping circuit. It should be expected to perform better EMI suppression.

To verify the advantage of the single-stage amplifier with the RC damping circuit over two-stage amplifiers, the variable-frequency modulator of the prototype in [48] is disabled and replaced by the fixed-frequency modulator as proposed in this chapter. Using the same values of input-side capacitances, a comparison has been done under the condition of 115Vdc and 100W rated power. 15.3dB DM noise reduction is observed at the fundamental switching frequency, as shown in Fig. 2.19. Since the RC damping circuit mitigates overshoot and ringing, an average of 9.83dB noise reduction in the high-frequency range (5M-30MHz) also has been achieved.

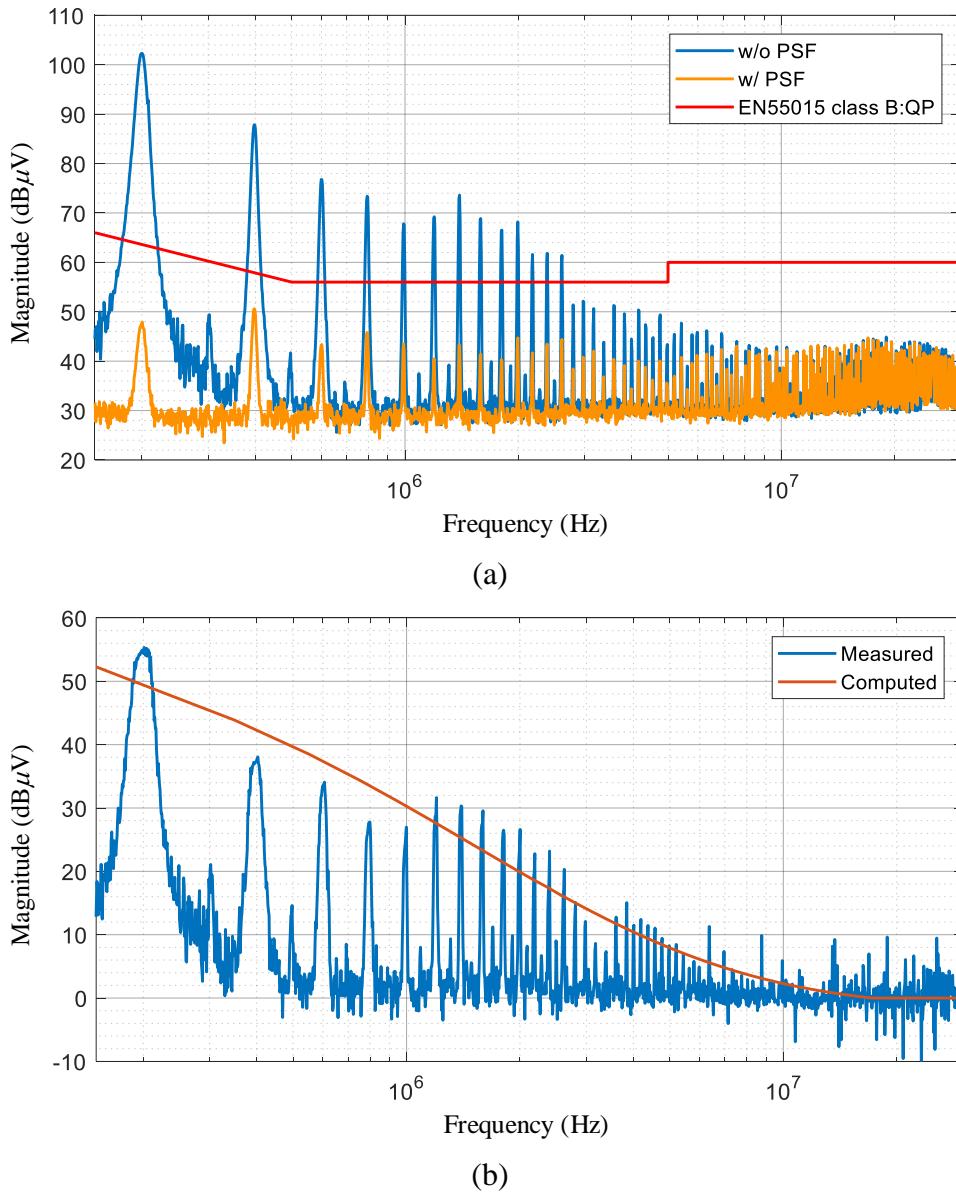


Fig. 2.18. EMI noise reduction. (a) Measured peak DM EMI noise with and without the PSF. (b) Measured and computed noise reduction by using the PSF.

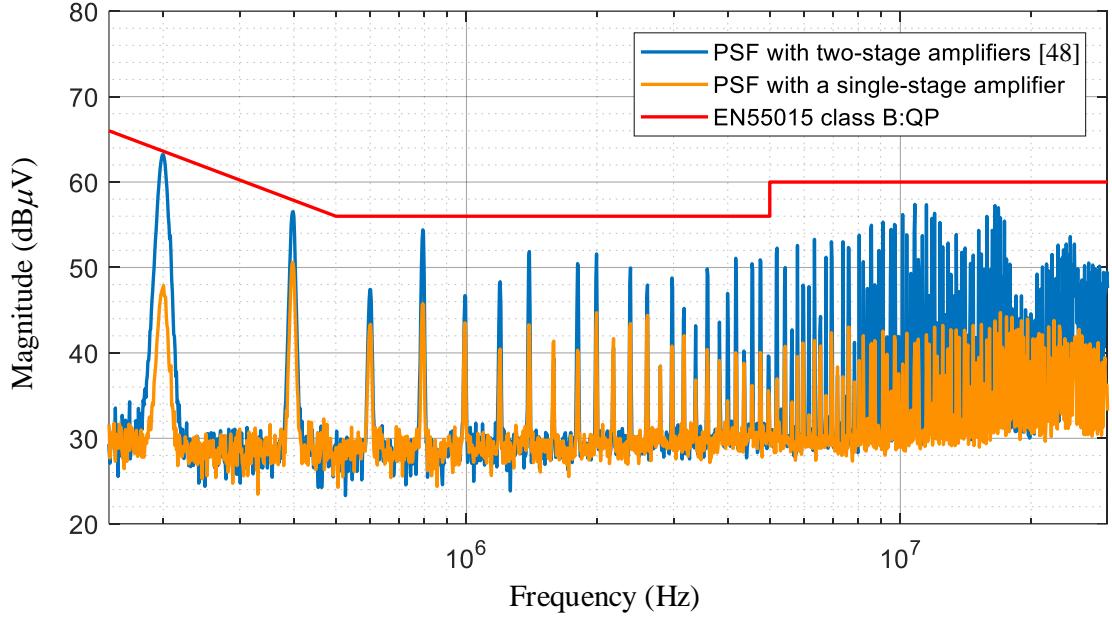


Fig. 2.19. Comparison of measured peak DM EMI noise.

2.4.4. Effect of the Ground Loop Inductance

In practice, the control ground is usually connected to the power ground by a zero-ohm resistor. Although the error amplifier is immediately grounded to the control ground, it may take a long way for the amplifier ground pin to find the power ground. Hence, an inductance L_{GND} exists in the ground loop between the control ground and the power ground, as illustrated in Fig. 2.13.

The working principle of the fast-current regulation circuit, as illustrated in Fig. 2.13, is based on sensing the voltage across R_s , v_{Rs} , and comparing v_{Rs} with the reference $v_{i,ref}$. When v_{Rs} is regulated to exactly follow $v_{i,ref}$, the current flowing through R_s is rectified sinusoid, with all high-frequency noise suppressed. However, the ground loop inductance makes the ground of the amplifier floating from the ground of R_s . Thus, it distorts the reference $v_{i,ref}$, resulting in inaccurate current regulation. The impedance of several tens of nH inductance is comparable with and even much larger than the 0.1Ω sensing resistance in the conducted EMI frequency range. Thus, the ground loop inductance can significantly degrade the performance of the current regulation circuit. Mathematical analysis and experimental verification will be given as follows.

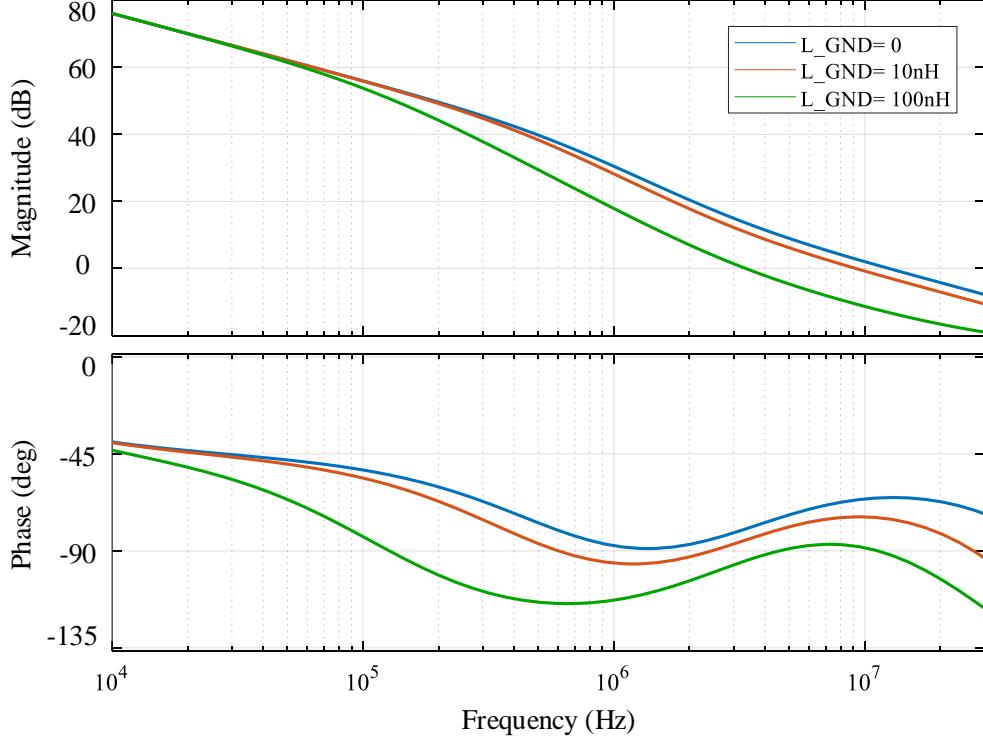


Fig. 2.20. Frequency response of the optimized fast-current regulation circuit with different values of ground loop inductances.

Consider the potential difference between the control ground v_{AGND} and the power ground v_{PGND} , with all voltages referenced to the power ground, (2.32)-(2.34) should be revised as follows.

$$I_{sen}(s) = \frac{V_{sen}(s) - (V_{AGND}(s) - V_i(s))}{R_f} \quad (2.54)$$

$$V_o(s) = V_{AGND}(s) - V_i(s) - I_{sen}(s)Z_{C_f} \quad (2.55)$$

$$I_o(s) = \frac{V_{AGND}(s) + G_{OA,ol}(s)V_i(s) - V_o(s)}{Z_{o,ol}} \quad (2.56)$$

$$V_{AGND}(s) = -Z_{GND}I_o(s) \quad (2.57)$$

where $Z_{GND} = sL_{GND}$.

Recalculate the open-loop gain $G_{OL}(s)$ using the method introduced in Section 2.4.2 with (2.32)-(2.34) replaced by (2.54)-(2.57). The frequency response of $G_{OL}(s)$ with

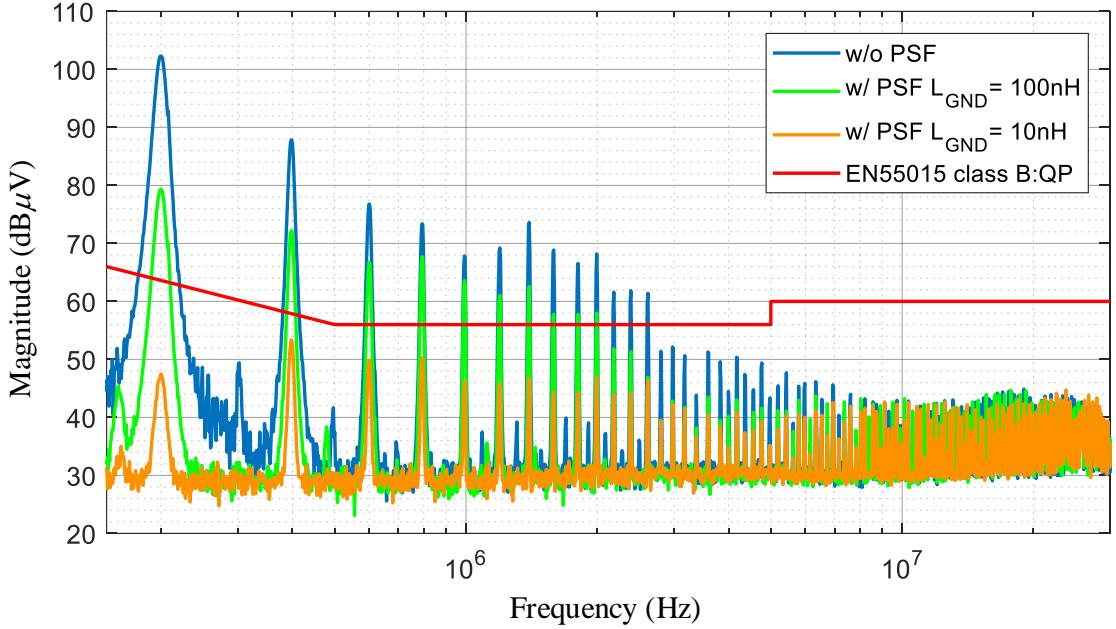


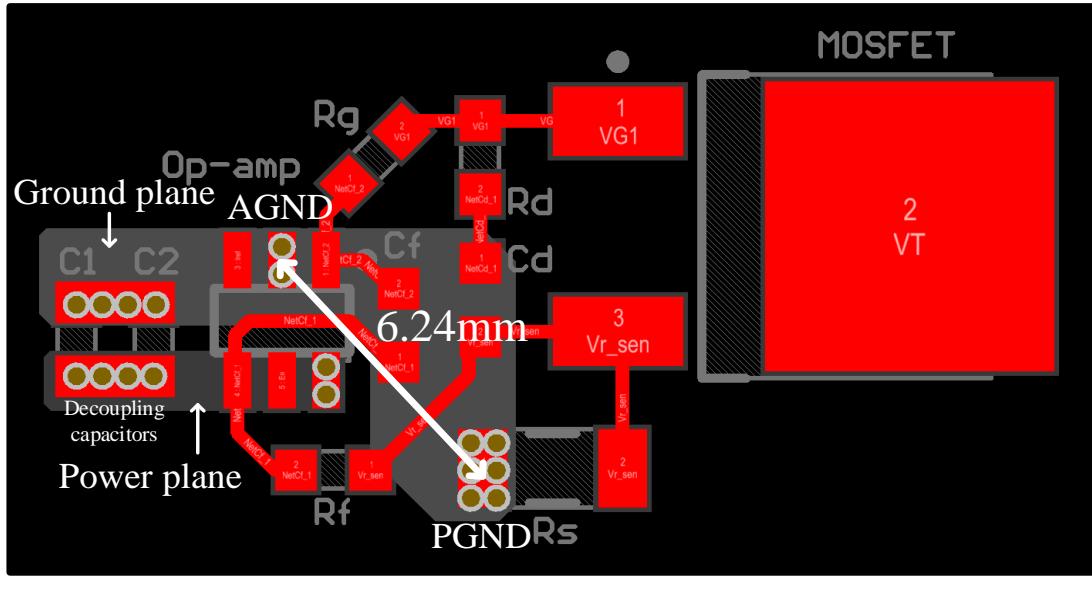
Fig. 2.21. Peak DM EMI noise level of the prototype with different ground loop inductances.

different values of ground loop inductance, as shown in Fig. 2.20, explains the reason for the above mentioned EMI suppression degradation from the perspective of control theory. It can be seen that the open-loop gain and phase margin of the fast-current regulation circuit decrease with the increase of ground loop inductance. If the ground loop inductance is smaller than 10nH, this effect is not significant. However, the open-loop gain and phase margin would be severely impaired by a substantial ground loop inductance; it limits the EMI suppression capability of the PSF.

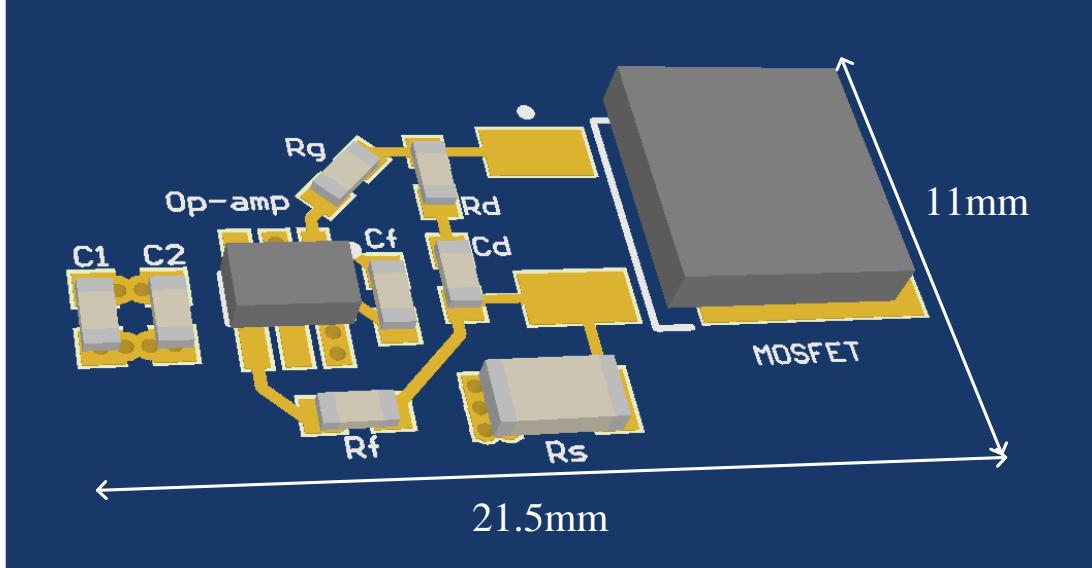
Under the condition of 115Vdc and 100W rated power, the measured DM EMI noise of the prototype with different ground loop inductances, i.e., 10nH, and 100nH, are shown in Fig. 2.21, compared with the results of removing the PSF.

Based on the approximation equation provide in [73], 10nH is equivalent to the inductance of a 15mm long, 1mm wide PCB trace. The package sizes of the error amplifier, MOSFET, and sensing resistor are space-saving; the ground loop inductance restriction in the single-stage amplifier configuration, compared with that in the two-stage amplifiers structure in [48], can be more conveniently satisfied with the aware of

grounding issue. A recommended PCB layout solution is illustrated in Fig. 2.22. The control ground is connected to the power ground through a copper plate via through holes. One through-hole only contributes 1nH inductance; the total ground loop inductance, therefore, is sufficiently smaller than 10nH. A remedial way for a fabricated PCB is just connecting the control ground with the power ground through a litz wire.



(a)

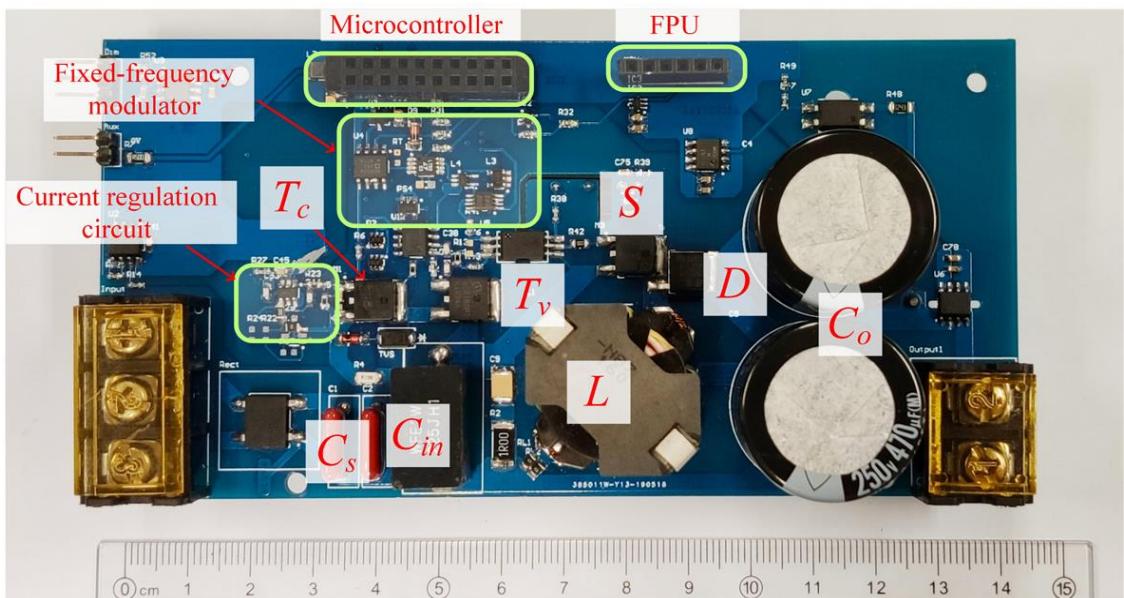


(b)

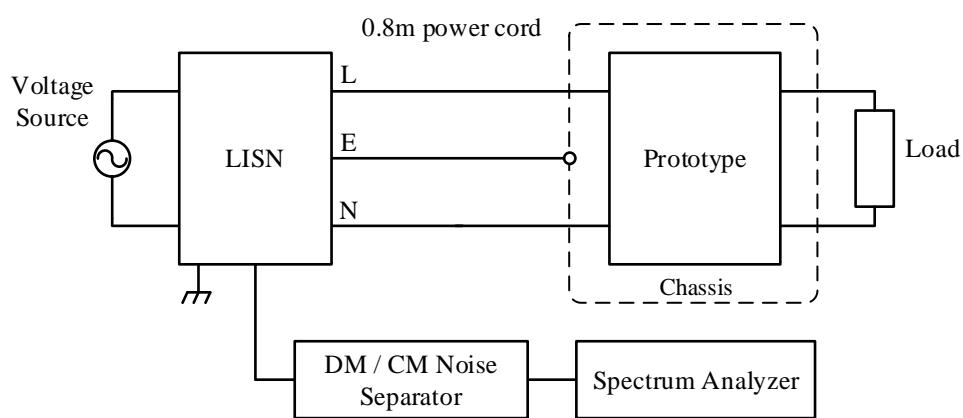
Fig. 2.22. A recommended PCB layout of the optimized fast-current regulation circuit. (a) 2-D view. (b) 3-D view.

2.5. Experimental Verification

A 100W, 90-264Vac / 200Vdc buck-boost converter prototype has been built to evaluate the EMI suppression performance. The photo of the prototype is shown in Fig. 2.23(a); EMI measurement equipment and connections are illustrated in Fig. 2.23(b). The values and part numbers of the components are tabulated in Table 2.3.



(a)



(b)

Fig. 2.23. Setup for testing EMI Performance. (a) Prototype buck-boost converter with the PSF. (b) Equipment and connections.

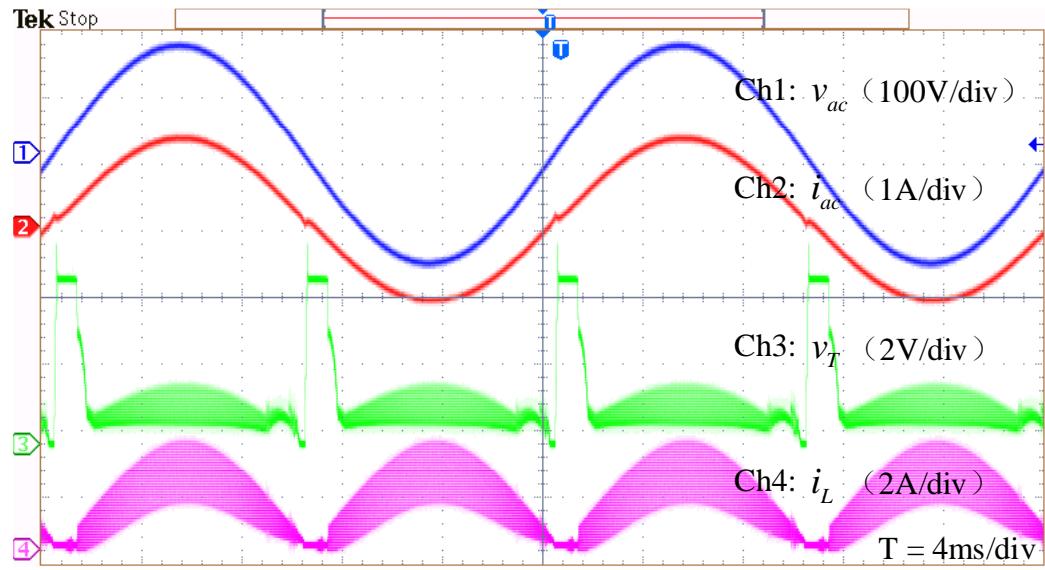
TABLE 2.3
COMPONENTS USED IN THE PROTOTYPE

Components	Value/ Part No.	Components	Value/ Part No.
C_x	220nF	T_1	STD19N3LLH6AG
C_s	200nF	T_2	IPD60R180P7
C_{in}	2.2μF	S_1	STD8N80K5
C_o	942μF	S_2	STPSC2H12
L	200μH	Op-amp	LTC6268-10

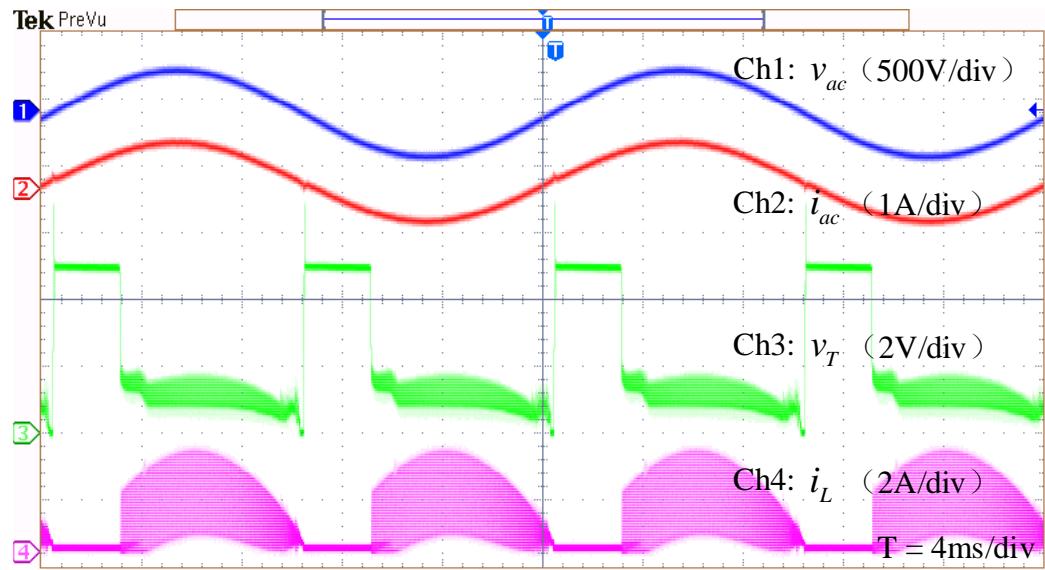
The waveforms of input voltage v_{ac} , input current i_{ac} , the voltage across the PSF v_T , and the inductor current i_L of the prototype under light- and high-line conditions, i.e., 115Vac and 230Vac, are shown in Fig. 2.24.

As illustrated in Fig. 2.25(a), unwanted oscillations appear in the input current when a variable-frequency modulator is adopted. The input current oscillation is mitigated using the fixed-frequency dynamic ramp modulator, which is shown in Fig. 2.25(b).

The power losses of switch S_1 and inductor L are highly dependent on the switching frequency. Since the switching frequency of the prototype in [48] is variable, a fair efficiency comparison of the prototypes cannot be obtained. Many techniques can be used to decrease the power loss of switching converters; however, these techniques are out of the scope of this chapter. This chapter is focused on reducing the power loss in the SPD. Compared with [48], 48.1% and 19.6% reduction of power dissipation in the SPD has been achieved by the dynamic ramp modulation under full rated power, low-line and high-line conditions, respectively. Fig. 2.26 shows comparisons of the power dissipation of the SPD under different input voltage and loading conditions.

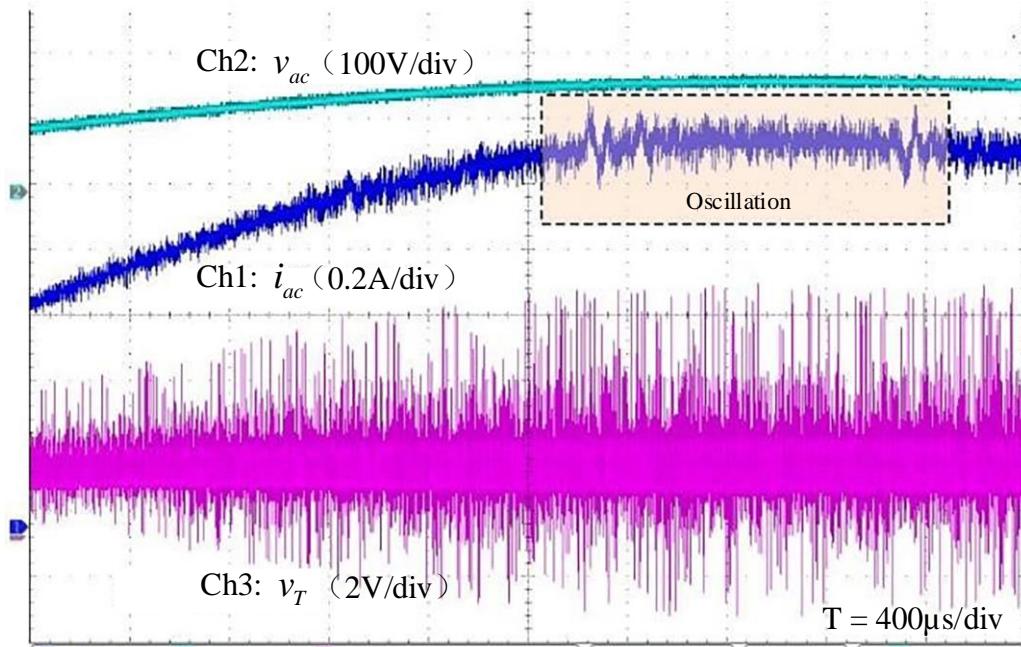


(a)

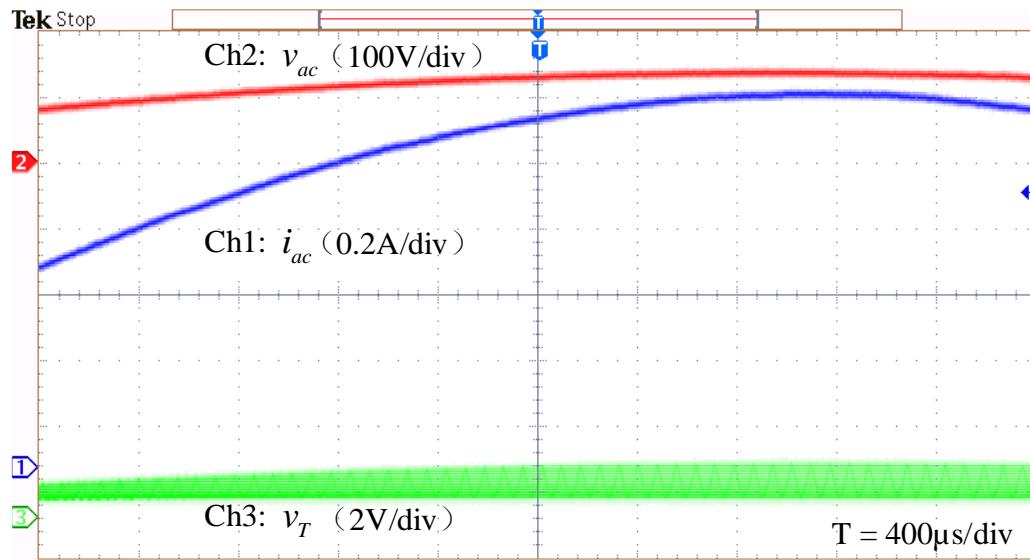


(b)

Fig. 2.24. Waveforms of the prototype under light- and high-line conditions.
 (a) $V_s = 115\text{V}$, rated 100W power. (b) $V_s = 230\text{V}$, rated 100W power.



(a)



(b)

Fig. 2.25. Comparisons between the variable-frequency operation and fixed-frequency operation. (a) Variable-frequency. (b) Fixed-frequency.

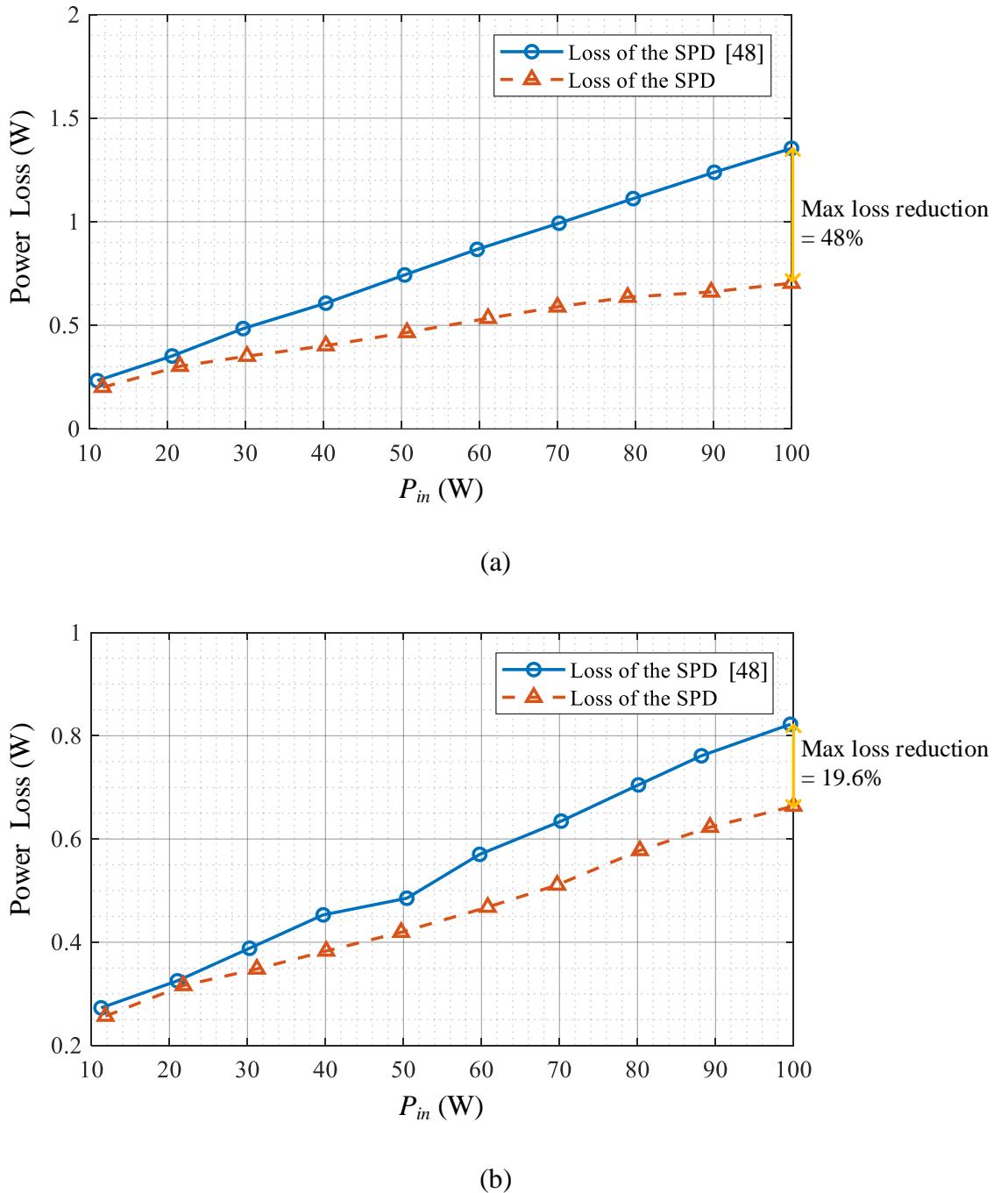
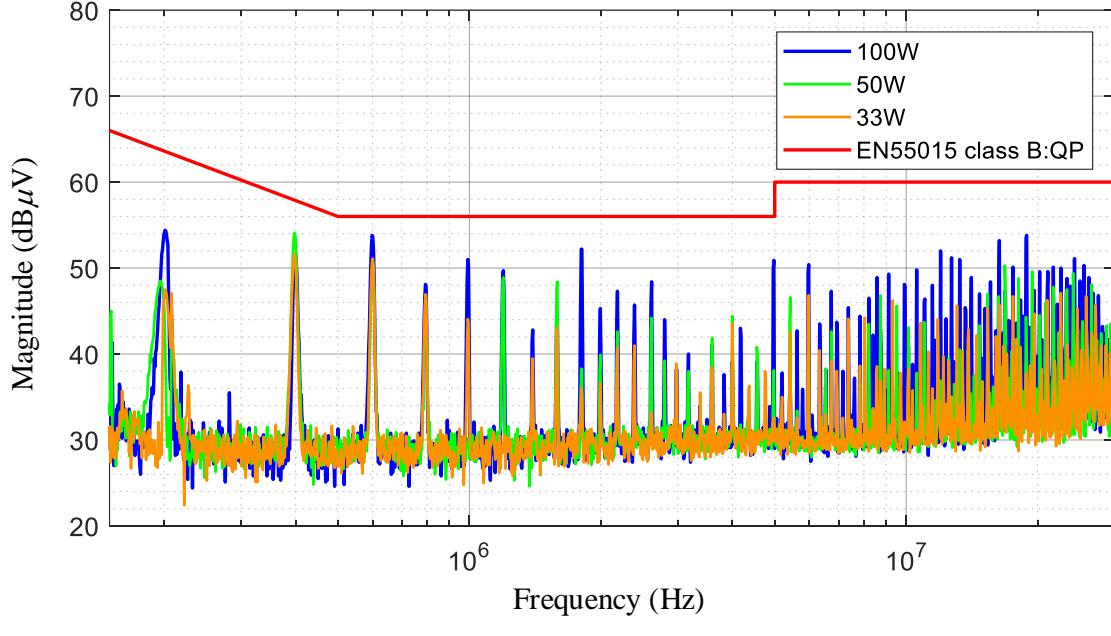


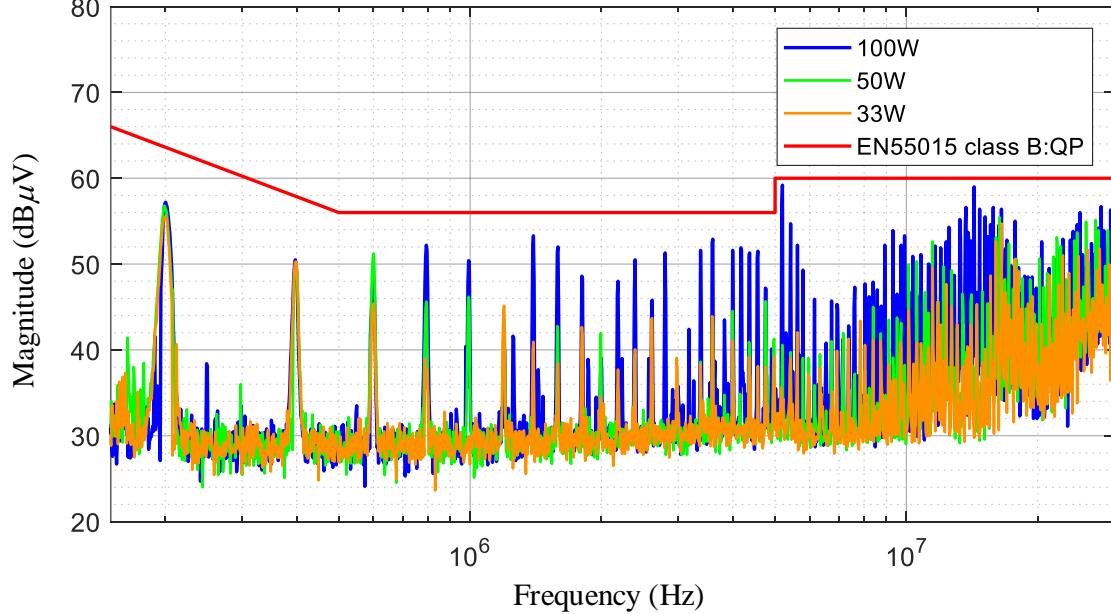
Fig. 2.26. Comparisons of power dissipation of the SPD under different loading conditions. (a) $V_s = 115V$. (b) $V_s = 230V$.

The measured DM and overall EMI (DM and CM) noise spectra under different load conditions (33%, 50%, and 100% of nominal load), low- and high-line conditions, are shown in Fig. 2.27. The PSF has already demonstrated a significant DM EMI noise reduction in Fig. 2.18. To reduce CM noise, a 680pF bypass capacitor C_Y is adopted as analyzed in [48], and the common-heatsink of switch S_1 and diode S_2 is grounded to the

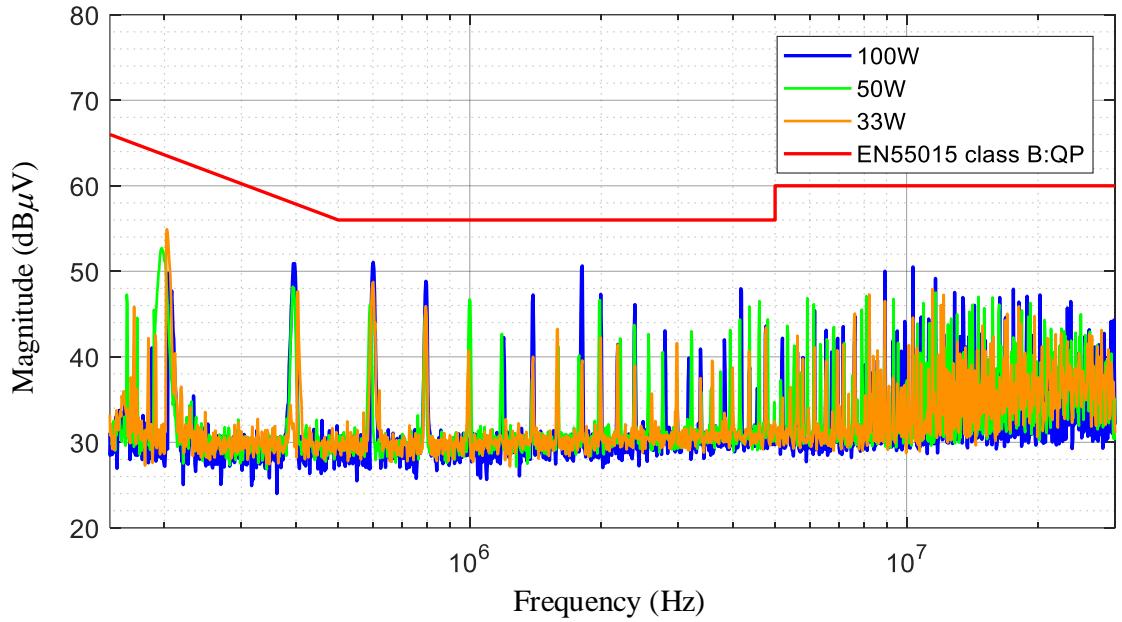
power return line, i.e., the source of switch S_1 , as suggested in [75], [76]. The overall EMI noise levels of the prototype have satisfied the EN55015 class B standard over the whole range of 150kHz to 30MHz, under low- and high-line conditions. In some peaks, DM values are higher in amplitude than the overall values due to slight variations of noise level from measurement to measurement.



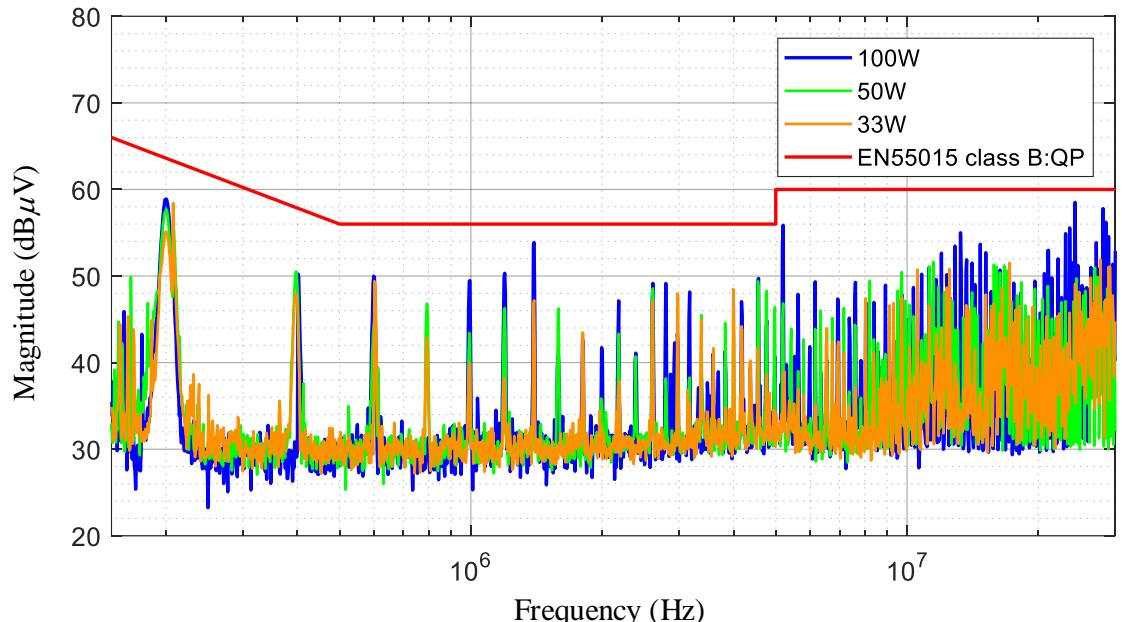
(a)



(b)



(c)



(d)

Fig. 2.27. Measured peak DM and overall EMI noise of the prototype under different loading conditions. (a) DM noise ($V_s = 115V$). (b) Overall EMI noise ($V_s = 115V$). (c) DM noise ($V_s = 230V$). (d) Overall EMI noise ($V_s = 230V$).

TABLE 2.4
COMPARISON BETWEEN THIS WORK AND PRIOR PUBLICATION

Items		[48]	This work
Input current oscillation		Not solved	Solved
Power dissipation in the SPD	Low-line, rated power	1.354 W	0.703W (-48.1%)
	High-line, rated power	0.826W	0.664W (-19.6%)
DM noise level	Switching frequency (200kHz)	-	Reduced by 15.3dB
	High-frequency range (5MHz-30MHz)	-	Reduced by 9.83dB on average
Number of wideband amplifiers		2	1
EMI suppression capability prediction		No	Yes
Critical PCB layout guidelines		No	Yes

2.6. Chapter Summary

A conducted EMI suppression method using the power semiconductor filter with the dynamic ramp modulation in fixed-frequency operation is presented in this chapter. The progress made in this chapter compared with [48] is shown in Table 2.4. Three issues associated with the PSF have been solved, making the PSF a practical solution for conducted EMI suppression.

- 1) The switching frequency of the converter with the PSF is fixed and set away from the grid-side resonant frequency, which suppresses input current oscillation without the aid of passive filters.
- 2) The voltage across the SPD is regulated at a low level regardless of input variations by the dynamic ramp modulation; compared with [48], 48.1% and 19.6% reduction of power dissipation in the SPD has been achieved under full rated power, low-line and high-line conditions. The total volume of the PSF is also reduced due to less demand for cooling system.

- 3) The proposed single-stage amplifier with the RC damping circuit, of simpler structure, has demonstrated better EMI suppression performance than that of the configuration of two-stage amplifiers. By reducing the number of wideband amplifiers, the ground loop inductance is reduced, and the cost of the fast-current regulation circuit is also halved.

This chapter also facilitates the design and implementation of the PSF in two aspects.

- 1) A method of predicting the EMI suppression capability of the PSF has been proposed. It does not need noise source impedance in the early design phase, which aids the analysis and design of the fast-current regulation circuit.
- 2) The ground loop inductance, in the fast-current regulation circuit, that could severely impair the EMI suppression performance of the PSF has been mathematically analyzed and validated with experimental results. PCB layout guidelines have also been given to mitigate the adverse effect of the ground loop inductance.

Chapter 3

INPUT ACTIVE COMMON-MODE FILTER

3.1. Chapter Introduction

As introduced in Chapter 1, there are four types of active CM filter (ACF) according to the sensing and compensation methods. Transformers are required in the current-sensing and voltage-compensation stages. However, parasitic capacitance and reduced magnetic permeability in the high-frequency range will impair transformers' performance.

Voltage-sensing and current-compensation (VSCC) ACF does not require transformers. It is thus a promising topology to achieve better high-frequency performance and smaller volume than the other three types [57]-[61]. In [57], a hybrid LCL EMI filter, including a VSCC section and two-side CM chokes, is proposed. Heldwein *et al.* [58] intuitively elaborated the fundamental principle of the VSCC section as a virtually magnified capacitance, which facilitates the analysis and design of ACFs. Many BJTs are used to construct a high output current operational amplifier (Op-amp) as the amplifying stage. Shin *et al.* [59] proposed a push-pull amplifier to circulate the CM noise and took the immunity of the ACF to high voltage transients into consideration. Takahashi *et al.* [60] used a current feedback Op-amp as the amplifying stage for very high-frequency applications. Zhang *et al.* [61] proposed a feedforward ACF based on accurate CM impedance measurement and an artificial fitted impedance network.

The prior art has demonstrated the viability and advantages of VSCC ACFs, but their operating range is still limited. The bandwidth of the VSCC ACFs is usually below several megahertz, and the structure has one VSCC section only. When the CM noise is too large to handle, the value of the CM inductor should be increased so that the required attenuation can be achieved. Compared with passive filters, the CM inductance in the ACF is reduced. However, the volume of CM chokes still dominates the total filter volume.

The VSAC section is essentially an active capacitor. Then, multiple active capacitors can be used in a multistage ACF when high attenuation is needed. Moreover, it is not only feasible to combine active capacitors with passive inductors but also possible to combine active capacitors with active inductors. Hence, the concept of the ACF can be extended, and a new perspective of ACF can be inspired.

The motivation of this chapter is to exploit the potential of using active devices in realizing a new VSAC ACF with small CM inductance. The proposed ACF has the following merits:

1) *Low cost and high immunity to high voltage transients*: The proposed active capacitor is connected to power lines through Y-capacitors; high voltage transients would appear. BJTs are used in the amplifying stage as they have better immunity to high voltage transients and lower cost than wideband Op-amps [59].

2) *Wide bandwidth*: In view of low CM noise power, class A amplifiers are chosen for their wide bandwidth and high linearity even though their power efficiency is lower than other types, such as class AB amplifiers. Since discrete components have larger parasitic parameters than IC Op-amps, the sophisticated configuration of the IC Op-amps is less applicable for the amplifying stage of the active capacitor. The proposed active capacitor uses minimal stages for the class-A amplifier to avoid performance degradation by the parasitic parameters of discrete BJTs. The ACF has a wide bandwidth from 150kHz to 30MHz.

3) *High attenuation*: The proposed active capacitor utilizes a common-collector (CC) amplifier to mitigate the input voltage divider effect and a common-emitter (CE) amplifier with active load to provide high gain. Hence, the proposed ACF provides high attenuation of the CM noise.

4) *General multistage structure*: The magnitude of CM noise is proportional to the area of pulsating voltage nodes. High-power converters usually have large heatsinks, resulting in high CM noise. Low-power converters usually have relatively lower CM

noise. This chapter has proposed a general ACF section that multiple sections can be cascaded to form a multistage structure. Different attenuation levels can be achieved.

A comparison with prior art VSCC ACFs is tabulated in Table 3.1. The fundamental principles and design of the proposed active capacitor will be given. Then, the stability and insertion loss of the active capacitor will be analyzed. The design of multistage ACF and the optimal number of ACF sections will be given. The performance of single-stage and multistage ACFs is evaluated on a commercial 90W laptop adaptor and a 1000W power supply for industrial applications.

TABLE 3.1
COMPARISON WITH PRIOR ART VSCC ACFs

Ref	EUT	Amplifier Design	Original $V_{CM,max}$	Max Attenuation Bandwidth	L_{cm}	Y-cap	P_{active}
[57]	600W PFC	Class A amplifier		EMI spectrum is not given.	26.5 μ H \times 2	64.8nF	-
[58]	6.8kVA SMC	Differential input stage + bias network + level shifter + class AB output stage	87dB μ V	10dB	150kHz-500kHz	320 μ H \times 2	80.1nF
[59]	2.2kW inverter	Class AB amplifier with damping circuit	77dB μ V	25dB	150kHz-6MHz	1mH+8mH	6.94nF
[60]	Motor drive system	Op-amp	120dB μ V	Loop gain = 2	4MHz-100MHz	2.2 μ H	0.6nF
[61]	Motor drive system	Op-amp + class AB amplifier	108dB μ V	13dB (w/o Lcm) 36dB (w/ Lcm)	150kHz-3.5MHz	220 μ H	2.2 μ F
This work	90W laptop adaptor 1000W power supply	CC amplifier + CE amplifier with active load	78dB μ V 100dB μ V	28dB 60dB	150kHz-30MHz	No 16 μ H \times 2	5.06nF 24.52nF
							273mW 1.206W

3.2. Analysis and Design of the Active Capacitor

Y-capacitors will lead to the leakage current due to the line voltage. Their values are thus restricted for safety reasons [77]. Considering that the conducted EMI frequency ranges from 150kHz to 30MHz, an ideal solution is to reduce the impedance of the Y-capacitor in the high-frequency range but maintain a high low-frequency impedance. Thus, an active capacitor, which is constructed by a fixed capacitor C connected in series with a controllable voltage source, is implemented, as shown in Fig. 3.1. The output voltage of the voltage source is derived from the terminal voltage v_s with a frequency-dependent gain $G_v(f)$. Thus, the equivalent capacitance $C_{act}(f)$ is

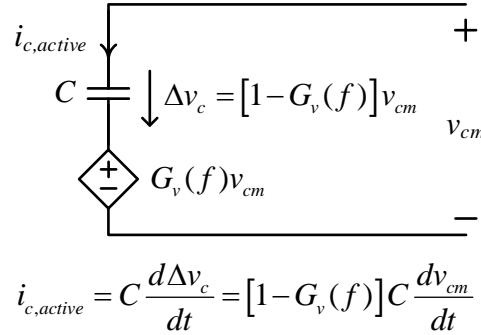


Fig. 3.1. Fundamental principles of an active capacitor.

$$C_{act}(f) = [1 - G_v(f)]C \quad (3.1)$$

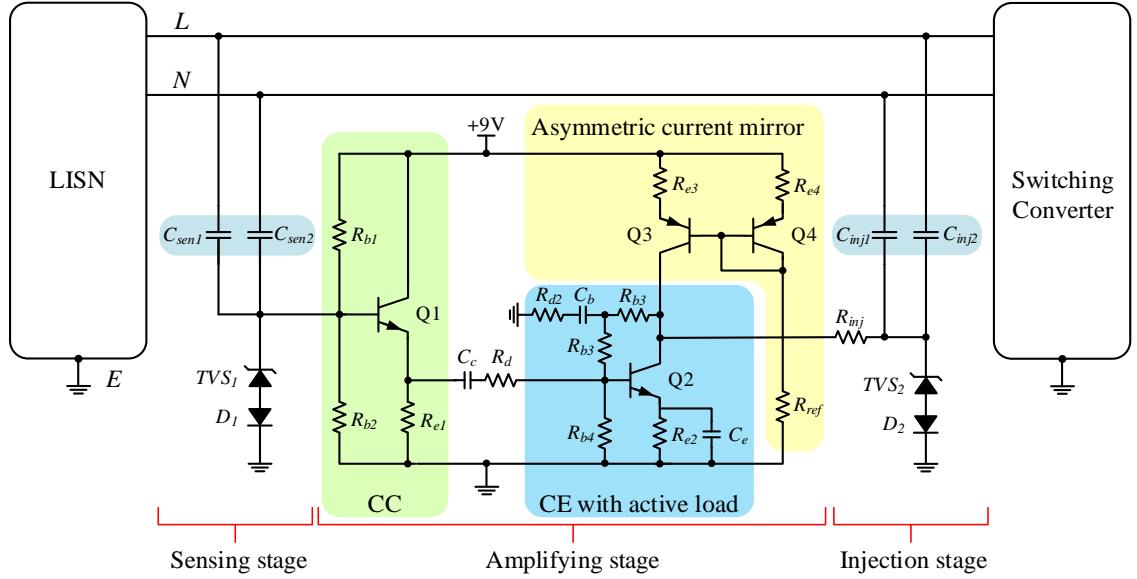
where f is operating frequency.

3.2.1. Design of the Active Capacitor

Fig. 3.2(a) shows the schematic diagram of the proposed active capacitor. The active capacitor consists of three parts: sensing capacitors, amplifying stage, and injection capacitors. Capacitors C_{sen1} and C_{sen2} with identical capacitance sense the common-mode noise voltage. The amplifying stage is the implementation of the controllable high-frequency voltage source in Fig. 3.1. The injection capacitors, C_{inj1} and C_{inj2} , are of the same value, circulate the majority CM noise current. Consequently, the CM noise flowing into the LISN is highly reduced. Furthermore, transient-voltage-suppression (TVS) diodes (SMAJ13A) and small-signal fast switching diodes (1N4148) are used to protect the amplifying stage from high voltage transients [59].

Since the total Y-capacitance (C_{sen} and C_{inj}) is restricted, the sensing capacitors have small capacitances. Thus, their impedances are large. The CC amplifier, having high input impedance, avoids attenuating the CM voltage appeared at the input of the high-gain CE amplifier.

In conventional CE amplifiers, using a large collector resistor can attain a high voltage gain. However, the use of a large collector resistor requires a high voltage supply and leads to more power consumption, limiting the value of the collector resistor and the gain. A current mirror, which acts as an active load, is used to provide a large equivalent



(a)

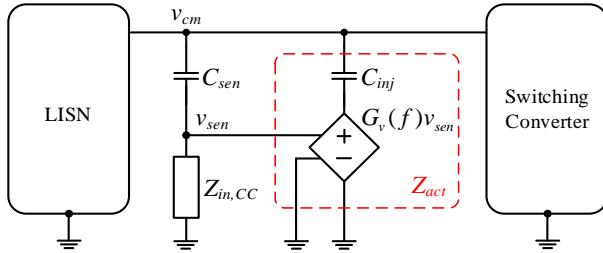


Fig. 3.2. Diagrams of the proposed active capacitor. (a) Schematic diagram. (b) Single-phase equivalent circuit.

resistance. Moreover, the active load is in asymmetric configuration; transistor Q4 has a much smaller quiescent current than Q3. Q1 is used as a voltage buffer and does not inject compensation current; the quiescent current of Q1 is much smaller than that of Q3. Thus, the power dissipation of the active capacitor can be reduced by one-half, as compared to the symmetric configuration in which Q3 branch and Q4 branch each approximately account for one-half of the total power dissipation.

Fig. 3.2(b) shows the single-phase equivalent circuit with the proposed active capacitor. $Z_{in,CC}$ represents the input impedance of the CC amplifier. At low-frequency, $v_{sen} \approx 0$, and $Z_{act} = Z_{inj}$; at high-frequency, $v_{sen} \approx v_{cm}$, and $Z_{act} = Z_{inj}/[1-G_v(f)]$.

Fig. 3.3 shows the small-signal model of the proposed active capacitor, and the circuit parameters are presented in Table 3.2. The procedure to determine the component values in Table 3.2 is shown in Appendix A.1 [78]. The following equations can be derived,

$$\left[I_x(s) - g_m V_{bex1}(s) - I_\mu(s) \right] r_o = I_\mu(s) Z_{C_\mu}(s) + V_{bex1}(s) \quad (3.2)$$

$$I_\mu(s) Z_{C_\mu}(s) + V_{bex1}(s) + \left[I_x(s) - I_\mu(s) + \frac{V_{bex1}(s)}{Z_{be}(s)} \right] R_{e3} = V_x(s) \quad (3.3)$$

$$I_\mu(s) Z_{C_\mu}(s) + \left[I_\mu(s) - \frac{V_{bex1}(s)}{Z_{be}(s)} \right] R_L = V_x(s) \quad (3.4)$$

$$Z_{AL}(s) = \frac{V_x(s)}{I_x(s)} \quad (3.5)$$

$$I_{sen}(s) = \frac{V_{cm}(s) - V_{b1}(s)}{Z_{Csen}(s)} \quad (3.6)$$

$$I_{sen}(s) = \frac{V_{b1}(s)}{R_{b1} \| R_{b2} \| Z_{C_\mu}(s)} + \frac{V_{be1}(s)}{Z_{be}(s)} \quad (3.7)$$

$$V_{e1}(s) = V_{b1}(s) - V_{be1}(s) \quad (3.8)$$

$$\frac{V_{be1}(s)}{Z_{be}(s)} + g_m V_{be1}(s) = \frac{V_{e1}(s)}{R_{e1} \| r_o} + \frac{V_{e1}(s) - V_{be2}(s)}{R_d} \quad (3.9)$$

$$\frac{V_{e1}(s) - V_{be2}(s)}{R_d} = \frac{V_{be2}(s)}{Z_{b3}(s) \| R_{b4} \| Z_{be}(s)} + \frac{V_{be2}(s) - V_o(s)}{Z_{C_\mu}(s) \| Z_{bc}(s)} \quad (3.10)$$

$$\frac{V_{be2}(s) - V_o(s)}{Z_{C_\mu}(s) \| Z_{bc}(s)} = g_m V_{be2}(s) + \frac{V_o(s)}{r_o \| Z_{b3}(s) \| Z_{AL}(s)} - I_{inj}(s) \quad (3.11)$$

$$I_{inj}(s) = \frac{V_{cm}(s) - V_o(s)}{Z_{C_{inj}}(s) + R_{inj}} \quad (3.12)$$

$$Z_{act}(s) = \frac{V_{cm}(s)}{I_{sen}(s) + I_{inj}(s)} \quad (3.13)$$

where $Z_{be}(s) = r_{be} \parallel Z_{C_{be}}(s)$, $Z_{C_{be}}(s) = 1/sC_{be}$, $Z_{C_\mu}(s) = 1/sC_\mu$, and

$R_L = [Z_{be} \parallel 1/g_m \parallel r_o] \parallel R_{ref} \approx R_{e4} \parallel R_{ref}$. By using Y- Δ transformation,

$Z_{bc}(s) = 2R_{b3} + sC_d R_{b3}^2 \parallel (R_{b3}^2 / R_{d2})$, and $Z_{b3}(s) = R_{b3} + 2R_{d2} + 2/sC_d$.

By using (3.2)-(3.13), the impedance characteristics of the proposed active capacitor $Z_{act}(s)$ is shown in Fig. 3.4(a). As shown in Fig. 3.4(b), the impedance of the passive capacitor at 150kHz is decreased by 111 times. In other words, the equivalent capacitance is amplified up to 111 times below 7.1MHz. Since the equivalent capacitance is increased, the self-resonant frequency of the active capacitor is lower than that of the passive capacitor. Between 7.1MHz and 30MHz, even if Z_{act} is larger than $Z_{passive}$, the impedance of the active capacitor is still low. Hence, the active capacitor can attenuate CM noise from 150kHz to 30MHz.

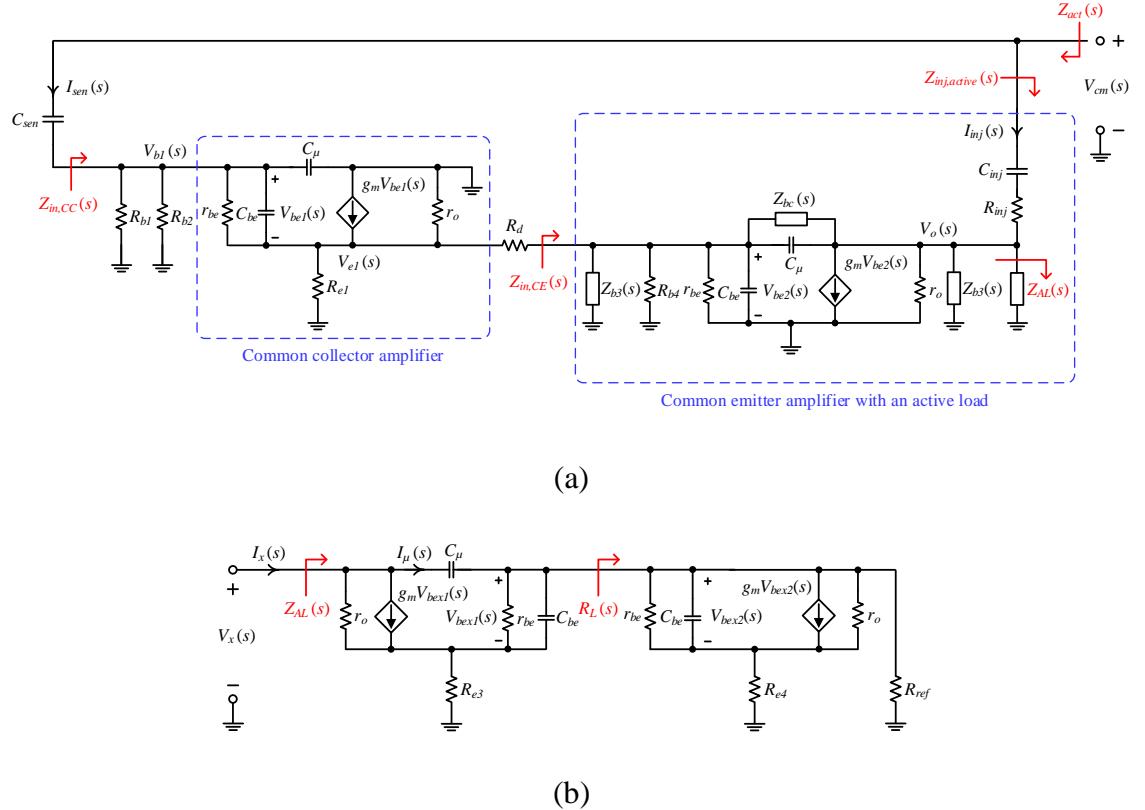


Fig. 3.3. Small-signal models. (a) The proposed active capacitor. (b) The active load circuit.

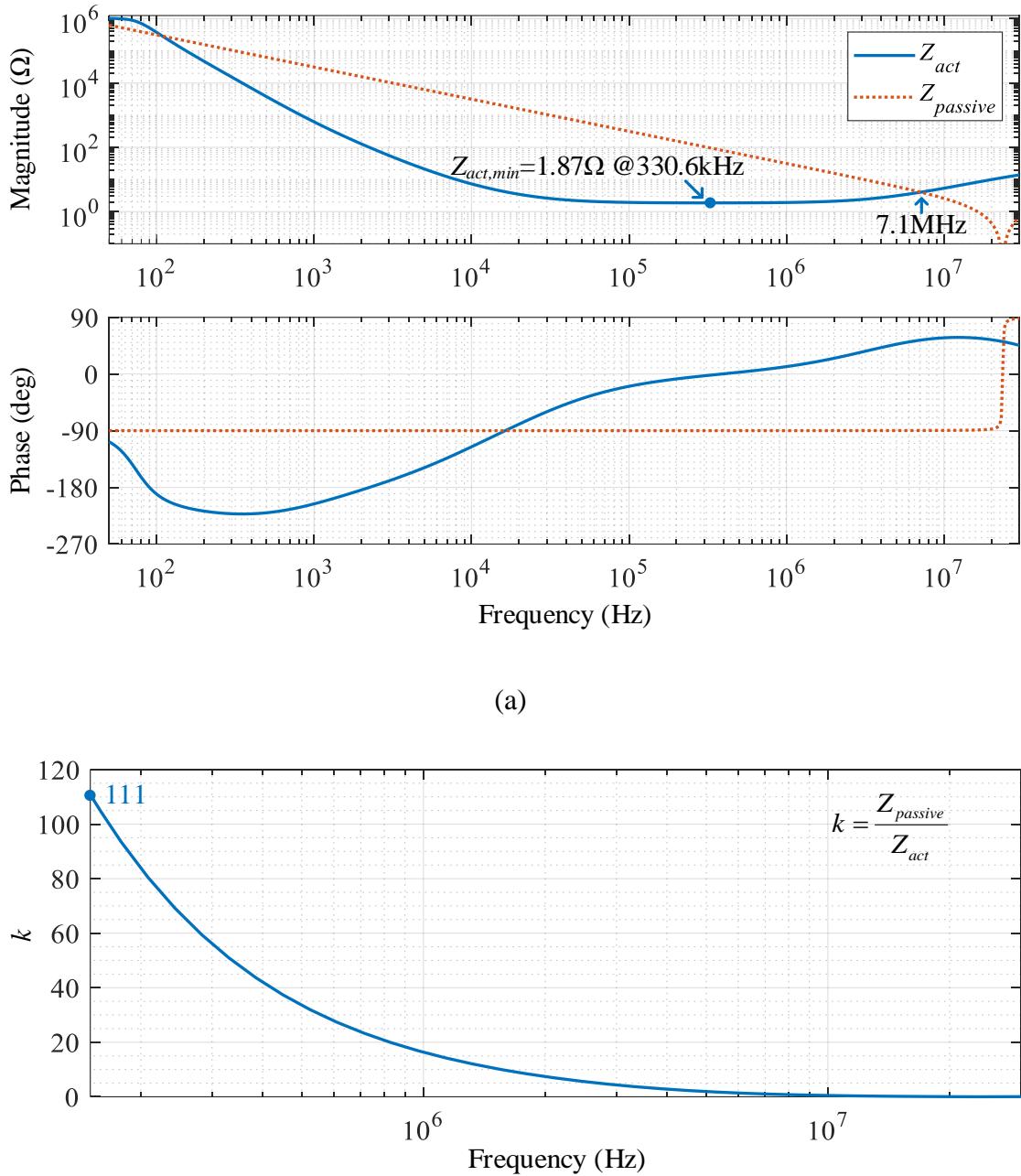


Fig. 3.4. Impedance characteristics of the proposed active capacitor. (a) Z_{act} and $Z_{passive}$.
(b) $k = Z_{passive}/Z_{act}$ ($C_{passive} = C_{sen} + C_{inj} = 5.06\text{nF}$).

TABLE 3.2
PARAMETERS OF THE PROPOSED ACTIVE CAPACITOR

Parameter	Value	Parameter	Value
C_{sen1}, C_{sen2}	330pF	R_{e3}	10Ω
C_{inj1}, C_{inj2}	2.2nF	C_e	20μF
R_{b1}	75kΩ	R_{e4}	220Ω
R_{b2}	100kΩ	R_{ref}	5.1kΩ
R_{e1}	2kΩ	R_{inj}	2Ω
C_c	10μF	Q1, Q2	2SCR293P5
R_d	100Ω	Q3, Q4	2SAR293P5
R_{b3}	12kΩ	r_{be}	433.9Ω
R_{b4}	8.2kΩ	g_m	1.04S
C_b	100nF	C_{be}	657.2pF
R_{d2}	10Ω	C_μ	27.3pF
R_{e2}	10Ω	r_o	1881Ω

For the sake of design, the basic principle, as shown in Fig. 3.1, is adopted. $Z_{act}(s)$ is re-expressed as follows:

$$Z_{act}(s) \approx Z_{inj,active}(s) = \frac{Z_{inj}(s)}{1 - G_v(s)} \quad (3.14)$$

$$G_v(s) = G_{v,CC}(s)G_{v,CE}(s) \quad (3.15)$$

$$G_{v,CC}(s) = \frac{Z_{in,CC}(s)}{Z_{C_{sen}}(s) + Z_{in,CC}(s)} \quad (3.16)$$

$$G_{v,CE}(s) = -\left[\frac{Z_{in,CE}(s)}{R_d + Z_{in,CE}(s)} \right] \left[Z_L(s) \parallel (Z_{inj} + Z_{act}) \right] g_m \quad (3.17)$$

where $Z_{in,CC}(s) = \left\{ r_{be} + (1 + g_m R_{be}) [R_{e1} \parallel r_o \parallel (R_d + Z_{in,CE}(s))] \right\} \parallel R_{b1} \parallel R_{b2}$,

$Z_{in,CE}(s) = Z_{b3}(s) \parallel R_{b4} \parallel r_{be}$, and $Z_L(s) = Z_{AL}(s) \parallel Z_{b3}(s) \parallel r_o$.

From (3.14)-(3.17), it can be noted that a high voltage gain $G_v(s)$ is essential to construct a low impedance path $Z_{act}(s)$ to circulate the CM noise. $G_v(s)$ depends on both $G_{v,CC}(s)$ and $G_{v,CE}(s)$. It is necessary to make the CC amplifier for $G_{v,CC}(s)$ be unity. CE amplifier with active load is used to provide a high gain $G_{v,CE}(s)$.

3.2.2. Stability of the CM Noise Circuit with the Active Capacitor

Fig. 3.5(a) shows the equivalent circuit for representing the CM noise propagation with the proposed active capacitor. The pulsating CM voltage source $V_s(s)$ generates noise current $I_n(s)$ through a capacitor C_p . C_p is the parasitic capacitance between switching nodes attached to heatsinks and the earth, which is much smaller than the active capacitor. Thus, the CM noise source can be regarded as a current source $I_n(s)$ due to its high output impedance characteristics.

$$I_n(s) = \frac{V_s(s)}{Z_{LISN}(s) \parallel Z_{act}(s) + Z_{C_p}(s)} \approx \frac{V_s(s)}{Z_{C_p}(s)} \quad (3.18)$$

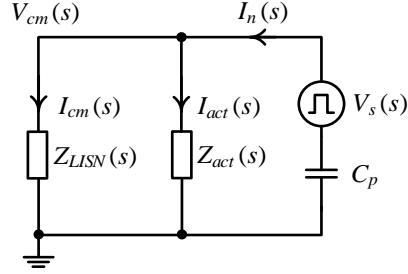
where $Z_{LISN}(s)$ is the impedance of the LISN.

The LISN used in the experiment is ETS-Lindgren 4825/2. Its simplified schematic diagram is shown in Fig. 3.5(b). It meets the requirements stipulated in CISPR 16-1 [4].

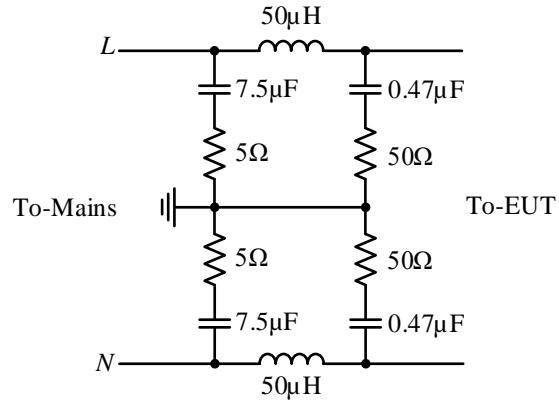
Based on the block diagram of the equivalent circuit shown in Fig. 3.5(c), the loop gain of the CM circuit $G_L(s)$ is

$$G_L(s) = \frac{I_{act}(s)}{I_{cm}(s)} = \frac{Z_{LISN}(s)}{Z_{act}(s)} \quad (3.19)$$

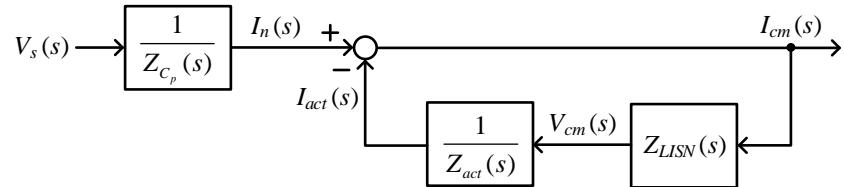
Based on (3.19), the frequency response of $G_L(s)$ is shown by the blue line in Fig. 3.6. $G_L(s)$ crosses the 0-dB axis at 20.2kHz with a phase margin of 61° .



(a)



(b)



(c)

Fig. 3.5. Stability analysis models. (a) Equivalent circuit for representing CM noise propagation. (b) Schematic diagram of the LISN. (c) Block diagram for representing the equivalent circuit.

3.2.3. Effect of Supply Cable Impedance

The converter is connected to the LISN via a supply cable, which has an impedance of $Z_{cable}(s)$ in series with $Z_{LISN}(s)$. For example, a 1m long three-wire cable has an inductance of $1.2\mu\text{H}$ per wire. Thus, the inductance of the CM path caused by the cable is $(1.2/2+1.2)\mu\text{H} = 1.8\mu\text{H}$. With $Z_{cable}(s)$ taken into account, $G_L(s)$ is expressed as

$$G_L(s) = \frac{Z_{LISN}(s) + Z_{cable}(s)}{Z_{act}(s)} \quad (3.20)$$

The frequency response of $G_L(s)$ with $Z_{cable}(s)$ is shown by the red line in Fig. 3.6. This small cable inductance can increase the magnitude of $G_L(s)$ in the high-frequency range. Simulator LTspice is used to validate the above analysis. The calculated results are in close agreement with the simulated results. The discrepancy in the low-frequency range is because the coupling and bypass capacitors (C_c and C_e) are ignored in the small-signal analysis for the sake of simplicity since the capacitances are very large; the discrepancy in the high-frequency range is due to the reason that the transistor SPICE model has more complicated high-frequency parameters than the small-signal model used in this chapter.

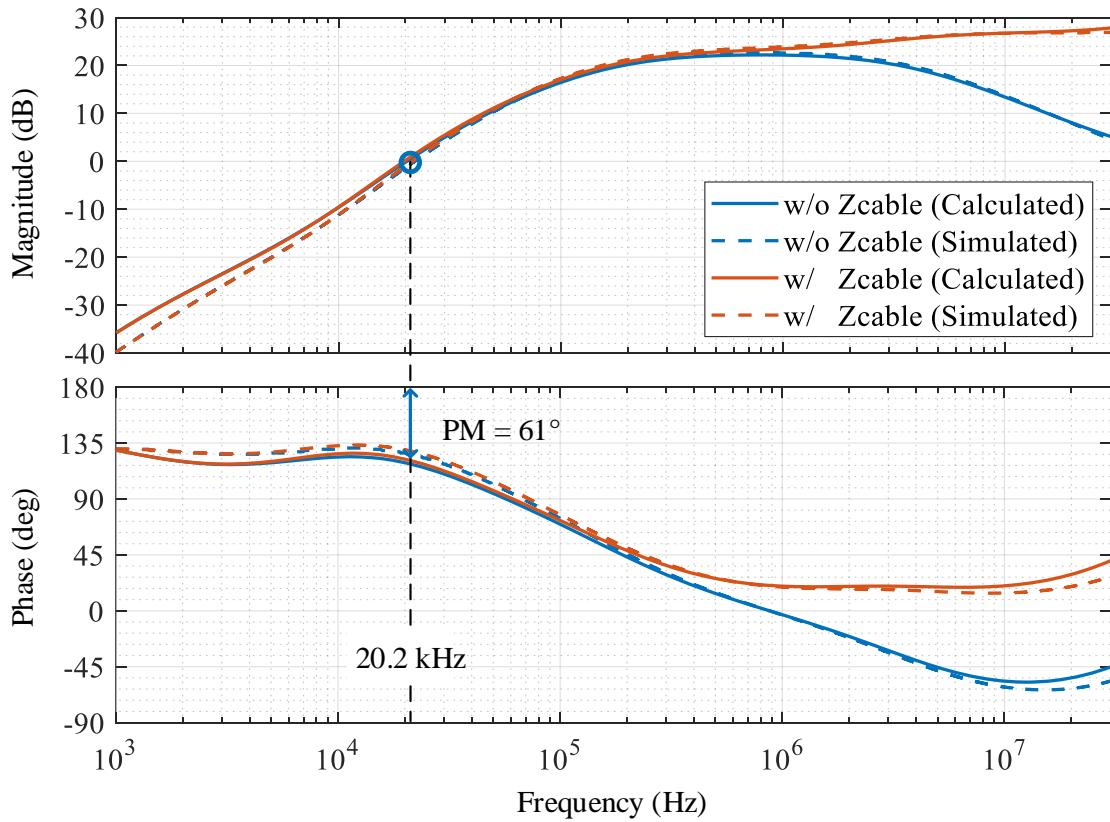


Fig. 3.6. Loop gain of the CM circuit with the active capacitor.

3.2.4. Output Voltage Swing of the Active Capacitor

The output voltage swing of the active capacitor can be derived from the circuit shown in Fig. 3.3(a).

$$\begin{aligned}
V_o(s) &= G_v(s)V_{cm}(s) \\
&= G_v(s) \frac{Z_{LISN}(s)Z_{act}(s)}{Z_{LISN}(s) + Z_{act}(s)} I_n(s) \\
&= G_v(s) \frac{Z_{LISN}(s)Z_{inj}(s)}{Z_{LISN}(s)(1-G_v(s)) + Z_{inj}(s)} I_n(s) \\
&= \frac{G_v(s)Z_{LISN}(s)}{Z_{LISN}(s)(1-G_v(s))sC_{inj} + 1} I_n(s)
\end{aligned} \tag{3.21}$$

According to (3.21), the output voltage swing Δv_o is dependent on the noise level. If the maximum CM noise voltage $V_{cm}(s)$ measured by the LISN is 80dB μ V, the magnitude of the corresponding noise current is 0.4mA (80dB μ V/25ohm). Taking the variation of the injection capacitance C_{inj} into account, the frequency response of Δv_o is shown in Fig. 3.7. Δv_o is maximum when there is resonance between $Z_{act}(s)$ and $Z_{LISN}(s)$. Its magnitude will decrease with the increase in C_{inj} . Since the switching frequency is usually higher than tens of kilo-Hertz, this peak voltage can be avoided. Compared with the typical value of V_{cc} ($\pm 15V$ or $\pm 30V$) in the prior art, V_{cc} is set at a much lower level at 9V to reduce power dissipation.

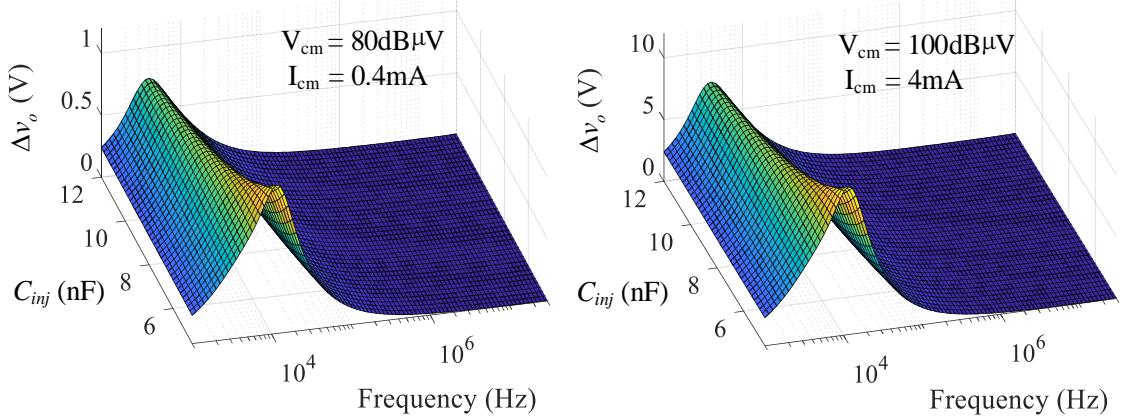


Fig. 3.7. Frequency response of Δv_o .

3.2.5. Insertion Loss of the Active Capacitor

The insertion loss of the active capacitor $IL_{act}(s)$ is calculated by the ratio of the noise voltage across the LISN without and with the active capacitor, as illustrated in Fig. 3.5(a).

Based on Fig. 3.5(a), without the active capacitor, the noise voltage V_{cm} is V'_{cm} . It can be shown that

$$V'_{cm}(s) = \frac{Z_{LISN}}{Z_{C_p}(s) + Z_{LISN}(s)} V_s(s) \quad (3.22)$$

With the active capacitor connected,

$$V_{cm}(s) = \frac{Z_{LISN}(s) \| Z_{act}(s)}{Z_{C_p}(s) + Z_{LISN}(s) \| Z_{act}(s)} V_s(s) \quad (3.23)$$

Considering that $Z_{LISN}(s) \ll Z_{C_p}(s)$,

$$\begin{aligned} IL_{ac}(s) &= \frac{V'_{cm}(s)}{V_{cm}(s)} = \frac{1 + \frac{Z_{LISN}(s)}{Z_{act}(s)}}{1 + \frac{Z_{LISN}(s)}{Z_{C_p}(s) + Z_{LISN}(s)}} \\ &\approx 1 + \frac{Z_{LISN}(s)}{Z_{act}(s)} \\ &= 1 + G_L(s) \end{aligned} \quad (3.24)$$

Hence, a high loop gain $G_L(s)$ is the key factor to increase the insertion loss of the active capacitor. When taking the input cable connected in series with the LISN into account, $Z_{LISN}(s)$ is revised as $Z_{LISN}(s) + Z_{cable}(s)$ in (3.24). The insertion losses of the active capacitor with and without $Z_{cable}(s)$ included are shown in Fig. 3.8.

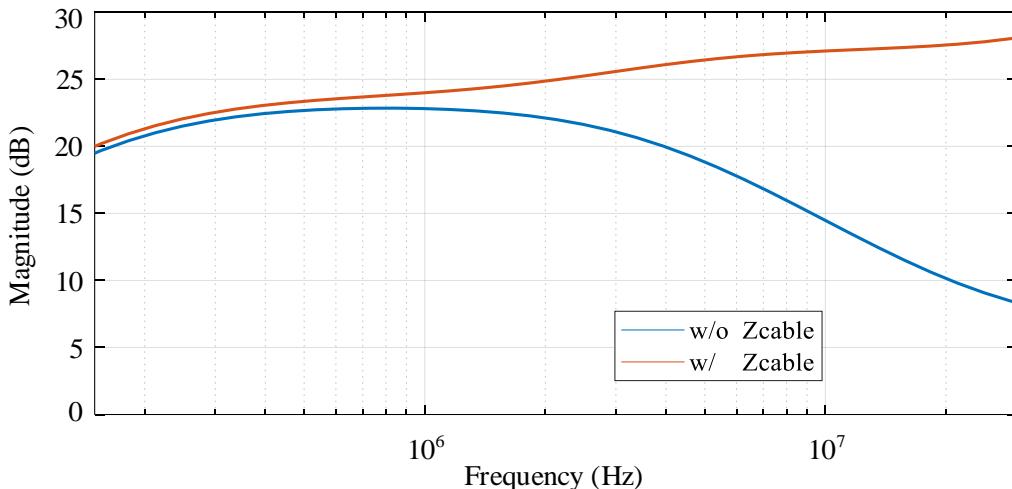


Fig. 3.8. Insertion loss of the active capacitor.

3.3. Multistage Active CM Filter

When high attenuation is needed, multiple active capacitors can be cascaded with CM inductors to form a multistage ACF. Based on the impedance mismatch principle of filter design, the low impedance element Z_{act} should be placed close to the high impedance CM noise source [79], as shown in Fig. 3.9(a) with the CM inductors modeled by inductor Z_{Lcm} .

3.3.1. Multistage Active CM Filter Design

The stability analysis of the CM noise propagation circuit with an active capacitor has been given in Section 3.2.2. The stability of the CM circuit with the multistage ACF is analyzed. Based on the model given in Fig. 3.9(b), the loop gain of filter section n $G_{L,act,n}(s)$ is

$$G_{L,act,n} = \frac{I_{act,n}(s)}{I_{cm,n}(s)} = \frac{Z_n(s)}{Z_{act}(s)} \quad (3.25)$$

$G_{L,act,n}(s)$ is used to examine the stability of each filter section. The stability of the entire multistage ACF also needs to be analyzed. By using (3.25), Fig. 3.9(b) can be reduced as Fig. 3.9(c). Then, Fig. 3.9(c) can be further reduced as Fig. 3.9(d). The loop gain of the entire multistage ACF is

$$G_{L,act} = \frac{\sum_{n=1}^n I_{act,n}(s)}{I_{cm,n}(s)} = \prod_{n=1}^n (1 + G_{L,act,n}) - 1 \quad (3.26)$$

Based on (3.26), the phase margin of the n -stage ACF is obtained by using LTspice, as shown in Fig. 3.10. The CM inductance in the multistage ACF is very small. A $16\mu\text{H}$ CM inductor is used in the prototype given in Section 3.4.

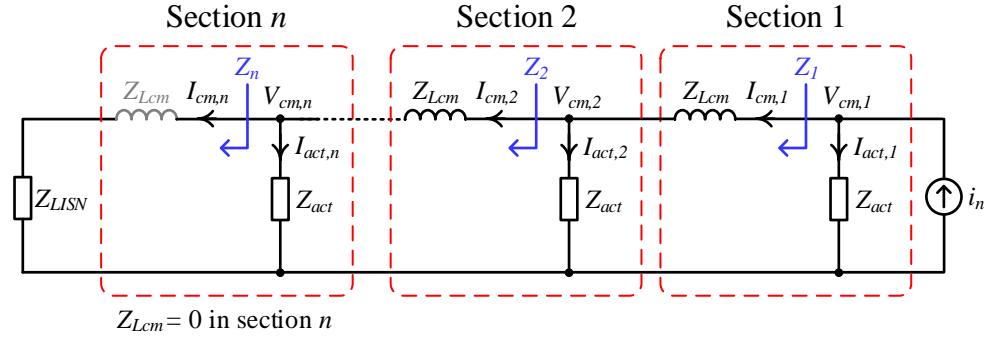
As the increase of filter sections, phase margins decrease. A higher phase margin can be obtained when using a higher injection capacitance C_{inj} . This is because the active capacitor can resonate with LISN-side inductive impedance, and the resonant frequency will decrease when increasing C_{inj} . Since Z_{LISN} with Z_{cable} taken into account is capacitive

in low-frequency and inductive in high-frequency, the resonance will be reduced when the resonant frequency is closer to the capacitive region of Z_{LISN} . The maximum capacitance is restricted by different safety standards for different applications.

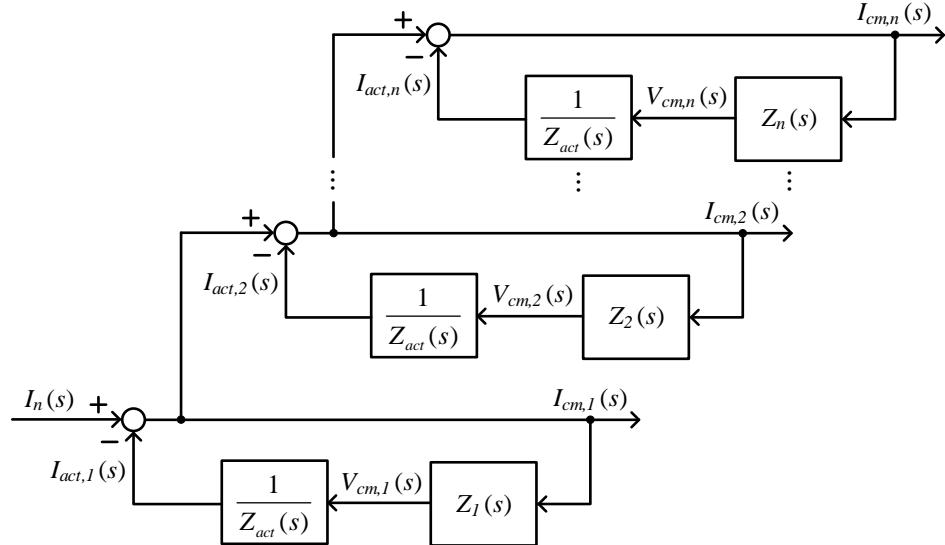
Phase margin can be improved by removing the CM choke in section n (close to the LISN). This is because the output impedance of the multistage ACF is dominated by the last section [70]. Removing L_{cm} in section n can mitigate the resonance between the LISN and the active capacitor; thus, a higher phase margin can be obtained. If the attenuation is below the requirement when removing $L_{cm,n}$, one more filter section can be added as the $(n-1)$ stage.

As a case study, a two-stage CLC ACF is proposed for a 1000W switching converter. The first section consists of an active capacitor and a $16\mu\text{H}$ CM choke; the second section has an active capacitor only. The injection capacitance in the active capacitor is 4.7nF for each line. The phase margin of the CLC ACF is 49.1° , as shown in Fig. 3.10.

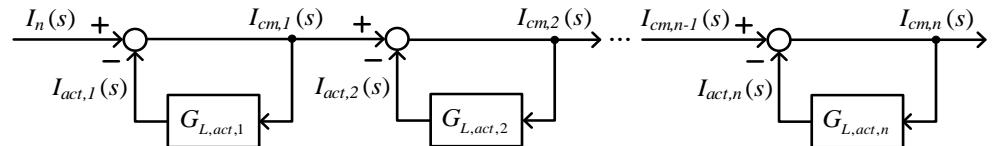
As shown in Fig. 3.9(a), majority noise current $I_n(s)$ is firstly circulated through the section-1 active capacitor, and then part of the residual noise current circulates through the section-2 active capacitor. Thus, the current flowing through the LISN is significantly reduced. Since the amplifying stage of the active capacitors is a class-A amplifier, it is important to set an appropriate quiescent current to avoid cut-off distortion. Hence, the quiescent current of section-1, $I_{CQ,1}$, is higher than that of section-2, $I_{CQ,2}$. The other parameters of the two active capacitors remain the same. Hence, the two active capacitors share the same small-signal model that facilitates the analysis and design of the CLC ACF. The proposed CLC ACF will be evaluated in Section 3.4.



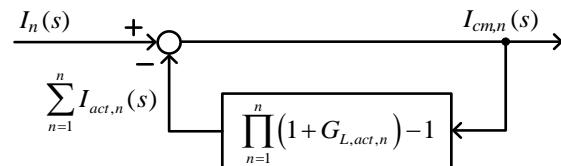
(a)



(b)



(c)



(d)

Fig. 3.9. Multistage ACF. (a) Equivalent circuit for representing CM noise propagation. (b) Block diagram of the CM noise propagation circuit. (c) Block diagram reduction of (b). (d) Block diagram reduction of (c).

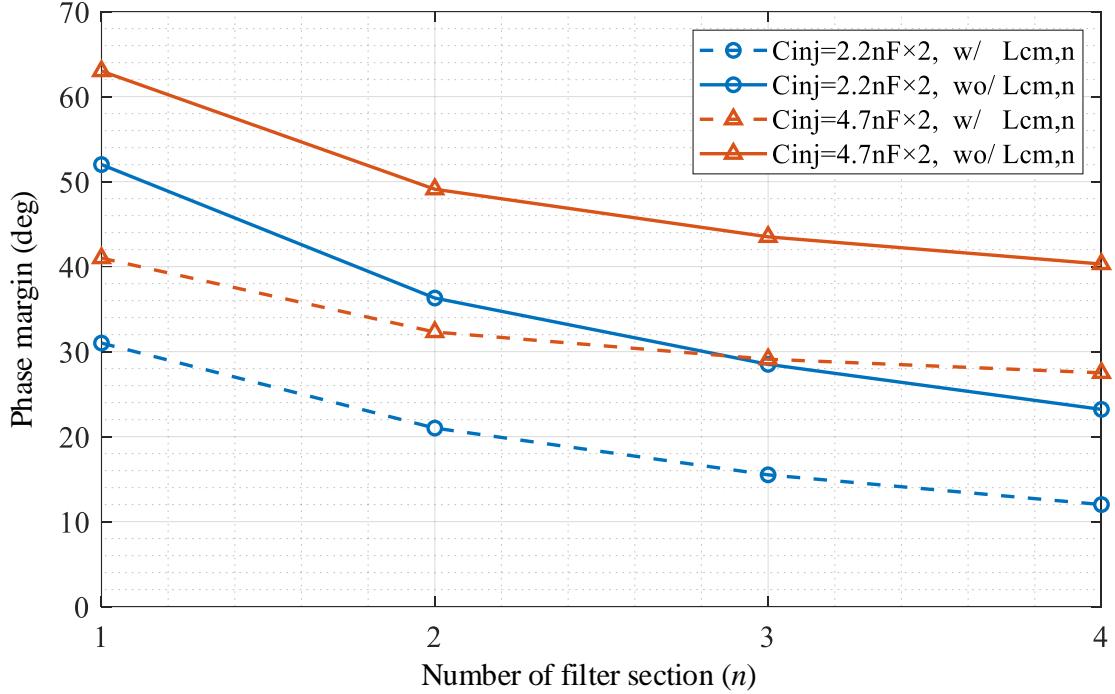


Fig. 3.10. Phase margin of the multistage ACF.

3.3.2. Optimal Number of Filter Sections

The analysis above shows the viability of using multistage ACF to achieve higher noise attenuation. The optimal number of filter sections that satisfy the required attenuation and have the smallest volume is studied. In order to achieve a specific attenuation at the design frequency, filters with different numbers of LC-stage are designed [80].

The design frequency is set at 150kHz, where the conducted EMI frequency starts. Based on the model shown in Fig. 3.9(a), the insertion loss of n -stage ACFs is expressed as

$$IL_n = 1 + \frac{nZ_{LISN,f_D} + \left(\frac{n^2+n}{2}\right)Z_{Lcm,f_D}}{Z_{act}} + \frac{\left(\frac{n^3-n}{6}\right)Z_{LISN,f_D}Z_{Lcm,f_D} + \left(\frac{n^4+2n^3-n^2-2n}{24}\right)Z_{Lcm,f_D}^2}{Z_{act}^2} + \dots + \frac{Z_{LISN,f_D}Z_{Lcm,f_D}^{n-1} + Z_{Lcm,f_D}^n}{Z_{act,f_D}^n} \quad (3.27)$$

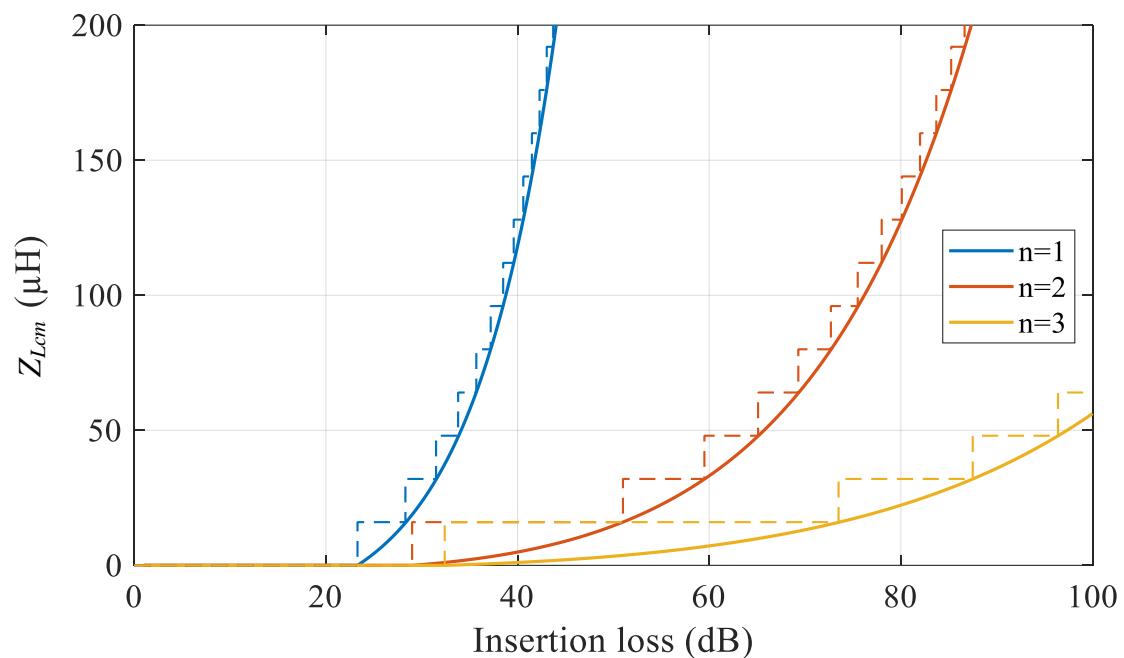
where Z_{LISN,f_D} , Z_{Lcm,f_D} , and Z_{act,f_D} are the impedance of the LISN, the CM choke, and the active capacitor at 150kHz. The proof of (3.27) is given in Appendix A.2.

The relationships between the required CM inductance and the insertion loss with $n = 1, 2$, and 3 are given in Fig. 3.11(a).

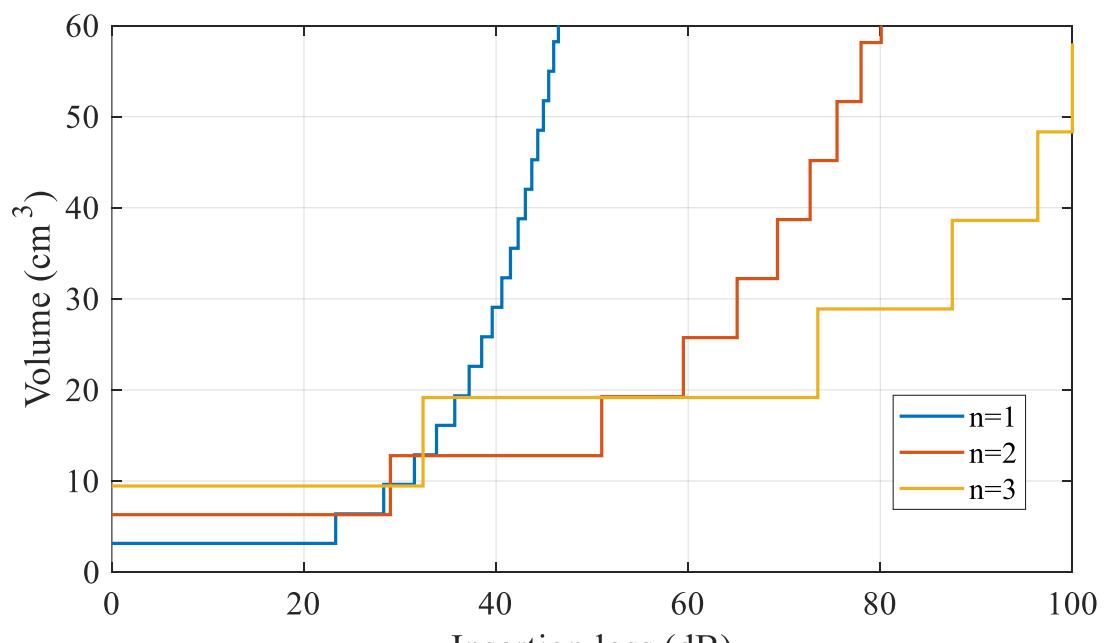
The next step is to translate the required CM inductance into the volume of the CM choke. For the sake of comparison, a 10A, 16 μ H CM choke with small DC resistance and good high-frequency response manufactured by Wurth Electronics (part no.: 7448421016) is taken as the basic unit for fabricating the required value of CM inductor. Taking the PCB volume of an active capacitor section ($3\text{cm} \times 2.1\text{cm} \times 0.5\text{cm} = 3.15\text{cm}^3$) into account, the relationships between the volume and the insertion loss with $n = 1, 2$, and 3 are shown in Fig. 3.11(b).

By comparing the volume curves of the multistage ACFs, the optimal number of ACF sections is derived and is shown in Fig. 3.11(c) (blue line). When the required attenuation is below 33.8dB, the single-stage structure is sufficient and cost-effective. Hence, the optimal number of ACF sections is modified, as shown by the red line in Fig. 3.11(c).

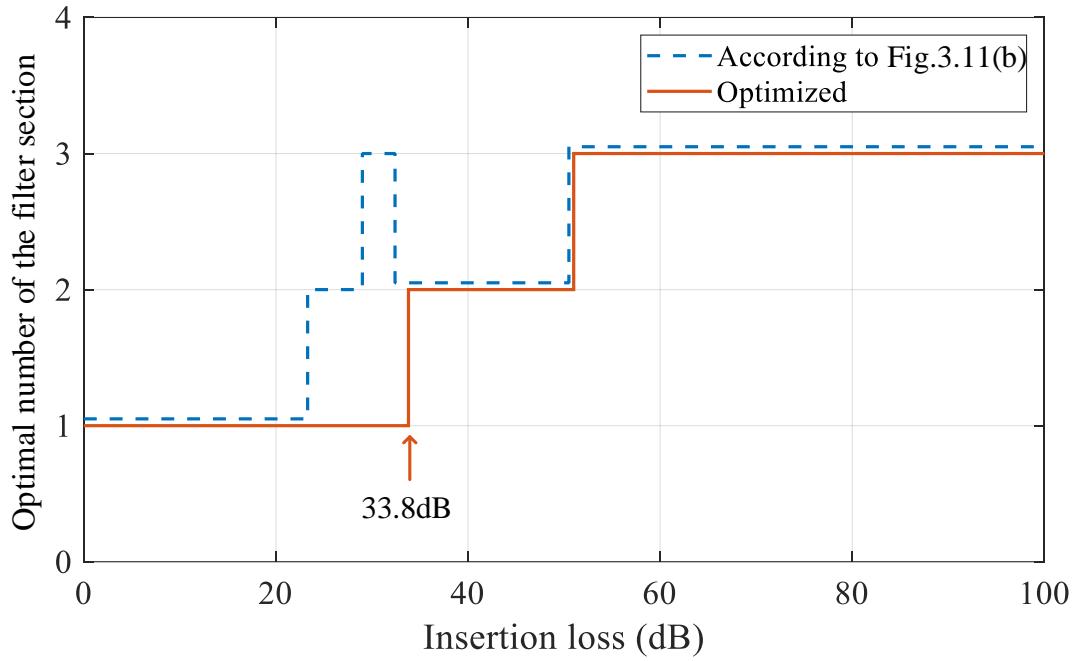
If the active capacitors in Fig. 3.9(a) are replaced by passive capacitors, the insertion losses of passive multistage CM filters are derived. A comparison of the required Z_{Lcm} is shown in Fig. 3.12. By using the proposed ACF, the required CM inductances are significantly reduced.



(a)



(b)



(c)

Fig. 3.11. Optimization of active capacitor stages for required insertion loss. (a) CM inductance. (b) Volume of ACFs with different stage numbers. (c) Optimal number of active capacitor stages.

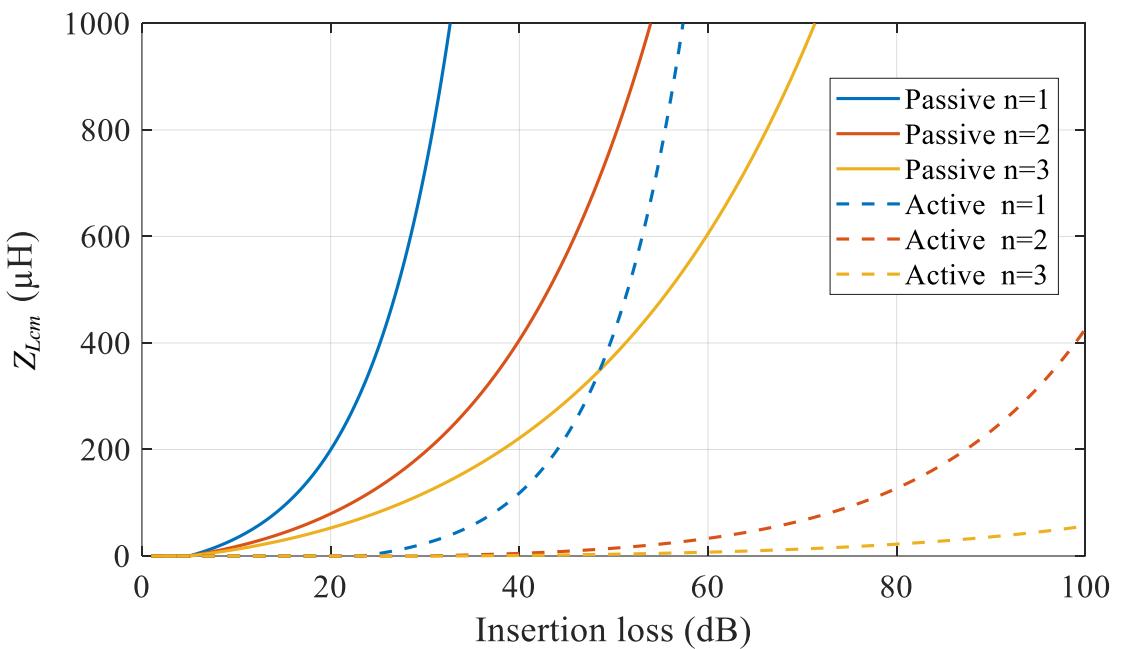


Fig. 3.12. Comparison of CM inductance curves of multistage CM passive filters and active filters.

3.4. Experimental Verification

The performance of single-stage and multistage ACFs is evaluated on two commercial power supplies with rated power of 90W for laptop adaptor and 1000W power supply for industrial applications.

3.4.1. Commercial 90W Laptop Adaptor

The proposed single-stage ACF has been applied to a commercial 90W laptop adaptor. The photos of the proposed active capacitor (A-cap), laptop adaptor, and connections of EMI measurement equipment are shown in Fig. 3.13. All original CM chokes (L_{cm1} , L_{cm2} , L_{cm3} , and earth line choke) and Y-capacitor of the laptop adaptor have been removed to test the ACF. The CM noise of the laptop adaptor has been measured under the following conditions: 1) without any CM filter, 2) with the A-cap connected but turns off its DC supply, 3) with the same passive capacitor as in the A-cap; 4) with the A-cap connected and turns on its DC supply; 5) with the A-cap and a $12.6\mu\text{H}$ CM choke, 6) with the same passive capacitor as in the A-cap and a $12.6\mu\text{H}$ CM choke, and 7) with the original passive filter, as shown in Fig. 3.14.

When turning off the DC supply of the active capacitor, transistors Q1-Q4 are in the cut-off state; C_{sen} and C_{inj} are in series with biasing resistors (values in tens of kilo-Ohm). Hence, the active capacitor only has small attenuation above 10MHz when turning off its DC supply. In order to show the performance of passive components, the CM EMI spectra of the converter with the same capacitor and inductor as in the ACF are shown in Fig. 3.14 by the yellow line.

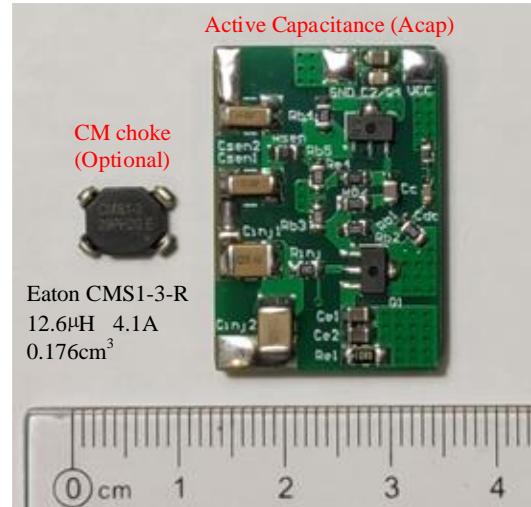
The passive capacitor has a good filtering effect from 2MHz, but it cannot suppress low-frequency noise due to the limit of Y-capacitance by safety standards. The proposed active capacitor magnifies the equivalent capacitance in the frequency range of conducted EMI; thus, it has considerable attenuation from 150kHz to 30MHz.

When the passive capacitor is used with a $12.6\mu\text{H}$ CM choke, it still cannot effectively suppress noise below 800kHz. A larger CM choke can contribute to more

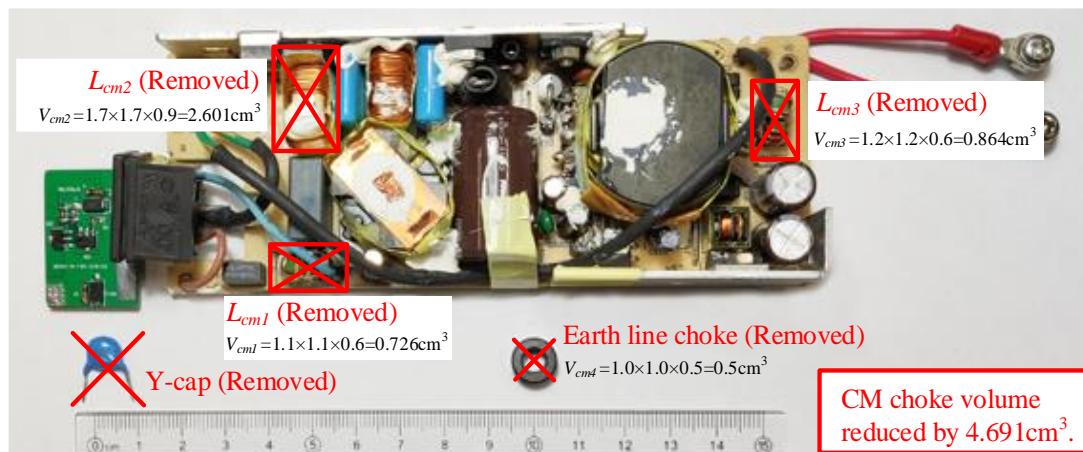
attenuation, but it will lead to bulky volume. When using the active capacitor with a $12.6\mu\text{H}$ CM choke, the high-frequency filtering performance is further improved. A higher margin against the limit line has been achieved by the proposed ACF (12dB) compared to the original passive filter (10dB at 115V and 5dB at 230V).

As shown in Fig. 3.15, the CM filter volume can be reduced by 32.5% with the proposed ACF. Since the PCB board dominates the ACF volume, further volume reduction can be expected by placing the components of the active capacitor in the adaptor or implementing it with monolithic integration.

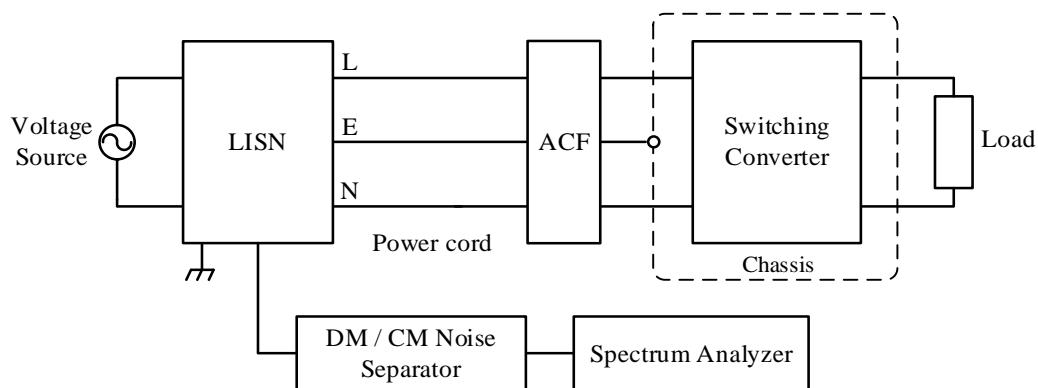
The sensing capacitance of the active capacitor is $330\text{pF} \times 2 = 660\text{pF}$, and the injection capacitance is $2.2\text{nF} \times 2 = 4.4\text{nF}$. The leakage current is 0.38mA at 240Vac, 50Hz, which is below the limit of 0.75mA for hand-held information technology (IT) equipment stated in *IEC 60950-1*.



(a)

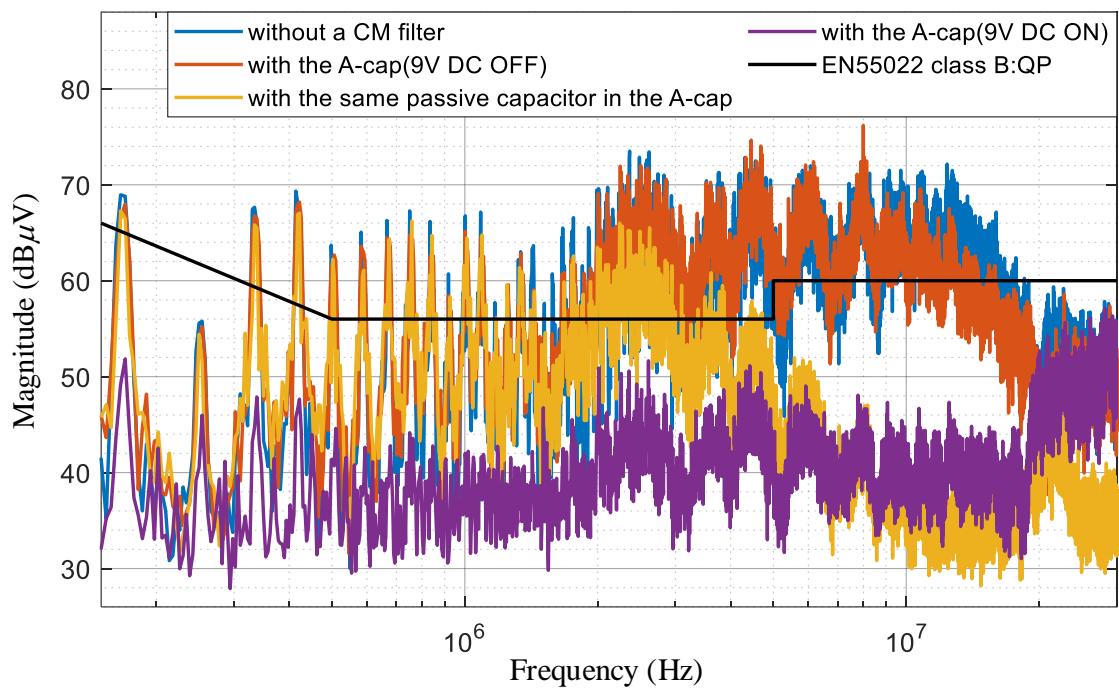


(b)

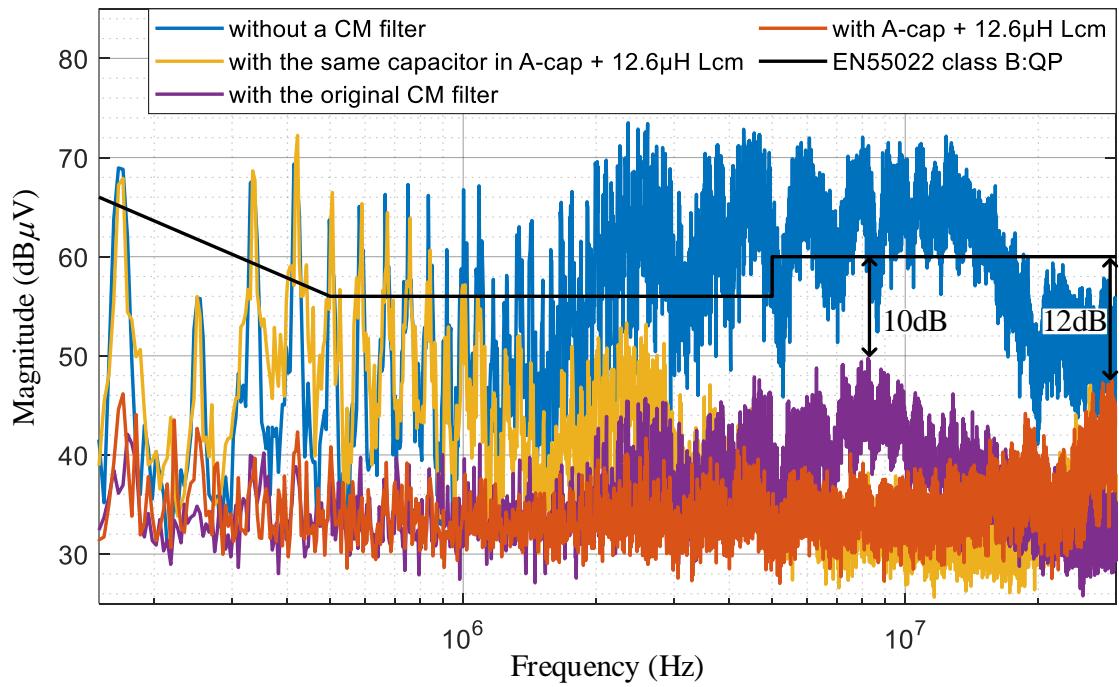


(c)

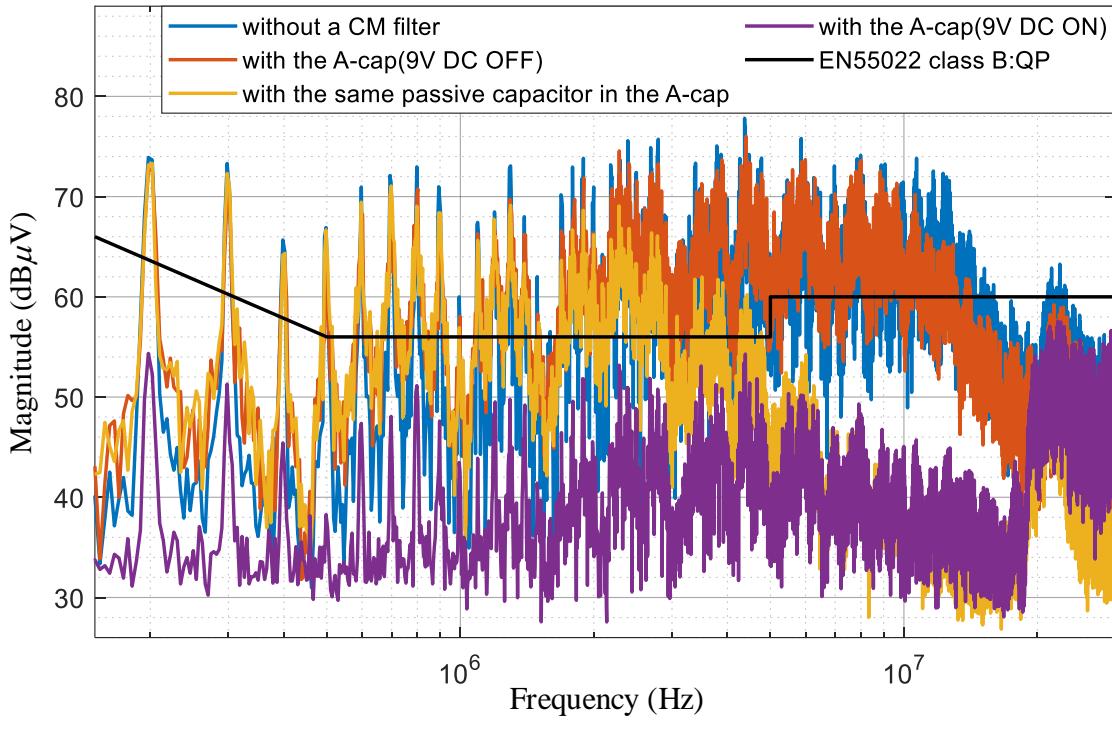
Fig. 3.13. Setup for EMI measurement. (a) The proposed active capacitor with an optional CM choke. (b) Inside view of the laptop adaptor with the ACF. (c) Equipment and connections.



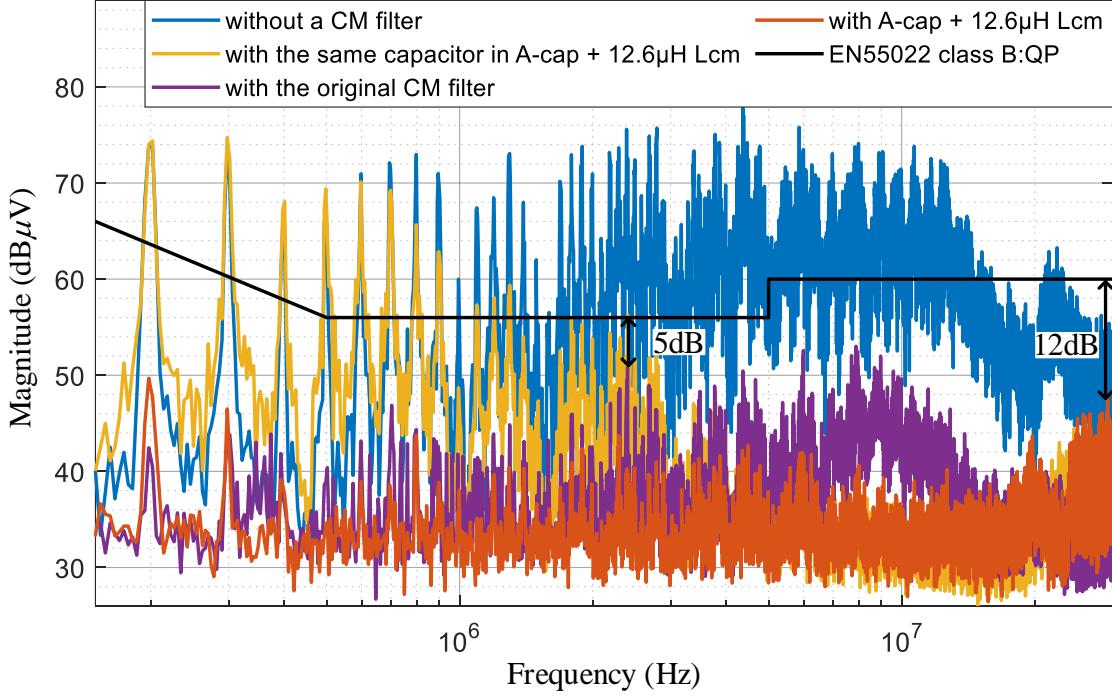
(a)



(b)



(c)



(d)

Fig. 3.14. Measured peak CM noise of the 90W laptop adaptor. (a) $V_s = 115V$, without L_{cm} . (b) $V_s = 115V$, with L_{cm} . (c) $V_s = 230V$, without L_{cm} . (d) $V_s = 230V$, with L_{cm} .

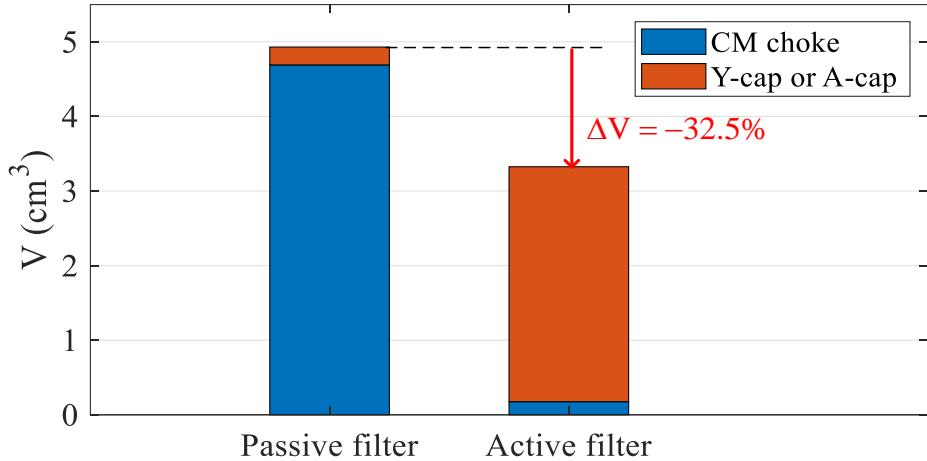


Fig. 3.15. Volume comparison of the original passive CM filter and the ACF.

3.4.2. Commercial 1000W Power Supply

The proposed CLC ACF has been applied to a commercial 1000W power supply that has universal input and 48Vdc output voltage. The photos of the CLC ACF and the 1000W power supply are shown in Fig. 3.16(a) and (b). The comparison of the converter with the original passive filter and the proposed CLC ACF is shown in Fig. 3.16(c). The comparison of the volume of CM chokes is shown in Fig. 3.16(d). The CM choke volume is reduced by 90.3%. All original CM chokes (L_{cm1} , L_{cm2} , L_{cm3}) and Y-capacitors of the power supply have been removed when testing the performance of the proposed ACF.

The CM noise measurements of the 1000W power supply under the following conditions: 1) without a CM filter, 2) with a single-stage ACF (an A-cap and a $16\mu\text{H}$ CM choke), 3) with a passive LC filter having the same values as in the ACF, 4) with the two-stage CLC ACF, and 5) with a passive CLC filter having the same values as in the ACF, have been shown in Fig. 3.17(a) and (b). The solid line and the dotted line present the results under low- and high-line conditions, respectively.

The passive CM filter with the same values in the ACF can only attenuate high-frequency noise but cannot attenuate low-frequency noise. The proposed ACF has a wider filtering bandwidth from 150kHz to 30MHz.

In order to make a fair comparison of filter volume, the proposed ACF should have similar filtering attenuation to the original passive filter. Since the CM spectra of the converter with the CLC ACF are already below the limit line, there is no need to add one more active section. Instead, an LC passive section, which has $16\mu\text{H}$ CM inductance and 4.4nF Y-capacitance, is added between the converter and the CLC ACF to further increase noise attenuation, particularly in the high-frequency range. As shown in Fig. 3.17(c) and Fig. 3.18, the proposed CLC ACF with an LC passive section has a similar EMI margin (5.4dB and 6dB) compared to the original passive filter, but the volume is reduced by 61.7%.

The total sensing capacitance of the CLC ACF is $330\text{pF} \times 2 \times 2 = 1.32\text{nF}$, and the total injection capacitance is $4.7\text{nF} \times 2 \times 2 = 18.8\text{nF}$; the additional Y-capacitance is 4.4nF . The leakage current is 1.85mA at 240V_{ac}, 50Hz, which is below the limit of 3.5mA for movable or stationary IT equipment stated in *IEC 60950-1*.

The CM inductance reduction also contributes to the reduction of DC resistance R_{dc} of CM chokes. By using a high-precision LCR meter (GW Instek LCR-819), the total R_{dc} , including the resistance in both windings, of the two $16\mu\text{H}$ CM chokes is $4.4 \times 2 = 8.8\text{m}\Omega$, and the total R_{dc} of the original CM chokes is $5.6\text{m}\Omega + 35.8\text{m}\Omega + 31.6\text{m}\Omega = 73\text{m}\Omega$, which will result in 5.52W power loss at low-line and 1.38W power loss at high-line with 1000W input power. A comparison of power dissipation in the original passive CM filter and the proposed ACF has been shown in Table 3.3. Due to the power loss reduction in the CM choke, the total power dissipation of the ACF is smaller than that of the passive CM filter.

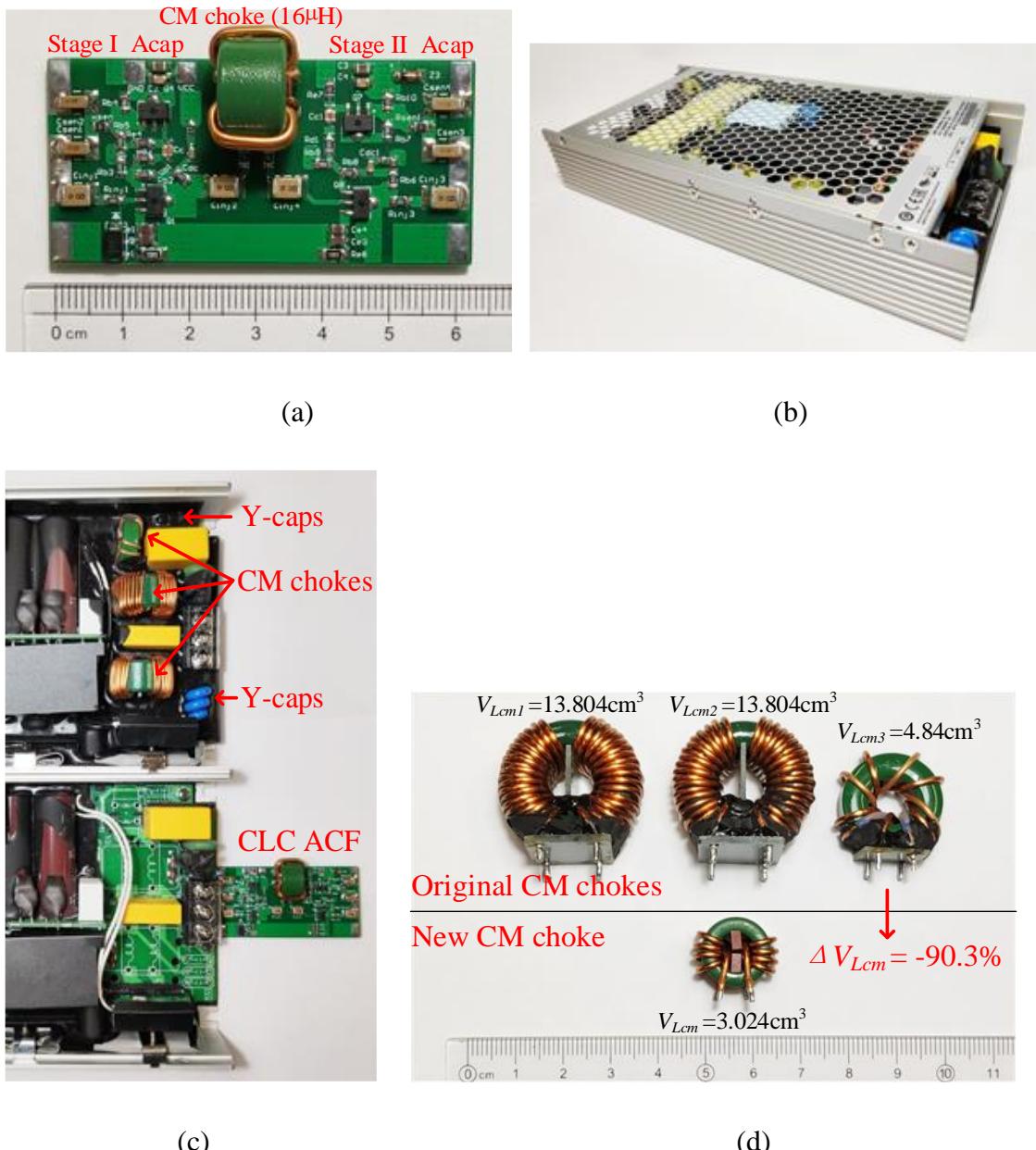
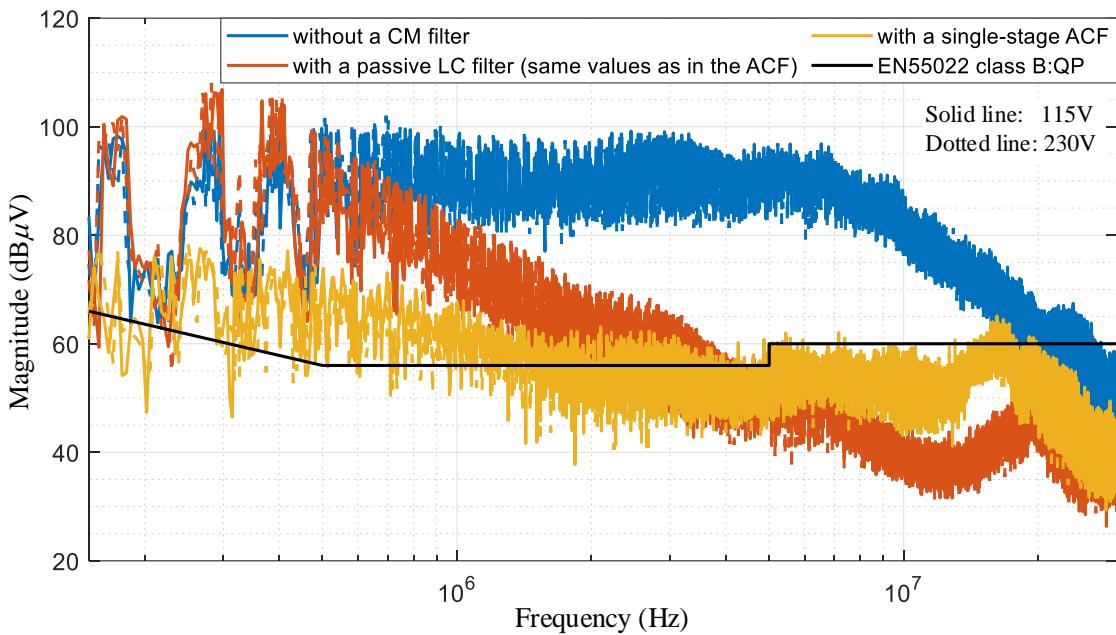
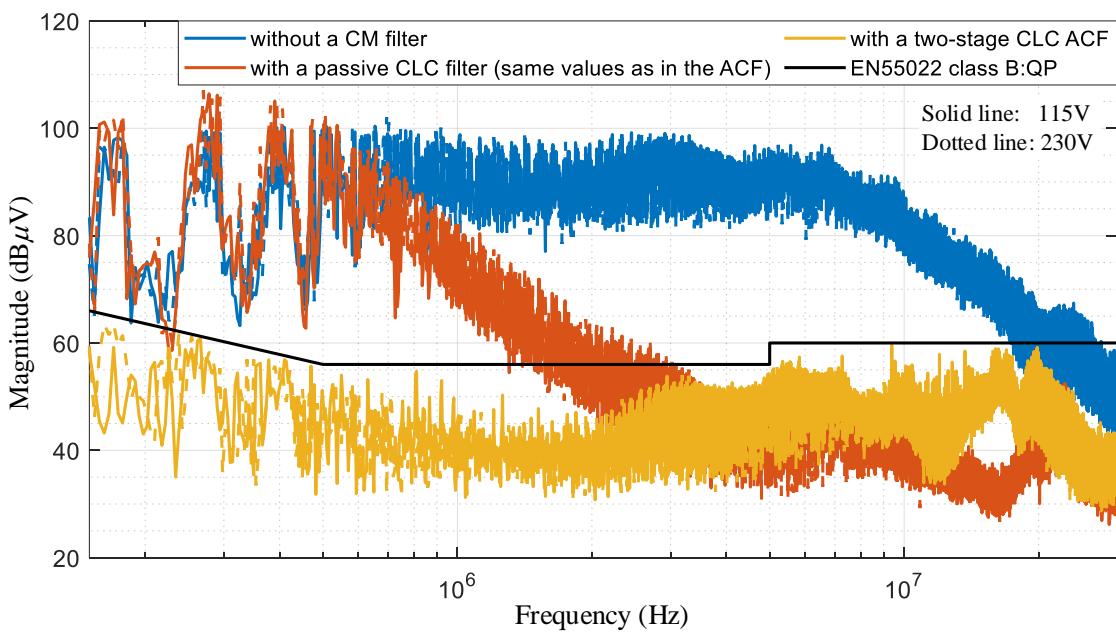


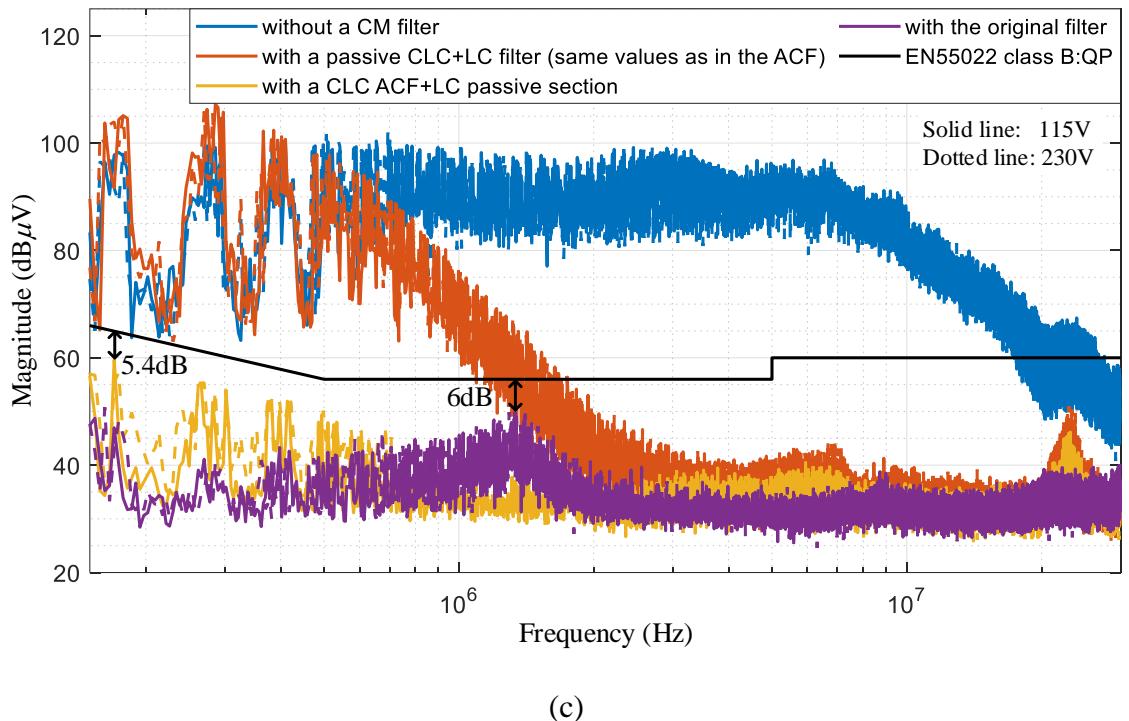
Fig. 3.16. Setup for EMI measurement. (a) The proposed CLC ACF. (b) Commercial 1000W power supply. (c) Comparison of the converter with the original passive filter and the proposed CLC ACF. (d) Comparison of the volume of CM chokes.



(a)



(b)



(c)

Fig. 3.17. Measured peak CM noise of the 1000W power supply. (a) Single-stage CM filters. (b) Two-stage CM filters. (c) Three-stage CM filters.

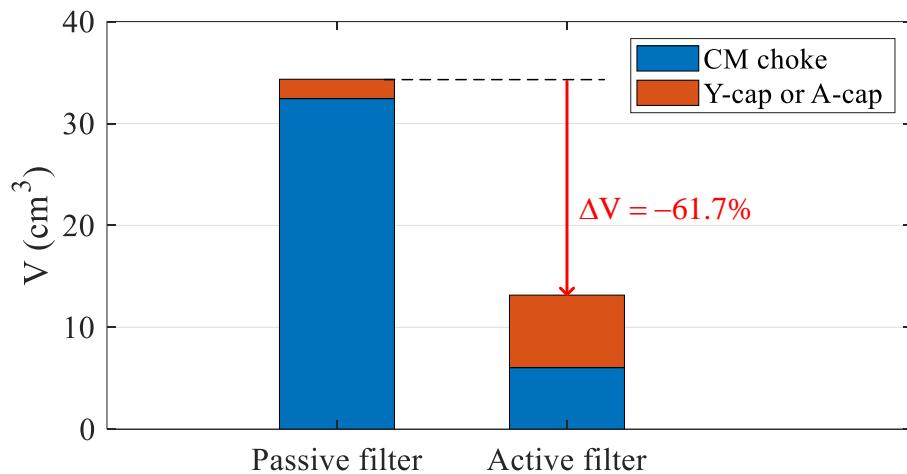


Fig. 3.18. Volume comparison of the original passive CM filter and the ACF.

TABLE 3.3

Comparison of Power Dissipation in the Passive and Active CM Filter

	Original CM Filter	Active CM Filter		
		P_{Lcm} (W)	P_{Lcm} (W)	P_{active} (W)
115V	5.52	0.665	1.206	1.871
230V	1.38	0.166	1.206	1.372

3.5. Chapter Summary

A high-attenuation wideband active CM filter section has been proposed in this chapter. Considering that the CM noise power is much smaller than the converter input power, a class-A amplifier with higher linearity than commonly used class AB amplifiers is used, even though the latter has higher power efficiency than the former. The class-A amplifier consists of a CC and a CE amplifier, rather than using the configuration of IC Op-amps, which reduces the effects of the parasitic parameters among discrete components and increases the bandwidth up to 30MHz. The high attenuation is achieved by the high-gain CE amplifier with an active load.

This chapter also extends the concept of the ACF to multistage configuration for pursuing a higher attenuation. The optimal number of ACF sections at a specific insertion loss has been given, which facilitates the design of ACFs for various applications. The design philosophy of the multistage ACF is to use minimal CM inductance and exploit the full potential of active devices; hence, significant CM filter volume reduction has been achieved. Further volume reduction is expected by monolithic integration. The power dissipation of the ACF is comparable with that of conventional passive filters and accounts for a small portion of the converter input power. The proposed ACF has been tested on two commercial products, a 90W laptop adaptor, and a 1000W power supply. The EMI measurement results show that the proposed ACF is an effective solution for CM noise suppression.

Chapter 4

OUTPUT ACTIVE COMMON-MODE FILTER

4.1. Chapter Introduction

Electric motors have been widely used in both household and industrial applications. PWM inverters-fed motor drives offer higher efficiency and better performance compared to traditional ones. However, the CM voltage generated by PWM inverters is stepwise; the high dv/dt causes CM current through parasitic capacitances, raising concerns of electromagnetic interference (EMI) [1].

A portion of the CM current will flow to the ground through motor bearings. The CM current also generates magnetic flux around the motor shaft and induces a shaft voltage [81], [82]. If this shaft voltage exceeds the insulation of the lubricant film in bearings, a circulating current will flow through a loop of “shaft-bearings-motor frame.” High bearing current will damage bearings in the forms of fluting, frosting, pitting, spark tracks, and welding [83], and finally lead to bearing failure. The mitigation methods for bearing failure can be classified into three approaches [84]: first, reinforce the insulation of bearings by using isolated bearings, such as ceramic bearings; second, bypass the bearing with a low-impedance path, such as grounding brushes/rings fabricated with conductive microfibers; third, reduce dv/dt by CM filters or cancellation techniques for paralleled inverters [20].

CM filters are most widely used to reduce EMI and protect bearings due to their low cost, robustness, and flexibility [85]-[88]. Passive RLC filters connected at the output of inverters can effectively reduce dv/dt , but their high power loss and bulky volume hinder the advance in power efficiency and density [84].

ACF are proposed for compactness by using active filtering techniques. The current-compensation ACFs can achieve high attenuation and compact size [89]-[61], especially for the voltage-sensing and current-compensation ACFs, since they do not need

transformers in either sensing or compensation stage [60], [61]. However, they circulate the CM current while leaving the CM voltage at motor terminals unchanged; only EMI noise flowing into the grid is attenuated, but the bearings still suffer from the original motor CM current. In such cases, an additional dv/dt filter for bearing protection is required. As an advantage, voltage-compensation ACFs alter the CM voltage profiles and thus reduce CM noise and protect bearings simultaneously; this makes voltage-compensation ACFs more suitable for motor drive systems.

A feedforward voltage-compensation ACF for motor drives is proposed in [51], and then continuous works have been devoted to advancing this design. Reference [90] proposes the use of an external power supply and a step-down turns ratio so that low-voltage BJTs can be used in high-voltage applications. Darlington pairs are used in the push-pull amplifier to reduce the loading effect. The push-pull amplifier is of class B type, which may have crossover distortion. Feedback voltage-compensation ACFs have also been proposed as an alternative approach [53], [91]; expensive high-voltage operational amplifiers are required for high-voltage motor drives. Furthermore, integrations of feedforward and feedback ACFs have been proposed to pursue better filtering performance [92], [93].

Aimed at eliminating the CM voltage, the prior art voltage-compensation ACFs duplicate the entire CM voltage, including both steep edges and high-amplitude plateaus. Significant power consumption becomes inevitable, especially in high-voltage motor drives; it also leads to bulky heatsinks, reducing power density. A high inductance is thus required to reduce the current and the resulting power dissipation of the ACFs [89]. In order to reduce the power dissipation and inductance, this chapter has proposed a new ACF that compensates for the rising/falling edges of CM voltage only. Both the CM noise spectrum at the grid interface and the CM current flowing through the motor are reduced.

The filters discussed above are all connected at the output of inverters; thus, they are called output filters. Since output filters cannot attenuate the CM current leaked from

inverters, filters connected at the input of inverters are inevitable and are called input filters.

This chapter proposed a holistic active CM filtering architecture for motor drive systems, including the input ACF proposed in Chapter 3 [94] and the new output ACF. The input ACF is used to attenuate CM noise injected into the grid. The output ACF is primarily devoted to reducing dv/dt for bearing protection; it also aids the input ACF to attenuate the CM noise.

4.2. Analysis and Design of the Output Active CM Filter

The proposed output ACF consists of three stages: reference stage, buffer stage, and output compensation stage. It is shown in Fig. 4.1.

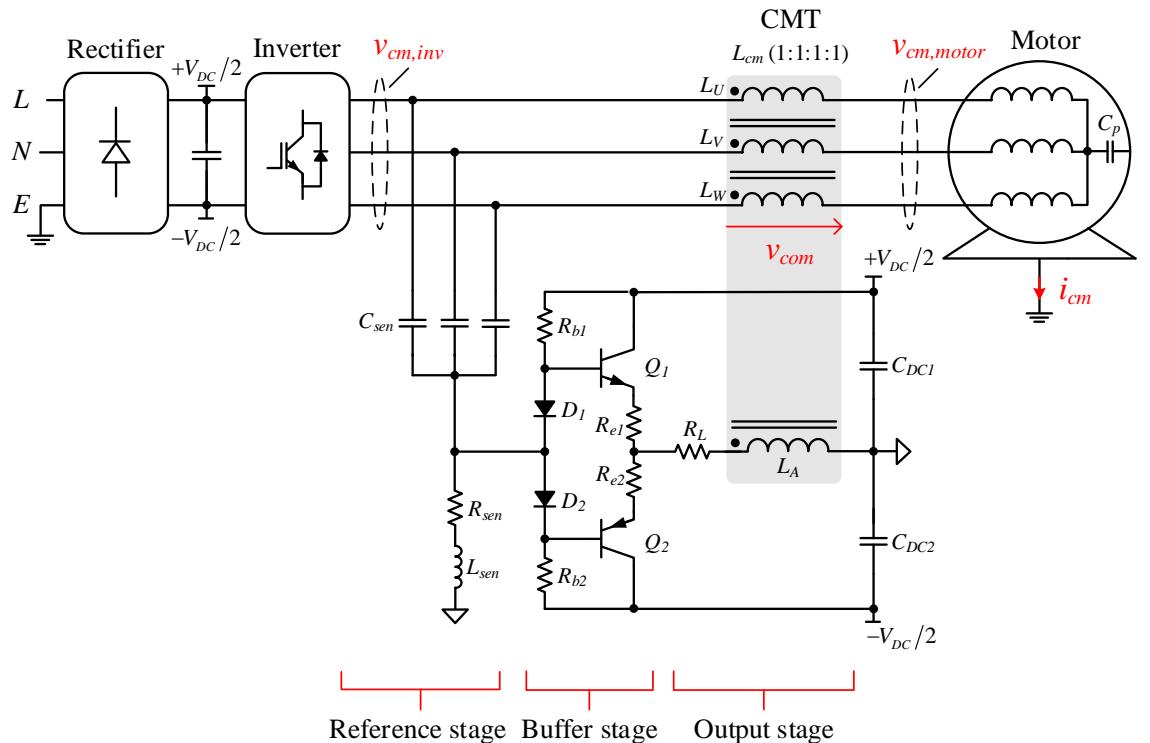


Fig. 4.1. Schematic diagram of the proposed output ACF.

4.2.1. Design of the Reference Stage

The CM transformer (CMT) shown in Fig. 4.1 has one primary winding (L_A) and three secondary windings (L_U , L_V , and L_W). A compensation voltage v_{com} is applied to the primary winding and then coupled to the secondary windings. Upon compensating the inverter-side CM voltage $v_{cm,inv}$ by v_{com} , the motor-side CM voltage $v_{cm,motor}$ will have a much smaller dv/dt . Fig. 4.2 shows four possible compensated waveforms. Fig. 4.2(a) shows a smooth start but a sharp end at the plateau; Fig. 2(b) shows a profile opposite to that in Fig. 4.2(a); Fig. 4.2(c) shows a profile having both smooth start and end but a steep rise in the middle; Fig. 4.2(d) shows a profile having a constant rising slope, which is between the steepest and smoothest ones in Figs. 4.2(a)-(c).

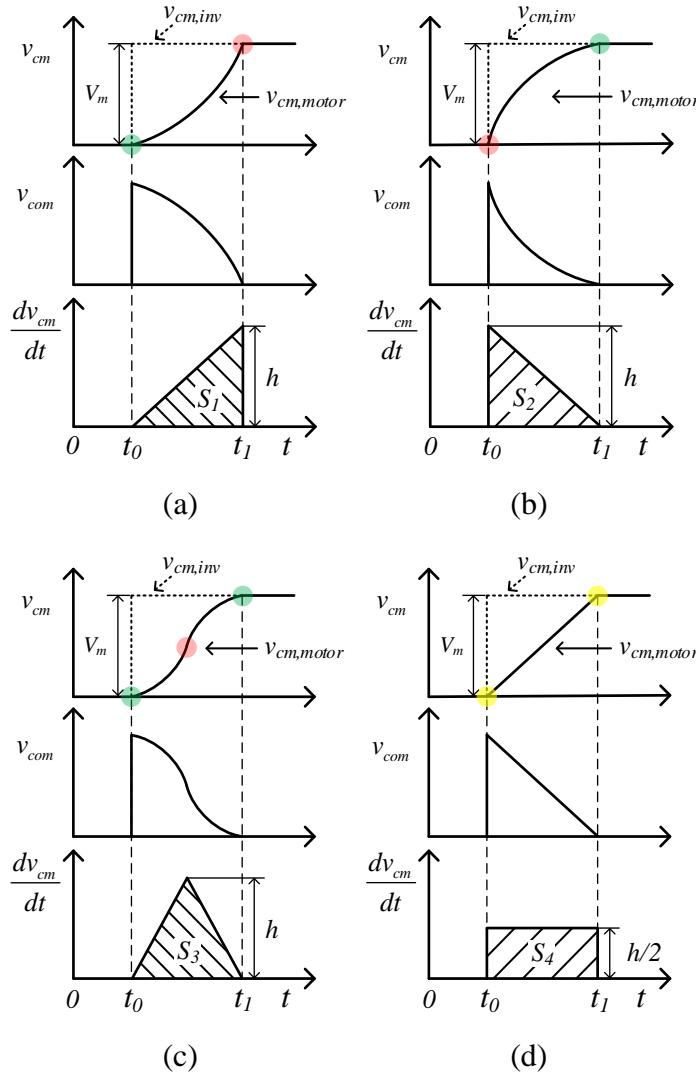


Fig. 4.2. Four possible waveforms of edge compensation.

The integral of $dv_{cm,motor}/dt$, illustrated by the shaded regions, is the increment of $v_{cm,motor}$, as expressed in (4.1). In the four cases, $v_{cm,motor}$ all rises from zero to V_m during an interval of $(t_1 - t_0)$. Hence, one can conclude $S_1 = S_2 = S_3 = S_4$.

$$S = \int_{t_0}^{t_1} \frac{dv_{cm,motor}}{dt} dt = V_m \quad (4.1)$$

Since the time intervals are the same, the peak values of $dv_{cm,motor}/dt$ in Figs. 4.2(a)-(c) are identical while that in Fig. 4.2(d) is one-half of the previous ones. Without loss of generality, more rising patterns exist, and the integrals of $dv_{cm,motor}/dt$ will remain the same. Based on knowledge of geometry, Fig. 4.2(d) has the lowest amplitude of $dv_{cm,motor}/dt$.

The CM current is the displacement current flowing through the parasitic capacitor C_p excited by $v_{cm,motor}$. The waveforms shown in Fig. 4.2(d) leads to the lowest peak CM current. Since the damage to bearings is determined by the peak motor CM current [95], [96], a triangular compensation voltage is optimal.

The triangular voltage is obtained with an RLC sensing circuit, as shown in Fig. 4.1. The values of RLC components are designed as follows.

1) C_{sen} : Since the sensing capacitors C_{sen} are connected at the output of the inverter, C_{sen} increases the total output capacitance of switching devices and leads to more switching loss. Hence, a small value of C_{sen} is preferred. C_{sen} is chosen to be 100pF each. A further smaller value might not be sufficient to dominate the effect of the parasitic elements.

2) R_{sen} : The equivalent circuit of the voltage reference generator is shown in Fig. 4.3, and the voltage reference v_{ref} is expressed as

$$L_{sen} C_{sen} \frac{d^2 v_{Csen}(t)}{dt^2} + R_{sen} C_{sen} \frac{dv_{Csen}(t)}{dt} + v_{Csen}(t) = V_m \quad (4.2)$$

$$v_{ref}(t) = V_m - v_{Csen}(t) \quad (4.3)$$

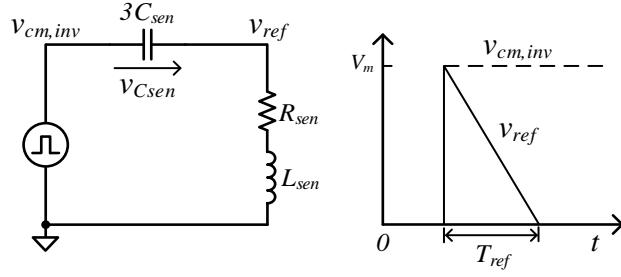


Fig. 4.3. The equivalent circuit of the voltage reference generator and its voltage waveforms.

The circuit is a typical second-order system. The step response under different damping factors is illustrated in Fig. 4.4(a). The damping factor ζ is expressed as

$$\zeta = \frac{R_{sen}}{2\sqrt{L_{sen}/C_{sen}}} \quad (4.4)$$

The waveforms of v_{ref} with different ζ are shown in Fig. 4.4(b). v_{ref} does not decline with an ideal constant slope as the desired waveform shown in Fig. 4.2(d); it has a long tail. Thus, the reference compensation time T_{ref} is defined as twice $T_{50\%}$ in which v_{ref} drops to one-half of its peak value, that is, $T_{ref} = 2T_{50\%}$. $T_{50\%}$ can be calculated by using the following equation.

$$v_{ref}(T_{50\%}) = \frac{1}{2}V_m \quad (4.5)$$

However, (4.5) is a transcendental equation without a closed-form solution. In order to facilitate the design, the second-order RLC circuit is reduced to a first-order RC circuit which has the same waveforms as shown in Fig. 4.2(b). Then, (4.2) is reduced into the form of (4.6), and T_{ref} is expressed as (4.7).

$$R_{sen}C_{sen} \frac{dv_{Csen}(t)}{dt} + v_{Csen}(t) = V_m \quad (4.6)$$

$$T_{ref} = 2 \ln 2 R_{sen} C_{sen} \quad (4.7)$$

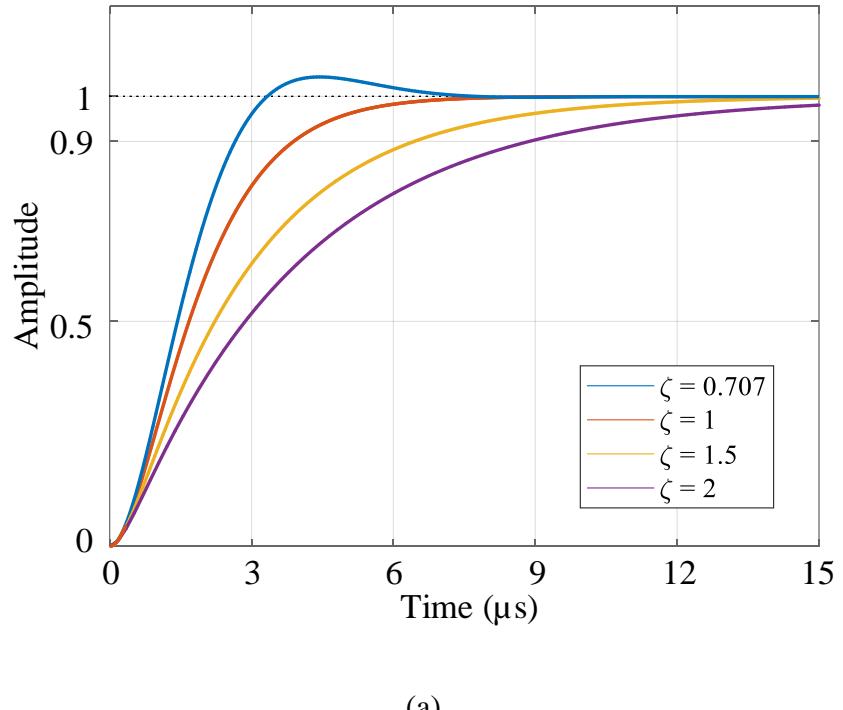
When T_{ref} is specified to fulfill the specifications of a system, R_{sen} can be derived as

$$R_{sen} = \frac{T_{ref}}{2 \ln 2 C_{sen}} \quad (4.8)$$

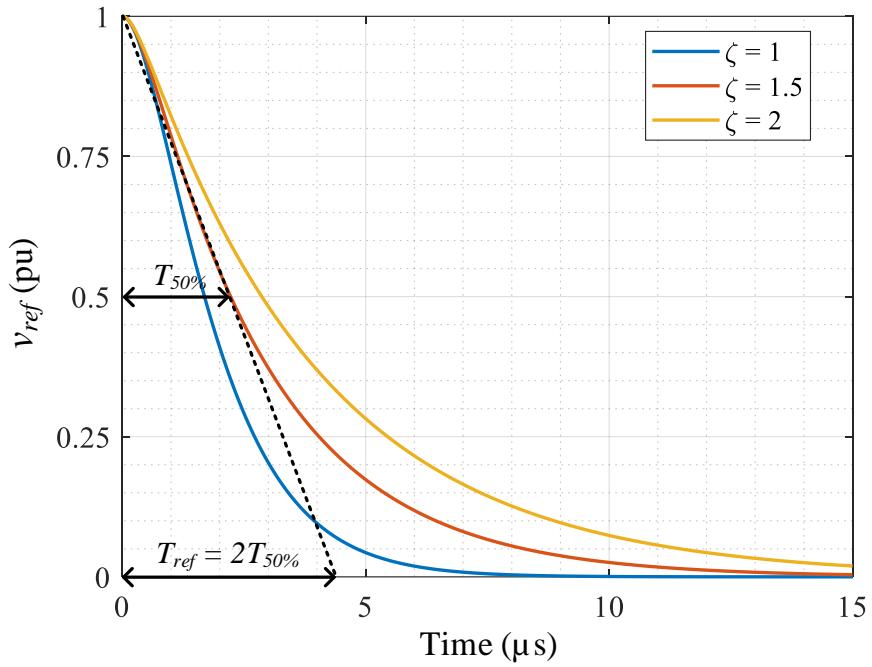
It should be noted that (4.6) is an approximation of (4.2), and a more accurate solution can be easily obtained by using simulation software. Derived from (4.6), (4.8) offers a starting point to fine-tune parameters on a simulator.

3) L_{sen} : L_{sen} is introduced to regulate the response of an RC circuit to approach the ideal triangular waveform. The triangular profile holds only for the initial $T_{50\%}$ because a tail voltage will inevitably appear afterward. Although the tail voltage makes the voltage transition smoother in implementation, the worst case is considered in this design phase.

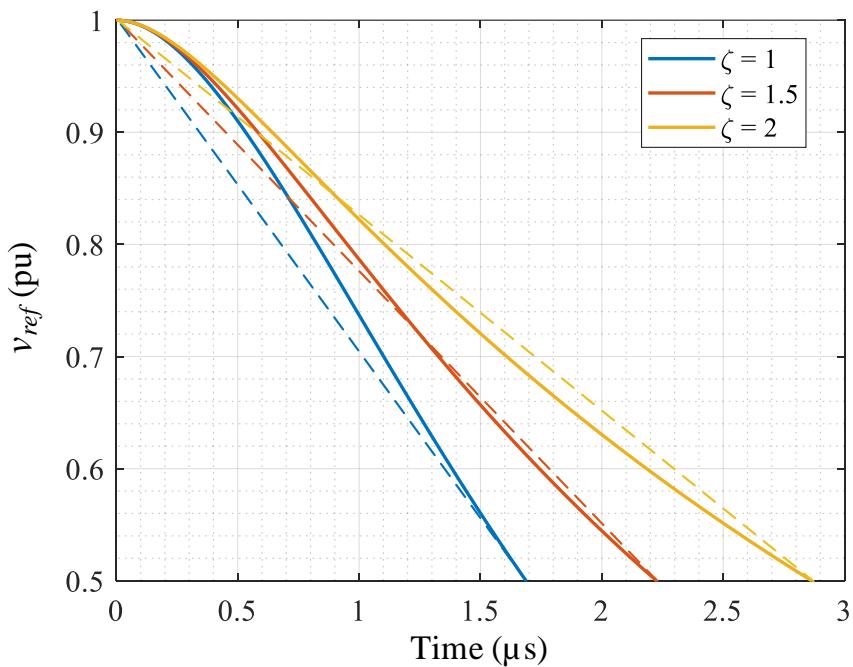
As shown in Fig. 4.4(c), when damping factor ζ is around 1.5, the initial half of v_{ref} has the most ideally constant slope. Hence, let $\zeta = 1.5$ and then L_{sen} can be derived.



(a)



(b)



(c)

Fig. 4.4. Waveforms of a second-order system with different ζ . (a) Step responses. (b) Voltage reference v_{ref} . (c) Zoomed waveforms of v_{ref} .

4.2.2. Design of the Buffer Stage

The buffer stage should have a high input impedance and a low output impedance. As shown in Fig. 4.1, a BJT-based class AB amplifier is used as the buffer stage. 300V, 150MHz, NPN KSC3503, and PNP KSA1381 are chosen for their high-voltage and high-bandwidth properties. Bias resistors (R_{b1} and R_{b2}) and diodes (D_1 and D_2) are used in the biasing circuit. Emitter resistors (R_{e1} and R_{e2}) are used to avoid thermal runaway.

In prior art, the output stage has a coupled inductor only. A high-value inductance is thus required to reduce the loading effect. If the inductance is not sufficiently high, Darlington pairs, which have a high current gain that results in a low output impedance, will be used. However, the bandwidth is compromised with Darlington pairs [97].

In the proposed design, the output stage consists of a resistor R_L and a coupled inductor L_{cm} . The resistive component of the output impedance of a conventional class AB amplifier is much smaller than R_L , and the inductive component is negligible compared to L_{cm} . Darlington pairs are thus not necessary for the proposed buffer stage. Hence, the proposed design has a simpler structure, wider bandwidth, and lower cost.

4.2.3. Design of the Output Stage

In the class AB amplifier, the NPN and PNP transistors conduct alternately, and the supply voltage is one-half of the DC link voltage V_{DC} . Hence, the power dissipation in the output ACF P_{loss} is expressed as

$$P_{loss} = \frac{1}{T_{sw}} \int_0^{T_{sw}} \frac{1}{2} V_{DC} i_L(t) dt = \frac{1}{2} V_{DC} |i_L|_{ave} \quad (4.9)$$

where T_{sw} is the switching period of the inverter. Since the direction of inductor current i_L changes during the operation of the push-pull amplifier, $|i_L|_{ave}$ is the average of the absolute value of i_L .

Given V_{DC} is predefined, a lower P_{loss} can be obtained if i_L is reduced. Since only L_{cm} is used in prior art, i_L can only be reduced by using a high inductance, resulting in a bulky CM transformer.

In the proposed output ACF, a resistor R_L is introduced into the output stage to reset i_L and thus reduce P_{loss} . The equivalent circuit of the proposed output stage is shown in Fig. 4.5(a). The voltage across the coupled inductor v_{com} is determined by primary-side and secondary-side excitations, as expressed as

$$v_{com} = L_{cm} \frac{di_L}{dt} + M \frac{di_{cm}}{dt} \quad (4.10)$$

where M is the mutual inductance.

v_{com} is dominated by the primary side based on two reasons. First, the high inductance of motor windings in the secondary loop mitigates the CM current. Second, the inductance L_{cm} in the proposed design is not very large to avoid bulkiness, which makes the primary-side current dominate the secondary-side current. Thus, Fig. 4.5(a) can be simplified as Fig. 4.5(b) to facilitate the circuit design.

Based on Fig. 4.5(b), i_L is described in (4.11). The excitation source v_{ref} is a piecewise function. In the first interval ($0 < t < T_{ref}$), v_{ref} decreases to zero with a constant slope. In the second interval ($t > T_{ref}$), $v_{ref} = 0$. Waveforms of v_{ref} , v_{com} , and i_L are shown in Fig. 4.6(a).

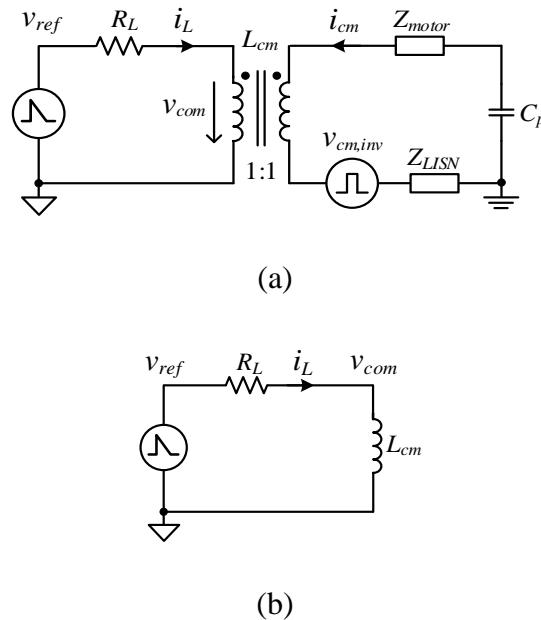
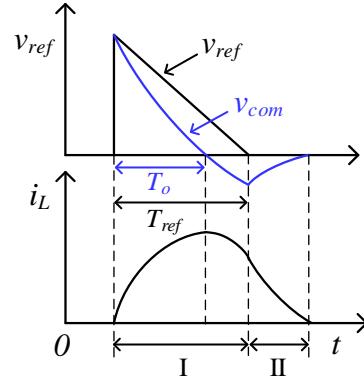
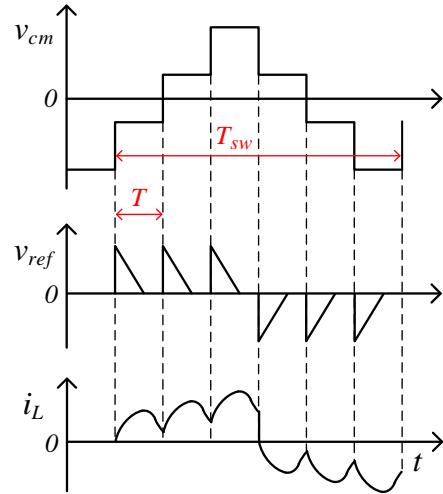


Fig. 4.5. Equivalent circuit of the output stage. (a) Full model. (b) Simplified model.



(a)



(b)

Fig. 4.6. Waveforms of the output stage. (a) waveforms excited by a single pulse. (b) waveforms during a switching cycle.

$$L_{cm} \frac{di_L(t)}{dt} + R_L i_L(t) = v_{ref}(t) \quad (4.11)$$

$$\begin{cases} v_{ref,I}(t) = V_m - \frac{V_m}{T_{ref}} t \\ v_{ref,II}(t) = 0 \end{cases}$$

$$\begin{cases} i_{L,I}(0) = 0 \\ i_{L,II}(0) = i_{L,I}(T_{ref}) \end{cases} \quad (4.12)$$

When a large R_L is used, i_L will decrease to zero before the next pulse appears, as shown in Fig. 4.6(a). In such a case, $|i_L|_{ave}$ in (4.9) can be calculated from a single pulse.

On the contrary, if R_L is not sufficiently large to reset i_L , the profiles of i_L in each pulse are not the same. Hence, (4.12) is revised as (4.13) to calculate i_L in an iterative way.

$$\begin{cases} i_{L,n,I}(0) = i_{L,n-1,II}(T - T_{ref}) \\ i_{L,n,II}(0) = i_{L,n,I}(T_{ref}) \end{cases} \quad (4.13)$$

where T is the interval between two pulses, and $T = T_{sw}/6$ in this illustration.

It should be noted that different modulation schemes have different switching patterns, and T will also fluctuate in different switching cycles when a specific modulation is in use. For the sake of simplicity, $T = T_{sw}/6$ is taken as an average of different switching patterns in this illustration. When i_L is obtained from (4.11) and (4.13), the power consumption of the ACF can be derived according to (4.9).

Same as $T_{50\%}$ used in the reference stage design to exclude the tail voltage effect, the slope of v_{com} is also calculated from its first half waveform.

$$v_{com}(T_{o,50\%}) = L_{cm} \frac{di_L(T_{o,50\%})}{dt} = \frac{1}{2} V_m \quad (4.14)$$

Based on (4.11) and (4.14), the output compensation time T_o can be calculated as (4.15). It is a measure of the slope of CM voltage after compensation.

$$T_o = \frac{2L_{cm}}{R_L} \ln \left[\frac{2(L_{cm} + R_L T_{ref})}{R_L T_{ref} + 2L_{cm}} \right] \quad (4.15)$$

Based on the above analysis, P_{loss} and T_o are functions of T_{ref} , R_L , and L_{cm} when V_{DC} and T_{sw} are predefined, which can be expressed as

$$\begin{cases} P_{loss} = f(T_{ref}, R_L, L_{cm}) \\ T_o = g(T_{ref}, R_L, L_{cm}) \end{cases} \quad (4.16)$$

It is challenging to obtain the solution of this multidimensional optimization problem. Hence, the dimensionality reduction method is used to facilitate the design. The first step is to investigate the impact of R_L and L_{cm} on P_{loss} and T_o with a fixed T_{ref} , a local optimum will be found. In the second step, the global optimum is identified by comparing

the local optimums calculated from different values of T_{ref} .

Fig. 4.7 shows the 3-D curves of P_{loss} and T_o as a function of R_L and L_{cm} , respectively, at a fixed T_{ref} . A larger L_{cm} corresponds to a higher T_o and thus smaller dv/dt , but the resulting bulky inductor is a concern. A higher R_L can reduce P_{loss} , but T_o will drop; the compensation performance is thus compromised. Hence, finding appropriate R_L and L_{cm} is of great importance.

By drawing different contours, the 3-D curves shown in Fig. 4.7 are flattened into 2-D curves and combined into one graph, as shown in Fig. 4.8. The red line and the black line represent P_{loss} and T_o , respectively.

The ACF is used to reduce dv/dt and CM current i_{cm} to protect bearings. Bearings of different sizes and materials have different immunity to i_{cm} . The switching frequency f_{sw} also affects the amplitude of i_{cm} . Thus, T_o should be designed according to the requirement of a specific application. For the cases in the early design phase, i_{cm} can be calculated by using EMI prediction methods. For the cases that a prototype is available, one can measure i_{cm} and set a T_o to reduce i_{cm} below a safety level.

Based on (4.9) and (4.11), P_{loss} is determined by V_{DC} , f_{sw} , T_{ref} , R_L , and L_{cm} ; it does not directly depend on the power rating of motor drive systems. Thus, the abovementioned design procedure for determining filter parameters is applicable for systems of different rated power.

The procedure of selecting the values of R_L and L_{cm} is given as follows:

Step 1: Select P_{loss} and T_o for a specific application.

For example, let P_{loss} accounts for 1% of the total power of the motor drive system. T_o is selected to reduce the peak CM current below a safe level for bearing protection. Since there is currently no standard to regulate the CM current flowing through the motor, the maximum allowable CM current is determined by considering the motor specifications. As a case study, $P_{loss} = 10W$ and $T_o = 4\mu s$.

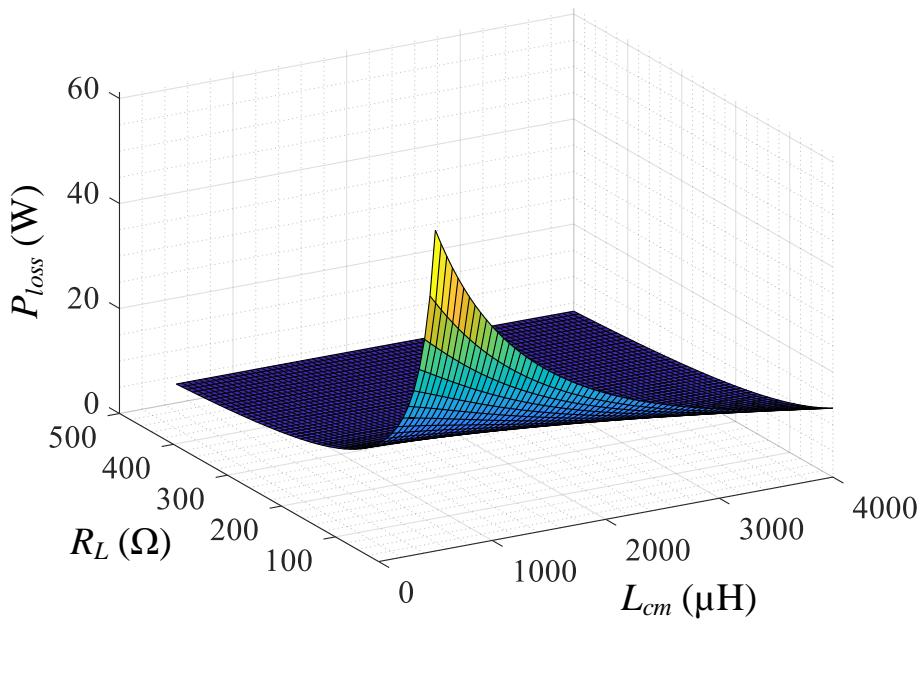
Step 2: Sweep T_{ref} from a value slightly higher than T_o . Since R_L shares a portion of the compensation voltage, the reference compensation time T_{ref} should be higher than the actual compensation time T_o .

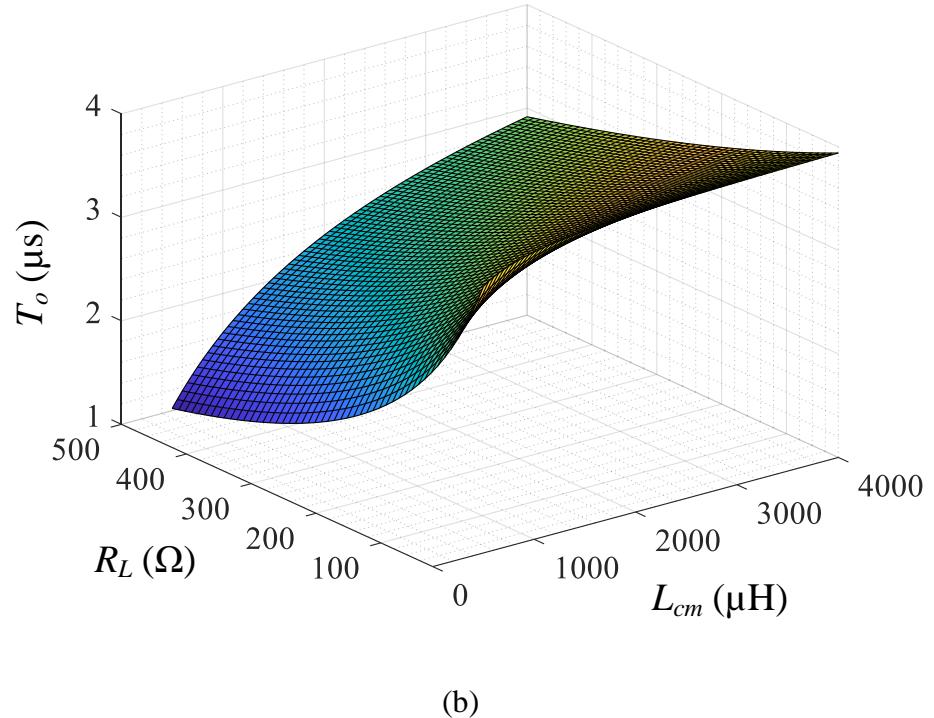
For example, when $T_{ref} = 4.5\mu s$, the blue dot ($L_{cm} = 3557\mu H$, $R_L = 132\Omega$) fulfills the above requirements, as shown in Fig. 4.8(a). When $T_{ref} = 5.5\mu s$, the blue dot moves to another point ($L_{cm} = 2402\mu H$, $R_L = 221\Omega$), as shown in Fig. 4.8(b). This illustrates that L_{cm} can be reduced by changing T_{ref} without increasing P_{loss} .

Step 3: Select optimal values of L_{cm} and R_L based on the results in *Step 2*.

As shown in Fig. 4.8(c), the required L_{cm} reduces as the increase of T_{ref} and finally falls to a steady level. When $T_{ref} = 8\mu s$, L_{cm} finds its smallest value at $2046\mu H$. Hence, the optimal values are $L_{cm} = 2046\mu H$ and $R_L = 348\Omega$. In the implementation, values higher than $6\mu s$ are all acceptable since the variation of L_{cm} with T_{ref} becomes insignificant.

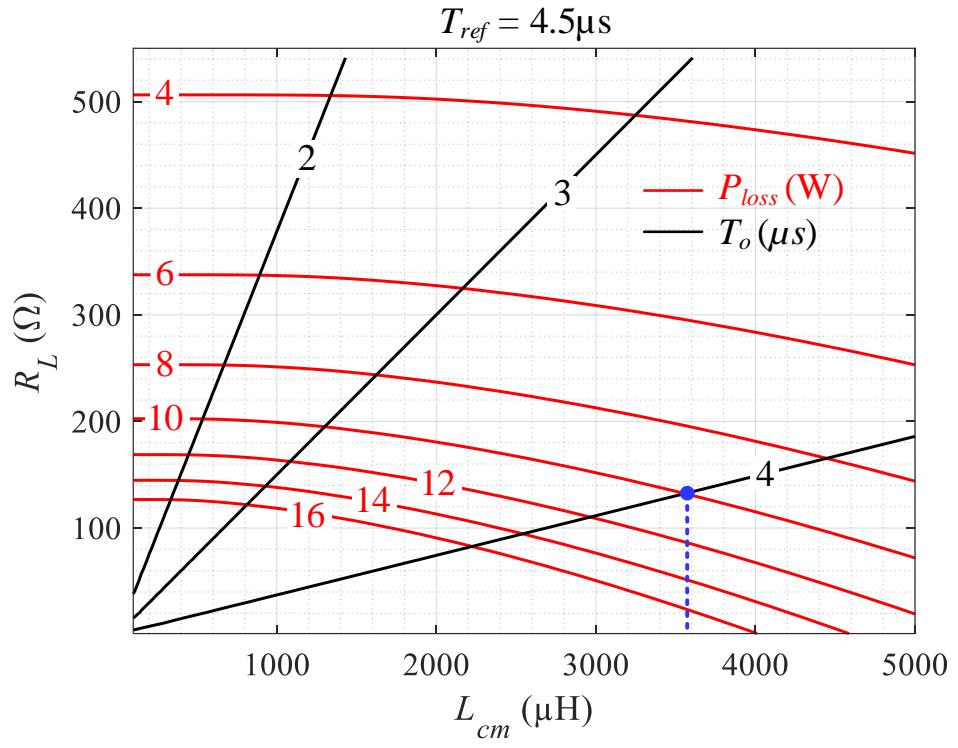
As shown in Fig. 4.8(a) and (b), the red contours closer to the origin of the coordinate axes get denser. This means the attempt to continuously reduce R_L with a given L_{cm} to pursue better compensation performance will have much higher power dissipation. Thus, the proposed output stage consists of R_L and L_{cm} , instead of a L_{cm} only in prior art.



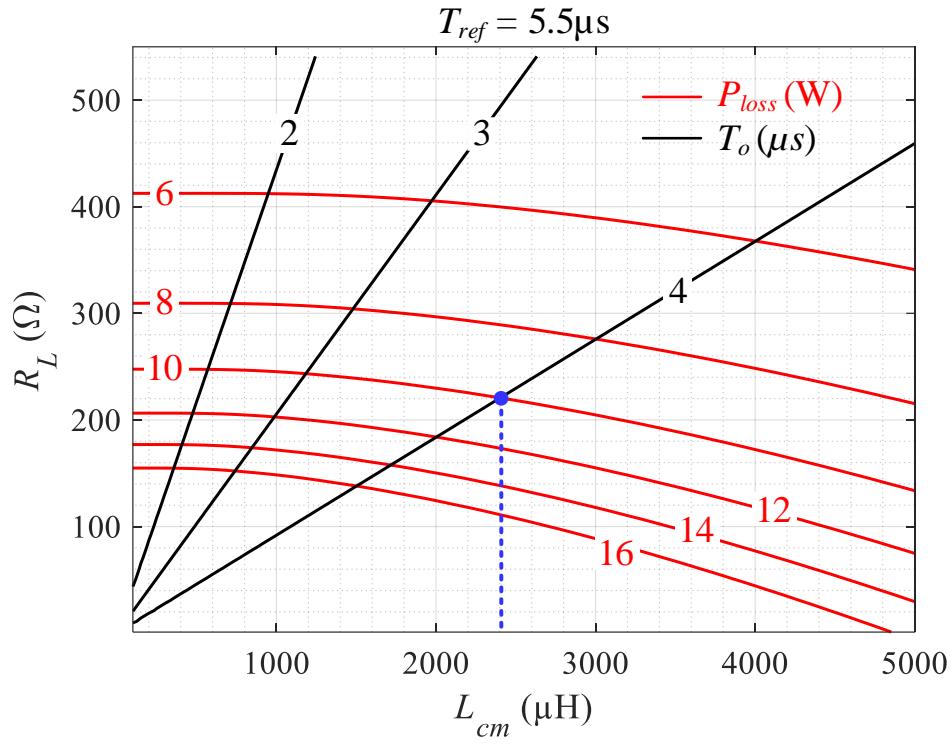


(b)

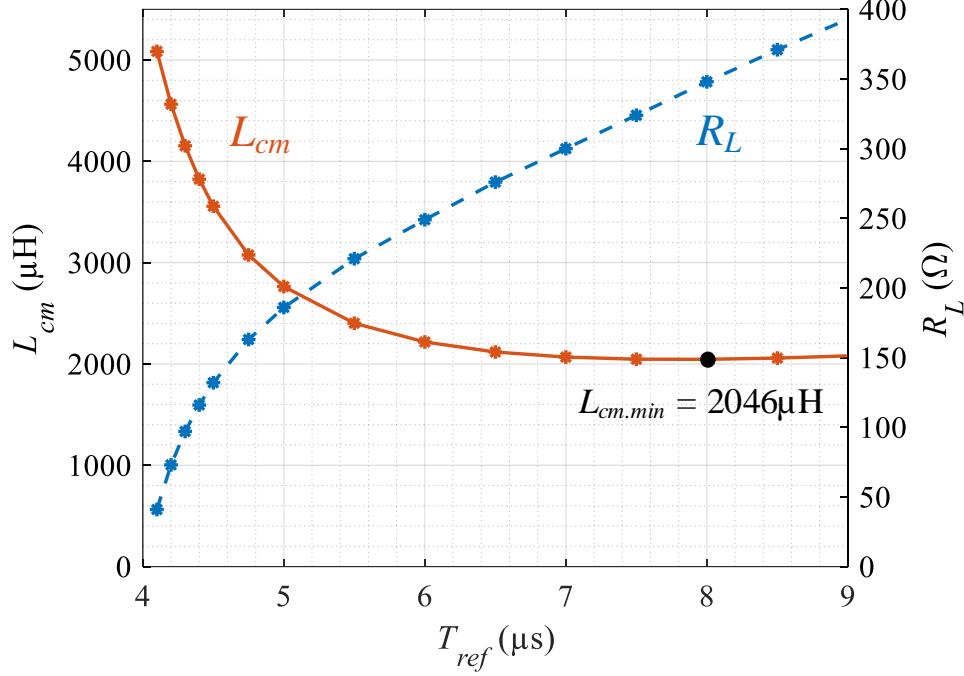
Fig. 4.7. 3-D curves ($V_{DC} = 300V$, $f_{sw} = 10kHz$, $T_{ref} = 4\mu s$). (a) P_{loss} as a function of L_{cm} and R_L . (b) T_o as a function of L_{cm} and R_L .



(a)



(b)



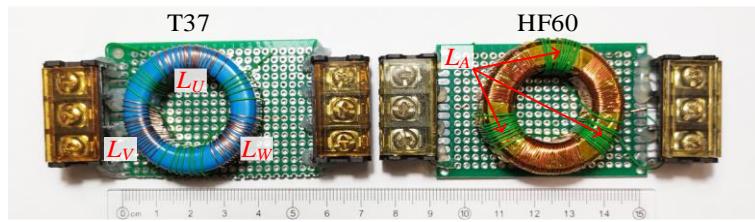
(c)

Fig. 4.8. Parameter design maps ($V_{DC} = 300V, f_{sw} = 10kHz$). (a) $T_{ref} = 4.5\mu s$. (b) $T_{ref} = 5.5\mu s$. (c) T_{ref} varies from $4.1\mu s$ to $9\mu s$.

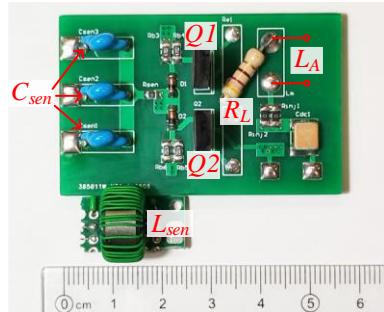
4.3. Experimental Verification and Discussion

In order to investigate the effect of different ferrite materials, two CMTs have been fabricated with materials of T37 and HF60. Material T37 has features of low loss factor and high initial permeability ($\mu_i = 6500$) [98]. Material HF60 has low initial permeability ($\mu_i = 1600$) but better high-frequency performance [99]. As shown in Fig. 4.9(a), the CMTs have one primary winding (L_A) and three secondary windings (L_U , L_V , and L_W). L_A is evenly distributed into three groups so that the coupling factors with three secondary windings are identical.

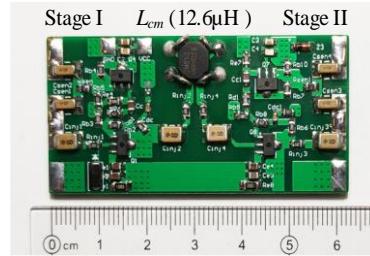
The photos of the proposed output ACF, the input ACF proposed in Chapter 3, and the motor drive system, which is a fan coil unit, have been shown in Fig. 4.9(b), (c), and (d), respectively. The equipment and connections for EMI measurement are shown in Fig. 4.9(e). The DC link voltage of the motor drive is 306V, and the switching frequency is 16kHz. The values and part numbers of the components used in the output ACF are tabulated in Table 4.1.



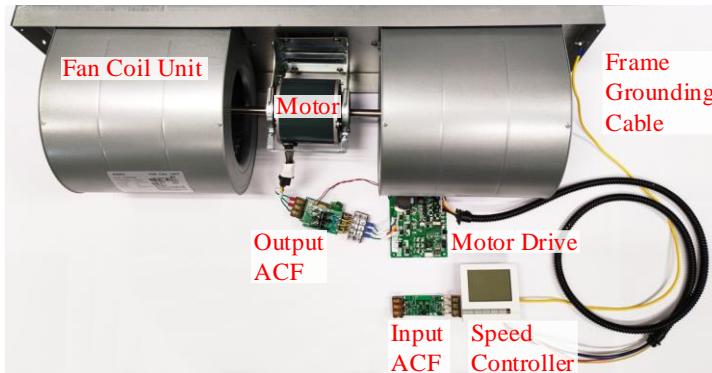
(a)



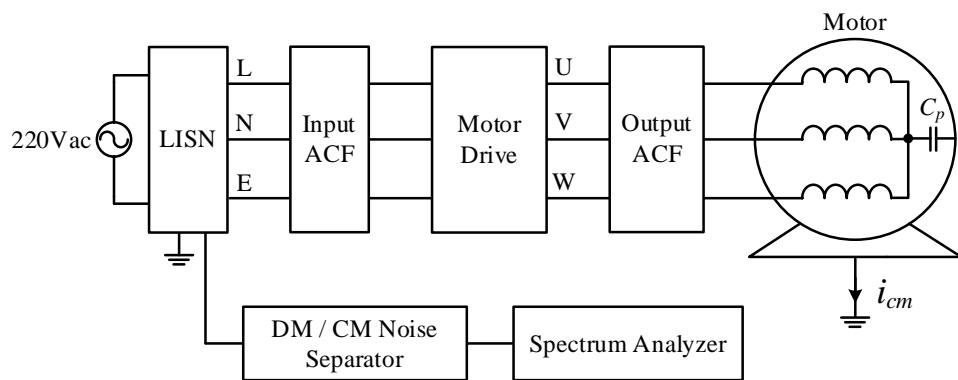
(b)



(c)



(d)



(e)

Fig. 4.9. Setup for CM performance evaluation. (a) CMTs fabricated with materials of T37 and HF60. (b) The proposed output ACF. (c) The input ACF proposed in Chapter 3. (d) The motor drive system. (e) Equipment and connections for EMI measurement.

TABLE 4.1
Components Used in the Proposed Output ACF

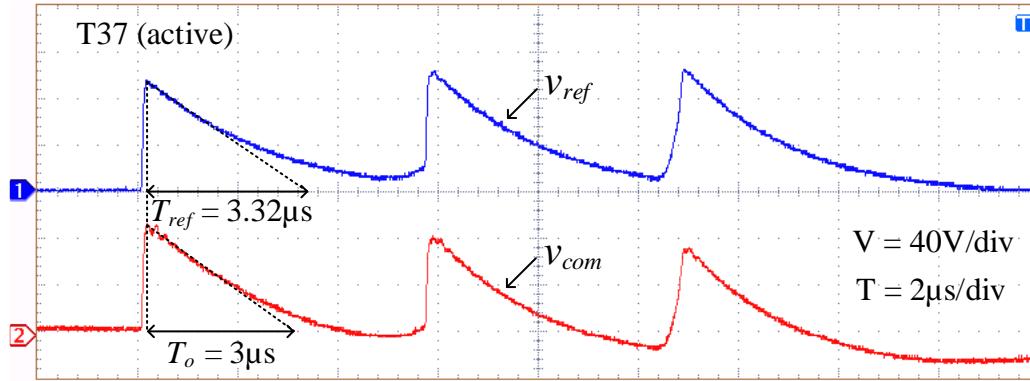
Components	Value/ Part No.	Components	Value/ Part No.
C_{sen}	100pF × 3	Q1	KSC3503
R_{sen}	10kΩ	Q2	KSA1381
L_{sen}	1.42mH	R_L	470Ω
R_{b2}, R_{b2}	41kΩ	L_{cm} (T37)	2.81mH
D_1, D_2	1N4148	L_{cm} (HF60)	2.29mH
C_{DC1}, C_{DC2}	1μF	T37 core	B64290L0674X037
R_{e1}, R_{e2}	10Ω	HF60 core	HF60T38X14X22

4.3.1. CM Voltage Compensation by the Output ACF

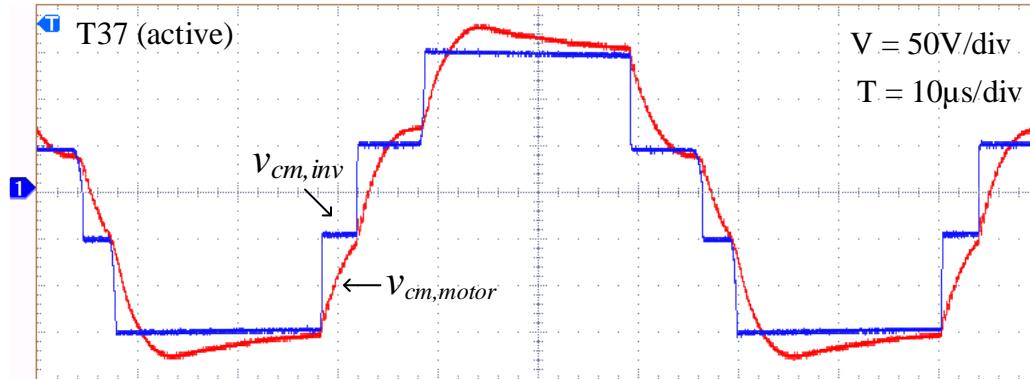
Fig. 4.10 shows experimental results of using the CMT fabricated with ferrite material T37. The reference voltage v_{ref} and compensation voltage v_{com} of the proposed output ACF are shown in Fig. 4.10(a). The CM voltages at the inverter-side $v_{cm,inv}$ and the motor-side $v_{cm,motor}$ with the output ACF are shown in Fig. 4.10(b). In order to compare with the passive CM choke, the active circuit of the output ACF is removed; waveforms of CM voltage with the passive CM choke are shown in Fig. 4.10(c).

The CMT of material HF60 has also been tested, and its waveforms are shown in Fig. 4.11.

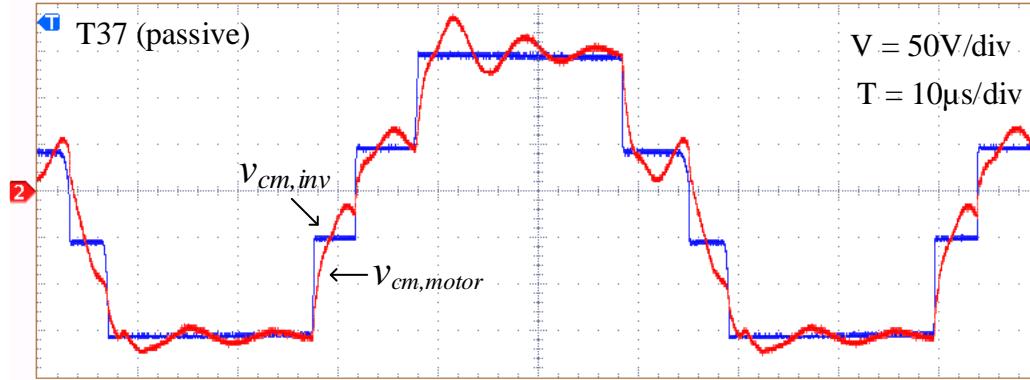
As shown in Figs. 4.10 and 4.11, the proposed output ACF has increased the rise time of CM voltage from around 100ns to 3μs. Passive CM chokes can also slow down dv/dt , but their performance is less significant, and resonance in $v_{cm,motor}$ is observed.



(a)

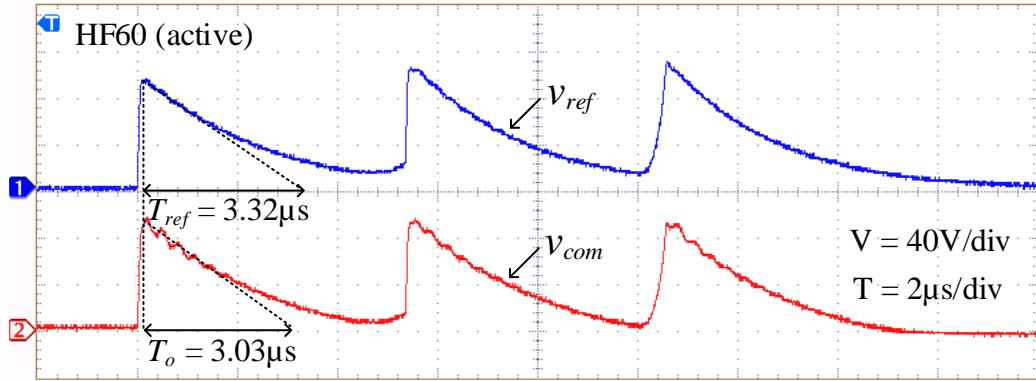


(b)

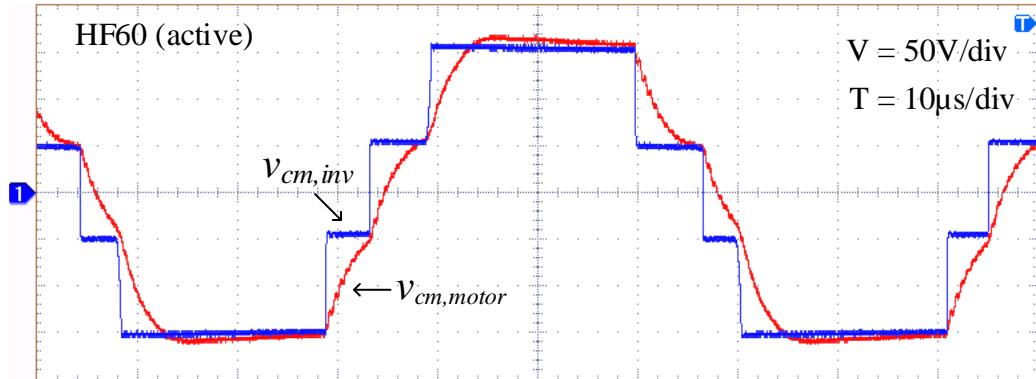


(c)

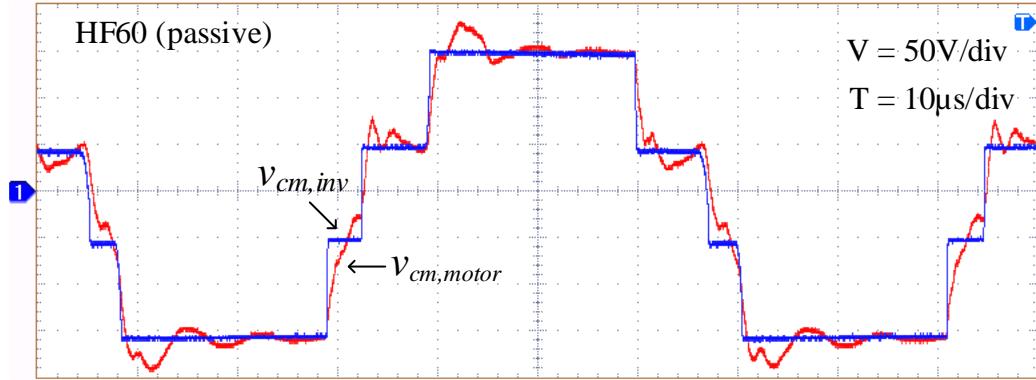
Fig. 4.10. Waveforms with the CMT fabricated with material T37. (a) v_{ref} and v_{com} of the output ACF. (b) $v_{cm,inv}$ and $v_{cm,motor}$ with the output ACF. (c) $v_{cm,inv}$ and $v_{cm,motor}$ with the passive CM choke by removing the active circuit.



(a)



(b)



(c)

Fig. 4.11. Waveforms with the CMT fabricated with material HF60. (a) v_{ref} and v_{com} of the output ACF. (b) $v_{cm,inv}$ and $v_{cm,motor}$ with the output ACF. (c) $v_{cm,inv}$ and $v_{cm,motor}$ with the passive CM choke by removing the active circuit.

4.3.2. CM EMI Spectrum

The CM noise spectra of the motor drive system with the two CMTs (T37 and HF60) under different filtering conditions have been measured, as shown in Fig. 4.12. The blue lines represent the CM noise spectra without a filter; the red lines show results with a passive CM choke; the yellow lines show results with the proposed output ACF; the purple lines show results with both output and input ACFs. In order to illustrate the insertion loss of the output ACF, the envelopes of the blue and yellow lines are drawn by black lines. The difference between the solid black line and the dashed black line represents the insertion loss of the output ACF. The motor drive system satisfies the EMC standard *IEC 61800-3* [100] with the input and the output ACFs.

It can be seen that the input ACF is most effective in attenuating CM noise. The output ACF has a maximum of 14dB attenuation higher than the passive CM choke. By using the output ACF, the noise is reduced to within the capacity of the input ACF. Otherwise, the input ACF will saturate when only a CM choke is used at the output side. This issue will be analyzed in Section 4.3.6.

The rise time of CM voltage is increased to 3 μ s with the output ACF. A longer rise time can be achieved by increasing T_{ref} and/or decreasing R_L , as analyzed in Section 4.2.3. Then the output ACF will have better filtering performance, but higher power dissipation will be expected.

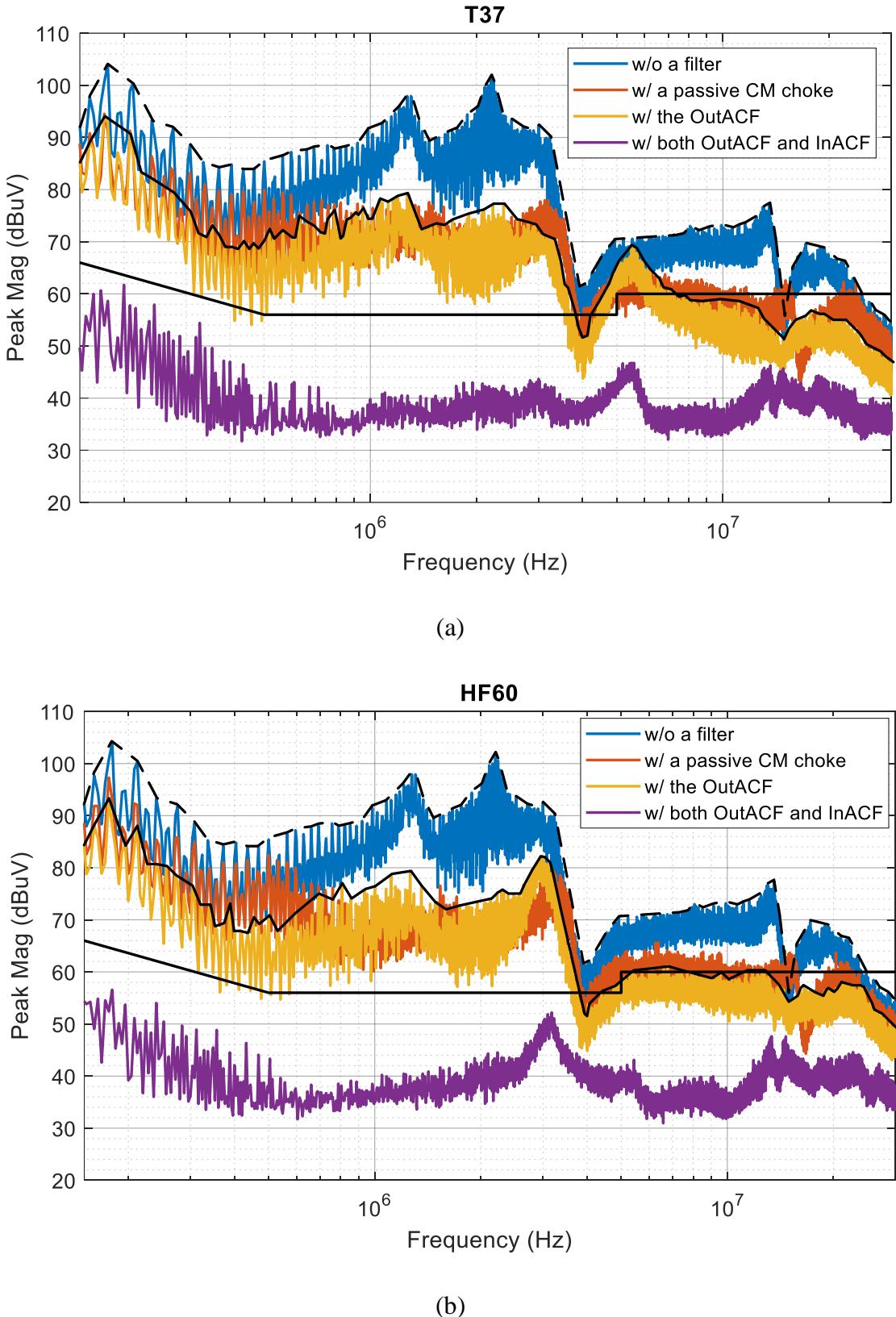


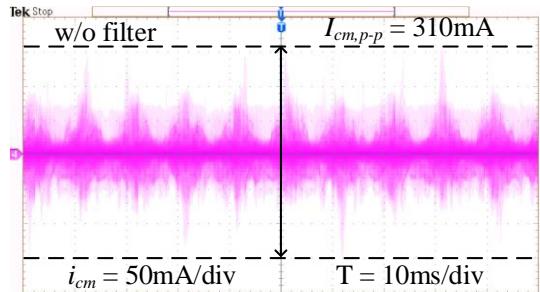
Fig. 4.12. Peak CM noise spectra of the motor drive system under different filtering conditions. (a) With ferrite material T37. (b) With ferrite material HF60.

4.3.3. CM Current Flowing Through the Motor

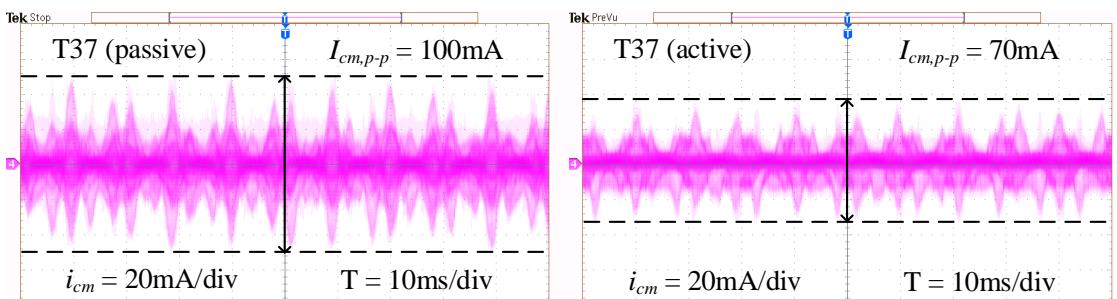
The waveforms of the CM current flowing through the motor without a filter, with a passive CM choke, and with the proposed output ACF have been shown in Fig. 4.13. Although the input ACF has good CM filtering performance, it can only attenuate the CM noise injected into the grid, but not the CM current leaked from the motor. Since the damage to bearings is determined by the peak motor CM current, the peak-to-peak CM current $I_{cm,p-p}$ have been measured as follows.

The original $I_{cm,p-p}$ without a filter is 310mA. $I_{cm,p-p}$ with a passive CM choke (T37) is 100mA, which is reduced by 67.7% [(310mA-100mA)/310mA] from its original value. By using the output ACF, $I_{cm,p-p}$ is further reduced by 30% [(100mA-70mA)/100mA].

The ferrite material HF60 has a slightly better performance than T37. $I_{cm,p-p}$ with a passive CM choke (HF60) is 90mA; it is reduced by 70.97% compared to its original value. By using the output ACF, $I_{cm,p-p}$ is reduced to 65mA, which is a further reduction of 27.78%. A lower $I_{cm,p-p}$ can be achieved by increasing T_{ref} and/or decreasing R_L at the cost of increased power dissipation.



(a)



(b)

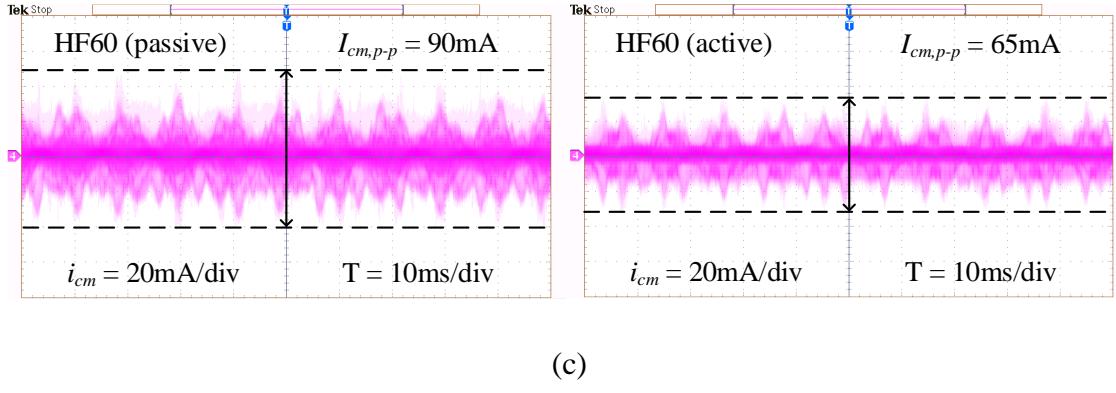


Fig. 4.13. Waveforms of CM current flowing through the motor. (a) Without a filter. (b) With ferrite material T37. (c) With ferrite material HF60.

4.3.4. Investigation into the Differences Between T37 and HF60

As introduced in the previous sections, the CMT fabricated with ferrite material HF60 has slightly better performance than that with T37. The most important difference is that the output ACF will have a much smaller power dissipation P_{loss} by using HF60 than T37, as shown in Fig. 4.14.

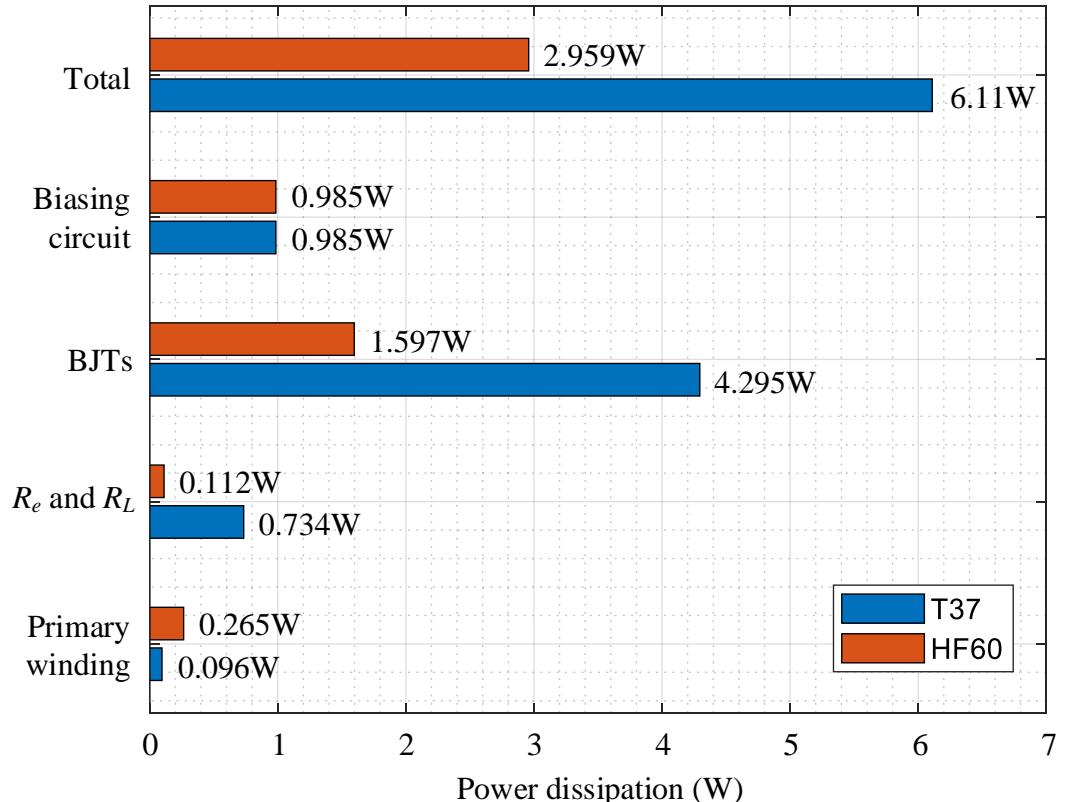


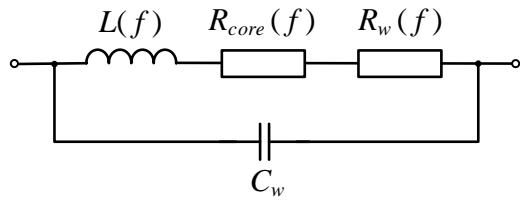
Fig. 4.14. Power dissipation of the output ACF with ferrite materials T37 and HF60.

P_{loss} of the biasing circuit is 0.985W; it is caused by a high DC link voltage V_{DC} and a small biasing current. According to (4.9), P_{loss} of the output ACF is determined by $|i_L|_{ave}$. $|i_L|_{ave}$ with the T37 CMT is 33.5mA, and it is 12.9mA with the HF60 CMT. There is a 2.6 times higher inductor current with T37 than with HF60. Hence, the output ACF with T37 CMT has higher power dissipation. BJTs consume the largest proportion of P_{loss} since their voltage is equal to $V_{DC}/2$ deducted by a triangular edge-compensation waveform, which has a significant RMS value.

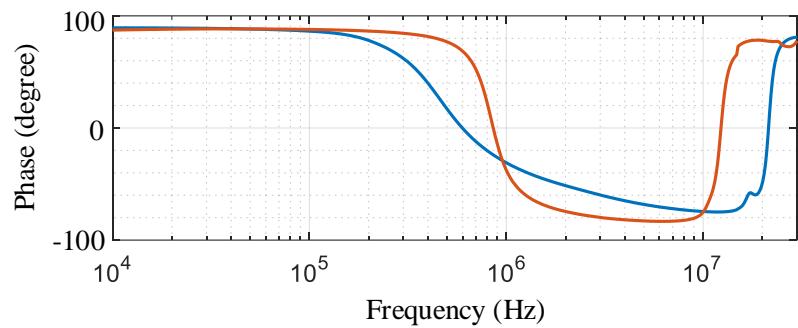
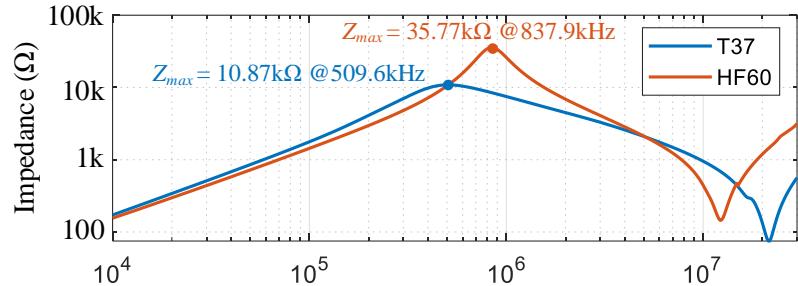
Contrary to the total power losses with the two types of cores, the P_{loss} of the primary winding with HF60 is 2.76 times higher than that with T37 (265mW/96mW=2.76). The above experimental results will be investigated as follows.

Since both CMTs (T37 and HF60) are tested with the same circuit, the different inductor currents are caused by the difference in impedance of the CMTs. The equivalent circuits for CM inductors have been analyzed in [101], [102], as shown in Fig. 4.15(a). The equivalent circuit of CM inductors is represented by a frequency-dependent inductance $L(f)$, equivalent core loss resistance $R_{core}(f)$, winding loss resistance $R_w(f)$, and winding parasitic capacitance C_w . The small-signal impedance curves of the CMTs are measured by impedance analyzer 4294A, as shown in Fig. 4.15(b). 4294A can also measure the inductance and ac resistance connected in series, as shown in Fig. 4.15(c).

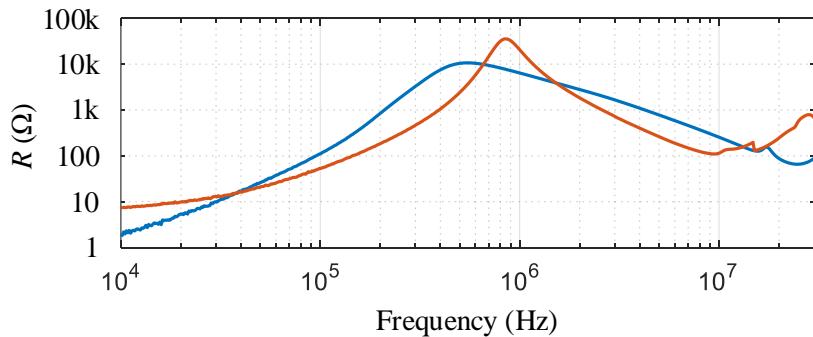
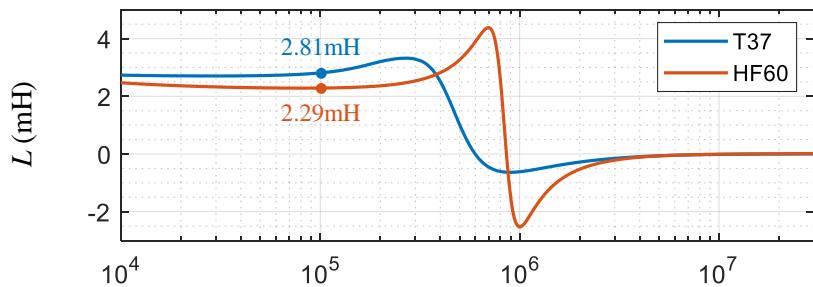
Impedance analyzer 4294A displays the inductance and ac resistance of measured impedance by separating the real and imaginary parts. However, the measured ac resistance is not the intrinsic core resistance of the CMT. In order to investigate this issue, an external 100pF capacitor is paralleled to the T37 CMT. The $L-R$ curve with the external capacitor is compared to the original one, as shown in Fig. 4.16. It is reasonable to observe the self-resonant frequency of impedance shifts to a lower frequency due to increased winding capacitance, but the ac resistance also changes with the additional capacitor. This validates that the ac resistance measured by the impedance analyzer cannot be used to model the $R_{core}(f)$ and $R_w(f)$ in Fig. 4.15(a).



(a)



(b)



(c)

Fig. 4.15. Impedance characteristics of CM inductors. (a) Equivalent circuit for CM inductors. (b) Impedance curves. (c) Curves of inductance and ac resistance.

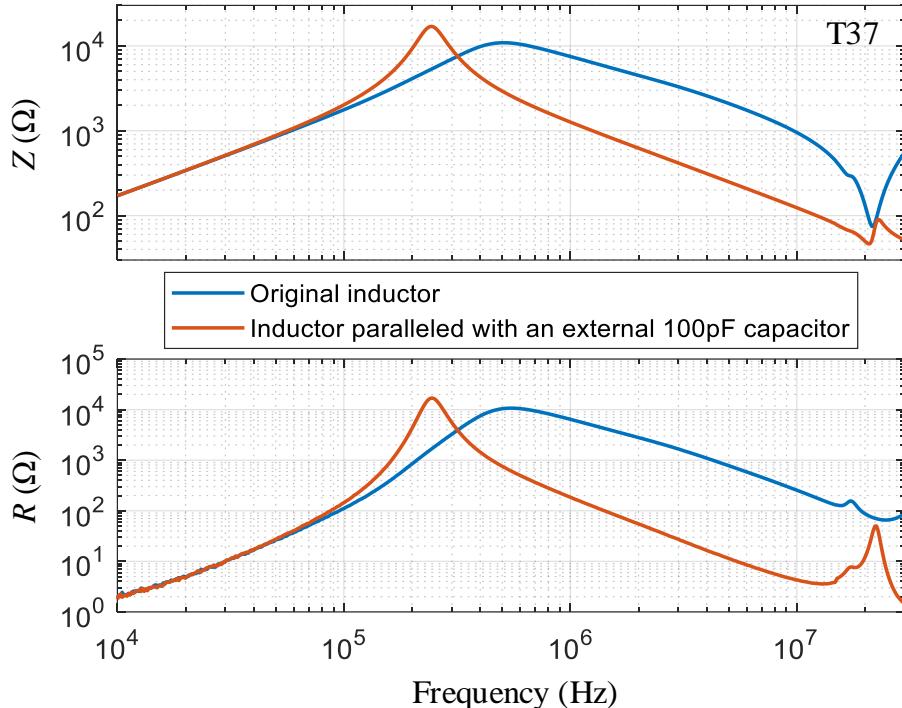


Fig. 4.16. Impedance characteristics of the CM inductor with and without an external 100pF capacitor.

Since the CMTs fabricated with T37 and HF60 use the same wire gauge and work under the same circuit, the winding loss has a negligible effect on the difference of power dissipation. Instead, the core loss leads to the noticeable difference in power dissipation. In order to investigate the large-signal response of the materials, the magnetic hysteresis loops of T37 and HF60 have been measured using the methods introduced in [103], as shown in Fig. 4.17.

According to Fig. 4.17, the operation of both CMTs has not entered the saturation region upon working with the output ACF. HF60 has a much wider hysteresis loop than T37, implying that HF60 has higher core loss and higher corresponding $R_{core}(f)$. This explains the HF60 CMT has a smaller inductor current. The high-loss feature of HF60, in turn, leads to a lower overall power dissipation of the output ACF. This is different from conventional power inductors in that the low-loss characteristic is preferable.

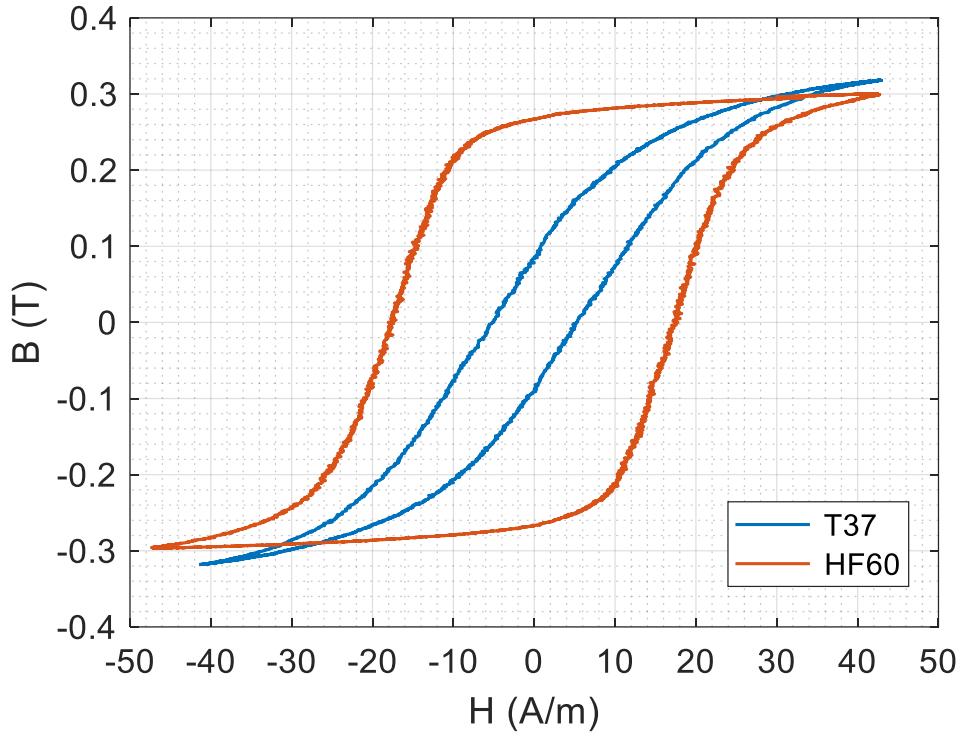


Fig. 4.17. B-H curves of T37 and HF60 (10kHz).

4.3.5. Investigation into Winding Configuration

Extensive works have been devoted to optimizing the winding design of single-phase inductors and CM chokes. However, the winding configuration of the CMT used in the output ACF that has three conventional secondary windings and one primary winding has not been investigated.

The CMTs tested in the previous sections use symmetrical primary winding configuration. In this section, a new T37 CMT in asymmetrical primary winding configuration has been made, as shown in Fig. 4.18, and tested with the same output ACF. Compensation voltage v_{com} , CM current flowing through the motor i_{cm} , and CM noise spectra of the motor drive system with output ACFs in different winding configurations are shown in Fig. 4.19.

In the asymmetrical CMT, the primary-to-secondary coupling coefficient of one phase is different from the other two. The resulting unbalanced leakage inductance will resonate with motor winding capacitances. Hence, resonance appears in one of the three

triangular v_{com} , caused by the asymmetrical phase with variation of the duty cycle. The resulting i_{cm} has a higher peak value (115mA) than that in symmetrical configuration (70mA). The CM noise spectra are nearly the same in the low frequency, but a resonant peak around 6MHz is observed with the asymmetrical CMT.

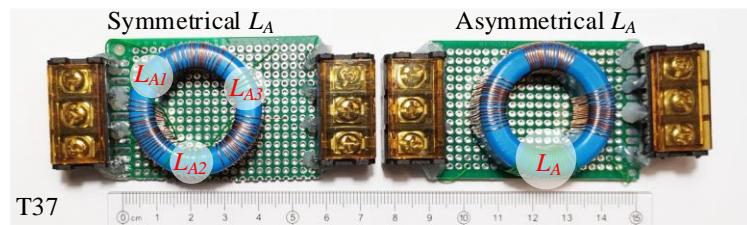
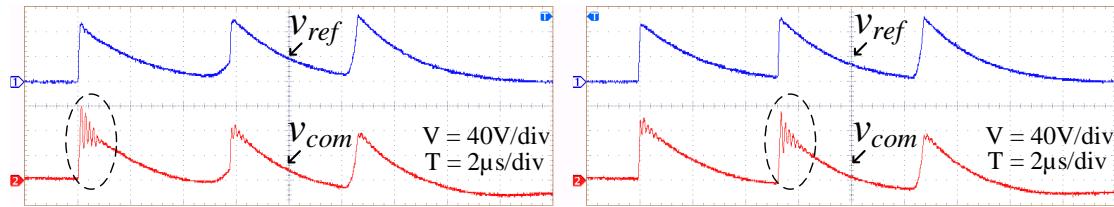
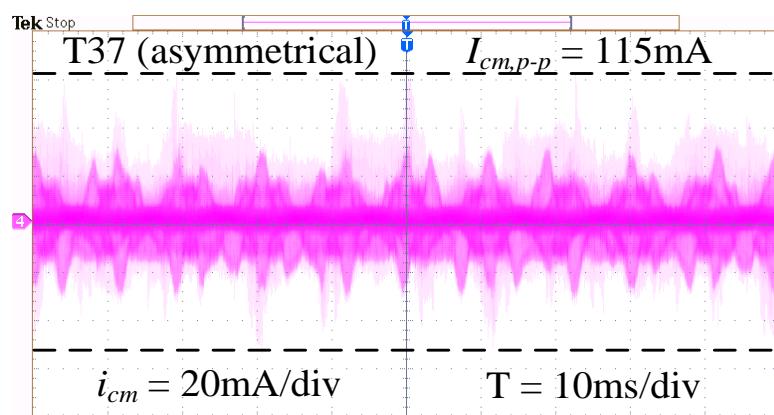


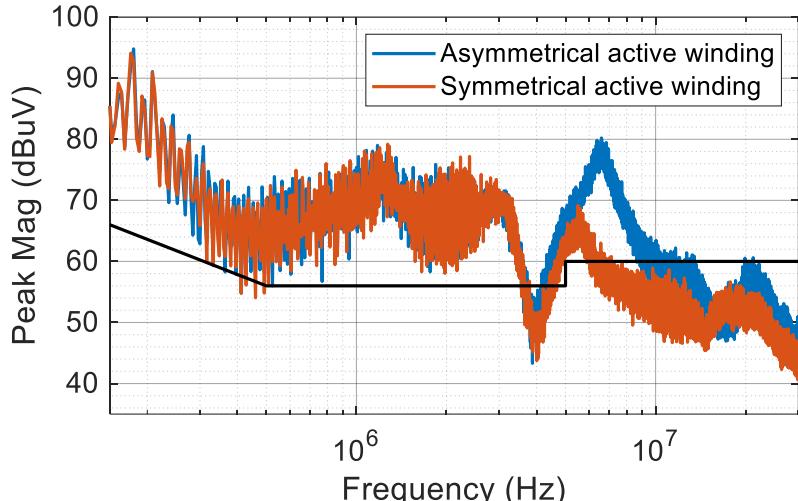
Fig. 4.18. CMTs of different primary winding configurations.



(a)



(b)



(c)

Fig. 4.19. Waveforms of the CMT with asymmetrical primary winding configuration. (a) v_{ref} and v_{com} of the output ACF in different switching cycles. (b) CM current flowing through the motor. (c) CM noise spectra of the motor drive system with the output ACF in different winding configurations.

4.3.6. Discussion on the Relationship Between Input and Output ACFs

A comparison of input and output ACFs has been shown in Table 4.2. The input ACF is used to attenuate the CM noise injected into the grid. Since the input ACF cannot attenuate the CM current flowing through the motor, it makes the output ACF primarily to reduce the motor CM current to protect bearings. The reduction of motor CM current also contributes to a lower CM noise spectrum, which gives aid to the input ACF. Nevertheless, the input ACF is indispensable since it still needs to attenuate the CM noise of the motor drive.

The input ACF is connected at the grid interface where the high-amplitude line-frequency voltage contains small noise. The line-frequency component can be easily excluded by the CM sensing circuit, which makes the input ACF act as a small-signal filter. On the contrary, the output ACF is connected at the output of the inverter, where the CM voltage has high amplitude and steep rising/falling edges. Thus, the output ACF is a large-signal filter.

TABLE 4.2
COMPARISON OF THE INPUT ACF AND THE OUTPUT ACF

	Input ACF	Output ACF
Objective	★ ★ Reduce CM noise into the grid	★ ★ Reduce $I_{cm,peak}$ to protect bearing ★ Reduce CM noise to aid the input ACF
Noise level	Small-signal filter	Large-signal filter
Limiting factor	Saturation due to large v_o swing	Higher power dissipation for a lower dv/dt
Power dissipation	Relatively low - Determined by • Output voltage v_o swing • Peak CM current $I_{cm,peak}$	Relatively high - Determined by • DC link voltage V_{DC} • Compensation time T_o

The output characteristics of the input ACF have been analyzed in Section 3.2.4; its output voltage v_o is equal to the product of the sensed CM voltage and a high gain. The amplifier will saturate when v_o swing is higher than the supply voltage. There are several ways to alleviate this issue: (a) increase the supply voltage; (b) increase the Y-capacitance; (c) decrease the voltage gain. This issue can be solved by reducing the CM current with the output ACF. By contrast, the input ACF saturates when only a CM choke is used at the output side.

The limiting factor of the output ACF is power dissipation. Higher power will be consumed to achieve a lower dv/dt . Moreover, the increment of power dissipation with the reduction of dv/dt is nonlinear; a much higher increment of power consumption is required to further reduce dv/dt .

Differences in noise levels leads to differences in power dissipation. The power dissipation of the input ACF is 1.5W, which is much lower than that of the output ACF. Since class A amplifier is used in the input ACF, the quiescent current should be higher than the peak CM current. The output ACF reduces the CM current, and thus v_o swing and quiescent current of the input ACF can be reduced, leading to lower power consumption. The power dissipation of the output ACF is mainly determined by DC link

voltage V_{DC} and compensation time T_o . Hence, the output ACF will have lower power dissipation in low-voltage motor drive systems; a longer T_o corresponds to a lower dv/dt and CM current at the cost of higher power consumption.

The flowchart of designing the proposed active CM filtering architecture is shown in Fig. 4.20. The first step is to design the output ACF with a selected compensation time T_o to reduce the CM current, as analyzed in Section 4.2.3. T_o will be increased until the peak CM current is reduced to a safe level. The safe level depends on manufacturers and varies from bearing to bearing.

The next step is to evaluate the CM spectrum of the motor drive system with the output ACF, then calculate the required further attenuation for the input ACF to satisfy EMC standards. The design procedures of the input ACF can be found in Section 3.2. If the required attenuation exceeds the capacity of the input ACF, T_o of the output ACF will be increased to aid the input ACF.

The design philosophy is to use the respective advantages of the input and output ACFs to protect bearings and satisfy EMC standards with low power dissipation and small volume.

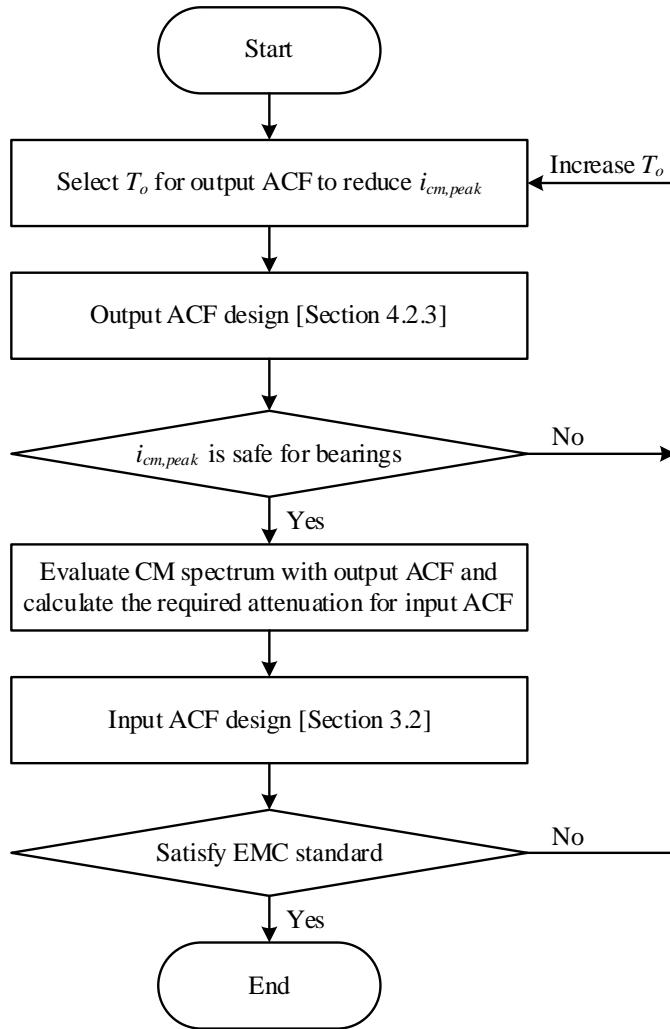


Fig. 4.20. Flowchart of designing the proposed active CM filtering architecture.

4.4. Chapter Summary

A new output ACF that compensates for rising/falling edges of CM voltage has been proposed to protect bearings and reduce CM noise. This chapter is not intended to completely suppress CM noise by the output ACF only, without considering power dissipation; instead, it proposes a holistic CM filtering architecture that utilizes the respective advantages of input and output ACFs to reduce power dissipation and volume. Characteristics and design considerations of the ACFs for motor drives are summarized as follows.

- 1) The input ACF is a small-signal filter, while the output ACF is a large-signal one. The input ACF can achieve high attenuation with lower power

consumption and smaller volume. The output ACF can reduce dv/dt at motor terminals and protect bearings while the input ACF cannot.

- 2) The power dissipation in the output ACF mainly depends on V_{DC} and T_o . V_{DC} determines the magnitude of CM voltage, and T_o regulates the compensation effect. The increment of power dissipation is higher than that of T_o . Higher power loss will result in bulky heatsinks, decreasing overall power density. Hence, dv/dt is reduced but not eliminated with the proposed output ACF.
- 3) Ferrite materials significantly impact the power consumption of the output ACF. The high-loss ferrite material HF60 has a higher large-signal ac resistance, which reduces the current and thus power dissipation of the output ACF.
- 4) The primary winding of the CMT used in the output ACF should have a symmetrical configuration to attain an identical coupling coefficient with secondary windings.

Chapter 5

CONCLUSION AND SUGGESTIONS FOR FURTHER WORK

5.1. Conclusion

This thesis has proposed an active DM filter, input active CM filter, and output active CM filter to develop the active EMI filtering technology.

For DM filtering of switching converters, an active high-impedance element, the PSF, operates with two DM capacitors forming a three-order filter. The DM noise injected into the grid is thus significantly reduced.

For CM filtering of switching converters, the Y-capacitance is restricted for safety considerations. An active capacitor magnifies the equivalent capacitance in the conducted EMI frequency while maintaining a small low-frequency capacitance to comply with safety regulations. This active low-impedance element can be cascaded with small CM chokes to form a multistage filter for pursuing higher attenuation.

For CM filtering of motor drive systems, the CM current flowing through the motor should also be mitigated to protect bearings. A high-impedance element, realized by a voltage-compensation ACF, is connected at the output of the inverter to reduce dv/dt and the CM current. Since the output ACF cannot attenuate the noise leaked from the inverter, an input ACF connected at the input of the inverter is also used. The input ACF is a small-signal filter, while the output ACF is a large-signal filter. This characteristic leads to other differences between the two ACFs that should be paid attention to when designing ACFs for motor drives.

5.2. Major Contributions

The major contributions of this thesis to advance the active EMI filtering technology are summarized as follows:

- 1) Proposed a fixed-frequency dynamic ramp modulator for switching converters

with the PSF. The input current oscillation that may occur in variable-frequency operation is mitigated. Since the voltage across the SPD is regulated at a low level, a considerable reduction of power dissipation in the SPD has been achieved.

- 2) Optimized the fast-current regulation circuit of the PSF by solving the issues of redundant gain stage design and inadequate capacitive load driving capability in prior work [48]. Hence, higher DM attenuation has been achieved. PCB layout guidelines also have been given to minimize the adverse effect of ground loop inductance on filtering performance.
- 3) Proposed a high-attenuation wideband ACF section. The high attenuation is achieved by the high-gain CE amplifier with an active load. The bandwidth covers the whole frequency range of conducted EMI (150 kHz - 30 MHz).
- 4) Proposed a new perspective for the classification of ACFs. They can be classified into two types: high-impedance elements, acting as active inductors, and low-impedance elements, acting as active capacitors. Based on this perspective, a general multistage ACF, which consists of multiple active capacitors and small CM inductors, has been proposed. This multistage configuration can fulfill the attenuation demands of different applications.
- 5) Proposed a new output ACF for motor drive systems. This new output ACF compensates for the steep rising/falling edges of CM voltage instead of eliminating CM voltages in the prior art. Hence, the power dissipation in the output ACF is reduced.
- 6) Proposed a holistic CM filtering architecture comprising input and output ACFs for motor drives. CM noise reduction and bearing protection are achieved simultaneously by taking advantage of the respective merits of input and output ACFs.

5.3. Suggestions for Further Research

The PSF has demonstrated significant DM filtering capability, and its power dissipation is reduced to a reasonably low level by the dynamic ramp modulator. Unlike conventional stand-alone EMI filters, the control of the PSF is coupled with switching converters. The modulation scheme is specifically designed for switching converters with the PSF. Other modulation schemes, such as soft-switching techniques, cannot be directly used in converters with the PSF. Hence, further research can either design a new stand-alone PSF or incorporate other modulation schemes into the current PSF.

The input ACF proposed in Chapter 3 needs an isolated DC supply, which is a 9V battery in this thesis. A low-cost, isolated, and on-board DC supply is worth investigating for commercial products. This on-board DC supply can be implemented through an auxiliary winding to draw power from the transformer of an isolated converter. An alternative way is to draw power from the AC input.

The output ACF proposed in Chapter 4 compensates for the rising/falling edges of CM voltages instead of eliminating CM voltages to reduce power dissipation. However, considerable power is still consumed in the buffer stage. Future research is expected to further reduce the power dissipation in the buffer stage.

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APPENDICES

A.1. Design Procedure of Component Values in Section 3.2.1

The procedure to determine the component values in Table 3.2 is explained as follows.

A. C_{sen} and C_{inj}

Since Y-capacitors will lead to leakage current, the total Y-capacitance is restricted for safety considerations. For example, the maximum leakage current is 0.75mA for hand-held information technology (IT) equipment, as stated in *IEC 60950-1* [77]. That is, the maximum total allowable Y-capacitance ($C_{sen}+C_{inj}$) is 9.947nF at 240Vac, 50Hz [80].

Based on the small-signal model shown in Fig. 3.3, the input impedance of the common-collector (CC) amplifier can be calculated as 30k Ω at 150kHz. In order to avoid severe voltage divider effect, the impedance of the sensing capacitors (C_{sen1} and C_{sen2}) at 150kHz should be smaller than 3k Ω , that is, $C_{sen}>354\text{pF}$. Thus, C_{sen} is chosen as $330\text{pF}\times 2$ with standard values.

The injection capacitors (C_{inj1} and C_{inj2}) circulate the common-mode (CM) current generated by the switching converter, and higher capacitance will result in a lower impedance path. The maximum allowable value of C_{inj} is $9.947\text{nF}-660\text{pF}=9.287\text{nF}$. C_{inj} is chosen as $2.2\text{nF}\times 2$ with available standard capacitors. The total Y-capacitance (5.06nF) is smaller than 9.947nF with a sufficient margin. A small resistor R_{inj} (2 Ω) is connected in series with C_{inj} to damp potential high-frequency ringing.

B. $R_{b1}, R_{b2}, R_{e1}, R_{b3}, R_{b4}, R_{e2}, R_{e3}, R_{e4}$, and R_{ref}

The DC biasing resistors are chosen to provide the BJT an appropriate operating point near the middle of its operating range to avoid cut-off and saturation distortion [97].

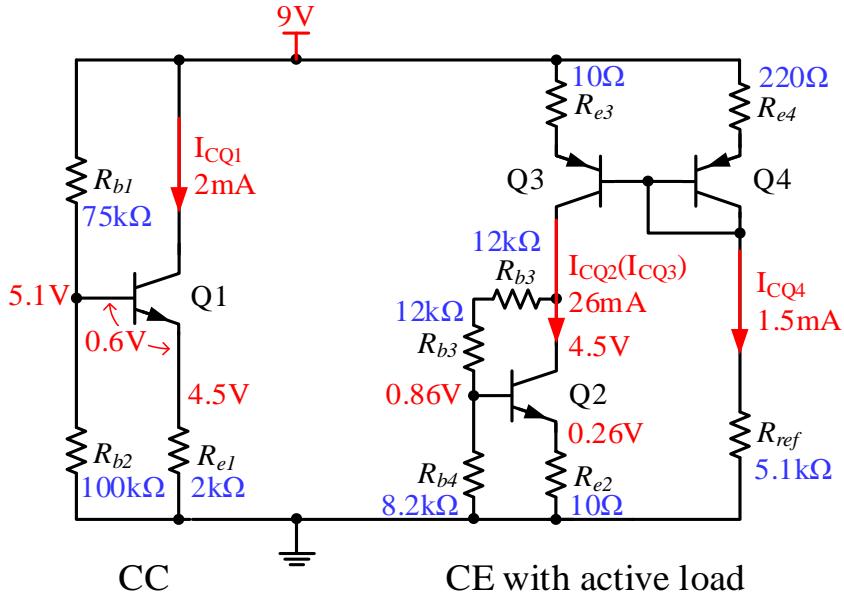


Fig. R1 Biasing circuit of the active capacitor.

The CC amplifier is a voltage buffer; thus, its quiescent current can be small. For example, set its DC point at $V_{CE}=9V/2=4.5V$, and $I_{CQ}=2mA$.

$$\text{The emitter resistor } R_{e1} = \frac{9V - 4.5V}{2mA} = 2.25k\Omega. \text{ Then choose } R_{e1}=2k\Omega.$$

The base terminal voltage is equal to $4.5V + 0.6V = 5.1V$. Choose $R_{b2}=100k\Omega$, then based on $\frac{100k\Omega}{100k\Omega + R_{b1}} \times 9V = 5.1V$, $R_{b1} = 76.47k\Omega$. Choose $R_{b1}=75k\Omega$.

The common-emitter (CE) amplifier needs to inject compensation current; thus, its quiescent current should be higher than the CM noise current. For example, set its DC point at $V_{CE} = 4.5V$, and $I_{CQ2} = 26mA$.

Choose a small 10Ω emitter resistor R_{e2} to avoid thermal runaway. The voltage across it will be $0.26V$. Then the base terminal voltage is $0.26V + 0.6V = 0.86V$. Choosing the biasing current around $0.1mA$, R_{b3} and R_{b4} can be derived as $12k\Omega$ and $8.2k\Omega$, respectively.

Let $R_{e3} = R_{e2} = 10\Omega$. Then, transistors Q2 and Q3 share the same quiescent current.

Since the amplifier is of class-A type, the power dissipation of the active capacitor is approximately equal to the product of the DC voltage (9V) and the sum of the quiescent currents of Q1, Q3, and Q4. I_{CQ4} should be one-tenth smaller than I_{CQ3} so that the power dissipation in Q4 branch is negligible as compared to that of Q3 branch; I_{CQ4} should also be higher than 1mA so as to be away from the cut-off region. Thus, the resistance range of R_{e4} is 100-260 Ω . R_{e4} is chosen to be 220 Ω .

$$R_{ref} = \frac{9V - 0.6V}{1.5mA} - 220\Omega = 5.38k\Omega. \text{ Choose } R_{ref} = 5.1k\Omega.$$

C. C_c and C_e

C_c is the coupling capacitor between the CC amplifier and the CE amplifier. C_e is the bypass capacitor to decrease the emitter impedance in the high-frequency range. The impedance of a 10 μ F capacitor is only 0.1 Ω at 150kHz, which is sufficiently small in the high-frequency range. Two 10 μ F capacitors can be connected in parallel to reduce the parasitic inductance effect in implementation.

D. C_b and R_{d2}

C_b is used to provide a high-frequency low-impedance path for the biasing resistor R_{b3} ; thus, it effectively breaks the feedback by R_{b3} between the base and collector of Q3 so that the voltage gain is not significantly reduced. Since the starting frequency of conducted EMI is 150kHz, 100nF capacitance has a sufficiently lower impedance than the 12k Ω R_{b3} . A small 10 Ω damping resistor R_{d2} is used in series with C_b . This resistance can be increased to enhance stability when large disturbances exist.

E. Q1 - Q4

As stated in the datasheet, the transition frequency of NPN BJT 2SCR293P5 and PNP BJT 2SAR293P5 is 320MHz. The maximum collector current of 2SCR293P5 and 2SAR293P5 is 1A. These parameters enable the active capacitor to have sufficient bandwidth and output current to compensate for the CM current. Based on the SPICE

models provided by Rohm Co., Ltd [R1], the procedure to determine parameters of the small-signal model of transistors is explained as follows. The small-signal model and SPICE model of transistor 2SCR293P5 is shown in Fig. R2 and Fig. R3, respectively.

The transconductance g_m is

$$g_m = \frac{I_{CQ}}{V_T} = \frac{26\text{mA}}{25\text{mV}} = 1.04 \text{ S} \quad (\text{A.1.1})$$

where I_{CQ} is the quiescent collector current of transistor Q2, and V_T is the volt equivalent of temperature and is 25mV at room temperature ($T=293\text{K}$) [97].

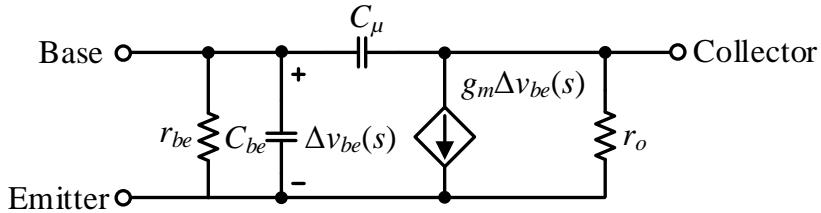


Fig. R2 Small-signal model of transistors used in the ACF (cf. Fig. 3.3).

```
.MODEL Q2SCR293P5 NPN
+ IS=500.00E-15
+ BF=451.29
+ VAF=48.900
+ IKF=4.2513
+ ISE=501.24E-15
+ NE=1.5637
+ BR=38.840
+ VAR=17.200
+ IKR=1.8267
+ ISC=2.9152E-12
+ NC=1.3407
+ NK=.97869
+ RE=.14
+ RB=2.8446
+ RC=.11402
+ CJE=87.669E-12
+ VJE=1.7347
+ MJE=.55171
+ CJC=18.808E-12
+ VJC=.63549
+ MJC=.41539
+ TFE=463.35E-12
+ XTF=432.42
+ VTF=40.605
+ ITF=67.031
+ TR=16.000E-9
+ XTB=1.5000
```

BF	Forward active current gain
VAF	Forward mode Early voltage
TF	Base forward transit time
TR	Base reverse transit time
CJE	Base-emitter zero-bias junction capacitance
CJC	Base-collector zero-bias junction capacitance

(a)

(b)

Fig. R3 SPICE model [R1]. (a) SPICE model of transistor 2SCR293P5. (b) Interpretation of key parameters.

The other parameters can be obtained by using formulas introduced in [R2]

$$\beta = BF = 451.29 \quad (\text{A.1.2})$$

$$r_{be} = \frac{\beta}{g_m} = \frac{451.29}{1.04} = 433.9\Omega \quad (\text{A.1.3})$$

$$r_o = \frac{VAF}{I_{CQ}} = \frac{48.9V}{26mA} = 1881\Omega \quad (\text{A.1.4})$$

$$C_{be} \approx g_m TF + 2CJE = 657.2\text{pF} \quad (\text{A.1.5})$$

$$C_\mu \approx \frac{TR}{r_o} + CJC = 27.3\text{pF} \quad (\text{A.1.6})$$

The biasing point can affect the small-signal parameters of transistors. A high-accuracy calculation can be obtained by using separate parameters of Q1-Q4. However, for the sake of simplicity, transistors Q1-Q4 use the same small-signal parameters of Q2 based on the following considerations:

The CC amplifier with transistor Q1 is a voltage follower that ideally has a unity gain. The CE amplifier with transistor Q2 provides a high gain and dominates the characteristics of the ACF. Transistors Q3 and Q4 are the complementary PNP pair of Q2; therefore, they share matching characteristics.

As shown in Fig. 3.6 in the Chapter 3, the calculated results are in close agreement with the simulated results.

Component values and operation of amplifiers are firstly examined by the simulator LTspice and then verified by experiment.

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https://www.mikrocontroller.net/attachment/168555/Modeling_BJTs_in_Multisim.pdf

A.2. Derivations of (3.27)

Based on the model shown in Fig. 3.9(a), the insertion loss of n -stage ACFs is expressed as

$$IL_{n=1} = 1 + \frac{Z_{LISN} + Z_{Lcm}}{Z_{act}} \quad (\text{A.2.1})$$

$$IL_{n=2} = 1 + \frac{2Z_{LISN} + 3Z_{Lcm}}{Z_{act}} + \frac{Z_{LISN}Z_{Lcm} + Z_{Lcm}^2}{Z_{act}^2} \quad (\text{A.2.2})$$

$$IL_{n=3} = 1 + \frac{3Z_{LISN} + 6Z_{Lcm}}{Z_{act}} + \frac{4Z_{LISN}Z_{Lcm} + 5Z_{Lcm}^2}{Z_{act}^2} + \frac{Z_{Lcm}^2Z_{LISN} + Z_{Lcm}^3}{Z_{act}^3} \quad (\text{A.2.3})$$

The general formula of the insertion loss of an n -stage ACF IL_n can be obtained by induction from (A.2.1)-(A.2.3).

PUBLICATIONS RELATED TO THIS THESIS

Journal Articles

- [1] J. W. Fan, J. P. Chow, W. Chan, **K. Zhang**, A. Relekar, K. Ho, C. Tung, K. Wang, and H. S. Chung, “Modeling and Experimental Assessment of the EMI Characteristics of Switching Converters With Power Semiconductor Filters,” *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2519-2533, 2020.
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Patent

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