

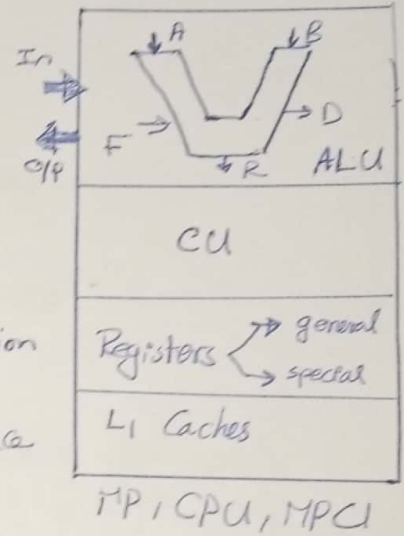
* Definitions :-

① Microprocessor :-

A microprocessor is an integrated circuit (IC) which can perform arithmetic and logic operations.

→ microprocessor consist of :-

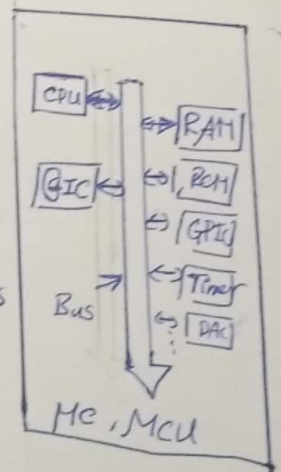
- Arithmetic and Logic unit (ALU)
 - perform logic and arithmetic operations
- Control unit (CU)
 - Control the flow of execution of instruction
- Registers
 - handle the results of operations to deduce the execution time of instructions
- I/O ports
 - to interact with other modules like RAM, ROM and Buses
- Memory (optional)
 - L1 Cache to matches the processor speed with main memory speed



② Micro Controller :-

A micro controller is an integrated circuit (IC) has an specific task consist of microprocessor (CPU), memory elements (RAM, ROM, L1, L2 caches), peripherals and general interrupt controllers.

- it can be a single chip or a multi-chip.

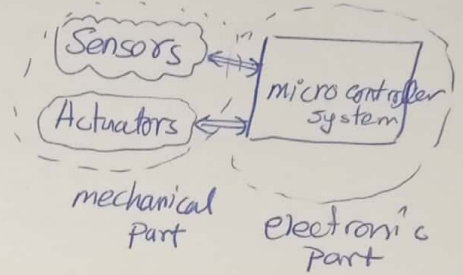


③ Embedded Systems :-

A single purpose system designed to perform one or more dedicated function, consist of hardware (MCU or SOC) and software (Bare metal or OS), with constraints like time, size and cost.

④ Mechatronic Systems :-

Systems mainly consist of two parts : electronic part (micro controllers) integrated within mechanical part (sensors and actuators) to control it. these systems used in Robots



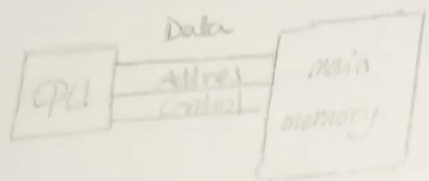
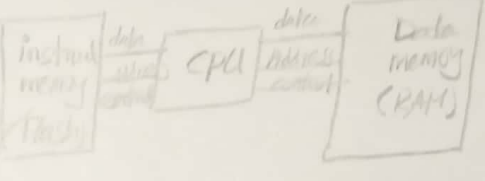
⑤ n-bit processor :-

- processor works only on n-bit of data at time.
- Data larger than n-bit has to be broken into n-bits pieces to be processed.

➔ Microprocessor vs. Microcontroller

| | Microprocessor | Microcontroller |
|--------------|---|---|
| Operation | general purpose | Special purpose |
| Architecture | Small scale processor perform arithmetic and logic operation consist of <ul style="list-style-type: none"> • ALU • CU • Registers • I/P ports • L₁ cache | integrated circuit perform specific task consist of <ul style="list-style-type: none"> • MPU • RAM • ROM • L₂ cache • GIC • peripherals (Timers, DAC, GPIO, ...) |
| Diagram | <p>The diagram shows a vertical stack of three boxes labeled 'ALU', 'CU', and 'Register'. To the right of the 'Register' box is a box labeled 'L₁ cache'. An arrow labeled 'I/P' points into the 'CU' box from the left, and an arrow labeled 'O/P' points out from the 'CU' box to the right.</p> | <p>The diagram shows a central horizontal bar labeled 'Buses'. Above the bus are two boxes labeled 'CPU' and 'GIC'. Below the bus are four boxes labeled 'RAM', 'ROM', 'GPIO', and 'SPI'. Arrows indicate bidirectional communication between the bus and each of these components.</p> |
| Power | power Consumption high | power Consumption Low |
| Architecture | Based on von-numann | Based on Harvard |
| Usage | Designed to perform Arithmetic and logic operations, and can't run without external module | Designed to perform few number of tasks, can work without external module, it is used in Embedded systems |

Von-Neumann Architecture vs Harvard Architecture

| Von-Neumann Archi. | Harvard Architecture |
|---|---|
| Data memory and instruction memory are only two sections from the main memory, this means that there is only one bus for data & instruction, this bus can't access the two section at one time. | Data memory and instruction mem. are separated memory, this means the CPU can access the two mem. at one time, there are two buses: Data bus, Address bus |
| low performance | High performance |
| Simple design | Complex design |
| Doesn't support pipelining | support pipelining |
| used in pc's and laptops | in microcontrollers and SOC |
|  |  |

Types of RAM:

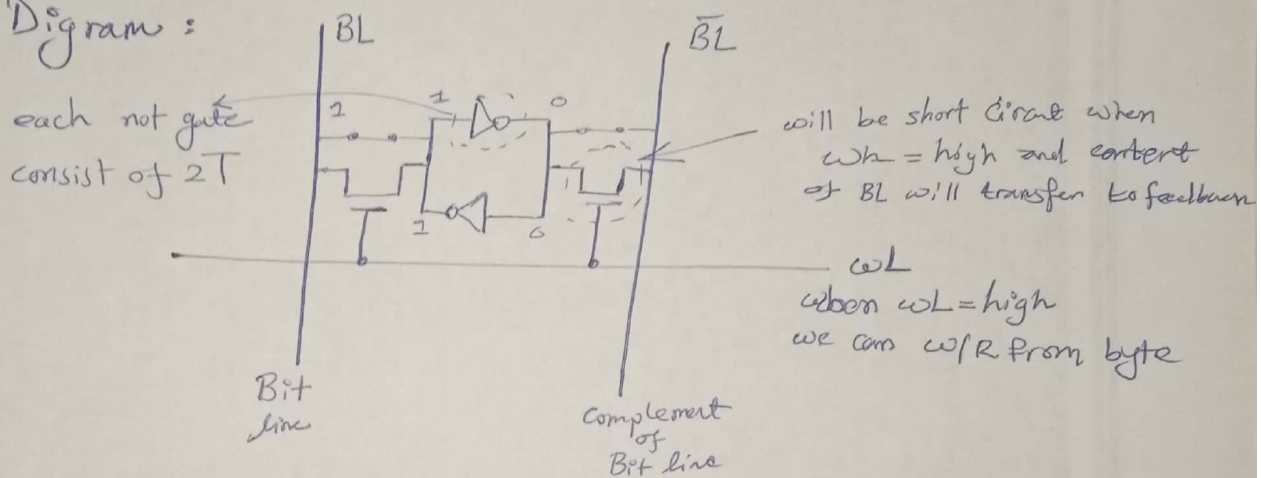
- ⇒ PROM: programmable Read only memory
 - OTP (programmable one time) since we burn the program on it one time and can't erase this program
 - for each bit there is a fuse
- ⇒ EPROM: Erasable programmable Read only memory
 - Can be reprogrammable for thousands of times
 - Can delete its whole content using UV waves
 - to delete its content, memory should be separated from circuit
 - Can't be erased electrically
- ⇒ Masked ROM: masked Read only memory
 - Can be programmed only one time by manufacturer
 - it is not user programmable ROM
 - used for Boot ROM code

⇒ Types of RAM :-

⇒ SRAM : static Random Access Memory.

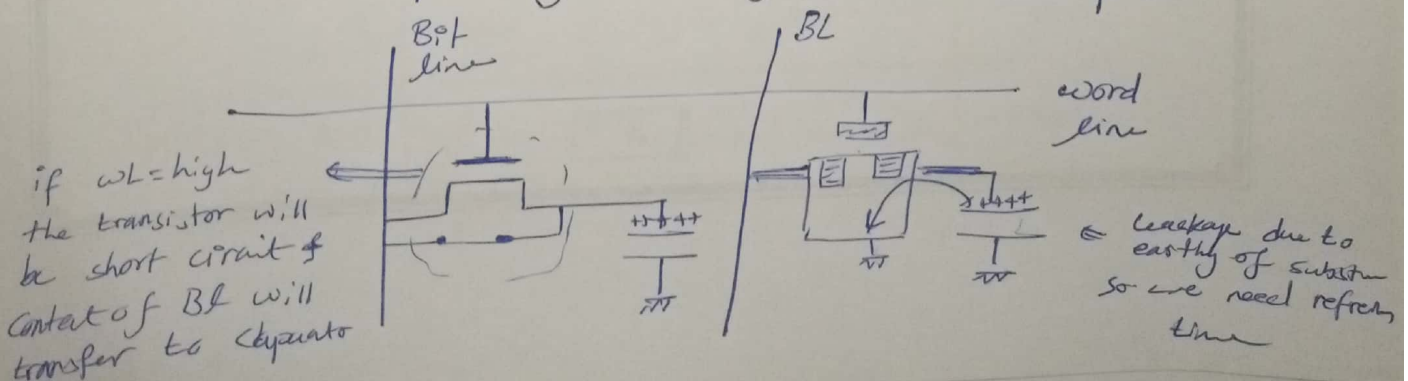
- Required 6 transistors for storing only one bit.
- Based on MOSFET technology.
- Volatile memory, if power off, all content of memory will be deleted.
- High speed memory than DRAM - since doesn't need refreshing time.
- It is the building block for caches memory.
- We can Read/write on it.
- It has complex design since it uses 6 transistor for each bit.
- We can access each byte in memory for W/R.

Diagram :



⇒ DRAM :- Dynamic Random Access Memory.

- Required 1 transistor and one capacitor for each bit
- Based on MOSFET technology
- Volatile memory
- It need almost 716 times refreshing, since the power leakage from capacitor to substrate
- Can't access the memory during refreshing time, so it is slower SRAM
- used for main memory, since it is cheaper than SRAM
- It has simple design and high power consumption



⇒ why ROM is only Read memory although we can write on it?

- Because we can't write on it at Runtime, since processor can read instructions only from it.
But we can write on it using the burner @ loading time

⇒ Comparison between Different types of memory:

| Type | volatile? | writable? | Erase size? | Max Erase size? | Cost | speed |
|------------|-----------|---|------------------|-----------------|-------------|----------------------------|
| SRAM | yes | yes | one byte | unlimited | Expensive | Fast |
| DRAM | yes | yes | one byte | unlimited | Moderate | Moderate |
| PROM | No | once, with a device programmer | Not Applicable | not Applicable | Moderate | Fast |
| EPROM | No | thousands of times with device programmer | whole memory | Limited | Moderate | Fast |
| EEPROM | No | yes | one Byte | limited | Expensive | Fast reading, slow writing |
| Flash | No | yes | Sector (section) | limited | moderate | Fast reading, slow writing |
| NVRAM | No | No yes | Byte | unlimited | Expensive | Fast |
| Masked ROM | No | No | not Applicable | Not Applicable | Inexpensive | Fast |