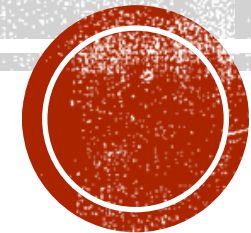
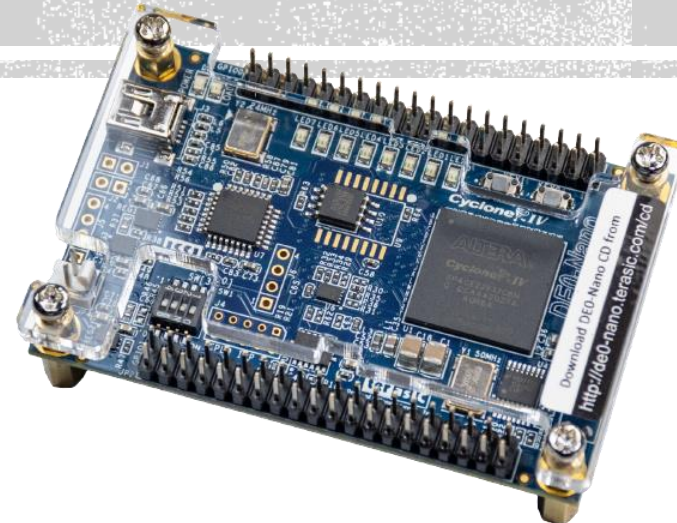


PROGRAMMATION VHDL

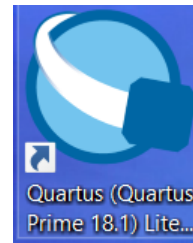


By Damian Sal y Rosas

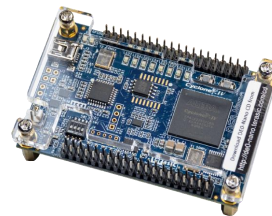
OBJECTIF:

- Faire un premier programme VHDL sur Quartus Lite 18.1
- Prends en main le cible DE0 Nano

■ Outils: **Quartus Lite**



■ Cible: DE0 Nano



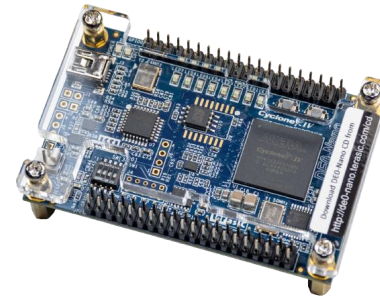
PREMIER PROGRAMME VHDL



Visualiser le
résultat sur
une lumière
LED



Programmation sur
Quartus Lite 18.1

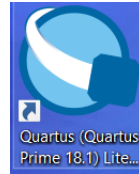


Validation sur la
cible **DE0 Nano**

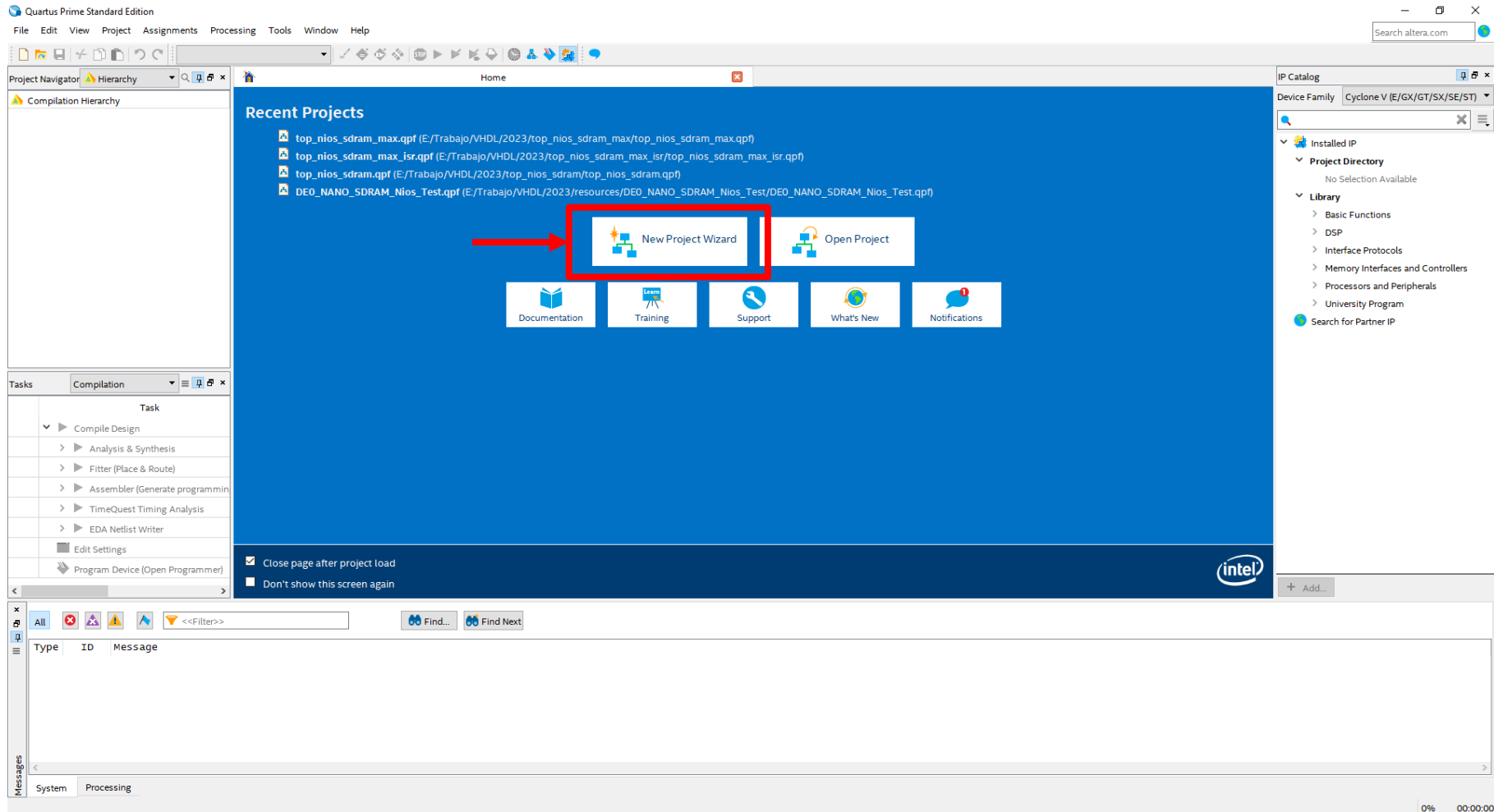
LET'S START ...



Lancer le programme



First: Il faut créer un projet
→ **New Project Wizard**



Etape 1: Créer un fichier de travail

Etape 2: New Project Wizard → ... sélectionner le repertoire → Next

1

Nom du projet

Nom de l'Entité Top

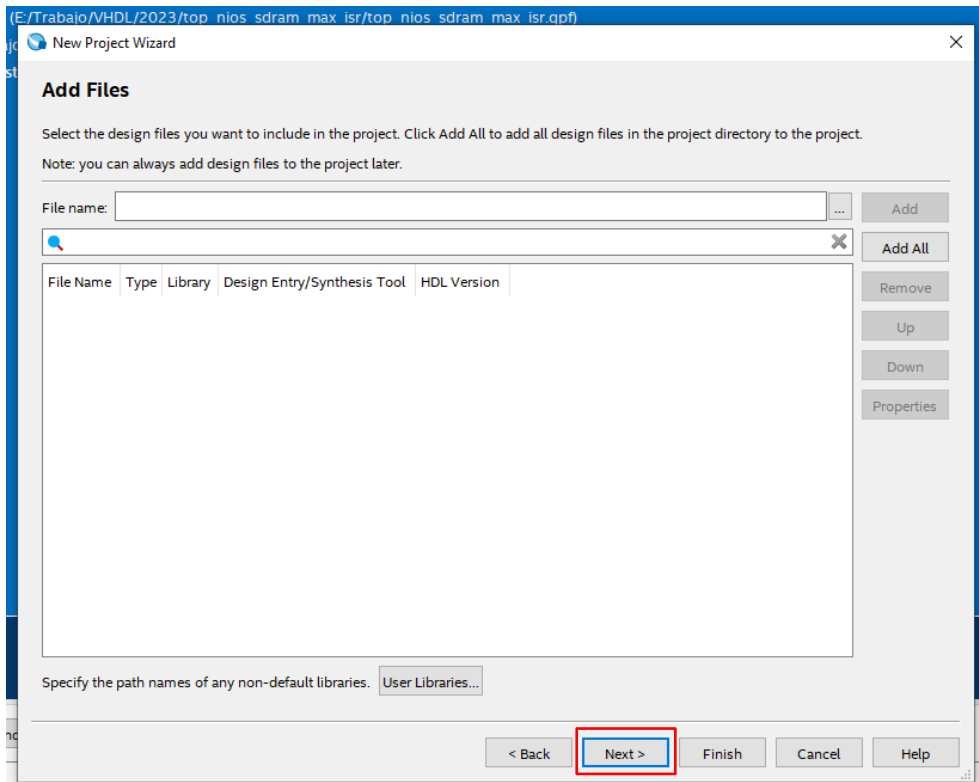
2

Sélectionner empty project → next

Considérations:

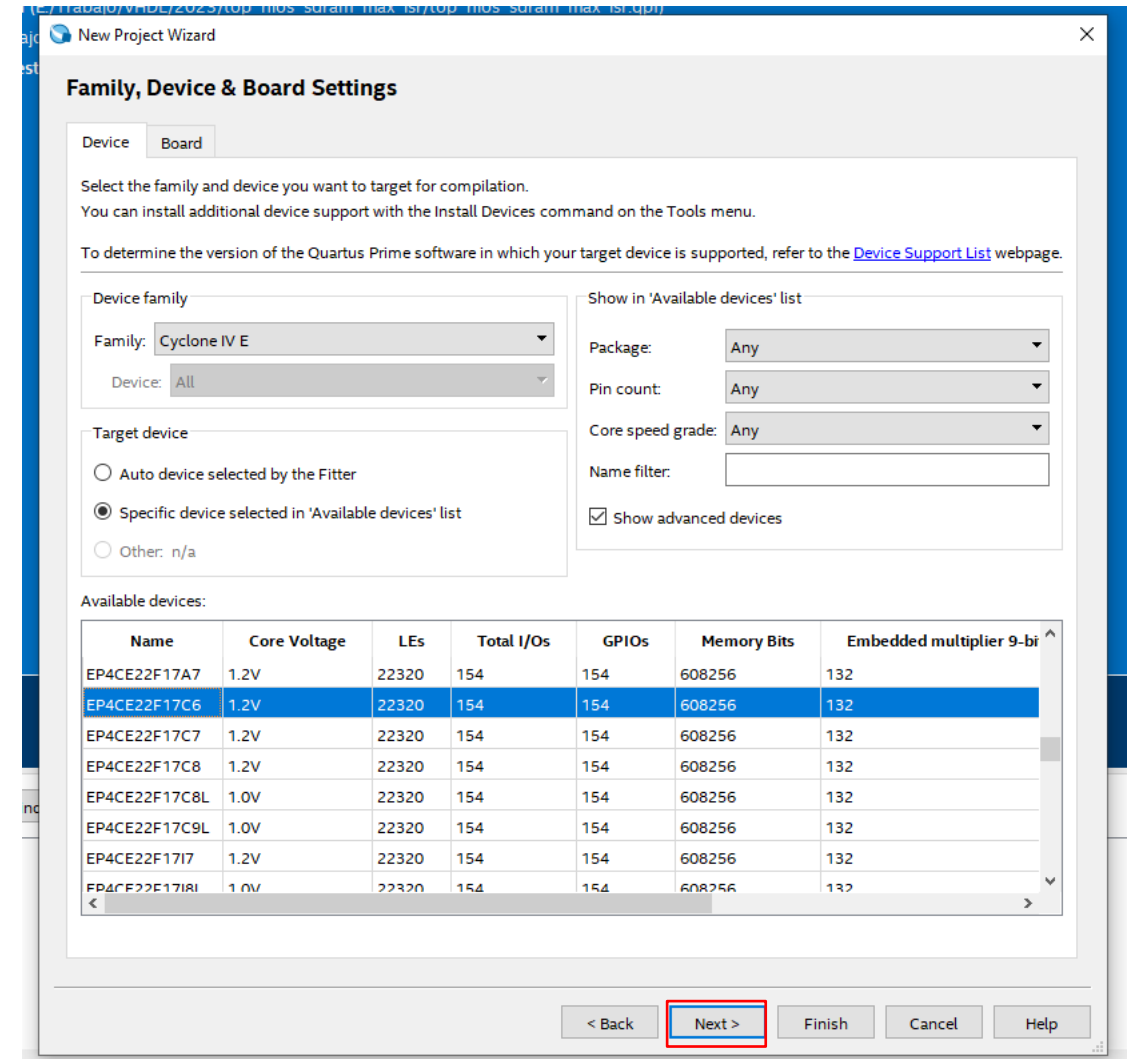
- **Short Name (le lien doit être court)**
- **Pas de espace dans le nom du projet**

3

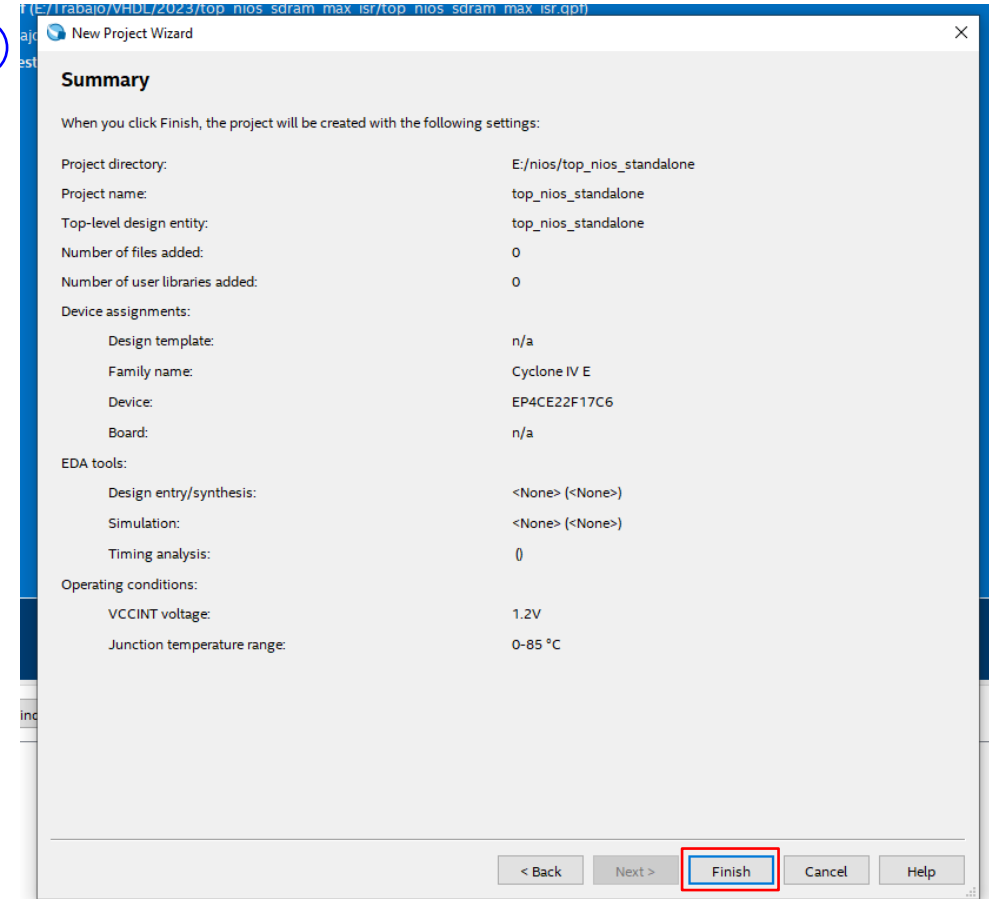
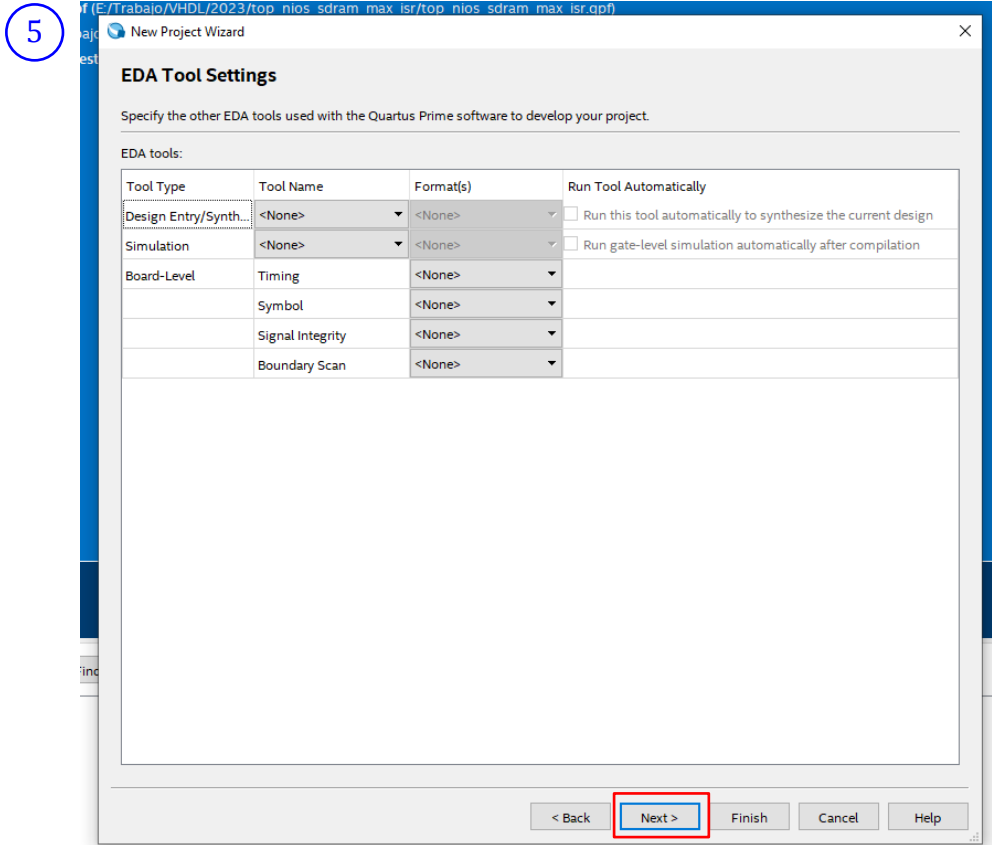


Etape 3:
pas de fichiers à ajouter → Next

4



Etape 4: sélectionner FPGA ... Altera
Cyclone IV EP4CE22F17C6 → Next



Etape 5: next → finish

* Sélectionner en mode simulation Altera
ModelSim – VHDL s'il faut simuler

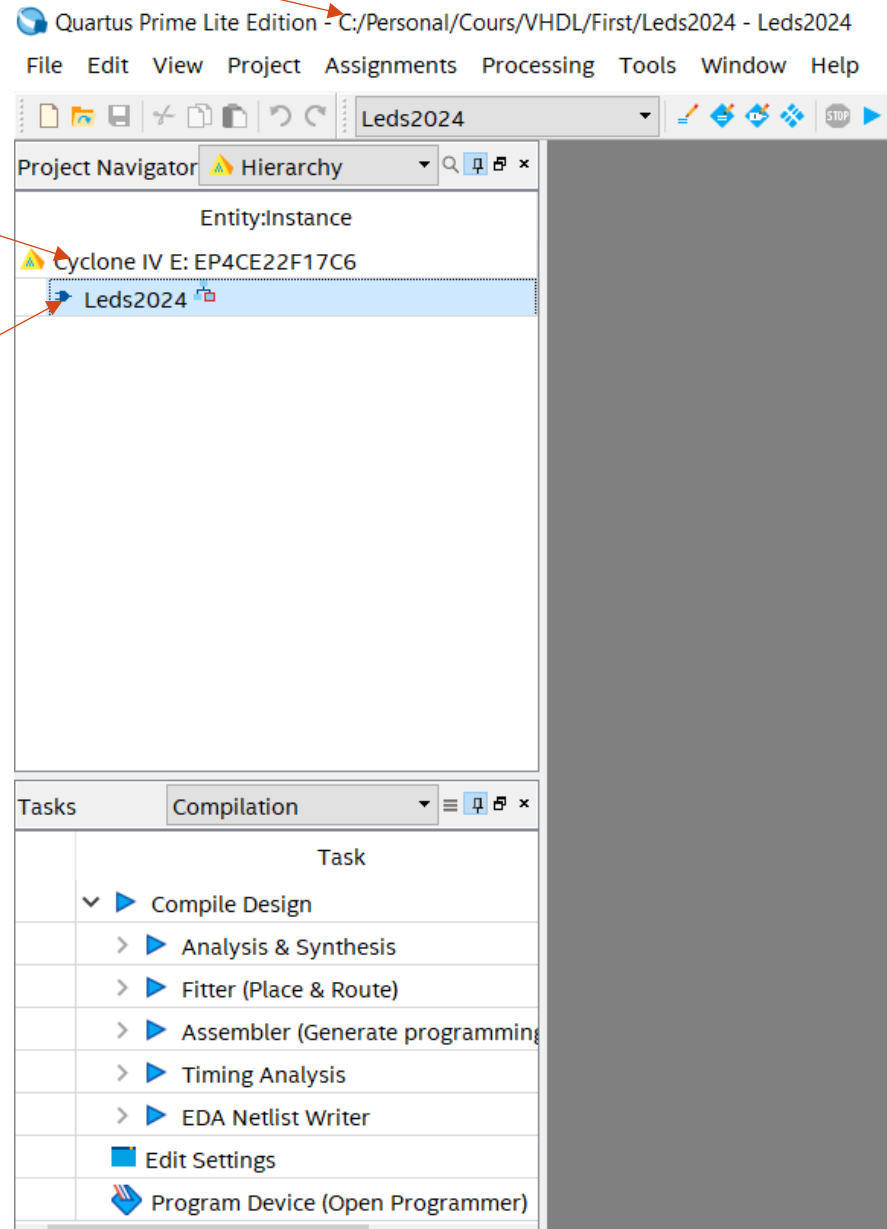
Directoire

CONSOLE DE TRAVAIL

Code du FPGA

Entité Top

Il faut ajouter le
fichier VHDL
pour le design
du circuit



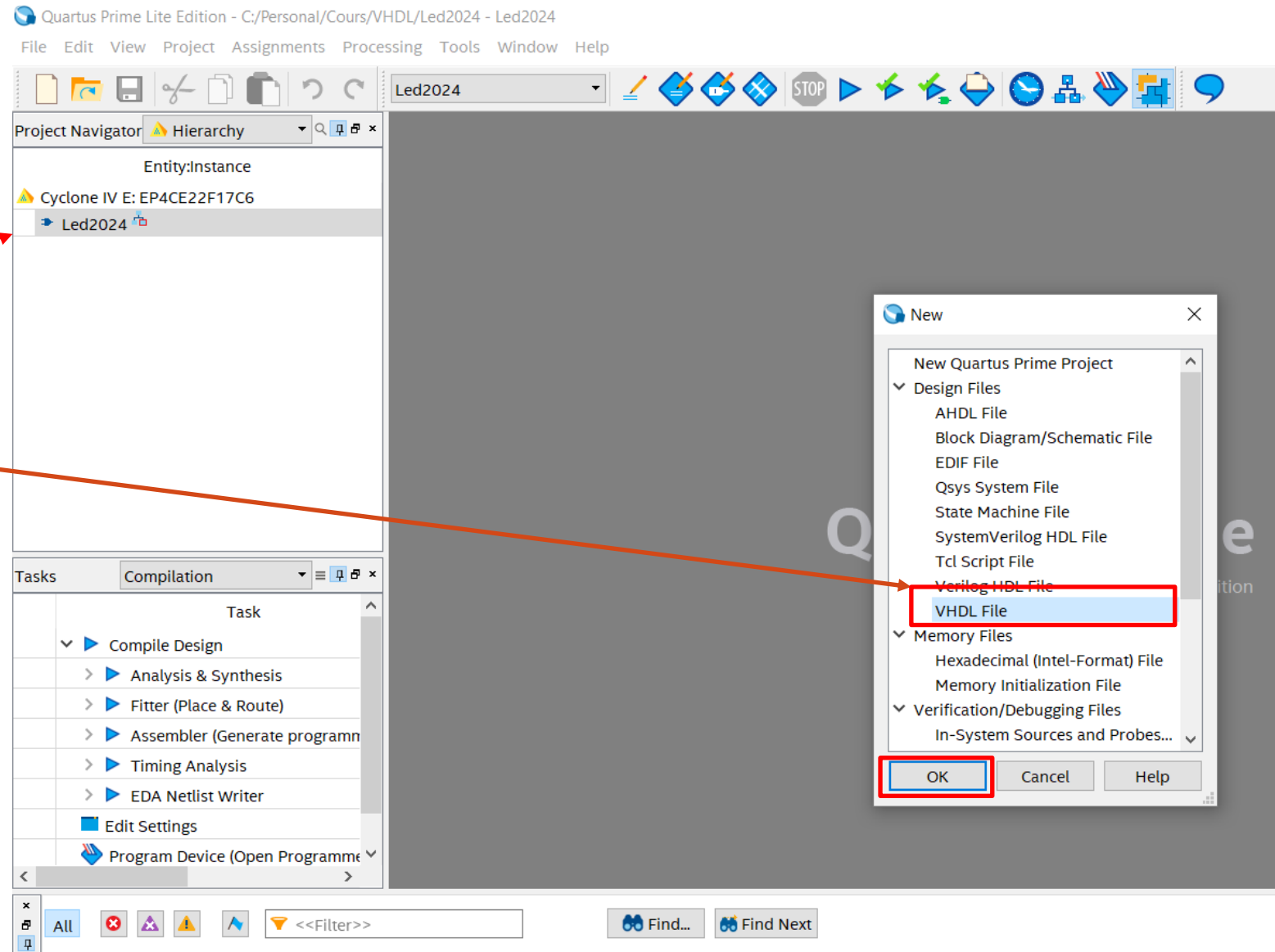
Ajouter un fichier VHDL sur la console de travail

Entité Top

Etape 1:

Sélectionner: File → New

- Choisir VHDL File -> OK



Ajouter un fichier VHDL sur la console de travail

Apparait un nom par défaut:

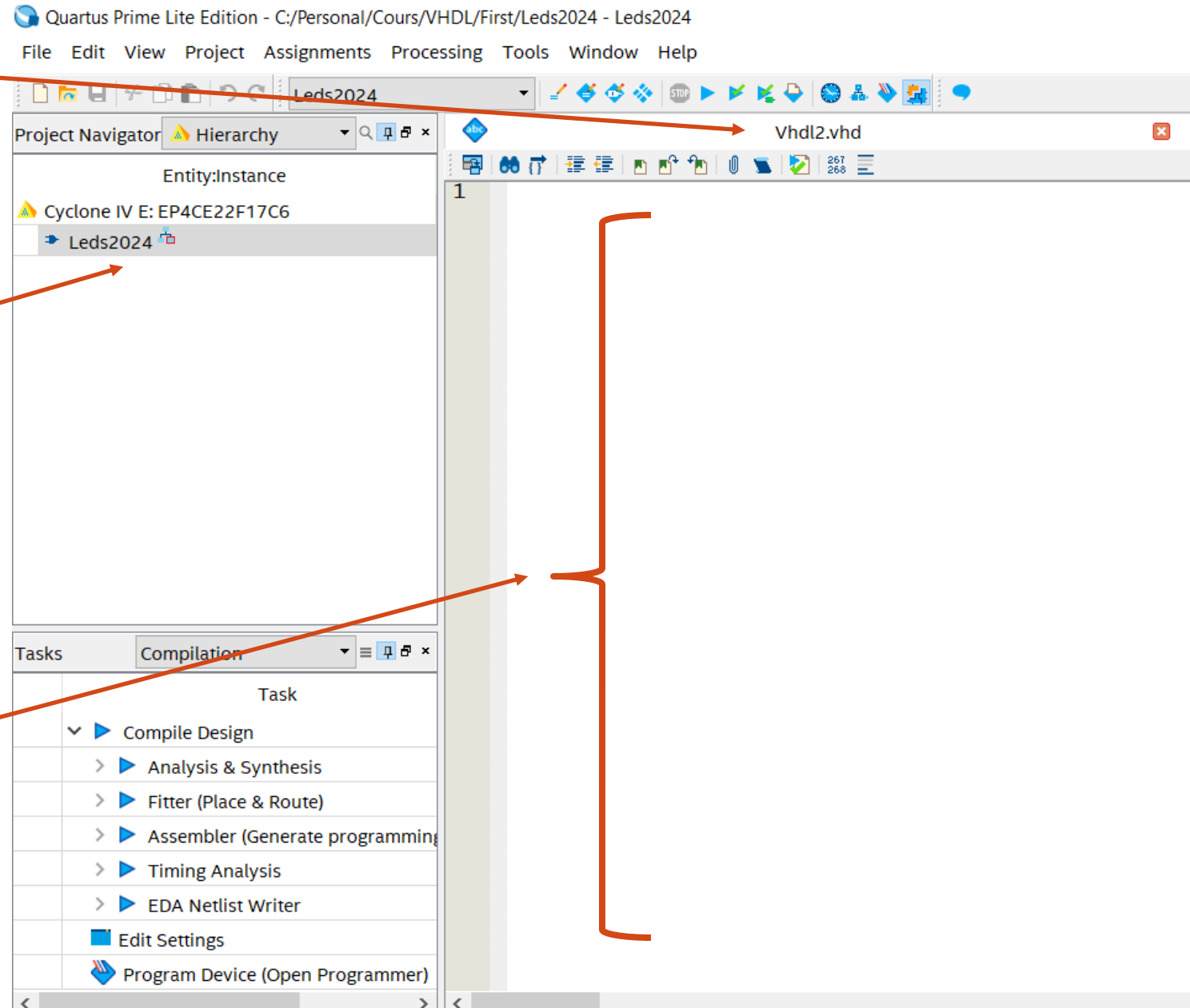
1. Il faut modifier le nom correspondant au nom de l'ENTITE

Entité Top

Après:

Il faut ajouter le code VHDL:

- library
- Entity
- architecture



Ajouter un fichier VHDL sur la console de travail

Etape 2:

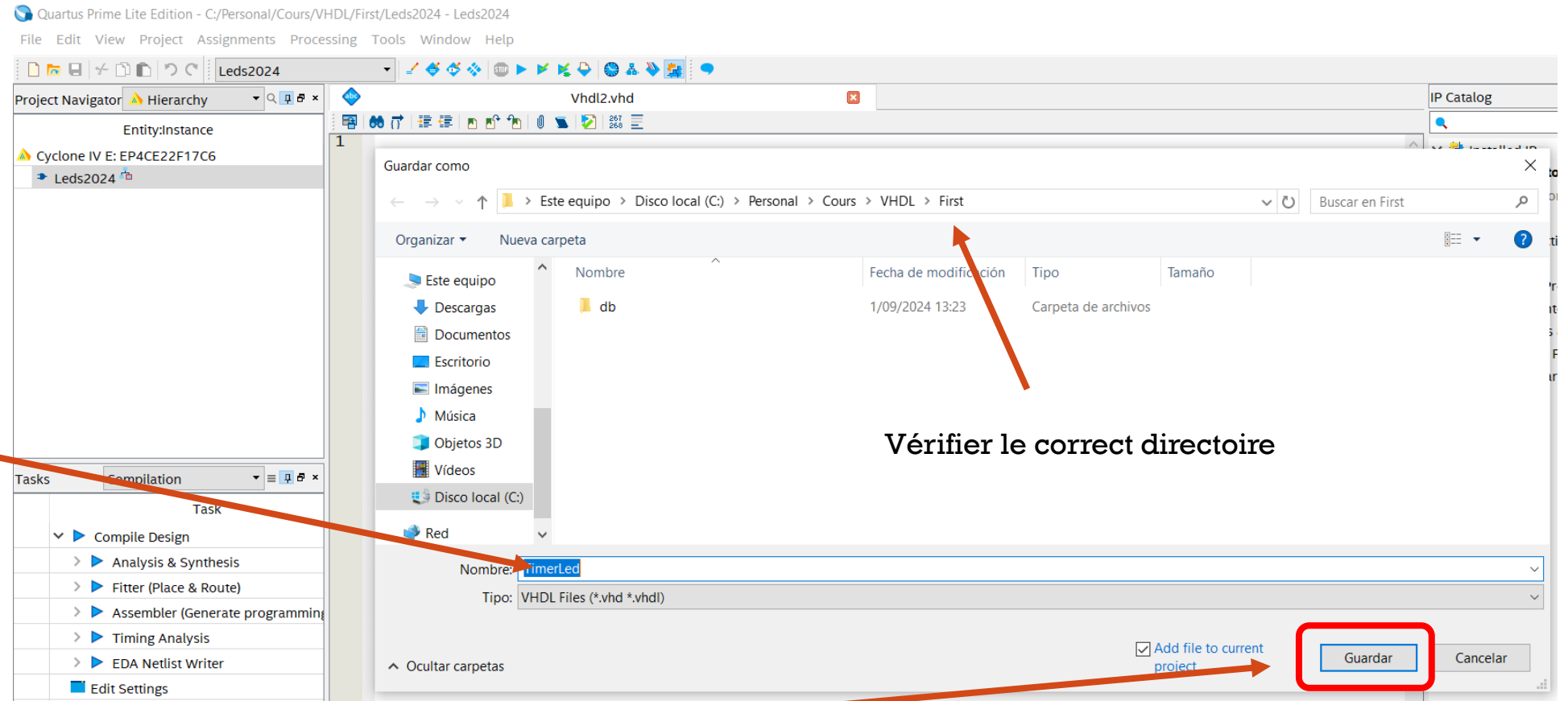
Garder le fichier avec le nom de l'entité

Exemple: TimerLed

File->SaveAs..

Indiquer le nom de l'entité

TimerLed

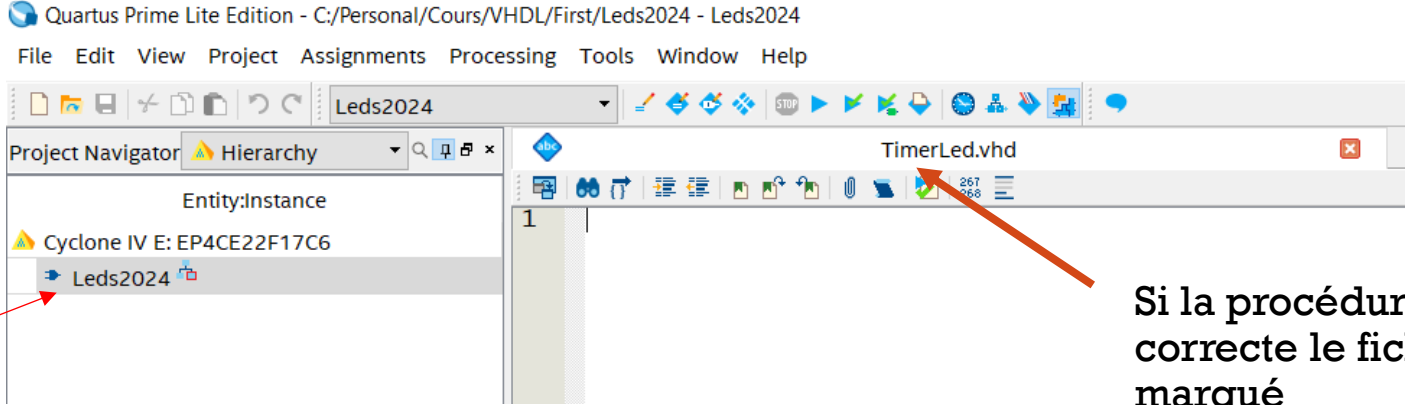


Finalement:

→ Save

Attention: l'entité s'appelle « TimerLed » et doit être désignée comme entité TOP

Ajouter un fichier VHDL sur la console de travail



The screenshot shows the Quartus Prime Lite Edition interface. The Project Navigator on the left displays the hierarchy: Entity:Instance, Cyclone IV E: EP4CE22F17C6, and Leds2024. A green box labeled "Entité Top" points to the Leds2024 entity. The main editor window shows the TimerLed.vhd file, which is marked with a green checkmark icon, indicating it is correctly added to the project.

Entité Top

Si la procédure est correcte le fichier est marqué
TimerLed.vhd

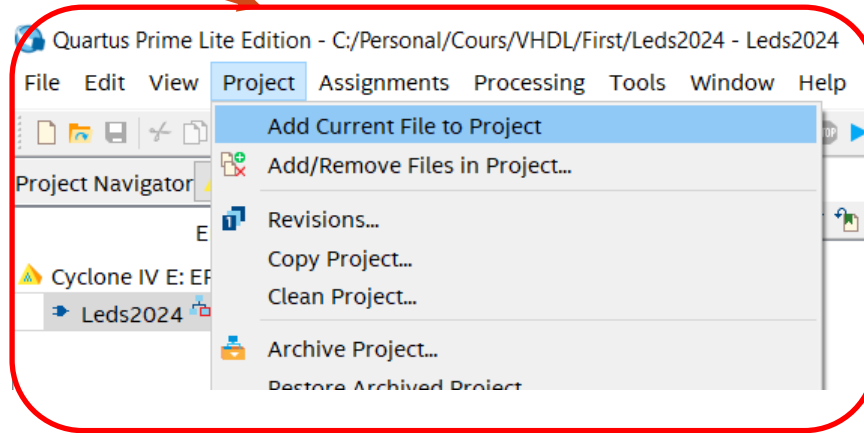
Etape 3:

On doit ajouter le fichier **TimerLed.vhd** au projet:

→Projet

→ Add current File to Project

Attention: l'entité s'appelle « TimerLed » et doit être désignée comme entité TOP



Ajouter le code « VHDL »

Etape 4:

Déclarer le code VHDL

- Library
- Entity
- Architecture

Quartus Prime Lite Edition - C:/Personal/Cours/VHDL/First/Leds2024 - Leds2024

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Hierarchy Leds2024

Entity:Instance

Cyclone IV E: EP4CE22F17C6

Leds2024

Library

Entity

Architecture

Tasks Compilation

Task

> Compile Design

Edit Settings

Program Device (Open Programmer)

TimerLed.vhd

```
1
2  -- declaration des libraries
3
4  library ieee;
5  use ieee.std_logic_1164.all;
6  use ieee.std_logic_unsigned.all;
7  use ieee.std_logic_arith.all;
8
9  entity TimerLed is
10
11    -- generic (declaration de constants);
12    -- port(declaration de ports d'entrée et sortie);
13  end TimerLed;
14
15  architecture Beh of TimerLed is
16
17    -- declaration de type de données, signals, composants
18
19  begin
20
21    -- declaration du "comportement" du circuit --
22
23  end Beh;
```

Erreur 2: changer l'entité « Leds2024 » à l'entité « TimerLed » comme entité TOP

Ajouter le code « VHDL »

Etape 5:

Compléter:

- Library
- Entity
- Architecture

Etape 6:

1. Clic dans:

→ Compile design

2. Résultat **X**: « erreurs dans le fichier »

Erreur 1: assignation d'une variable

Erreur 2: Entité top incorrecte

Quartus Prime Lite Edition - C:/Personal/Cours/VHDL/First/Leds2024 - Leds2024

File Edit View Project Assignments Processing Tools Window Help

Leds2024

Project Navigator Hierarchy

Entity:Instance

Cyclone IV E: EP4CE22F17C6

Leds2024

Library

Entity

Architecture

TimerLed.vhd

```
1
2 -- declaration des libraries
3
4 library ieee;
5 use ieee.std_logic_1164.all;
6 use ieee.std_logic_unsigned.all;
7 use ieee.std_logic_arith.all;
8
9 entity TimerLed is
10     generic(max: natural:=2500000);
11     port(clk:in std_logic;
12         rst:in std_logic;
13         led: out std_logic); -- signal led
14 end TimerLed;
15
16
17 architecture Beh of TimerLed is
18 begin
19
20     process(clk,rst)
21         variable temp:integer range 0 to max;
22         variable tout:std_logic;
23     begin
24         if (rst='0') then
25             led<='0';
26             temp:=0;
27             tout:='0';
28         elsif (rising_edge(clk)) then
29             temp:=temp+1;
30             if (temp=max) then
31                 temp:=0;
32                 tout:=not tout;
33             end if;
34             led<=tout;
35         end if;
36     end process;
37
38 end Beh;
```

Tasks

Compile Design

Edit Settings

Program Device (Open Programmer)

Erreur 1

Correction du code « VHDL »

Etape 7:

Erreur 1:

Correction du code VHDL

temp:=temp+1;

The screenshot shows the Quartus Prime IDE. On the left, the 'Tasks' pane is open, showing the 'Compilation' task. The 'Compile Design' task is selected. On the right, the VHDL code is displayed. The code is a process for a timer LED. The line `temp:=temp+1;` is highlighted in blue. Below the code, the 'Messages' pane shows a list of errors and warnings. The error 12019 is highlighted, indicating a syntax error at line 29 near the text `temp:=temp+1;`.

```
18 begin
19
20 process(clk,rst)
21   variable temp:integer range 0 to max;
22   variable tout:std_logic;
23 begin
24   if (rst='0') then
25     led<='0';
26     temp:=0;
27     tout:='0';
28   elsif (rising_edge(clk)) then
29     temp:=temp+1;
30     if (temp=max) then
31       temp:=0;
32       tout:=not tout;
33   end if;
34 end process;
```

Messages:

- Command: quartus_map --read_settings_files=on --write_settings_files=off Leds2024 -c Leds2024
- 18236 Number of processors has not been specified which may cause overloading on shared machines.
- 20030 Parallel compilation is enabled and will use 4 of the 4 processors detected
- 12019 Can't analyze file -- file Leds2024.vhd is missing
- 10500 VHDL syntax error at TimerLed.vhd(29) near text "="; expecting "(", or "'", or "."
- 12021 Found 0 design units, including 0 entities, in source file timerled.vhd
- Quartus Prime Analysis & Synthesis was unsuccessful. 1 error, 2 warnings
- 293001 Quartus Prime Full Compilation was unsuccessful. 3 errors, 2 warnings

Etape 7:

Erreur 2:

Indiquer l'entité top: TimerLed

The screenshot shows the Quartus Prime IDE. On the left, the 'Tasks' pane is open, showing the 'Compilation' task. The 'Compile Design' task is selected. On the right, the VHDL code is displayed. The code is a process for a timer LED. The line `temp:=temp+1;` is highlighted in blue. Below the code, the 'Messages' pane shows a list of errors and warnings. The error 12007 is highlighted, indicating that the top-level design entity 'Leds2024' is undefined. A red arrow points from the text 'Indiquer l'entité top: TimerLed' to this error message.

```
18 begin
19
20 process(clk,rst)
21   variable temp:integer range 0 to max;
22   variable tout:std_logic;
23 begin
24   if (rst='0') then
25     led<='0';
26     temp:=0;
27     tout:='0';
28   elsif (rising_edge(clk)) then
29     temp:=temp+1;
30     if (temp=max) then
31       temp:=0;
32       tout:=not tout;
33   end if;
34 end process;
```

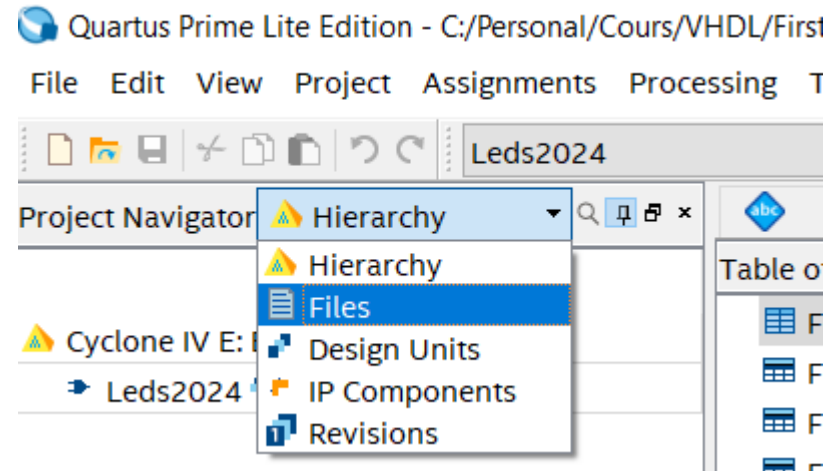
Messages:

- Command: quartus_map --read_settings_files=on --write_settings_files=off Leds2024 -c Leds2024
- 18236 Number of processors has not been specified which may cause overloading on shared machines.
- 20030 Parallel compilation is enabled and will use 4 of the 4 processors detected
- 12019 Can't analyze file -- file Leds2024.vhd is missing
- 12021 Found 2 design units, including 1 entities, in source file timerled.vhd
- 12007 Top-level design entity "Leds2024" is undefined
- Quartus Prime Analysis & Synthesis was unsuccessful. 1 error, 2 warnings
- 293001 Quartus Prime Full Compilation was unsuccessful. 3 errors, 2 warnings

Correction du code « VHDL »

Etape 7: Correction de l'Erreur 2:

1. Click Hierarchy → Files



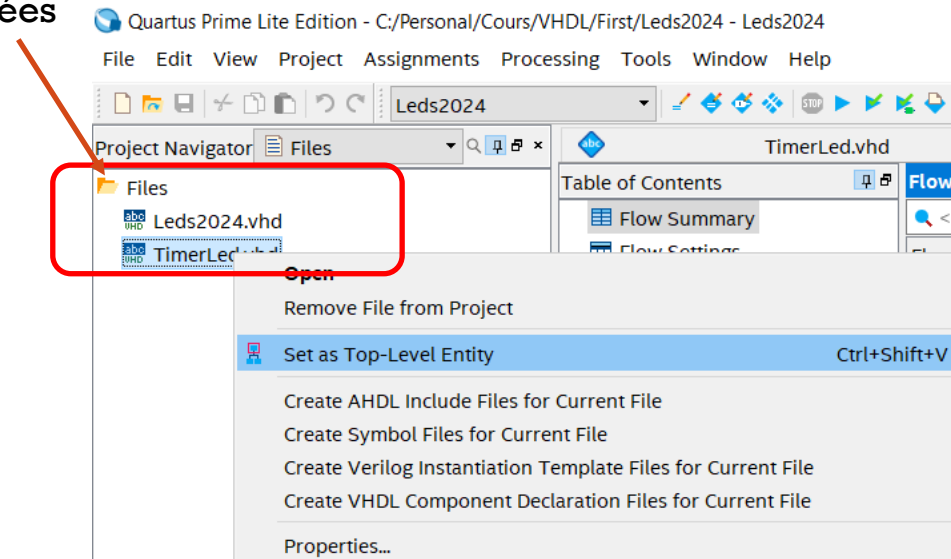
Etape 7: Correction de l'Erreur 2:

La liste des entités VHDL sont visualisées

2. Click droite in Entité TimerLet

Sélectionner:

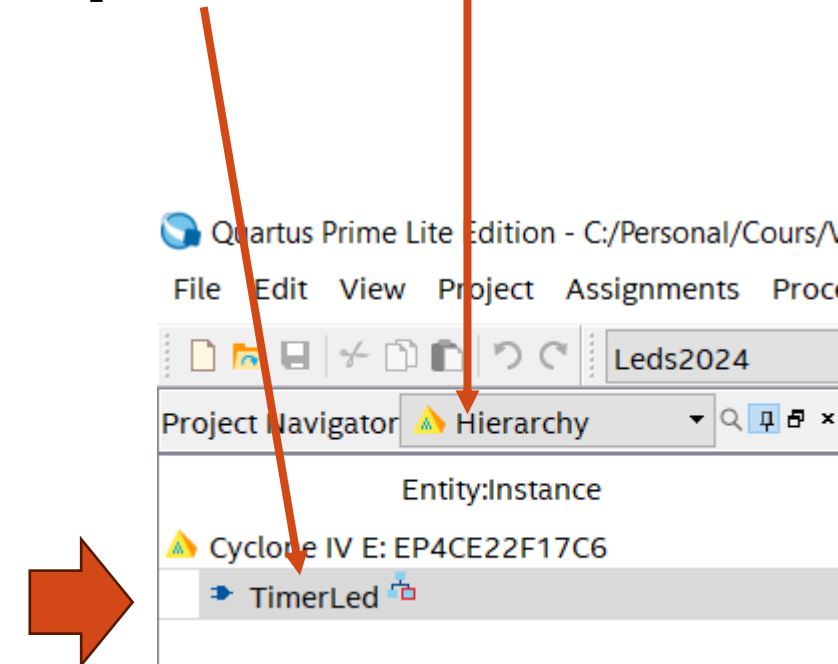
→ Set as Top-Level Entity



Etape 7: Correction de l'Erreur 2:

3. Sélectionner Hierarchy

4. Vérifier que TimerLed est l'entité top



Compilation réussie du programme VHDL

Quartus Prime Lite Edition - C:/Personal/Cours/VHDL/First/Leds2024 - Leds2024

File Edit View Project Assignments Processing Tools Window Help

Leds2024

Project Navigator Hierarchy

Entity: Instance

Cyclone IV E: EP4CE22F17C6

TimerLed

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- Timing Analyzer

Flow Summary

<<Filter>>

Flow Status	Successful - Sun Sep 01 18:41:06 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Leds2024
Top-level Entity Name	TimerLed
Family	Cyclone IV E
Device	EP4CE22F17C6
Timing Models	Final
Total logic elements	40 / 22,320 (< 1 %)
Total registers	24
Total pins	3 / 154 (2 %)
Total virtual pins	0
Total memory bits	0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	0 / 4 (0 %)

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer

All

<<Filter>>

Find... Find Next

Type	ID	Message
Info	144001	Generated suppressed messages file C:/Personal/Cours/VHDL/First/output_files/Leds2024.fit.smsg
Info		Quartus Prime Fitter was successful. 0 errors, 5 warnings
Info		*****
Info		Running Quartus Prime Assembler
Info		Command: quartus_asm --read_settings_files=off --write_settings_files=off Leds2024 -c Leds2024
Warning	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global
Info	115031	Writing out detailed assembly data for power analysis
Info	115030	Assembler is generating device programming files

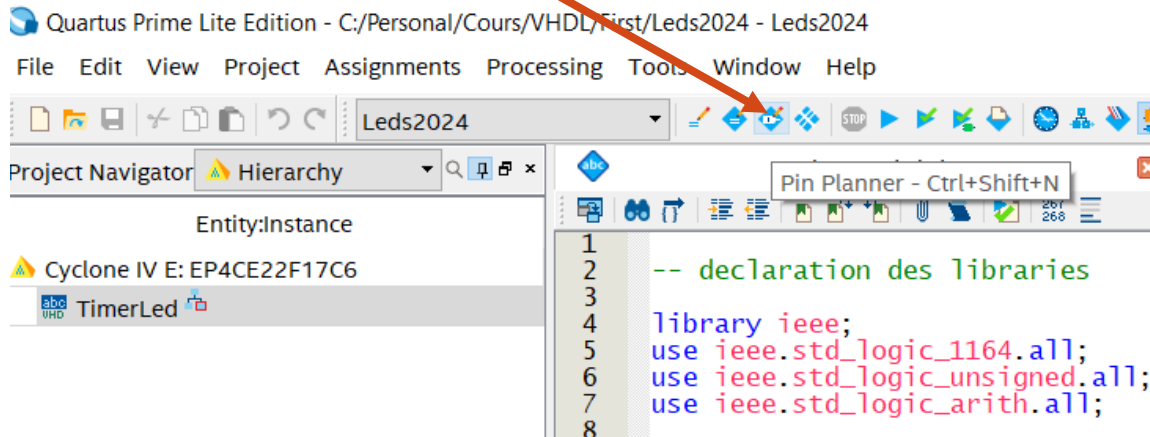
Entité top:
TimerLed.vhd

Process de compilation
réussi

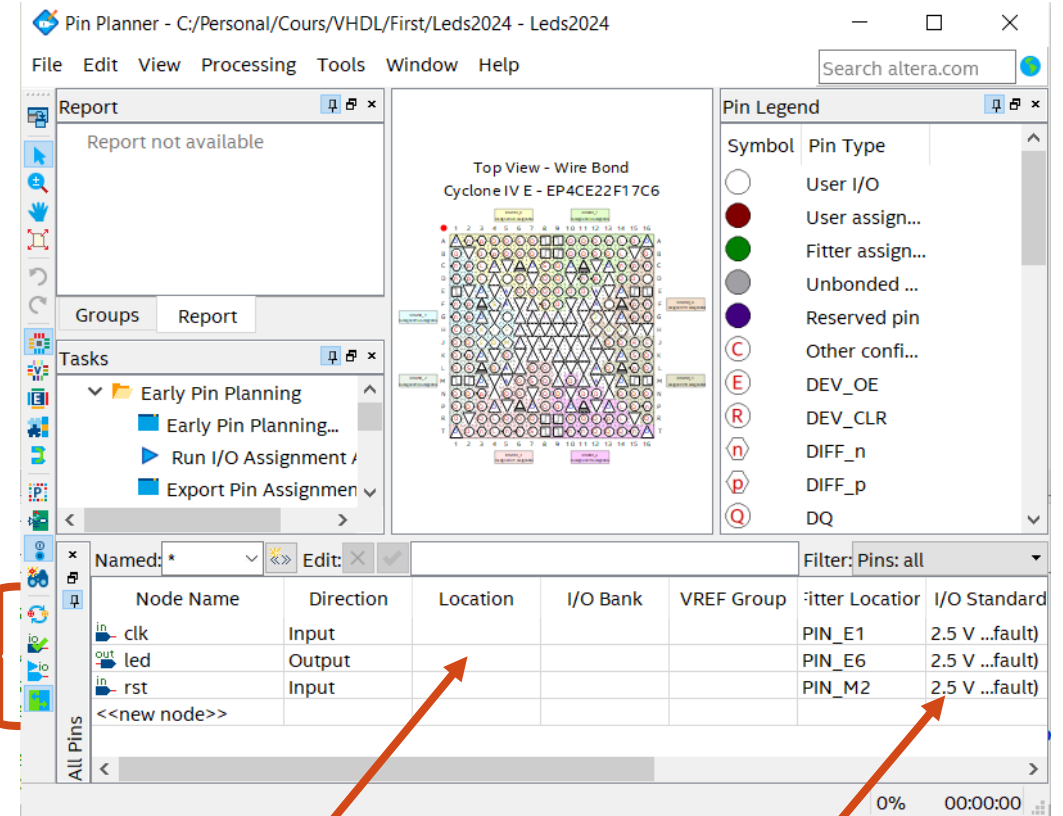
Assignment de pins

- Une fois que la compilation est réussie, il faut assigner les entrées et sorties du FPGA (pins)
- L'assignation de pins est faite avec l'option **Pin Planner**

Click → PinPlanner



Entrées et
sorties de
l'entité



Indiquer le port du FPGA
(voir datasheet DE0 Nano)

Indiquer la tension du port
(voir datasheet DE0 Nano)

Assignment de pins

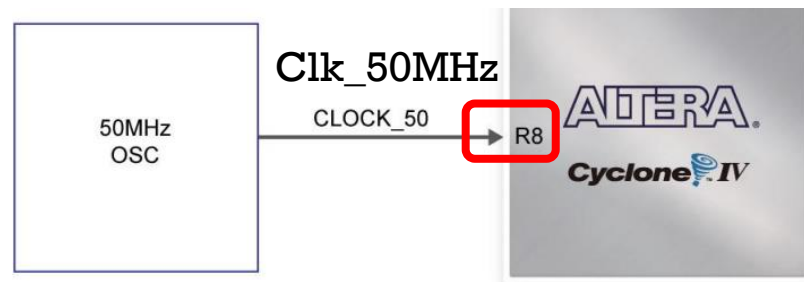
Entrées et sorties du FPGA

Table 3-1 Pin Assignments for Push-buttons

Signal Name	FPGA Pin No.	Description	I/O Standard
rst KEY[0]	PIN_J15	Push-button[0]	3.3V
KEY[1]	PIN_E1	Push-button[1]	3.3V

Table 3-2 Pin Assignments for LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
led LED[0]	PIN_A15	LED Green[0]	3.3V
LED[1]	PIN_A13	LED Green[1]	3.3V
LED[2]	PIN_B13	LED Green[2]	3.3V
LED[3]	PIN_A11	LED Green[3]	3.3V
LED[4]	PIN_D1	LED Green[4]	3.3V
LED[5]	PIN_F3	LED Green[5]	3.3V
LED[6]	PIN_B1	LED Green[6]	3.3V
LED[7]	PIN_L3	LED Green[7]	3.3V



Assignment de pins

Pin Planner - C:/Personal/Cours/VHDL/First/Leds2024 - Leds2024

File Edit View Processing Tools Window Help

Search altera.com

Report

Report not available

Groups Report

Tasks

- Early Pin Planning
 - Early Pin Planning...
 - Run I/O Assignment...

Top View - Wire Bond
Cyclone IV E - EP4CE22F17C6

Pin Legend

Symbol	Pin Type
○	User I/O
●	User assign...
●	Fitter assign...
●	Unbonded ...
●	Reserved pin
○	Other confi...
○	DEV_OE
○	DEV_CLR
○	DIFF_n
○	DIFF_p
○	DQ

Named: * Edit: 3.3-V LVTTTL Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in clk	Input	PIN_r8	3	B3_NO	PIN_E1	3.3-V LVTTTL
out led	Output	PIN_a15	7	B7_NO	PIN_E6	3.3-V LVTTTL
in rst	Input	PIN_j15	5	B5_NO	PIN_M2	3.3-V LVTTTL
<<new node>>						

All Pins

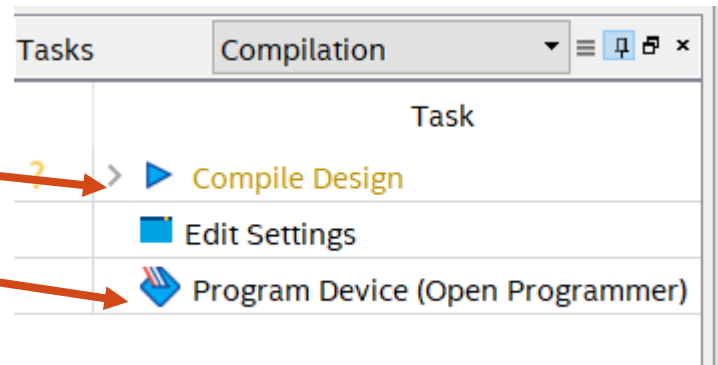
0% 00:00:00

Fermer la
fenêtre après
l'assignation
de pins

Validation sur la carte

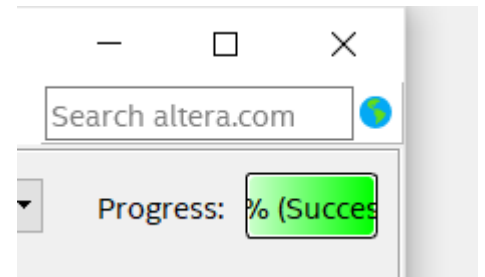
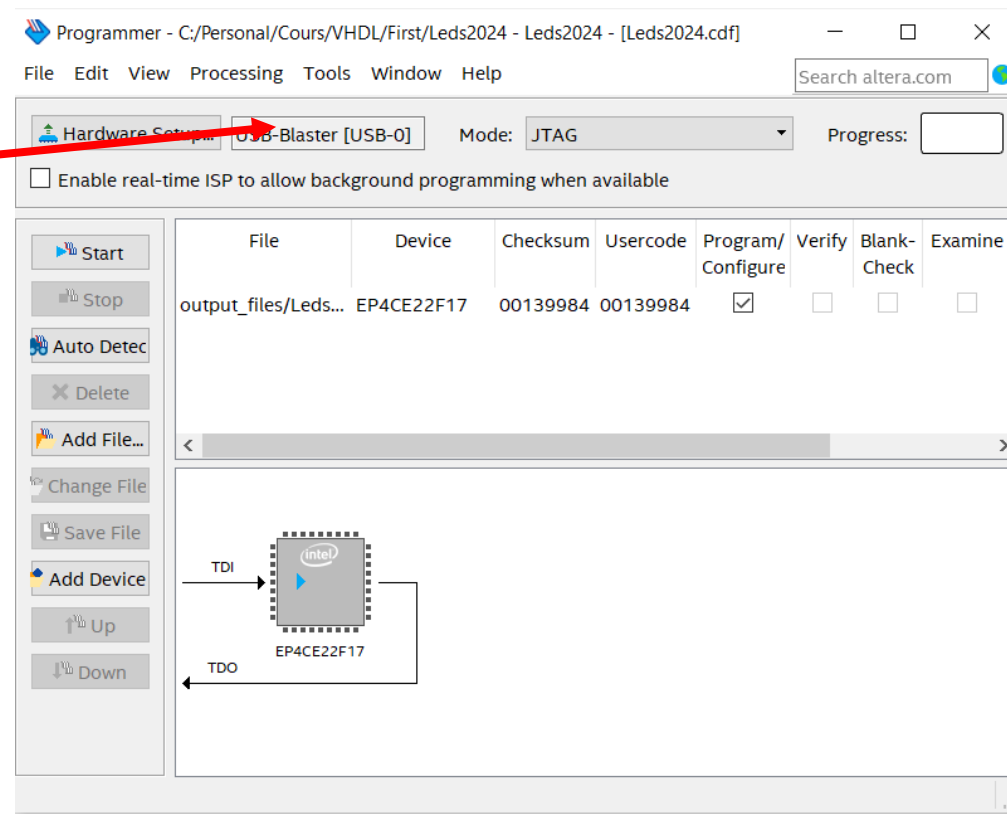
1. Compiler une 2eme fois (click)

2. Programmer la carte



3. Sélectionner USB-Blaster

4. Envoi du fichier .sof vers la carte



5. Programmation ok

