

STM32 CubeMX

1. Description

1.1. Project

Project Name	Bachelor
Board Name	custom
Generated with:	STM32CubeMX 6.2.0
Date	05/27/2021

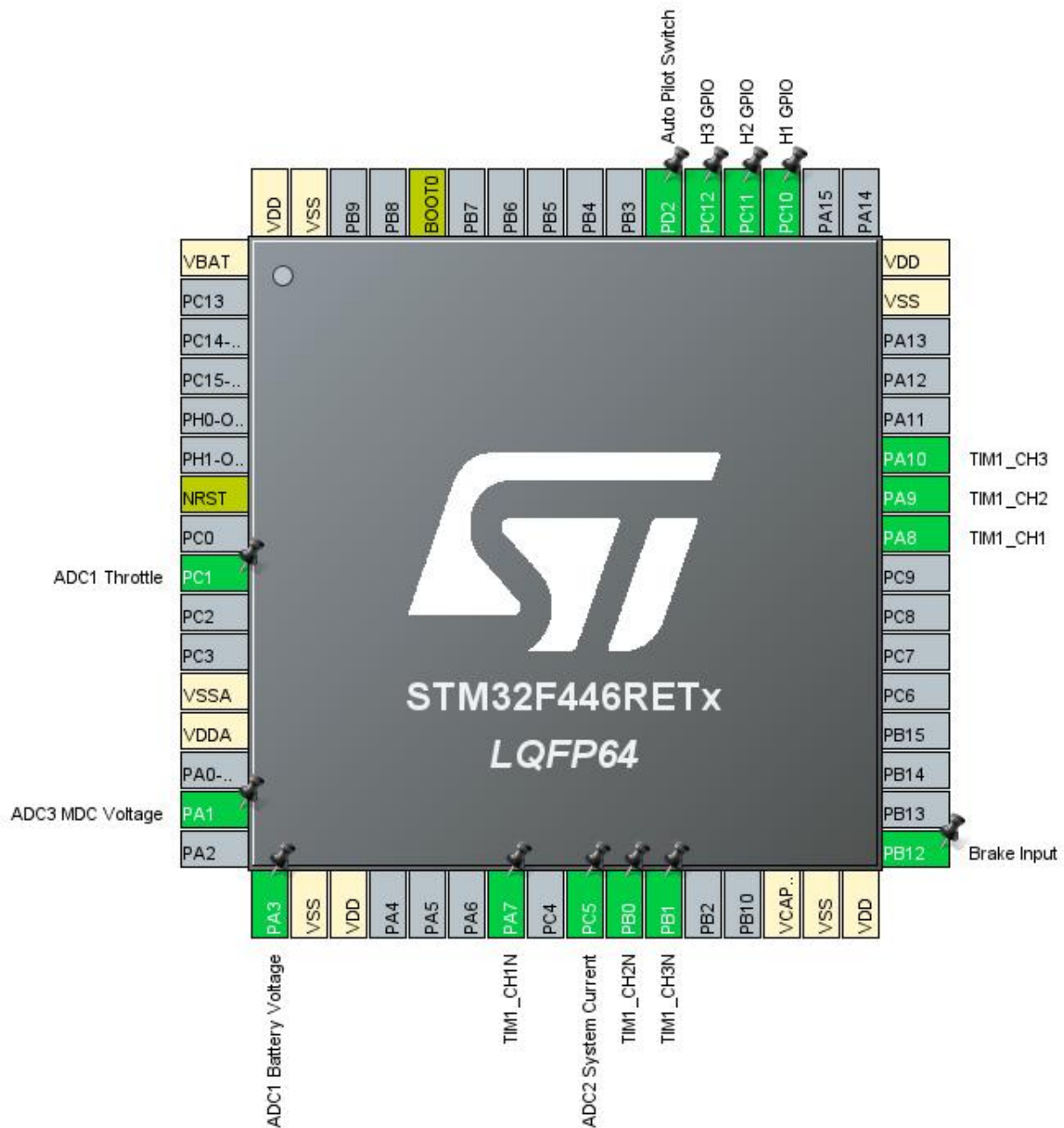
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration

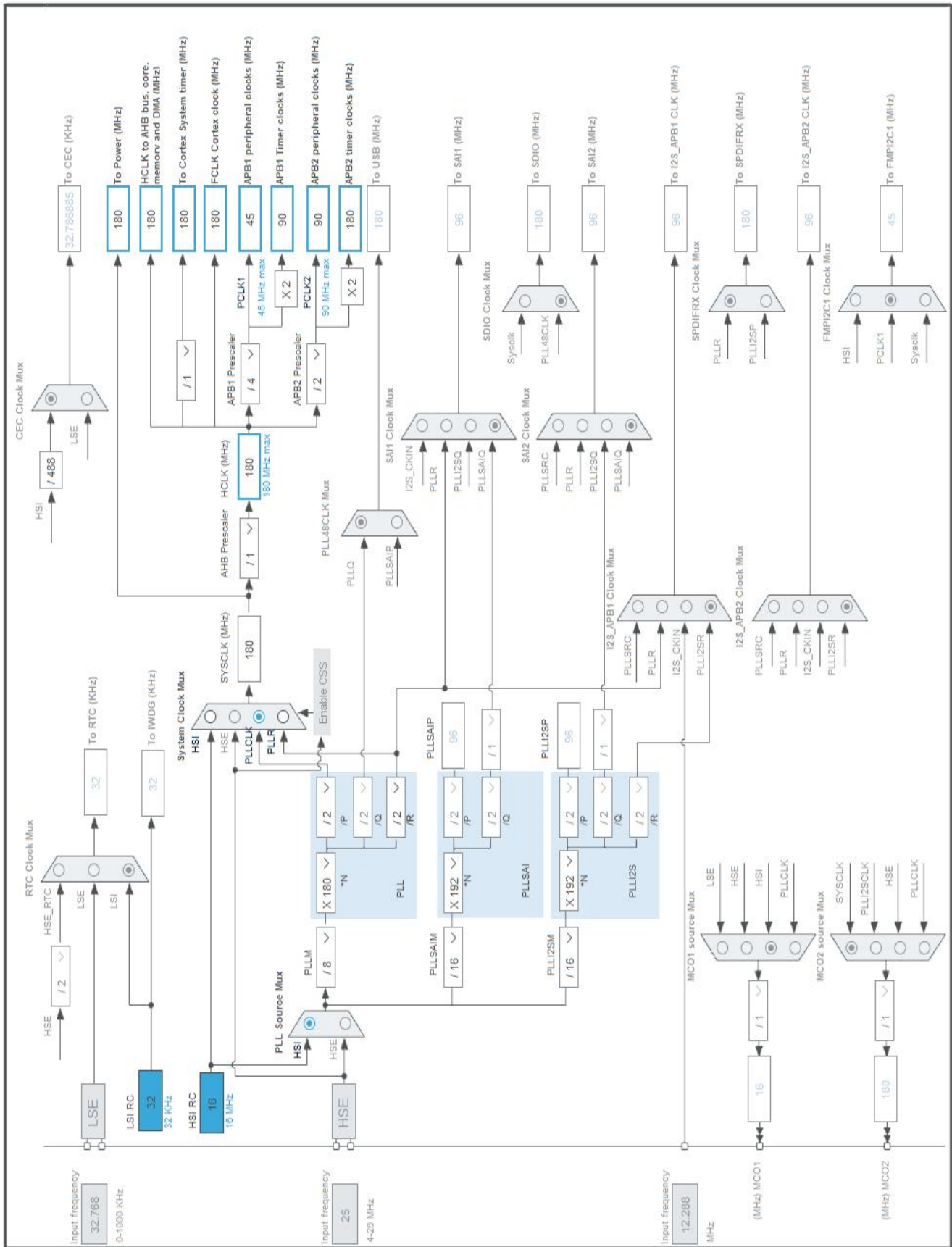


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
9	PC1	I/O	ADC1_IN11	ADC1 Throttle
12	VSSA	Power		
13	VDDA	Power		
15	PA1	I/O	ADC3_IN1	ADC3 MDC Voltage
17	PA3	I/O	ADC1_IN3	ADC1 Battery Voltage
18	VSS	Power		
19	VDD	Power		
23	PA7	I/O	TIM1_CH1N	
25	PC5	I/O	ADC2_IN15	ADC2 System Current
26	PB0	I/O	TIM1_CH2N	
27	PB1	I/O	TIM1_CH3N	
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Input	Brake Input
41	PA8	I/O	TIM1_CH1	
42	PA9	I/O	TIM1_CH2	
43	PA10	I/O	TIM1_CH3	
47	VSS	Power		
48	VDD	Power		
51	PC10 *	I/O	GPIO_Input	H1 GPIO
52	PC11 *	I/O	GPIO_Input	H2 GPIO
53	PC12 *	I/O	GPIO_Input	H3 GPIO
54	PD2 *	I/O	GPIO_Input	Auto Pilot Switch
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Bachelor
Project Folder	C:\Users\kenne\git\JohanSebastianBachelor\Bachelor
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_TIM1_Init	TIM1
6	MX_ADC2_Init	ADC2
7	MX_ADC3_Init	ADC3
8	MX_TIM8_Init	TIM8
9	MX_TIM2_Init	TIM2
10	MX_TIM6_Init	TIM6

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

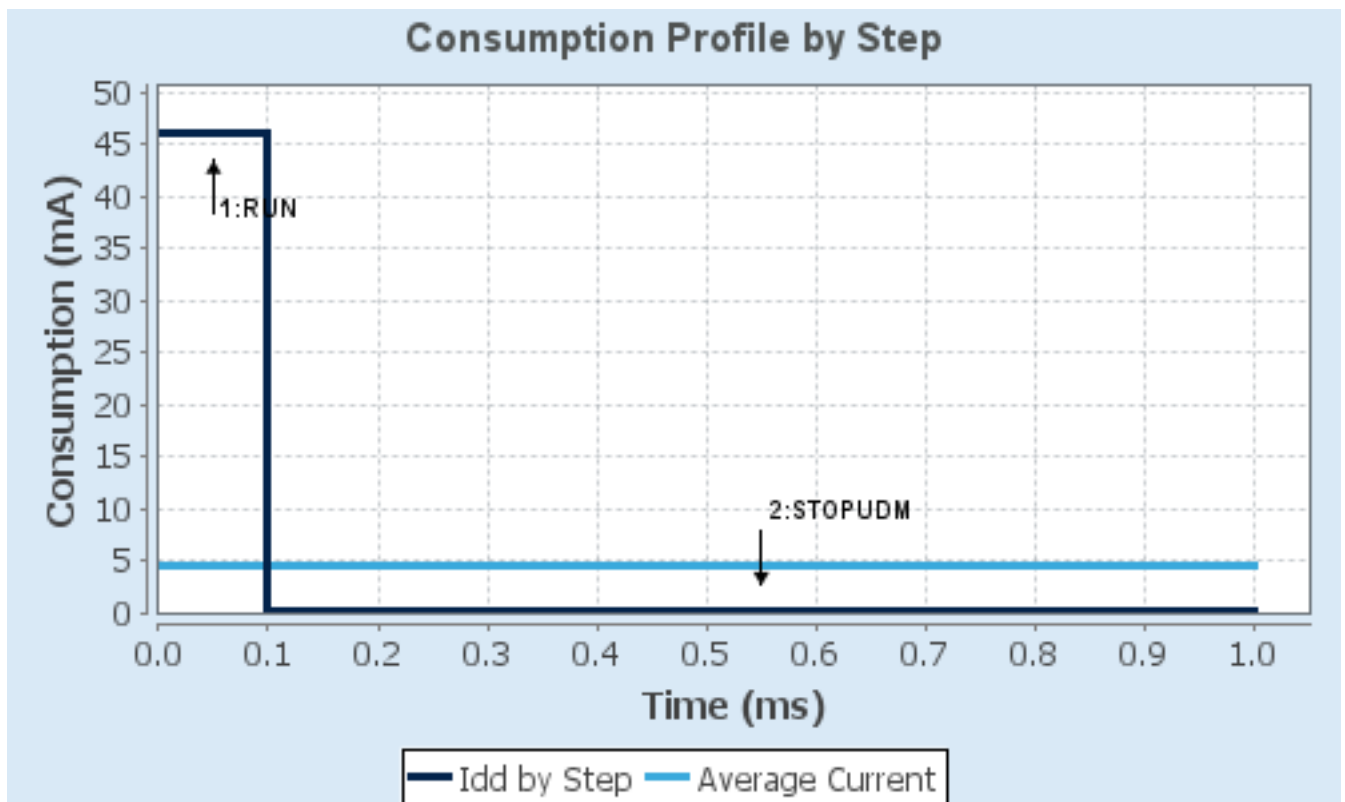
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/P REFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 μ A
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	98.02	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN3

mode: IN11

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode

Triple combined regular simultaneous + injected simultaneous mode *

DMA Access Mode

DMA access mode 1

Delay between 2 sampling phases

5 Cycles

ADC_Settings:

Clock Prescaler

PCLK2 divided by 4

Resolution

12 bits (15 ADC Clock cycles)

Data Alignment

Right alignment

Scan Conversion Mode

Enabled

Continuous Conversion Mode

Disabled

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

Enabled *

End Of Conversion Selection

EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion

2 *

External Trigger Conversion Source

Timer 8 Trigger Out event *

External Trigger Conversion Edge

Trigger detection on the rising edge

Rank

1

Channel

Channel 11 *

Sampling Time

3 Cycles

Rank

2 *

Channel

Channel 3

Sampling Time

3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions

0

WatchDog:

Enable Analog WatchDog Mode

false

7.2. ADC2

mode: IN15

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Triple combined regular simultaneous + injected simultaneous mode *
DMA Access Mode	DMA access mode 1
Delay between 2 sampling phases	5 Cycles

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Enabled *
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	2 *
<u>Rank</u>	1
Channel	Channel 15
Sampling Time	3 Cycles
<u>Rank</u>	2 *
Channel	Channel 15
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0
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WatchDog:

Enable Analog WatchDog Mode	false
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7.3. ADC3

mode: IN1

7.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment

Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Enabled *
End Of Conversion Selection	EOC flag at the end of single channel conversion
ADC_Regular_ConversionMode:	
Number Of Conversion	2 *
<u>Rank</u>	1
Channel	Channel 1
Sampling Time	3 Cycles
<u>Rank</u>	2 *
Channel	Channel 1
Sampling Time	3 Cycles
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

7.4. RCC

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

7.5. SYS

Timebase Source: SysTick

7.6. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

Channel3: PWM Generation CH3 CH3N

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	3000 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Enable *
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	80 *

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	Low *
CH Idle State	Reset
CHN Idle State	Set *

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	Low *
CH Idle State	Reset
CHN Idle State	Set *

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	Low *
CH Idle State	Reset
CHN Idle State	Set *

7.7. TIM2

Clock Source : Internal Clock

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.8. TIM6

mode: Activated

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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7.9. TIM8

Clock Source : Internal Clock

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	12000 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Update Event *

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	ADC1 Throttle
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	ADC1 Battery Voltage
ADC2	PC5	ADC2_IN15	Analog mode	No pull-up and no pull-down	n/a	ADC2 System Current
ADC3	PA1	ADC3_IN1	Analog mode	No pull-up and no pull-down	n/a	ADC3 MDC Voltage
TIM1	PA7	TIM1_CH1N	Alternate Function Push Pull	Pull-down *	Low	
	PB0	TIM1_CH2N	Alternate Function Push Pull	Pull-down *	Low	
	PB1	TIM1_CH3N	Alternate Function Push Pull	Pull-down *	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	Pull-down *	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	Pull-down *	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	Pull-down *	Low	
GPIO	PB12	GPIO_Input	Input mode	Pull-down *	n/a	Brake Input
	PC10	GPIO_Input	Input mode	Pull-down *	n/a	H1 GPIO
	PC11	GPIO_Input	Input mode	Pull-down *	n/a	H2 GPIO
	PC12	GPIO_Input	Input mode	Pull-down *	n/a	H3 GPIO
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Auto Pilot Switch

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	High *
ADC3	DMA2_Stream1	Peripheral To Memory	High *
ADC2	DMA2_Stream2	Peripheral To Memory	High *

ADC1: DMA2_Stream0 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

ADC3: DMA2_Stream1 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

ADC2: DMA2_Stream2 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
ADC1, ADC2 and ADC3 interrupts	true	0	0
TIM8 update interrupt and TIM13 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream1 global interrupt	true	0	0
DMA2 stream2 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM6 global interrupt and DAC1, DAC2 underrun error interrupts	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
ADC1, ADC2 and ADC3 interrupts	false	true	true
TIM8 update interrupt and TIM13 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream1 global interrupt	false	true	true
DMA2 stream2 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware

System Core

Analog

Timers

Connectivity

Multimedia

Computing

DMA 

ADC1 

TIM1 

GPIO 

ADC2 

TIM2 

IIVIC 

ADC3 

TIM6 

RCC 

TIM8 

SYS 

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00141306.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00135183.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00155929.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note http://www.st.com/resource/en/application_note/DM00161778.pdf

Application note http://www.st.com/resource/en/application_note/DM00213525.pdf

Application note http://www.st.com/resource/en/application_note/DM00220769.pdf

Application note http://www.st.com/resource/en/application_note/DM00227538.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note http://www.st.com/resource/en/application_note/DM00281138.pdf

Application note http://www.st.com/resource/en/application_note/DM00296349.pdf

Application note http://www.st.com/resource/en/application_note/DM00327191.pdf

Application note http://www.st.com/resource/en/application_note/DM00354244.pdf

Application note http://www.st.com/resource/en/application_note/DM00373474.pdf

Application note http://www.st.com/resource/en/application_note/DM00315319.pdf

Application note http://www.st.com/resource/en/application_note/DM00380469.pdf

Application note http://www.st.com/resource/en/application_note/DM00395696.pdf

Application note http://www.st.com/resource/en/application_note/DM00431633.pdf

Application note http://www.st.com/resource/en/application_note/DM00493651.pdf

Application note http://www.st.com/resource/en/application_note/DM00536349.pdf

Application note http://www.st.com/resource/en/application_note/DM00725181.pdf