TimerBlox: Monostable Pulse Generator (One Shot)

FEATURES

- **Pulse Width Range: 1µs to 33.6 Seconds**
- Configured with 1 to 3 Resistors
- Pulse Width Max Error:
  - <2.3% for Pulse Width > 512µs
  - <3.4% for Pulse Width of 8µs to 512µs
  - <4.9% for Pulse Width of 1µs to 8µs
- Four LTC6993 Options Available:
  - Rising-Edge or Falling-Edge Trigger
  - Retriggerable or Non-Retriggerable
- Configurable for Positive or Negative Output Pulse
- Fast Recovery Time
- 2.25V to 5.5V Single Supply Operation
- 70µA Supply Current at 10µs Pulse Width
- 500µs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –55°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Watchdog Timer
- Frequency Discriminators
- Missing Pulse Detection
- Envelope Detection
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

DESCRIPTION

The LTC®6993 is a monostable multivibrator (also known as a "one-shot" pulse generator) with a programmable pulse width of 1µs to 33.6 seconds. The LTC6993 is part of the TimerBlox® family of versatile silicon timing devices.

A single resistor, R_{SET}, programs an internal master oscillator frequency, setting the LTC6993's time base. The output pulse width is determined by this master oscillator and an internal clock divider, N_{DIV}, programmable to eight settings from 1 to 2^{21}.

$$t_{OUT} = \frac{N_{DIV} \bullet R_{SET}}{50k\Omega} \bullet 1\mu s,\ N_{DIV} = 1, 8, 64, ..., 2^{21}$$

The output pulse is initiated by a transition on the trigger input (TRIG). Each part can be configured to generate positive or negative output pulses. The LTC6993 is available in four versions to provide different trigger signal polarity and retrigger capability.

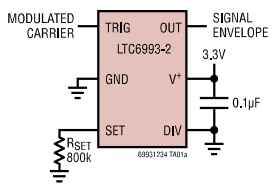
DEVICE	INPUT POLARITY	RETRIGGER
LTC6993-1	Rising-Edge	No
LTC6993-2	Rising-Edge	Yes
LTC6993-3	Falling-Edge	No
LTC6993-4	Falling-Edge	Yes

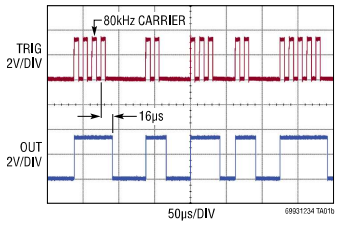
The LTC6993 also offers the ability to dynamically adjust the width of the output pulse via a separate control voltage.

For easy configuration of the LTC6993, use the TimerBlox LTC6993: One Shot Web-Based Design Tool.

TYPICAL APPLICATION

Envelope Detector





PIN FUNCTIONS (DCB/S6)

V+ (Pin 1/Pin 5): Supply Voltage (2.25V to 5.5V). This supply should be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1µF capacitor.

DIV (Pin 2/Pin 4): Programmable Divider and Polarity Input. The DIV pin voltage (V_{DIV}) is internally converted into a 4-bit result (DIVCODE). V_{DIV} may be generated by a resistor divider between V+ and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that V_{DIV} settles quickly. The MSB of DIVCODE (POL) determines the polarity of the OUT pins. When POL = 0 the output produces a positive pulse. When POL = 1 the output produces a negative pulse.

SET (Pin 3/Pin 3): Pulse Width Setting Input. The voltage on the SET pin (V_{SET}) is regulated to 1V above GND. The amount of current sourced from the SET pin (I_{SET}) programs the master oscillator frequency. The I_{SET} current range is 1.25µA to 20µA. The output pulse will continue indefinitely if I_{SET} drops below approximately 500nA, and will terminate when I_{SET} increases again. A resistor connected between SET and GND is the most accurate way to set the pulse width. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

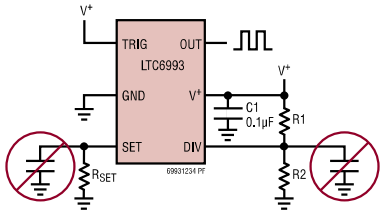
Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the V_{SET} voltage.

TRIG (Pin 4/Pin 1): Trigger Input. Depending on the version, a rising or falling edge on TRIG will initiate the output pulse. LTC6993-1 and LTC6993-2 are rising-edge sensitive. LTC6993-3 and LTC6993-4 are falling-edge sensitive.

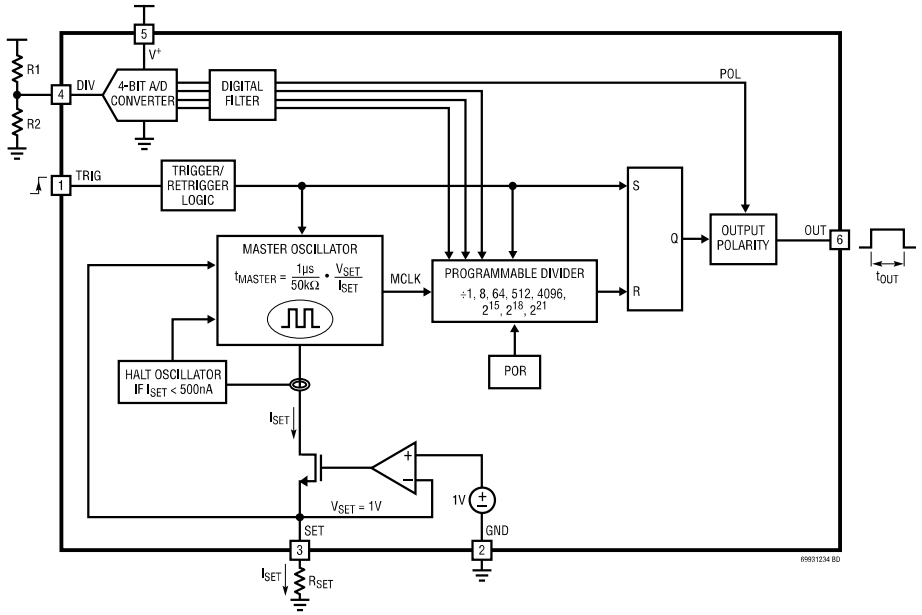
The LTC6993-2 and LTC6993-4 are retriggerable, allowing the pulse width to be extended by additional trigger signals that occur while the output is active. The LTC6993-1/LTC6993-3 will ignore additional trigger inputs until the output pulse has terminated.

GND (Pin 5/Pin 2): Ground. Tie to a low inductance ground plane for best performance.

OUT (Pin 6/Pin 6): Output. The OUT pin swings from GND to V+ with an output resistance of approximately 30Ω. When driving an LED or other low impedance load a series output resistor should be used to limit source/sink current to 20mA.



BLOCK DIAGRAM (S6 package pin numbers shown)



OPERATION

Table 1. DIVCODE Programming

DIVCODE	POL	N_{DIV}	Recommended t_{OUT}	R1 (k)	R2 (k)	V_{DIV}/V^+
0	0	1	1µs to 16µs	Open	Short	≤ 0.03125 ±0.015
1	0	8	8µs to 128µs	976	102	0.09375 ±0.015
2	0	64	64µs to 1.024ms	976	182	0.15625 ±0.015
3	0	512	512µs to 8.192ms	1000	280	0.21875 ±0.015
4	0	4,096	4.096ms to 65.54ms	1000	392	0.28125 ±0.015
5	0	32,768	32.77ms to 524.3ms	1000	523	0.34375 ±0.015
6	0	262,144	262.1ms to 4.194sec	1000	681	0.40625 ±0.015
7	0	2,097,152	2.097sec to 33.55sec	1000	887	0.46875 ±0.015
8	1	2,097,152	2.097sec to 33.55sec	887	1000	0.53125 ±0.015
9	1	262,144	262.1ms to 4.194sec	681	1000	0.59375 ±0.015
10	1	32,768	32.77ms to 524.3ms	523	1000	0.65625 ±0.015
11	1	4,096	4.096ms to 65.54ms	392	1000	0.71875 ±0.015
12	1	512	512µs to 8.192ms	280	1000	0.78125 ±0.015
13	1	64	64µs to 1.024ms	182	976	0.84375 ±0.015
14	1	8	8µs to 128µs	102	976	0.90625 ±0.015
15	1	1	1µs to 16µs	Short	Open	≥ 0.96875 ±0.015

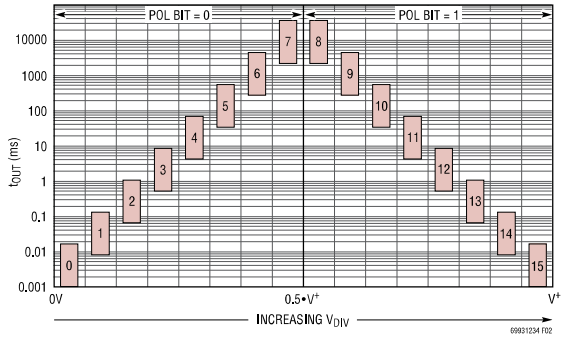


Figure 2. Pulse Width Range and POL Bit vs DIVCODE