TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS280C

November 1997 - Revised July 2003

CD54HC4514, CD74HC4514, CD74HC4515

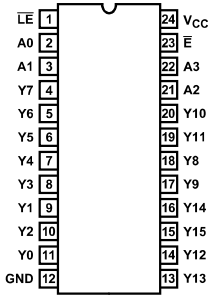
High-Speed CMOS Logic 4- to 16-Line Decoder/Demultiplexer with Input Latches

Features

- **Multifunction Capability**
  - **Binary to 1-of-16 Decoder**
  - **1-to-16 Line Demultiplexer**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

Pinout

CD54HC4514
(CERDIP)
CD74HC4514, CD74HC4515
(PDIP, SOIC)
TOP VIEW



Description

The CD54HC4514, CD74HC4514, and CD74HC4515 are high-speed silicon gate devices consisting of a 4-bit strobed latch and a 4- to 16-line decoder. The selected output is enabled by a low on the enable input ($\overline{E}$). A high on $\overline{E}$ inhibits selection of any output. Demultiplexing is accomplished by using the $\overline{E}$ input as the data input and the select inputs (A0-A3) as addresses. This $\overline{E}$ input also serves as a chip select when these devices are cascaded.

When Latch Enable ($\overline{LE}$) is high the output follows changes in the inputs (see truth table). When $\overline{LE}$ is low the output is isolated from changes in the input and remains at the level (high for the 4514, low for the 4515) it had before the latches were enabled. These devices, enhanced versions of the equivalent CMOS types, can drive 10 LSTTL loads.

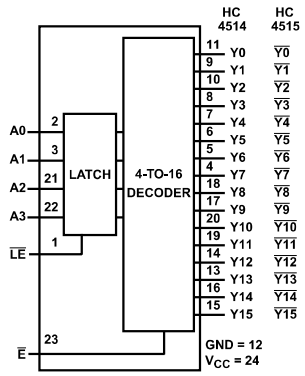
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4514F3A	-55 to 125	24 Ld CERDIP
CD74HC4514E	-55 to 125	24 Ld PDIP
CD74HC4514EN	-55 to 125	24 Ld PDIP
CD74HC4514M	-55 to 125	24 Ld SOIC
CD74HC4514M96	-55 to 125	24 Ld SOIC
CD74HC4515E	-55 to 125	24 Ld PDIP
CD74HC4515EN	-55 to 125	24 Ld PDIP
CD74HC4515M	-55 to 125	24 Ld SOIC
CD74HC4515M96	-55 to 125	24 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



DECODE TRUTH TABLE ($\overline{LE}$ = 1)

ENABLE	DECODER INPUTS A3	A2	A1	A0	ADDRESSED OUTPUT 4514 = LOGIC 1 (HIGH) 4515 = LOGIC 0 (HIGH)
0	0	0	0	0	Y0
0	0	0	0	1	Y1
0	0	0	1	0	Y2
0	0	0	1	1	Y3
0	0	1	0	0	Y4
0	0	1	0	1	Y5
0	0	1	1	0	Y6
0	0	1	1	1	Y7
0	1	0	0	0	Y8
0	1	0	0	1	Y9
0	1	0	1	0	Y10
0	1	0	1	1	Y11
0	1	1	0	0	Y12
0	1	1	0	1	Y13
0	1	1	1	0	Y14
0	1	1	1	1	Y15
1	X	X	X	X	All Outputs = 0, 4514 All Outputs = 1, 4515

X = Don't Care; Logic 1 = High; Logic 0 = Low