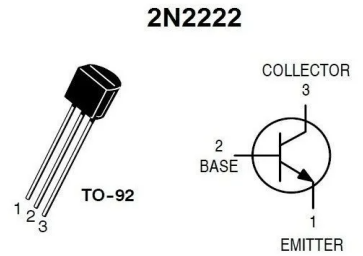
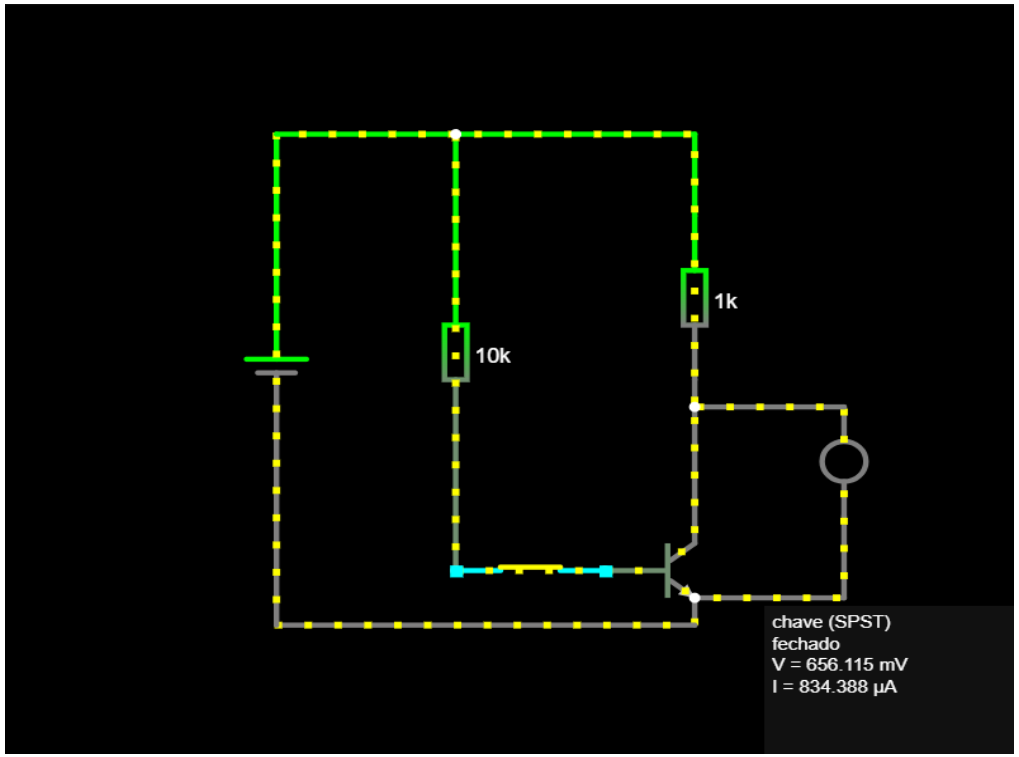
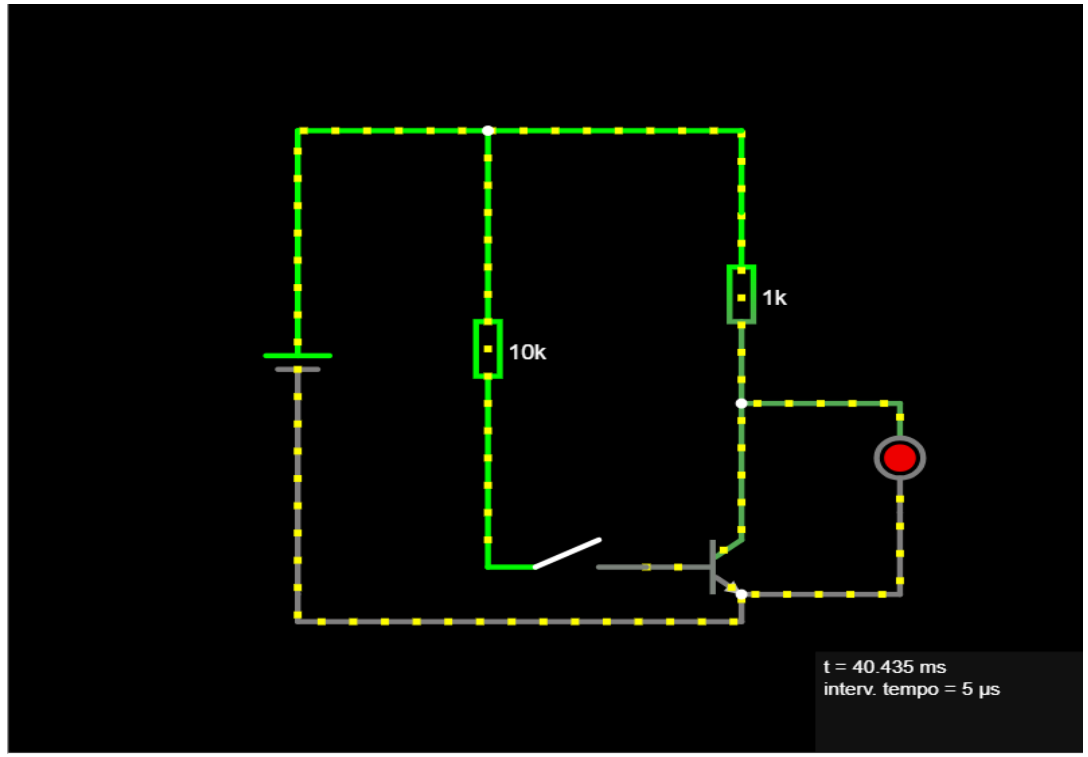
Circuito Logico NOT







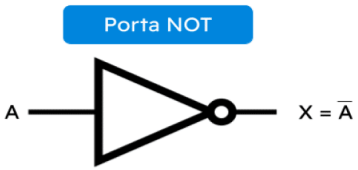


Tabela da Verdade	
A	X
0	1
1	0

Schematic	Circuito Logico NOT	Create at	2025-03-28
		Update at	2025-03-28
		Page	P1
Drawn	Diogo Otero	UFCD 6024	
Reviewed	Diogo Otero		
		Version	Size
EasyEDA		V1.0	
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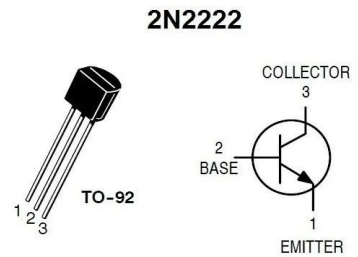
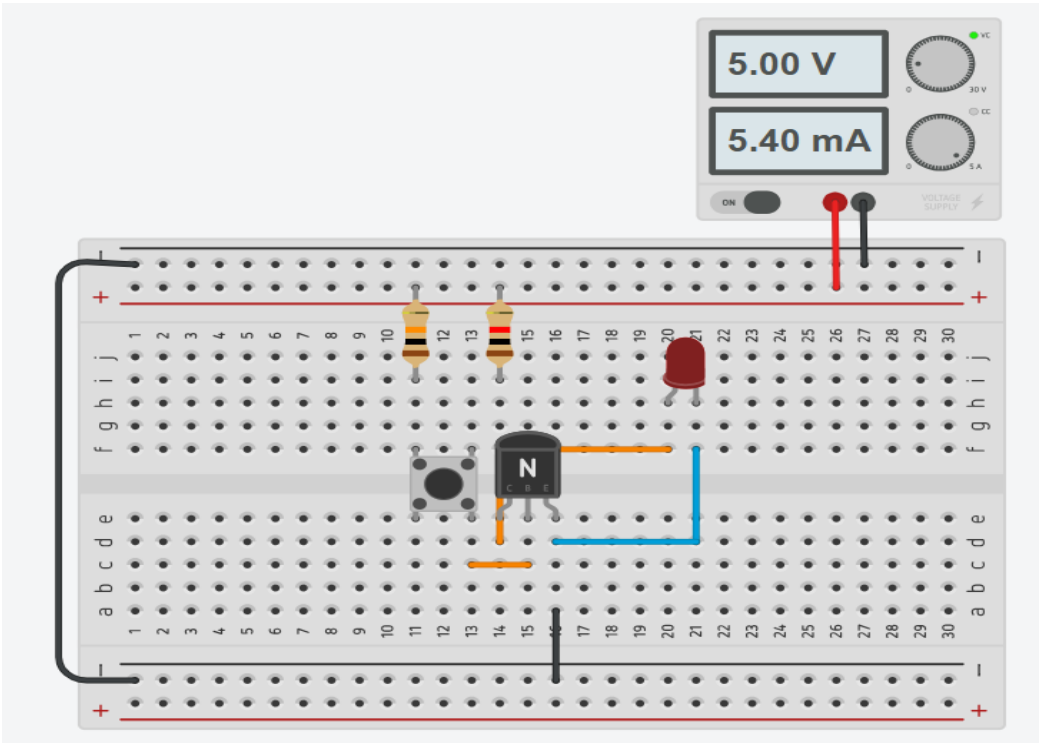
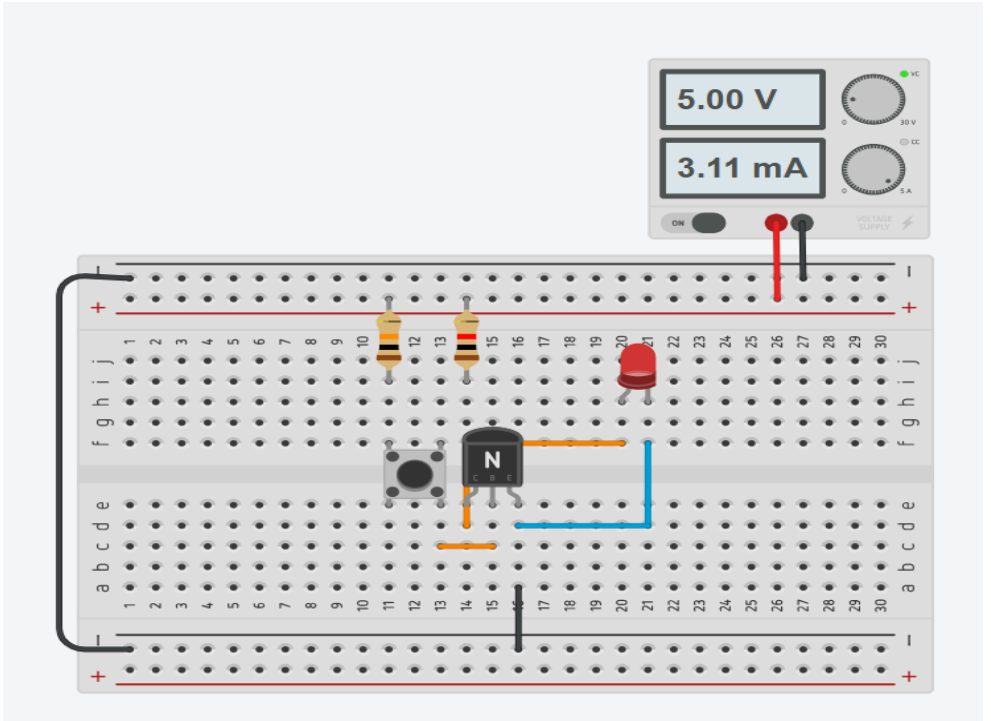
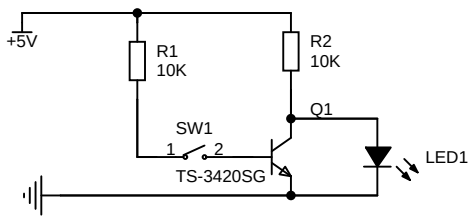
Circuito Logico NOT



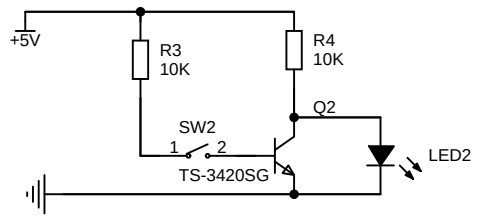


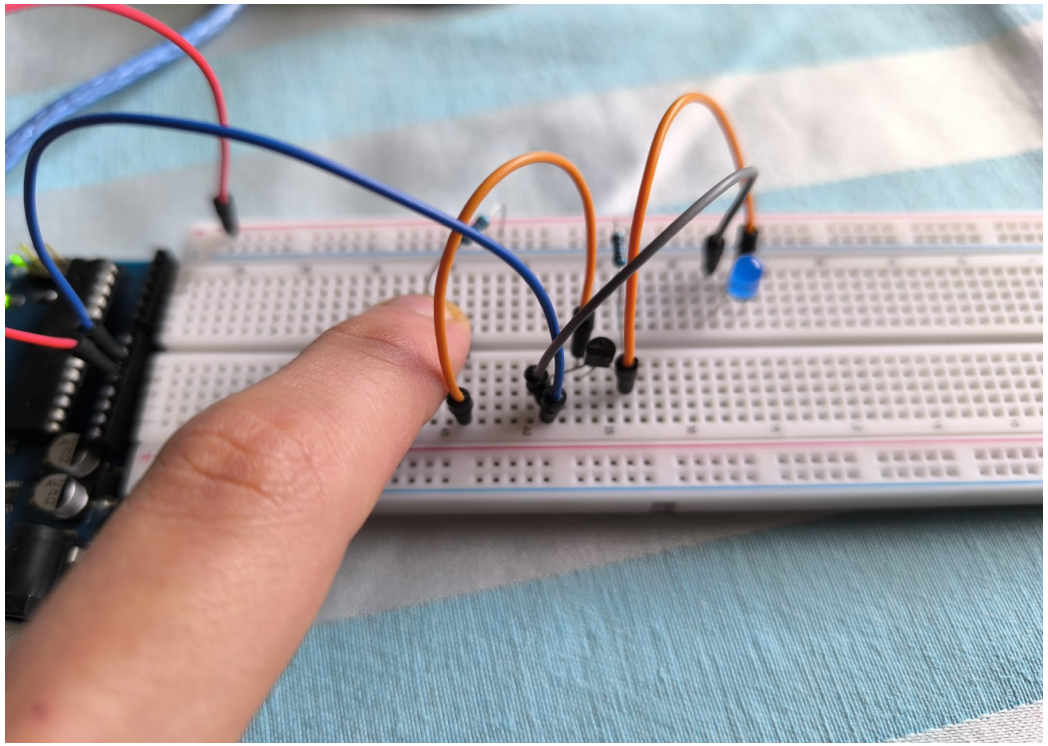


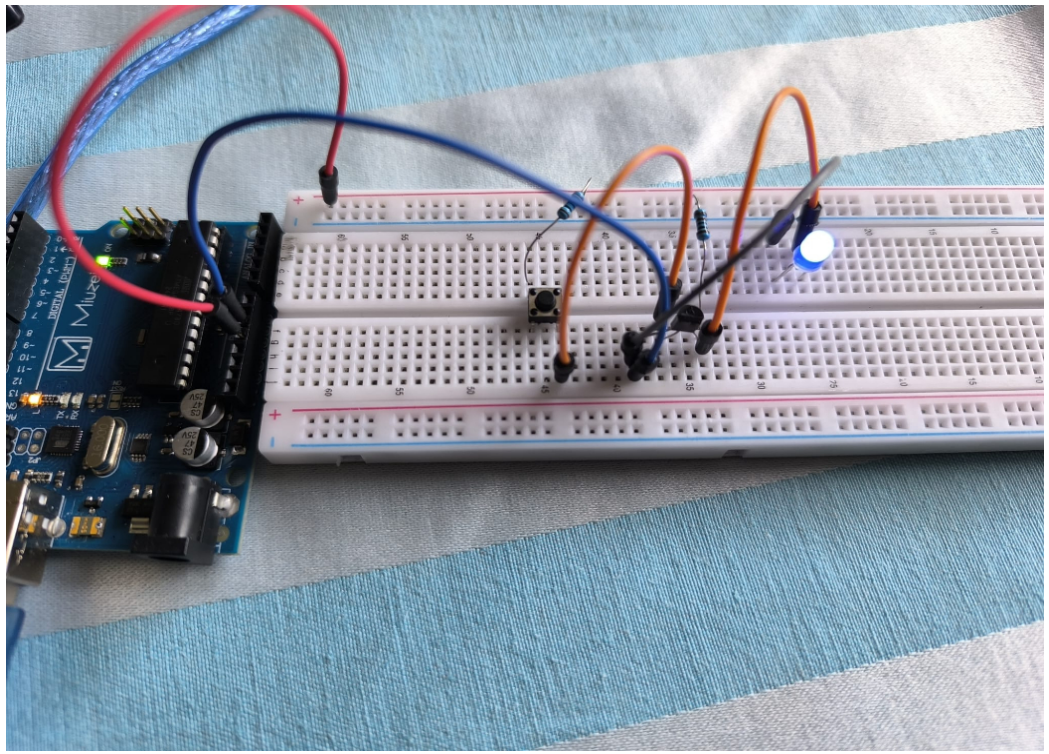


Schematic	Circuito Logico NOT	Create at	2025-03-28
		Update at	2025-03-28
		Page	P2
Drawn	Diogo Otero	UFCD 6024	
Reviewed	Diogo Otero		
		Version	Size
EasyEDA		V1.0	

Circuito Logico NOT







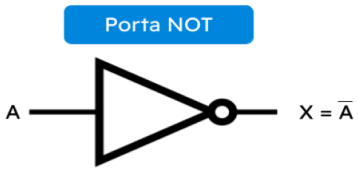


Tabela da Verdade	
A	X
0	1
1	0

Schematic	Circuito Logico NOT	Create at	2025-03-28
		Update at	2025-03-28
		Page	P3
Drawn	Diogo Otero	UFCD 6024	
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