More Efficient Design

- ☐ Use already available arithmetic circuit and incorporate logical operations
- ☐ Procedure
 - > Design the arithmetic section independently
 - \triangleright Take the circuit, consider $C_{in} = 0$, and determine which logic operations are automatically generated from the arithmetic circuit
 - ➤ Modify the circuit to incorporate required but not automatically generated logic operations



More Efficient Design

☐ Use already available arithmetic circuit and incorporate logical operations

51	s ₀	Yi
0	0	0
0	1	B_i
1	0	B;
1	1	1

	8		
51	50	Xi	Y_i
0	0	Ai	0
0	1	A,	B
1	0	A,	B_i
1	1	A,	1

OR XOR AND NOT



More Efficient Design

☐ Use already available arithmetic circuit and incorporate logical operations

51	s ₀	Yi
0	0	0
0	1	B_i
1	0	B;
1	1	1

$$62 = 0 \rightarrow \text{arithmetic}$$

$$62 = 1 \rightarrow \text{logical}$$

<i>s</i> ₂	51	<i>s</i> ₀	Xi	Y,	Ci	$F_i = X_i \oplus Y_i$	Operation	Required operation
1	0	0	A,	0	0	$F_i = A_i$	Transfer A	OR
1	0	1	A,	B_i	0	$F_i = A_i$ $F_i = A_i \oplus B_i$	XOR	XOR
1	1	0	A,	B;	0	$F_i = A_i \odot B_i$	Equivalence (X-Nor	AND
i	1	1	Ai	1	0	$F_i = A_i'$	NOT	NOT

fppt.com

Incorporating remaining functions

☐ Unresolved cases

s_2	s_1	s_0	X_i	Y_i	Automatically Obtained F_i	Required F_i
1	0	0	A_i	0	$F_i = A_i$	$F_i = A_i + B_i$
1	1	0	A_i	B_i'	$F_i = A_i \odot B_i$	$F_i = A_i B_i$
	-	-	À			

Auz control bit पत जुना i/p हे A+B मिला

$$(A+B) \oplus O = A+B$$

$$A_{Bi}$$
 A_{Bi}
 A

fppt.com

$K \overline{U} \overline{U} \overline{B} \overline{Z} \overline{J} \longrightarrow \overline{A} \overline{B} \overline{B} + AB + B \overline{B} = AB$

	s_2	s_1	s_0	X_i	Y_i	Automatically Obtained F_i	Required F_i
$\mathbb{B} \longrightarrow$	1	0	0	$\tilde{A_i}$	0	$F_i = A_i$	$F_i = A_i + B_i$
B	1	1	0	A_i	B_i'	$F_i = A_i \odot B_i$	$F_i = A_i B_i$

$$X = A + S_2 \overline{S_1} \overline{S_0} B + S_2 S_1 \overline{S_0} \overline{B}$$

Incorporating remaining functions

From Table 9-3, we see that when $s_2 = 1$, the input carry C_i in each stage must be 0. With $s_1 s_0 = 00$, each stage as it stands generates the function $F_i = A_i$. To change the output to an OR operation, we must change the input to each full-adder circuit from A_i , to $A_i + B_i$. This can be accomplished by ORing B_i and A_i when $s_2 s_1 s_0 = 100$.

The other selection variables that give an undesirable output occur when $s_2 s_1 s_0 = 110$. The unit as it stands generates an output $F_i = A_i \odot B_i$ but we want to generate the AND operation F_i = $A_i B_i$. Let us investigate the possibility of ORing each input A_i with some Boolean function K_i . The function so obtained is then used for X_i when $s_2 s_1 s_0 = 110$:

$$F_{i} = X_{i} \oplus Y_{i} = (A_{i} \oplus K_{i}) \oplus B'_{i} = A_{i}B_{i} + K_{i}B_{i} + A'_{i}K'_{i}B'_{i}$$
(A + K)
Careful inspection of the result reveals that if the variable $K_{i} = B'_{i}$, we obtain an output:

$$F_{i} = A_{i}B_{i} + B'_{i}B_{i} + A_{i}B_{i}B'_{i} = A_{i}B_{i}$$

Two terms are equal to 0 because $B_i B'_i = 0$. The result obtained is the AND operation as required. The conclusion is that, if A_i is ORed with B'_i when $s_2s_1s_0 = 110$, the output will generate the AND operation.

Final Boolean Functions

☐ Combining the arithmetic and logical cases, we get the final form of the Boolean function as:

$$X_{i} = A_{i} + s_{2}s_{1}'s_{0}'B_{i} + s_{2}s_{1}s_{0}'B_{i}'$$

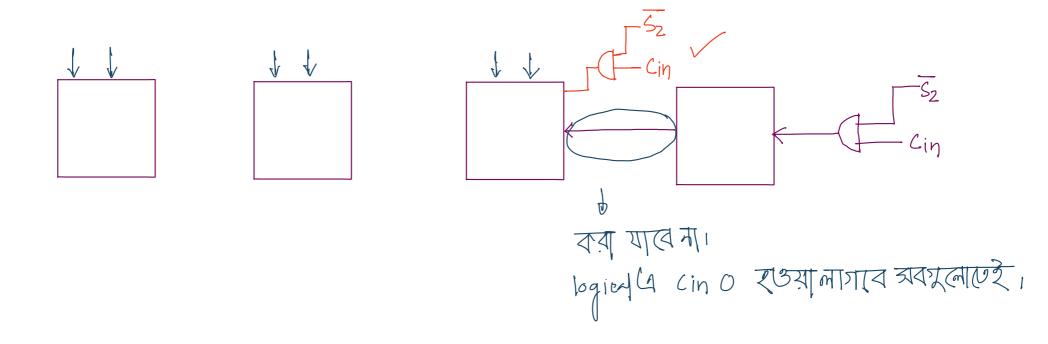
$$Y_{(i)} = s_0 B_i + s_1 B_i'$$

$$Z_i = \underline{\underline{s}_2'} C_i$$

पि logical operation पर राह्य यान रें ० र्ट्स

यणि hit पत जाता

Selection					
s ₂	<i>s</i> ₁	50	Cin	Output	Function
0	0	0	0	F = A	Transfer A
0	0	0	1	F = A + 1	Increment A
0	0	1	0	F = A + B	Addition
0	0	1	1	F = A + B + 1	Add with carry
0	i	0	0	F = A - B - 1	Subtract with borrow
Õ	1	0	1	F = A - B	Subtraction
0	1	ī	0	F = A - 1	Decrement A
0	ī	1	1	F = A	Transfer A
1	0	0	X	$F = A \vee B$	OR
1	Ō	1	X	$F = A \oplus B$	XOR
1	1	0	X	$F = A \wedge B$	AND
1	1	1	X	$F = \overline{A}$	Complement A



CT Q

Let's See Another Example

Derive the input equations (Xi, Yi and Zi) for the parallel adders to be used in the ALU which satisfies the following functional design specification.

s ₂	s ₁	c _{in}	Required Functions
0	0	0	F = AB + C
0	0	1	F = AB + C + 1
0	1	0	F = AB
0	1	1	F = AB + 1
1	0	X	F = (AB)'
1	1	X	F = AB



AB

AB

AB

AB

AB

arithmetic
$$X = AB$$

 $Y = \overline{5_1} C$
 $Z = Cin \overline{5_2}$

Required Function

C O AB+C

AB+C+1

AB+C+1

AB+C+1

AB+C+1

AB+1

$$F = (AB)'$$
 $F = AB$

SI=0 (O Y= C parithmetical si=1 (O Y=0) O (O AB)

AB+C+1

A

5251 add करत मिलारे राष्ट्र,

Finally
$$X = AB$$

$$Y = \overline{S_1} C + S_2 \overline{S_1}$$

$$Z = \overline{S_2} Cin$$

Solution

S ₂	S ₁	C _{in}	X	Y	Z	Required Functions
0	0	0	AB	С	0	F= AB + C
0	0	1	AB	С	1	F = AB + C +1
0	1	0	AB	0	0	F = AB
0	1	1	AB	0	1	F = AB + 1
1	0	X	AB	1	X	F = (AB)'
1	1	X	AB	0	X	F = AB



Solution

$$\square X = AB$$

$$\square$$
 Y = s_1 ' C

$$\square$$
 Z = s_2 , c_{in}

☐ Then for logical operations,

$$> X = AB$$

$$Y = S_1' C + S_2 S_1'$$

$$\geq$$
 Z = s_2 , c_{in}

