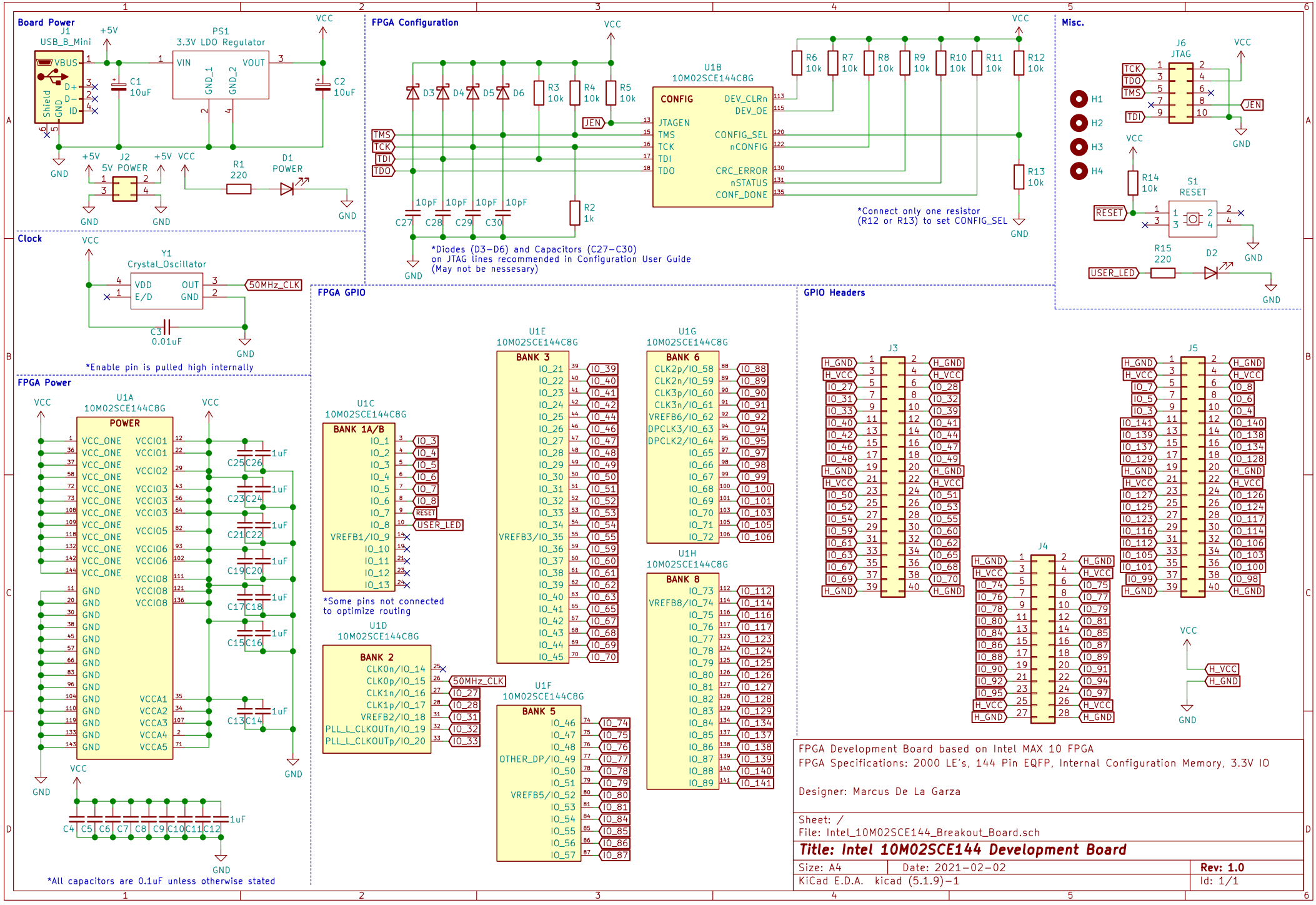
Board Power
J1
USB_B_Mini
VBUS
D+
D−
ID
Shield
GND
+5V
C1
10uF
PS1
3.3V LDO Regulator
VIN
VOUT
GND_1
GND_2
VCC
C2
10uF
J2
5V POWER
R1
220
D1
POWER
FPGA Configuration
D3
D4
D5
D6
R3
10k
R4
10k
R5
10k
JEN
TMS
TCK
TDI
TDO
10pF
C27
C28
C29
C30
R2
1k
U1B
10M02SCE144C8G
CONFIG
JTAGEN
DEV_CLRn
DEV_OE
CONFIG_SEL
nCONFIG
CRC_ERROR
nSTATUS
CONF_DONE
R6
10k
R7
10k
R8
10k
R9
10k
R10
10k
R11
10k
R12
10k
R13
10k
*Connect only one resistor
(R12 or R13) to set CONFIG_SEL
*Diodes (D3–D6) and Capacitors (C27–C30)
on JTAG lines recommended in Configuration User Guide
(May not be nessesary)
Misc.
J6
JTAG
H1
H2
H3
H4
R14
10k
S1
RESET
R15
220
D2
USER_LED
Clock
Y1
Crystal_Oscillator
VDD
E/D
OUT
GND
50MHz_CLK
C3
0.01uF
*Enable pin is pulled high internally
FPGA Power
U1A
10M02SCE144C8G
POWER
VCC_ONE
VCCIO1
VCCIO2
VCCIO3
VCCIO5
VCCIO6
VCCIO8
GND
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
C25
C26
C23
C24
C21
C22
C19
C20
C17
C18
C15
C16
C13
C14
1uF
C4
C5
C6
C7
C8
C9
C10
C11
C12
*All capacitors are 0.1uF unless otherwise stated
FPGA GPIO
U1C
10M02SCE144C8G
BANK 1A/B
IO_1
IO_2
IO_3
IO_4
IO_5
IO_6
IO_7
IO_8
VREFB1/IO_9
IO_10
IO_11
IO_12
IO_13
RESET
USER_LED
*Some pins not connected
to optimize routing
U1D
10M02SCE144C8G
BANK 2
CLK0n/IO_14
CLK0p/IO_15
CLK1n/IO_16
CLK1p/IO_17
VREFB2/IO_18
PLL_L_CLKOUTn/IO_19
PLL_L_CLKOUTp/IO_20
50MHz_CLK
U1E
10M02SCE144C8G
BANK 3
VREFB3/IO_35
U1F
10M02SCE144C8G
BANK 5
OTHER_DP/IO_49
VREFB5/IO_52
U1G
10M02SCE144C8G
BANK 6
CLK2p/IO_58
CLK2n/IO_59
CLK3p/IO_60
CLK3n/IO_61
VREFB6/IO_62
DPCLK3/IO_63
DPCLK2/IO_64
U1H
10M02SCE144C8G
BANK 8
VREFB8/IO_74
GPIO Headers
J3
J4
J5
H_GND
H_VCC
FPGA Development Board based on Intel MAX 10 FPGA
FPGA Specifications: 2000 LE's, 144 Pin EQFP, Internal Configuration Memory, 3.3V IO
Designer: Marcus De La Garza
Sheet: /
File: Intel_10M02SCE144_Breakout_Board.sch
Title: Intel 10M02SCE144 Development Board
Size: A4
Date: 2021-02-02
Rev: 1.0
KiCad E.D.A. kicad (5.1.9)-1
Id: 1/1