Design of DC–AC Converters

A Comprehensive Study

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Abstract

This document presents a comprehensive study on the design and analysis of DC–AC converters, commonly known as inverters, which are essential components in modern power electronic systems. The work systematically explores the fundamental operating principles, including voltage and current relationships, switching mechanisms, and modulation techniques. A detailed examination of various inverter topologies is provided, covering single-phase and three-phase configurations, full-bridge and half-bridge designs, as well as advanced multilevel structures such as the Cascaded H-Bridge inverters.

Each topology is analyzed in terms of performance metrics, including output voltage quality, Total Harmonic Distortion (THD), efficiency, and power handling capabilities. The document also addresses modulation strategies such as Pulse Width Modulation (PWM), Sinusoidal PWM (SPWM), and Space Vector PWM (SVPWM), highlighting their influence on output waveform quality and harmonic content. Furthermore, practical considerations for converter implementation are discussed, including conduction and switching losses, filter design, gate drive requirements, and overall system efficiency.

The study integrates theoretical foundations with numerical examples and design cheat sheets, providing a practical framework for engineers and researchers to select, analyze, and implement DC–AC converters across a wide range of applications such as renewable energy systems, uninterruptible power supplies (UPS), motor drives, and grid-connected systems. This document aims to serve both as an academic reference and a practical guide, bridging the gap between theory and real-world inverter design.

Contents

1 Overview

1.1 What is a DC/AC Converter (Inverter)?

A DC/AC converter, commonly known as an **inverter**, is an electronic device that converts direct current (DC) input voltage into alternating current (AC) output voltage. The primary function of the inverter is to generate an AC waveform of desired frequency and amplitude from a DC power source.

Inverters are essential components in modern power electronics systems, enabling the integration of renewable energy sources, providing reliable backup power, and facilitating variable-speed motor control. Depending on the application, they can operate as standalone units or as grid-connected systems.

1.2 Common Applications

DC/AC converters are employed in a wide range of applications, including:

- **Solar Inverters:** Convert DC power from photovoltaic (PV) panels into AC power for grid connection or local consumption.
- **Uninterruptible Power Supply (UPS) Systems:** Ensure continuous AC power to critical loads during power outages.
- **Motor Drives:** Provide variable-frequency AC power to control the speed and torque of AC motors in industrial and automotive systems.
- **Grid-Tied Systems:** Interface distributed generation units with the utility grid, maintaining synchronization and power quality.

1.3 Key Performance Metrics

The performance of an inverter is evaluated using several key parameters:

- **Efficiency (η):** Indicates the ratio of output AC power to input DC power, representing how effectively the inverter converts energy.

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\%$$

- **Total Harmonic Distortion (THD):** Measures the distortion in the output voltage or current waveform compared to an ideal sinusoidal signal.

$$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + \dots}}{V_1} \times 100\%$$

  Lower THD indicates better waveform quality and reduced stress on connected loads.

- **Output Voltage Regulation:** Defines the inverter's ability to maintain a stable output voltage despite variations in input voltage, load conditions, or temperature.

1.4 Document Organization

This document is organized into four main parts:

- **Part I – Introduction:** Provides an overview of inverter concepts, applications, and performance parameters.

- **Part II – Inverter Topologies:** Discusses different inverter configurations, including single-phase, three-phase, and multilevel structures. Each topology includes circuit diagrams, operating principles, loss analyses, and numerical examples.
- **Part III – Conclusion:** Summarizes performance comparisons, efficiency considerations, and practical selection guidelines for various inverter types.
- **Part IV – Appendices:** Offers supplementary material on component selection, simulation setups, and key references.

2 Single-Phase Half-Bridge Inverter

2.1 Description of operation

The single-phase half-bridge inverter is one of the simplest inverter topologies. It consists of two switching devices (transistors or IGBTs/MOSFETs) connected in series across a DC bus V_{dc}. The midpoint between the two switches is connected to the load (possibly via a filter). In practical implementations the DC bus is split by two series capacitors so that the midpoint of the capacitors provides a virtual neutral; the output therefore swings approximately between $+V_{dc}/2$ and $-V_{dc}/2$.

Key operational points:

- When the upper device (S_1) is ON and the lower device (S_2) is OFF, the load sees approximately $+V_{dc}/2$.
- When S_1 is OFF and S_2 is ON, the load sees approximately $-V_{dc}/2$.
- Both switches must never be ON simultaneously (shoot-through). A small dead-time is inserted between complementary commands to avoid overlap.
- By modulating the duty (via PWM) of the switches with a sinusoidal reference, a near-sinusoidal fundamental component is synthesized at the load.

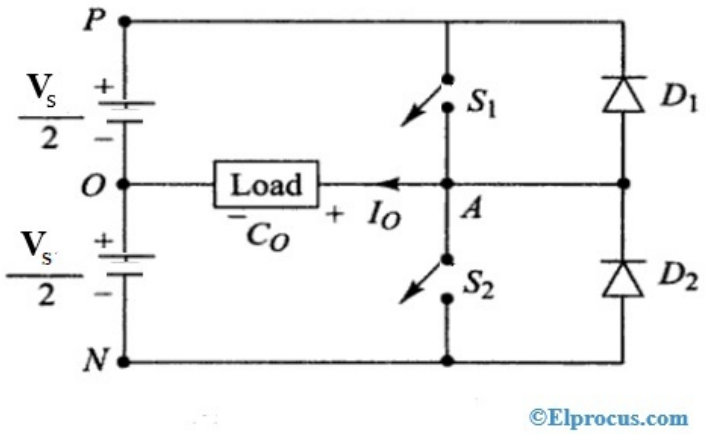

Figure 1: Single-phase half-bridge inverter (conceptual).

Schematic (example)

2.1.1 Switching sequence

A common switching scheme (complementary PWM) is:

1. **Positive half-cycle:** Upper switch S_1 PWM follows the sinusoidal reference; lower S_2 is complementary (OFF when S_1 is ON).
2. **Negative half-cycle:** S_2 PWM follows the inverted sinusoidal reference and S_1 is complementary.
3. **Dead-time:** Inserted between switching transitions to prevent simultaneous conduction.

Timing table (idealized):

Interval	S_1	S_2	
$t_0 \to t_1$	ON	OFF	$(+V_{dc}/2)$
$t_1 \to t_2$	OFF	ON	$(-V_{dc}/2)$

More advanced modulation (unipolar/bipolar, phase-shifted carriers) modifies the sequence to reduce harmonics.

2.1.2 Key waveforms (input DC, output AC, switch signals)

Describe (and include) the following typical waveforms:

- **Input DC:** Constant V_{dc} with split capacitors creating $\pm V_{dc}/2$ rails.
- **Switch gate signals:** Complementary PWM pulses with dead-time between transitions.
- **Midpoint (inverter output) waveform:** A high-frequency PWM waveform switching between $+V_{dc}/2$ and $-V_{dc}/2$. After low-pass filtering, the fundamental approximates a sinusoid.
- **Filtered output:** Near-sinusoidal $v_o(t)$ with harmonics reduced according to filter design and switching frequency.

2.1.3 Applications and power range

Typical application scenarios:

- Low-to-medium power single-phase systems: small UPS units, microinverters for PV, small motor drives, lab power supplies.
- Because the half-bridge inherently provides half the voltage excursion of a full-bridge, it is most common in lower-power equipment or where the DC bus is easily split by capacitors.

Typical practical power range (order of magnitude): from a few watts (microinverters) up to several kilowatts for well-designed, cooled modules. For higher voltages/power or to avoid the midpoint-splitting requirement, designers generally prefer full-bridge or multilevel topologies.

2.1.4 Operating equations

A. Output voltage

- **Instantaneous (ideal square-mode) peak:**

$$V_{o,\text{peak(inst)}} = \frac{V_{dc}}{2}$$

(The unloaded instantaneous output alternates between $\pm V_{dc}/2$.)

- **Fundamental (SPWM) peak:** In the linear modulation range the fundamental peak of the output is proportional to the modulation index M. For a half-bridge:

$$V_{1,\text{peak}} \;=\; M \cdot \frac{V_{dc}}{4}$$

(Reasoning: a full-bridge synthesizes a fundamental of $M \cdot V_{dc}/2$ for the same M; the half-bridge amplitude is half that value.)

- **RMS of the fundamental (useful AC output):**

$$V_{o,\text{rms}} \;=\; \frac{V_{1,\text{peak}}}{\sqrt{2}} \;=\; \frac{M\,V_{dc}}{4\sqrt{2}}$$

- **Modulation index:**

$$M \;=\; \frac{V_{\text{control}}}{V_{\text{carrier}}}$$

Typical linear range: $0 \le M \le 1$. For $M > 1$ (over-modulation) the output becomes non-linear and more distorted.

B. Output current Let the load be represented by a phasor impedance $Z = |Z|\angle\theta_Z$ and the fundamental output phasor be V_1.

- **Phasor current (fundamental):**

$$\underline{I_1} \;=\; \frac{\underline{V_1}}{Z} \quad\Rightarrow\quad I_{o,\text{rms}} \;=\; \frac{V_{o,\text{rms}}}{|Z|}$$

- **Resistive load (R):** $i(t) = v(t)/R$. For a sinusoidal fundamental

$$I_{o,\text{rms}} \;=\; \frac{V_{o,\text{rms}}}{R}, \qquad I_{o,\text{peak}} = \sqrt{2}\,I_{o,\text{rms}}$$

- **General load with phase angle φ:** the current lags/leads voltage by φ where $\varphi = \arg(Z)$.

C. Power equations

- **Active (real) output power:**

$$P_{\text{out}} \;=\; V_{o,\text{rms}} \cdot I_{o,\text{rms}} \cdot \cos(\varphi)$$

where φ is the phase angle between voltage and current (load power factor angle).

- **Apparent power:**

$$S \;=\; V_{o,\text{rms}} \cdot I_{o,\text{rms}}$$

- **Power factor:**

$$\text{PF} \;=\; \cos(\varphi) \;=\; \frac{P_{\text{out}}}{S}$$

2.2 Modulation

2.2.1 PWM principle

Pulse Width Modulation (PWM) is the most common technique used to synthesize a sinusoidal fundamental from a DC source by switching power devices at a high frequency. A sinusoidal *reference* (control) signal at the desired output frequency f_o is compared with a high-frequency *carrier* (typically a triangular or sawtooth) at switching frequency f_s. Wherever the reference is greater than the carrier the top device is commanded ON (or the corresponding topology-dependent rule is applied); otherwise the complementary device is ON. The resulting high-frequency pulse train contains a fundamental component at f_o and switching-related harmonics centered around integer multiples of f_s.

Key points:

- Linear modulation (small signal, $M \leq 1$) — the fundamental amplitude is proportional to the control amplitude.
- Overmodulation ($M > 1$) — the relation becomes non-linear and the waveform approaches a square wave as M increases, increasing distortion.
- Dead-time between complementary switches is required to prevent shoot-through; dead-time introduces distortion and low-order even/odd harmonic content.

2.2.2 Switching frequency

Denote the switching (carrier) frequency by f_s and the desired output (fundamental) frequency by f_o. Typical design considerations:

- Choose $f_s \gg f_o$ so that switching harmonics are well separated from the fundamental and can be attenuated by a filter.
- Higher f_s reduces low-order harmonic amplitude in the load band and simplifies filter design, but increases switching losses and EMI.
- Practical values: low-power converters often use several kHz to tens of kHz; higher performance (smaller filters, quieter outputs) may use tens to hundreds of kHz depending on devices and thermal limits. (Select f_s consistent with the chosen semiconductor, gate drive, and thermal budget.)

2.2.3 Modulation index

The modulation index M quantifies the amplitude of the reference signal relative to the carrier:

$$M \;=\; \frac{V_{\text{control}}}{V_{\text{carrier}}}$$

where V_{control} is the peak amplitude of the sinusoidal reference and V_{carrier} the peak amplitude of the carrier. In the linear PWM region:

$$0 \leq M \leq 1.$$

2.2.4 Output fundamental voltage vs. M

Under sinusoidal PWM in the linear region and assuming ideal filtering, the fundamental peak of the output is proportional to M. For the half-bridge topology (midpoint switching between $\pm V_{dc}/2$) the fundamental peak is:

$$V_{1,\text{peak}} \;=\; M \cdot \frac{V_{dc}}{4}$$

and the RMS value of the fundamental is

$$V_{1,\text{rms}} = \frac{V_{1,\text{peak}}}{\sqrt{2}} = \frac{M\,V_{dc}}{4\sqrt{2}}.$$

These relations assume ideal SPWM, linear modulation, and an output filter that removes switching components. Note: in a full-bridge topology the corresponding peak is twice the half-bridge value (for the same M).

2.3 E. Harmonic Content

2.3.1 THD formula

Total Harmonic Distortion (THD) of the output voltage (or current) is defined as the ratio of the RMS value of all harmonic components (all components except the fundamental) to the RMS value of the fundamental:

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \quad \text{or} \quad \text{THD\%} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100\%$$

where V_n is the RMS amplitude of the n-th harmonic and V_1 the RMS amplitude of the fundamental.

2.3.2 Dominant harmonics

For sinusoidal PWM (SPWM) the dominant harmonic energy appears:

- Around the switching frequency and its integer multiples (i.e. near kf_s, $k = 1, 2, \ldots$), often in the form of $(kf_s \pm mf_o)$ sidebands where m is a small integer.
- Low-order harmonics (near the fundamental) are relatively small in linear SPWM, but non-idealities (dead-time, unbalanced DC bus, modulation nonlinearity/overmodulation) introduce low-order components.
- For an ideal square-wave (no PWM filtering), only odd harmonics exist and the n-th odd harmonic amplitude falls approximately as $1/n$. For a square wave of peak A, the fundamental peak is $V_{1,\text{peak}} = \frac{4A}{\pi}$ and the odd harmonic amplitudes are $\frac{4A}{n\pi}$ for $n = 1, 3, 5, \ldots$.

2.3.3 Effect of switching frequency

- **Higher** f_s moves switching harmonics further away from the fundamental band, making it easier to filter them out with a smaller passive filter and reducing measured THD at the line frequency.
- **Lower** f_s places harmonic energy closer to the fundamental and may require larger filters or produce unacceptable THD for sensitive loads.
- **Trade-off:** increasing f_s reduces output harmonic distortion but increases switching losses (and possibly EMI). The optimal f_s balances efficiency, thermal limits, filter size, and EMI constraints.
- **Modulation and topology effects:** unipolar or multilevel modulation schemes and space-vector methods reduce low-order harmonic content compared with simple bipolar SPWM for the same f_s, allowing improved THD or lower f_s for the same performance.

Practical design note: evaluate THD after the output filter and under the expected load conditions; account for dead-time, dc-bus imbalance, switching device non-idealities and measurement bandwidth when reporting THD (specify whether THD is referenced to the filtered fundamental, which harmonic orders are included, and the measurement bandwidth).

2.4 Loss Analysis

2.4.1 Conduction losses

Conduction losses occur when semiconductor devices or passive elements carry current and dissipate energy due to their non-zero on-resistance or forward voltage.

Switch conduction loss For a switching device (MOSFET/IGBT) with on-resistance $R_{ds(on)}$, the RMS conduction loss is

$$P_{\text{cond,sw}} \;=\; I_{\text{rms,sw}}^2 \, R_{ds(on)} \tag{1}$$

where

$$I_{\text{rms,sw}} \;=\; \sqrt{\frac{1}{T}\int_0^T i_{\text{sw}}^2(t)\,\mathrm{d}t}$$

is the RMS current through the particular switch over one switching period T. For many practical estimates with sinusoidal load current and complementary switching, a first approximation is $I_{\text{rms,sw}} \approx I_{o,\text{rms}}$ multiplied by a duty-related factor (evaluate exactly from the known switching pattern).

Diode conduction loss (if applicable) When freewheeling diodes conduct, losses are

$$P_{\text{cond,diode}} \;=\; V_F \cdot I_{\text{avg}} \;+\; r_D \cdot I_{\text{rms}}^2 \tag{2}$$

where V_F is the diode forward voltage (approximate constant drop), r_D its dynamic resistance, I_{avg} the average diode current during conduction, and I_{rms} the diode RMS current.

Total conduction loss Sum conduction losses for all conducting elements (switches and diodes):

$$P_{\text{cond}} \;=\; \sum_{\text{switches}} P_{\text{cond,sw}} \;+\; \sum_{\text{diodes}} P_{\text{cond,diode}}. \tag{3}$$

2.4.2 B. Switching losses

Switching losses occur during finite-voltage and current transitions when semiconductors switch states.

Turn-on / turn-off energy The energy dissipated during a single turn-on and turn-off of a device are

$$E_{\text{on}} \;=\; \int_{t_{\text{on,start}}}^{t_{\text{on,end}}} v_{\text{sw}}(t)\, i_{\text{sw}}(t)\,\mathrm{d}t, \qquad E_{\text{off}} \;=\; \int_{t_{\text{off,start}}}^{t_{\text{off,end}}} v_{\text{sw}}(t)\, i_{\text{sw}}(t)\,\mathrm{d}t.$$

In practice E_{on} and E_{off} are obtained from device datasheets or measured waveforms.

Total switching loss For a switching frequency f_s and N_{switches} switching devices:

$$P_{\text{sw}} \;=\; (E_{\text{on}} + E_{\text{off}})\; f_s \; N_{\text{switches}}. \tag{4}$$

Dead-time effects Dead-time (non-overlap time between complementary switches) prevents shoot-through but causes:

- Conduction of body diodes during transitions — increases diode conduction losses.
- Distortion of the fundamental (low-order harmonics) and DC-offsets, changing RMS currents and thus conduction losses.
- A practical approach: include an extra loss term P_{dead} obtained from measured diode conduction during dead-time or by simulation.

2.4.3 Filter losses

Losses in passive filtering components (inductors and capacitors) reduce inverter efficiency and must be estimated.

Inductor losses

- **DC-resistance (DCR) loss:**

$$P_{L,\mathrm{DCR}} \;=\; I_{L,\mathrm{rms}}^2 \,\mathrm{DCR}_L \tag{5}$$

  where $I_{L,\mathrm{rms}}$ is the inductor RMS current (including ripple).

- **Core loss:** commonly modelled with a Steinmetz-type equation

$$P_{\mathrm{core}} \;=\; k\, f^{\alpha}\, B_{\mathrm{pk}}^{\beta}\, V_{\mathrm{core}} \tag{6}$$

  where k, α, β are empirical Steinmetz coefficients (from the core datasheet), f the relevant flux frequency (often switching frequency or its harmonic content), B_{pk} the peak flux density, and V_{core} the core volume.

Capacitor ESR loss Capacitor loss due to equivalent series resistance (ESR):

$$P_C \;=\; I_{C,\mathrm{rms}}^2 \,\mathrm{ESR} \tag{7}$$

where $I_{C,\mathrm{rms}}$ is the RMS ripple current through the capacitor (estimate from filter design or simulate).

Total filter loss

$$P_{\mathrm{filter}} \;=\; P_{L,\mathrm{DCR}} + P_{\mathrm{core}} + P_C. \tag{8}$$

2.4.4 Gate drive losses

Energy required to charge/discharge gate capacitances at each switching transition:

$$P_{\mathrm{gate}} \;=\; Q_g\, V_{gs}\, f_s\, N_{\mathrm{switches}} \tag{9}$$

where Q_g is the device total gate charge (from datasheet), V_{gs} the gate drive amplitude, f_s the switching frequency and N_{switches} the number of driven gates. If the gate driver returns energy to the driver or uses active recovery, effective gate-drive losses may be reduced.

2.4.5 Total efficiency

Collecting all contributions, the overall inverter efficiency is

$$\eta \;=\; \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} \;+\; P_{\mathrm{cond}} \;+\; P_{\mathrm{sw}} \;+\; P_{\mathrm{filter}} \;+\; P_{\mathrm{gate}}} \times 100\%. \tag{10}$$

Practical notes on evaluation

- Device datasheets typically provide $R_{ds(on)}$, Q_g, and either tabulated $E_{\mathrm{on}}, E_{\mathrm{off}}$ (for a given V_{dc} and I) or switching loss curves — use those values and scale carefully to your operating point.
- Accurate loss estimation usually requires either time-domain simulation (SPICE/LTspice/Synopsys) or experimental measurement because of waveform-dependent integrals and non-idealities (voltage/current overlap, dv/dt, di/dt, dead-time conduction).
- When presenting numerical results, include clear assumptions: V_{dc}, switching frequency f_s, device temperatures (since $R_{ds(on)}$ depends on temperature), and the load waveform.

2.5 Numerical example

Given specifications:

- DC bus: $V_{dc} = 400$ V
- Desired AC output (fundamental): $V_{o,\text{rms}} = 115$ V
- Output power: $P_{\text{out}} = 500$ W (assumed resistive for simplicity)
- Switching frequency: $f_s = 20$ kHz
- Semiconductor (example): $R_{ds(on)} = 40$ mΩ, $E_{on} = 1$ mJ, $E_{off} = 1$ mJ, total gate charge $Q_g = 60$ nC, $V_{gs} = 12$ V
- Filter estimates: inductor DCR $= 0.10$ Ω, core loss ≈ 0.5 W, capacitor ESR $= 0.05$ Ω, capacitor RMS ripple current ≈ 1 A

Step 1 — Compute modulation index and currents

From the half-bridge fundamental relation (linear SPWM):

$$V_{1,\text{rms}} = \frac{M\,V_{dc}}{4\sqrt{2}} \quad \Rightarrow \quad M = \frac{4\sqrt{2}\,V_{1,\text{rms}}}{V_{dc}}.$$

With the chosen numbers:

$$M = \frac{4\sqrt{2}\cdot 115}{400} = 1.626 \text{ (dimensionless)}$$

$\Rightarrow$ *This indicates over-modulation:* for linear SPWM we require $M \leq 1$. Practical remedies: increase V_{dc} (see note below) or use a full-bridge topology (which yields twice the half-bridge fundamental for the same V_{dc}).

Output current (assume resistive load: $I_{o,\text{rms}} = P_{out}/V_{o,\text{rms}}$):

$$I_{o,\text{rms}} = \frac{500}{115} = 4.3478 \text{ A}, \qquad I_{o,\text{peak}} = \sqrt{2}\,I_{o,\text{rms}} = 6.1488 \text{ A}.$$

Step 2 — Conduction losses

Approximate total switch conduction loss (both switches combined, approximate $I_{\text{rms,sw}} \approx I_{o,\text{rms}}$):

$$P_{\text{cond,sw}} = N_{\text{switches}}\, I_{o,\text{rms}}^2\, R_{ds(on)} = 2\cdot(4.3478)^2\cdot 0.04 \approx 1.51 \text{ W}.$$

Diode conduction (small during dead-time; example estimate):

$$P_{\text{cond,diode}} = V_F \cdot I_{\text{avg}} + r_D\, I_{\text{rms}}^2 \approx 0.7\cdot(0.435) + 0.02\cdot(0.8696)^2 \approx 0.32 \text{ W}.$$

Total conduction:

$$P_{\text{cond}} \approx 1.51 + 0.32 = 1.83 \text{ W}.$$

Step 3 — Switching losses

Using datasheet energies E_{on} and E_{off} (per device):

$$P_{\text{sw}} = (E_{on} + E_{off})\, f_s\, N_{\text{switches}} = (1\times 10^{-3} + 1\times 10^{-3})\cdot 20\times 10^3 \cdot 2 = 80.0 \text{ W}.$$

Step 4 — Filter losses

$$P_{L,\text{DCR}} = I_{L,\text{rms}}^2\,\text{DCR}_L = (4.3478)^2\cdot 0.10 \approx 1.89 \text{ W}.$$

Core loss (assumed from core datasheet / estimate) ≈ 0.5 W.

Capacitor ESR loss:

$$P_C = I_{C,\text{rms}}^2 \,\text{ESR} = 1.0^2 \cdot 0.05 = 0.05 \text{ W}.$$

Total filter loss:

$$P_{\text{filter}} \approx 1.89 + 0.5 + 0.05 = 2.44 \text{ W}.$$

Step 5 — Gate drive losses

$$P_{\text{gate}} = Q_g \, V_{gs} \, f_s \, N_{\text{switches}} = 60 \times 10^{-9} \cdot 12 \cdot 20 \times 10^3 \cdot 2 \approx 0.029 \text{ W}.$$

Step 6 — Sum and efficiency

Sum of losses:

$$P_{\text{losses}} = P_{\text{cond}} + P_{\text{sw}} + P_{\text{filter}} + P_{\text{gate}} \approx 1.83 + 80.0 + 2.44 + 0.029 = 84.30 \text{ W}.$$

Overall efficiency:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{losses}}} \times 100\% = \frac{500}{500 + 84.30} \times 100\% \approx 85.6\%.$$

Design note and recommendations:

- The computed modulation index $M \approx 1.63 > 1$ shows that with $V_{dc} = 400$ V the half-bridge cannot produce the target 115 V_{rms} in the *linear SPWM region*. Options:
  1. Increase DC bus to $V_{dc,\text{min}} = 4\sqrt{2}\, V_{o,\text{rms}} \approx 651$ V so that $M \leq 1$ (linear SPWM achievable).
  2. Use a **full-bridge** topology: for the same V_{dc}, a full-bridge gives roughly twice the half-bridge fundamental amplitude; with $V_{dc} = 400$ V a full-bridge can produce $V_{o,\text{rms, max}} \approx 400/(2\sqrt{2}) \approx 141.4$ V_{rms} with $M = 1$.
  3. Allow over-modulation or use selective harmonic elimination — both increase distortion and require careful analysis.
- Switching losses dominate this example (80 W). To reduce them:
  - Lower switching frequency (if filter size/THD budget allows).
  - Choose devices with lower E_{on}/E_{off} at your operating point (look at datasheet curves, not just single numbers).
  - Use soft-switching/topologies (e.g., ZVS) or synchronous rectification where applicable.
- Always validate estimates with time-domain simulation (SPICE/LTspice/MATLAB Simulink) and prototype measurements — datasheet energy values depend strongly on V_{dc}, I and gate drive conditions.

2.5.1 Design cheatsheet — Single-Phase Inverter (quick reference)

Key equations

$$V_{1,\text{rms}} = \frac{M\,V_{dc}}{4\sqrt{2}} \quad \text{(half-bridge, SPWM)}$$

$$M = \frac{V_{\text{control}}}{V_{\text{carrier}}}, \quad 0 \le M \le 1 \text{ (linear)}$$

$$I_{o,\text{rms}} = \frac{P_{\text{out}}}{V_{1,\text{rms}}}$$

$$P_{\text{cond,sw}} = I_{\text{rms,sw}}^2\, R_{ds(on)}$$

$$P_{\text{cond,diode}} = V_F I_{\text{avg}} + r_D I_{\text{rms}}^2$$

$$P_{\text{sw}} = (E_{on} + E_{off})\, f_s\, N_{\text{switches}}$$

$$P_{L,\text{DCR}} = I_{L,\text{rms}}^2\, \text{DCR}_L, \quad P_C = I_{C,\text{rms}}^2\, \text{ESR}$$

$$P_{\text{gate}} = Q_g\, V_{gs}\, f_s\, N_{\text{switches}}$$

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{losses}}} \times 100\%$$

Quick selection / design checklist

1. **Define specs:** P_{out}, $V_{o,\text{rms}}$, f_o, THD budget, ambient/maximum case temp.
2. **Choose V_{dc}:** ensure required fundamental amplitude with $M \le 1$ (compute $V_{dc,\text{min}} = 4\sqrt{2}V_{o,\text{rms}}$ for half-bridge).
3. **Switch selection:** check $R_{ds(on)}$ @ $\text{T}_{\text{junction}}$, E_{on}/E_{off} curves vs V_{dc} and I, Q_g and maximum V_{ds} rating.
4. **Switching frequency f_s:** trade-off between filter size/THD and switching losses; pick device/gate-driver pair accordingly.
5. **Filter design:** choose cutoff $f_c \ll f_s$ but $f_c \gg f_o$; estimate L using allowable ripple and C for voltage ripple and energy buffering; check DCR and core loss.
6. **Thermal design:** compute conduction + switching loss per device, derive required heatsink/thermal path, include margin (20–30%).
7. **EMI and snubbers:** evaluate dv/dt and di/dt; add RC snubbers or RC+RCD for clamp; follow layout rules for minimizing parasitics.
8. **Protection and control:** overcurrent, overvoltage, short-circuit, desaturation detection; dead-time strategy; current sensing (shunt, Hall), and control loop bandwidth.
9. **Validate:** perform time-domain switching simulations and laboratory measurements (power, thermal, THD, EMI).

Rules-of-thumb

- Keep switching losses under 10–20% of total losses when practical (higher switching loss fraction degrades efficiency markedly).
- If $M > 1$ is required by spec, prefer full-bridge or raise V_{dc} — do not rely on heavy over-modulation for clean output.

- Use gate drivers that support controlled turn-on/turn-off (adjustable gate resistances) to balance switching vs conduction trade-offs.
- Always report loss estimates with clear assumptions: V_{dc}, f_s, T_{junction}, and whether energies E_{on}, E_{off} are taken from datasheet at the same conditions.

3 Single-Phase Full-Bridge (H-Bridge) Inverter

3.1 Circuit Topology

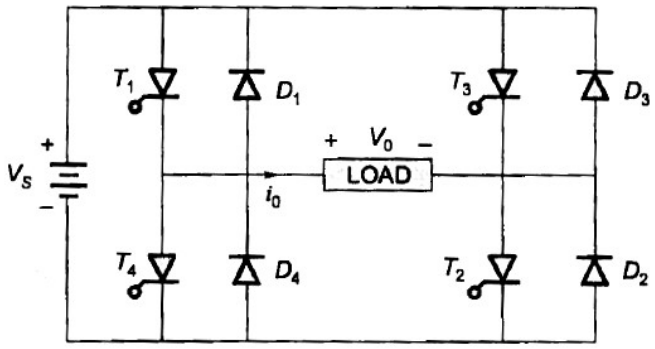

Figure 2: Single-phase full-bridge inverter (conceptual H-bridge).

Circuit diagram (conceptual)

Description of operation The full-bridge inverter uses two legs of complementary switches to apply either $+V_{dc}$ or $-V_{dc}$ across the load. By driving the left and right legs in complementary (or appropriately modulated) manners, the load sees a bipolar waveform that alternates between $+V_{dc}$ and $-V_{dc}$. Compared to the half-bridge, the full-bridge provides twice the voltage swing for the same DC bus and therefore can produce higher AC output amplitude without increasing V_{dc}.

Key operational points

- If the left leg midpoint is driven to $+V_{dc}$ while the right midpoint is at 0 (or vice-versa depending on reference), the load sees a positive voltage; reversing states produces negative voltage.
- Never turn both switches on the same leg simultaneously — insert dead-time to avoid shoot-through.
- Modulation (SPWM, unipolar/bipolar, SVPWM, etc.) controls the effective fundamental amplitude and harmonic content.

3.2 Switching sequence

Common switching schemes:

- **Bipolar SPWM:** Both legs are modulated by the same carrier; one leg uses the reference, the other uses the inverted reference. Output toggles between $+V_{dc}$ and $-V_{dc}$. Simpler but has higher switching harmonics.

- **Unipolar SPWM:** Each leg is individually compared to a carrier (or phase-shifted carriers). Output can take three levels $+V_{dc}, 0, -V_{dc}$ within a switching period — this reduces dominant low-order harmonics and the effective voltage step seen by the load.
- **Dead-time:** Inserted between complementary gate commands on each leg to avoid simultaneous conduction; dead-time causes small distortion and must be compensated if precise waveform is required.

Typical timing table (idealized)

Interval	Left leg (S1/S3)	Right leg (S2/S4)
$t_0 \to t_1$	S_1 ON, S_3 OFF	S_2 OFF, S_4 ON $(+V_{dc})$
$t_1 \to t_2$	S_1 OFF, S_3 ON	S_2 ON, S_4 OFF $(-V_{dc})$

3.3 Key waveforms (input DC, output AC, switch signals)

- **Input DC:** Constant V_{dc} (single, non-split bus).
- **Gate signals:** PWM pulses applied to each switch; complementary on each leg with dead-time.
- **Output (midpoint difference) waveform:** Bipolar PWM that switches between $\pm V_{dc}$; after filtering the fundamental approximates a sinusoid.
- **Filtered output:** Near sinusoidal $v_o(t)$ with lower THD if unipolar or advanced modulation is used.

3.4 Applications and power range

The full-bridge is widely used where a larger AC amplitude is required for a given DC bus:

- UPS systems, grid-tied inverters (low-to-medium voltage), motor drives, audio amplifiers (class-D), and power supplies.
- Typical practical power range: small units (tens of watts) up to tens or hundreds of kilowatts depending on cooling, packaging and semiconductor choices. Full-bridge is the default for medium-power single-phase converters.

3.5 Operating equations

A. Output voltage

- **Instantaneous (ideal square-mode) peak:**

$$V_{o,\text{peak(inst)}} = V_{dc}$$

(The output alternates between $\pm V_{dc}$.)

- **Fundamental (SPWM) peak:** In the linear modulation region the fundamental peak for a full-bridge under SPWM is

$$V_{1,\text{peak}} = M \cdot \frac{V_{dc}}{2}$$

where M is the modulation index (see below). This is twice the half-bridge fundamental for the same M and V_{dc}.

- **RMS of the fundamental:**

$$V_{1,\text{rms}} \;=\; \frac{V_{1,\text{peak}}}{\sqrt{2}} \;=\; \frac{M\,V_{dc}}{2\sqrt{2}}.$$

- **Modulation index (definition and range):**

$$M \;=\; \frac{V_{\text{control}}}{V_{\text{carrier}}}, \qquad 0 \le M \le 1$$

  In practice $M > 1$ indicates over-modulation (nonlinear region) and eventually square-wave operation as M grows.

B. Output current Let the load impedance phasor be $Z = |Z|\angle\theta_Z$ and fundamental voltage phasor V_1.

- **Phasor current (fundamental):**

$$\underline{I_1} \;=\; \frac{\underline{V_1}}{Z} \quad\Rightarrow\quad I_{o,\text{rms}} \;=\; \frac{V_{1,\text{rms}}}{|Z|}$$

- **Resistive load:** $I_{o,\text{rms}} = V_{1,\text{rms}}/R, \quad I_{o,\text{peak}} = \sqrt{2}\,I_{o,\text{rms}}$.
- **Reactive loads:** current phase angle $\varphi = \arg(Z)$; harmonic currents depend on load linearity and filter characteristics.

C. Power equations

- **Active (real) output power:**

$$P_{\text{out}} \;=\; V_{1,\text{rms}} \cdot I_{1,\text{rms}} \cdot \cos(\varphi)$$

  where φ is the voltage-current phase angle at the fundamental.

- **Apparent power:**

$$S \;=\; V_{1,\text{rms}} \cdot I_{1,\text{rms}}$$

- **Power factor:**

$$\text{PF} \;=\; \cos(\varphi) \;=\; \frac{P_{\text{out}}}{S}$$

D. Modulation

PWM principle Pulse width modulation synthesizes the desired sinusoidal fundamental by switching the H-bridge at a high carrier frequency f_s while modulating with a low-frequency reference f_o. For the full-bridge the same SPWM principle applies, but topologies and carrier arrangements (bipolar vs unipolar) change harmonic injection.

Switching frequency

- Use $f_s \gg f_o$ so switching harmonics are removable by the filter.
- Typical ranges: a few kHz to several tens of kHz for medium-power converters; tens to hundreds of kHz in high-frequency designs (trade-off with switching loss).

Modulation index

$$M \;=\; \frac{V_{\text{control}}}{V_{\text{carrier}}}, \qquad 0 \le M \le 1$$

In the linear region the relationship between M and the fundamental is given above.

Output fundamental voltage vs. M For linear SPWM (full-bridge):

$$V_{1,\text{peak}} \;=\; M \cdot \frac{V_{dc}}{2}, \qquad V_{1,\text{rms}} = \frac{M\,V_{dc}}{2\sqrt{2}}.$$

For $M = 1$ the maximum achievable RMS fundamental is $V_{dc}/(2\sqrt{2})$.

E. Harmonic Content

THD formula

$$\text{THD} \;=\; \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \quad \text{or} \quad \text{THD\%} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100\%.$$

Dominant harmonics

- **Bipolar SPWM:** switching harmonics concentrated at kf_s and sidebands $kf_s \pm mf_o$.
- **Unipolar SPWM / multilevel:** lower low-order harmonic content in the fundamental band; dominant energy still near switching frequency but with reduced magnitude.
- **Square-wave (overmodulation):** only odd harmonics present; n-th odd harmonic amplitude falls roughly as $1/n$. For a $\pm V_{dc}$ square wave of amplitude V_{dc}, the fundamental peak is $V_{1,\text{peak}} = \frac{4V_{dc}}{\pi}$.

Effect of switching frequency

- Increasing f_s shifts switching harmonics higher in frequency and reduces the portion of harmonic energy in the line band after filtering, lowering THD (at the cost of higher P_{sw}).
- Unipolar PWM and multilevel modulation reduce low-order harmonics for a given f_s, enabling either lower f_s for the same THD or improved THD for the same f_s.
- Dead-time, non-ideal device transitions and bus imbalance introduce additional low-order distortion — include these effects in simulations/measurements.

Practical note: for a specified $V_{o,\text{rms}}$ and V_{dc}, the designer should check that $M \le 1$. If $M > 1$, consider increasing V_{dc} or using a full-bridge (if not already used) or multilevel topology to meet the voltage requirement without entering the over-modulation regime.

3.5.1 Loss Analysis

A. Conduction losses Conduction losses occur whenever current flows through non-ideal resistive or diode elements (MOSFET/IGBT on-resistance, diode forward drop and dynamic resistance, filter DCR, etc.).

Switch conduction loss For a semiconductor switch with on-resistance $R_{ds(on)}$, the RMS conduction loss is

$$P_{\text{cond,sw}} \;=\; I_{\text{rms,sw}}^2\, R_{ds(on)} \tag{11}$$

where $I_{\text{rms,sw}}$ is the RMS current through that particular device calculated over one switching period. The total switch conduction loss is the sum over all switches (or equivalently the number of concurrently conducting switches multiplied by the per-switch loss when currents are similar).

Diode conduction loss (if applicable) Diode (body diode or discrete freewheeling diode) conduction loss may be approximated by

$$P_{\text{cond,diode}} \;=\; V_F\, I_{\text{avg}} \;+\; r_D\, I_{\text{rms}}^2 \tag{12}$$

where V_F is the diode forward voltage (approximate DC drop), r_D the dynamic resistance, I_{avg} the average diode conduction current and I_{rms} the diode RMS current. For synchronous designs (MOSFETs used as synchronous rectifiers) diode conduction loss is often reduced.

Total conduction loss

$$P_{\text{cond}} \;=\; \sum_{\text{switches}} I_{\text{rms,sw}}^2 R_{ds(on)} \;+\; \sum_{\text{diodes}} \left(V_F I_{\text{avg}} + r_D I_{\text{rms}}^2\right) \tag{13}$$

B. Switching losses Switching losses occur during finite voltage/current overlap at transitions and depend strongly on device characteristics and gate drive.

Turn-on / Turn-off energy

$$E_{\text{on}} \;=\; \int_{t_{\text{on,start}}}^{t_{\text{on,end}}} v_{\text{sw}}(t)\, i_{\text{sw}}(t)\, \mathrm{d}t, \qquad E_{\text{off}} \;=\; \int_{t_{\text{off,start}}}^{t_{\text{off,end}}} v_{\text{sw}}(t)\, i_{\text{sw}}(t)\, \mathrm{d}t.$$

Datasheets often provide E_{on} and E_{off} for representative conditions (specific V_{dc} and I).

Total switching loss If switches are switching at frequency f_s and there are N_{switches} devices that switch each cycle:

$$P_{\text{sw}} \;=\; (E_{\text{on}} + E_{\text{off}})\; f_s\; N_{\text{switches}}. \tag{14}$$

Note: depending on modulation method (bipolar vs unipolar SPWM, phase-shifted carriers, SVPWM) the effective number of switching events per fundamental period and per device may change — use the appropriate N_{switches} (or per-device switching count) for accurate estimates.

Dead-time effects Dead-time (non-overlap) prevents shoot-through but causes:

- Increased diode conduction (additional $P_{\text{cond,diode}}$);
- Low-order harmonic distortion and possible DC offset on the output;
- Slight change in RMS currents (hence conduction loss).

Include a dead-time loss term P_{dead} either from measurement/simulation or approximate it from estimated diode conduction during dead-time.

C. Filter losses Losses in the output filter (inductors and capacitors) reduce usable output power and must be estimated.

Inductor losses

- **DCR loss:**

$$P_{L,\text{DCR}} \;=\; I_{L,\text{rms}}^2\, \text{DCR}_L \tag{15}$$

  where $I_{L,\text{rms}}$ includes ripple current from switching.

- **Core loss:** use empirical Steinmetz (or generalized) model

$$P_{\text{core}} \;=\; k\, f^{\alpha}\, B_{\text{pk}}^{\beta}\, V_{\text{core}} \tag{16}$$

  with coefficients from the core manufacturer.

Capacitor ESR loss

$$P_C \;=\; I_{C,\mathrm{rms}}^2\,\mathrm{ESR} \tag{17}$$

where $I_{C,\mathrm{rms}}$ is the capacitor ripple RMS current.

Total filter loss

$$P_{\mathrm{filter}} \;=\; P_{L,\mathrm{DCR}} + P_{\mathrm{core}} + P_C.$$

D. Gate drive losses Gate charging energy per switching event:

$$P_{\mathrm{gate}} \;=\; Q_g\, V_{gs}\, f_s\, N_{\mathrm{switches}} \tag{18}$$

where Q_g is total gate charge per device and V_{gs} the gate drive amplitude. If gate energy is recovered or active gate drivers are used, effective loss may be lower.

E. Total efficiency Combining losses,

$$\eta \;=\; \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{cond}} + P_{\mathrm{sw}} + P_{\mathrm{filter}} + P_{\mathrm{gate}}} \times 100\%. \tag{19}$$

F. Numerical example Given (example) specifications:

- DC bus: $V_{dc} = 400$ V
- Desired AC output (fundamental): $V_{o,\mathrm{rms}} = 115$ V
- Output power: $P_{\mathrm{out}} = 500$ W (assumed resistive)
- Switching frequency: $f_s = 20$ kHz
- Semiconductor (example): $R_{ds(on)} = 40$ mΩ, $E_{on} = 1$ mJ, $E_{off} = 1$ mJ, total gate charge $Q_g = 60$ nC, $V_{gs} = 12$ V
- Filter estimates: inductor DCR = 0.10 Ω, core loss ≈ 0.5 W, capacitor ESR = 0.05 Ω, capacitor RMS ripple current ≈ 1 A

Step 1 — Modulation index and currents

For a full-bridge (linear SPWM):

$$V_{1,\mathrm{rms}} \;=\; \frac{M\,V_{dc}}{2\sqrt{2}} \qquad \Rightarrow \qquad M \;=\; \frac{2\sqrt{2}\,V_{1,\mathrm{rms}}}{V_{dc}}.$$

Numerically:

$$M \;=\; \frac{2\sqrt{2}\cdot 115}{400} = \frac{2.8284\cdot 115}{400} \approx 0.813.$$

($M \le 1 \rightarrow$ linear modulation acceptable.)

Output current (resistive load):

$$I_{o,\mathrm{rms}} \;=\; \frac{P_{\mathrm{out}}}{V_{o,\mathrm{rms}}} = \frac{500}{115} \approx 4.3478\ \mathrm{A}, \qquad I_{o,\mathrm{peak}} = \sqrt{2}\,I_{o,\mathrm{rms}} \approx 6.149\ \mathrm{A}.$$

Step 2 — Conduction losses

Assume at any time two switches conduct (one per leg). Approximate per-device RMS current $I_{\mathrm{rms,sw}} \approx I_{o,\mathrm{rms}}$. Then:

$$P_{\mathrm{cond,sw}} \approx N_{\mathrm{concurrent}} \cdot I_{o,\mathrm{rms}}^2\, R_{ds(on)} = 2\cdot (4.3478)^2 \cdot 0.04 \approx 1.51\ \mathrm{W}.$$

Estimate diode conduction loss (dead-time / body diode):

$$P_{\text{cond,diode}} \approx 0.32 \text{ W} \quad \text{(same approximation as prior example).}$$

Total conduction:

$$P_{\text{cond}} \approx 1.51 + 0.32 = 1.83 \text{ W}.$$

Step 3 — Switching losses

Using datasheet energies and $N_{\text{switches}} = 4$ switching devices:

$$P_{\text{sw}} = (E_{on} + E_{off})\, f_s\, N_{\text{switches}} = (1 \times 10^{-3} + 1 \times 10^{-3}) \cdot 20 \times 10^3 \cdot 4 = 160.0 \text{ W}.$$

Note: depending on modulation style (e.g., unipolar SPWM) the effective switching per device may be lower — adjust N_{switches} accordingly if using per-device switching counts.

Step 4 — Filter losses

$$P_{L,\text{DCR}} = I_{L,\text{rms}}^2\, \text{DCR}_L \approx (4.3478)^2 \cdot 0.10 \approx 1.89 \text{ W}.$$

Core loss ≈ 0.5 W. Capacitor ESR:

$$P_C = I_{C,\text{rms}}^2\, \text{ESR} = 1^2 \cdot 0.05 = 0.05 \text{ W}.$$

Total filter:

$$P_{\text{filter}} \approx 1.89 + 0.5 + 0.05 = 2.44 \text{ W}.$$

Step 5 — Gate drive losses

$$P_{\text{gate}} = Q_g\, V_{gs}\, f_s\, N_{\text{switches}} = 60 \times 10^{-9} \cdot 12 \cdot 20 \times 10^3 \cdot 4 \approx 0.058 \text{ W}.$$

Step 6 — Sum and efficiency

Sum of losses:

$$P_{\text{losses}} \approx P_{\text{cond}} + P_{\text{sw}} + P_{\text{filter}} + P_{\text{gate}} \approx 1.83 + 160.0 + 2.44 + 0.058 \approx 164.33 \text{ W}.$$

Efficiency:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{losses}}} \times 100\% = \frac{500}{500 + 164.33} \times 100\% \approx 75.2\%.$$

Discussion and practical notes:

- In this example switching losses dominate (160 W) because four devices switch each period at a relatively high energy per transition. To reduce P_{sw}:
  - Lower switching frequency f_s if filter / THD budget allows.
  - Select devices with lower E_{on}/E_{off} at the operating V_{dc} and I (consult datasheet curves).
  - Employ modulation methods that reduce per-device switching (e.g., bipolar vs unipolar tradeoffs), or topologies with soft switching (ZVS/ZCS).
  - Use half-bridge with higher V_{dc} or multilevel topologies to reduce required switching stress for a given AC amplitude.
- If unipolar PWM is used, effective switching per device may be reduced relative to bipolar SPWM, lowering P_{sw}. Likewise, using synchronous MOSFET conduction reduces diode losses.
- Always corroborate analytic estimates with time-domain switching simulations (SPICE/LTspice/PLECS/Sim and prototype measurements — datasheet E_{on}, E_{off}, and $R_{ds(on)}$ depend on junction temperature, gate drive conditions and operating voltage.
- Report assumptions clearly when presenting the numerical example (device temps, conduction duty, modulation scheme).

3.5.2 Design cheatsheet — Full-Bridge Inverter (quick reference)

Key equations (full-bridge, SPWM, linear region)

$$V_{1,\text{peak}} = M \cdot \frac{V_{dc}}{2} \tag{20}$$

$$V_{1,\text{rms}} = \frac{M\,V_{dc}}{2\sqrt{2}} \tag{21}$$

$$M = \frac{V_{\text{control}}}{V_{\text{carrier}}}, \qquad 0 \le M \le 1 \tag{22}$$

$$I_{o,\text{rms}} = \frac{P_{\text{out}}}{V_{1,\text{rms}}} \tag{23}$$

$$P_{\text{out}} = V_{1,\text{rms}} \cdot I_{o,\text{rms}} \cdot \cos\varphi \tag{24}$$

$$S = V_{1,\text{rms}} \cdot I_{o,\text{rms}} \tag{25}$$

$$\text{PF} = \cos\varphi = \frac{P_{\text{out}}}{S} \tag{26}$$

Loss equations (per device / element)

$$P_{\text{cond,sw}} = I_{\text{rms,sw}}^2\, R_{ds(on)} \tag{27}$$

$$P_{\text{cond,diode}} = V_F\, I_{\text{avg}} + r_D\, I_{\text{rms}}^2 \tag{28}$$

$$P_{\text{sw}} = (E_{\text{on}} + E_{\text{off}})\, f_s\, N_{\text{switches}} \tag{29}$$

$$P_{\text{gate}} = Q_g\, V_{gs}\, f_s\, N_{\text{switches}} \tag{30}$$

$$P_{L,\text{DCR}} = I_{L,\text{rms}}^2\, \text{DCR}_L \tag{31}$$

$$P_C = I_{C,\text{rms}}^2\, \text{ESR} \tag{32}$$

$$P_{\text{core}} = k\, f^{\alpha}\, B_{\text{pk}}^{\beta}\, V_{\text{core}} \quad \text{(Steinmetz)} \tag{33}$$

Overall efficiency

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{cond}} + P_{\text{sw}} + P_{\text{filter}} + P_{\text{gate}}} \times 100\%$$

Filter / L–C design rules (quick)

- **Cutoff frequency:** choose filter cutoff f_c such that

  $$f_o \ll f_c \ll f_s.$$

  A practical guide: $5f_o \lesssim f_c \lesssim f_s/10$ (tune to THD vs. size trade-off).

- **LC cutoff:**

  $$f_c = \frac{1}{2\pi\sqrt{L\,C}}$$

- **Inductor ripple approximation (conservative):** for a PWM step V_{step} at f_s,

  $$\Delta I_L \approx \frac{V_{\text{step}}}{L\, f_s}$$

  where V_{step} can be conservatively taken as V_{dc} (or the maximum instantaneous step seen by the filter). Choose L so that $\Delta I_L \le$ allowable ripple.

- **Choose C** to limit voltage ripple and set f_c with chosen L; verify capacitor RMS current rating and ESR.

Quick sizing rules & checks

- $\boxed{V_{dc,\min} = \dfrac{2\sqrt{2}\,V_{o,\mathrm{rms}}}{M_{\max}}}$ — for linear SPWM set $M_{\max} = 1$. If spec requires smaller V_{dc}, use full-bridge (or multilevel) or accept overmodulation.
- Check that each switch voltage rating $V_{ds,\max} > V_{dc}\times$ safety margin (typically 1.2–1.5).
- Ensure continuous current rating of switches $I_{cont} > I_{o,\mathrm{rms}}$ with margin (20–50% depending on cooling).
- Thermal margin: account for $R_{ds(on)}(T_j)$ increase with junction temperature; compute worst-case conduction loss at max T_j.
- Gate driver: gate voltage V_{gs} and drive current must support chosen Q_g at switching speed; include gate driver supply dissipation.
- EMI: fast edges reduce switching losses but increase EMI — apply snubbers, common-mode chokes, and layout mitigation as needed.

Component selection checklist

1. **Switches:** voltage rating $\geq 1.2-1.5 \times V_{dc,\max}$; check $R_{ds(on)}$ vs T_j; review E_{on}, E_{off} vs V_{dc}, I.
2. **Diodes / synchronous MOSFETs:** low V_F / low conduction losses; consider synchronous MOSFETs to reduce diode loss.
3. **Gate driver:** can source/sink required peak gate current; supports dead-time and protection features.
4. **Inductor core:** select core material with low core loss at switching harmonics; DCR and thermal limits acceptable.
5. **Capacitors:** energy buffering, low ESR, RMS current rating adequate.
6. **Thermal management:** heatsink or cooling plan sized from summed per-device losses; include margin.
7. **Sensing & protection:** accurate current sense for control and protection; overcurrent / desat / overvoltage detection.

Rules of thumb

- Keep switching losses under $\sim 10-30\%$ of total losses where possible to preserve high efficiency.
- If $M > 1$ for required output, prefer raising V_{dc} or using multilevel/full-bridge topology rather than heavy over-modulation.
- When in doubt, simulate a time-domain switching cycle (including dead-time and device datasheet curves) rather than relying only on analytic approximations.
- Always state assumptions (temperatures, f_s, modulation method, measurement bandwidth) when reporting THD or efficiency.

4 Three-Phase Two-Level Inverter — Operating Equations

This section collects the operating equations and key relations for a balanced three-phase, two-level inverter (three-leg, each leg a half-bridge connected to a DC link V_{dc}). When a different topology (three-level, NPC, cascaded H-bridges, etc.) is used, some relations (maximum achievable voltage, modulation limits) must be adapted.

4.1 Circuit Topology

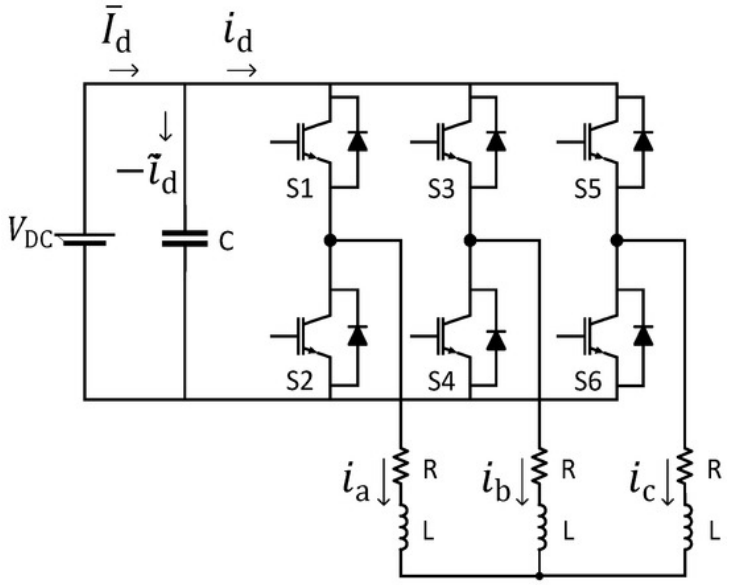

Figure 3: Three-phase inverter.

Circuit diagram (conceptual)

4.2 Notation and conventions

- V_{dc} – DC link voltage (total voltage between positive and negative rails).
- $v_a(t), v_b(t), v_c(t)$ – phase-to-neutral instantaneous voltages (phase voltages).
- $v_{ab}(t) = v_a - v_b$ – line-to-line instantaneous voltage between phases a and b.
- $V_{1,\text{peak}}$ – fundamental phase-to-neutral voltage peak (first harmonic).
- $V_{1,\text{rms}} = V_{1,\text{peak}}/\sqrt{2}$ – fundamental phase RMS.
- $V_{LL,\text{rms}}$ – fundamental line-to-line RMS (between any two phases).
- M – modulation index defined below.

A. Output voltage

- **Instantaneous (ideal two-level) peak:** each phase (phase-to-neutral) switches between $\pm V_{dc}/2$ (for a half-bridge leg referenced to the negative rail), so the instantaneous extreme value is

$$v_{a,\text{inst(max)}} = \pm\frac{V_{dc}}{2}.$$

- **Fundamental (SPWM) peak (phase-to-neutral):** under sinusoidal PWM (SPWM) in the linear modulation region the fundamental phase peak is proportional to the modulation index M:

$$V_{1,\text{peak}} \;=\; M \cdot \frac{V_{dc}}{2}.$$

  This relation assumes the usual definition of M as the ratio of reference (control) peak to carrier peak (see below).

- **Phase RMS (fundamental):**

$$V_{1,\text{rms}} \;=\; \frac{V_{1,\text{peak}}}{\sqrt{2}} \;=\; \frac{M\,V_{dc}}{2\sqrt{2}}.$$

- **Line-to-line RMS:** for a balanced, symmetric three-phase set,

$$V_{LL,\text{rms}} \;=\; \sqrt{3}\,V_{1,\text{rms}} \;=\; \frac{M\,V_{dc}\,\sqrt{3}}{2\sqrt{2}}.$$

- **Modulation index (definition and range):**

$$M \;=\; \frac{V_{\text{control}}}{V_{\text{carrier}}}$$

  where V_{control} is the peak amplitude of the sinusoidal reference and V_{carrier} is the peak amplitude of the triangular (or other) carrier. For SPWM the linear range is

$$0 \le M \le 1.$$

  Note: using space-vector PWM (SVPWM) or other optimal carrier strategies increases the maximum usable modulation amplitude before over-modulation. With the same reference convention, SVPWM has a higher effective maximum linear modulation (approximately $M_{\text{SVPWM,max}} \approx \frac{\sqrt{3}}{2} \approx 0.866$ relative to certain normalization conventions) and therefore yields a larger fundamental for the same reference amplitude — consult the precise definition used in your controller as conventions vary.

B. Output current Assume a balanced three-phase load (each phase impedance Z, angle φ).

- **Phase (fundamental) current phasor:**

$$\underline{I_1} \;=\; \frac{\underline{V_1}}{Z} \quad\Rightarrow\quad I_{1,\text{rms}} \;=\; \frac{V_{1,\text{rms}}}{|Z|}.$$

- **Resistive (Y-connected) load:** $I_{1,\text{rms}} = V_{1,\text{rms}}/R, \quad I_{1,\text{peak}} = \sqrt{2}\,I_{1,\text{rms}}$.

- **Line currents:** for a Y-connected balanced load, line currents equal phase currents ($I_{\text{line}} = I_{\text{phase}}$). For delta-connected loads, $I_{\text{line}} = \sqrt{3}\,I_{\text{phase}}$ (phasor relationship) — check connection when computing conductor sizing and losses.

- **Harmonic currents:** harmonic content of phase currents depends on load linearity and filter design; non-linear loads draw harmonic currents that may cause neutral or DC-bus stress if not handled.

C. Power equations For a balanced three-phase system:

- **Active (real) output power:**

$$P_{\text{out}} \;=\; 3\,V_{1,\text{rms}}\,I_{1,\text{rms}}\,\cos(\varphi) \;=\; \sqrt{3}\,V_{LL,\text{rms}}\,I_{LL,\text{rms}}\,\cos(\varphi).$$

  Use the first form when phase quantities are known, the second when line-line measurements are used.

- **Apparent power:**

$$S \;=\; 3\,V_{1,\text{rms}}\,I_{1,\text{rms}} \;=\; \sqrt{3}\,V_{LL,\text{rms}}\,I_{LL,\text{rms}}.$$

- **Power factor:**

$$\text{PF} \;=\; \cos(\varphi) \;=\; \frac{P_{\text{out}}}{S}.$$

- **Per-phase power (balanced):** $P_{\text{phase}} = P_{\text{out}}/3 = V_{1,\text{rms}} I_{1,\text{rms}} \cos\varphi$.

D. Modulation

PWM principle Sinusoidal PWM compares each of the three phase references ($v_{ref,a} = V_{\text{control}}\sin(\omega_o t)$, $v_{ref,b} = V_{\text{control}}\sin(\omega_o t - 2\pi/3)$, $v_{ref,c} = V_{\text{control}}\sin(\omega_o t + 2\pi/3)$) with a carrier to generate switching signals for the three legs. Space-vector PWM (SVPWM) is an alternative that directly synthesizes the desired three-phase space vector by time-domain allocation of inverter switching states and is more efficient in DC-link utilization.

Switching frequency

- Choose switching frequency f_s such that $f_s \gg f_o$ (output fundamental). Typical values depend on power level and devices: low-power converters often use tens of kHz; medium/high-power may use lower f_s to reduce switching losses unless wide-bandgap devices are used.
- Trade-offs: higher f_s reduces filter size and THD but increases switching and gate-drive losses and may increase EMI.

Modulation index formula

$$M \;=\; \frac{V_{\text{control}}}{V_{\text{carrier}}}$$

For SPWM linear region $0 \le M \le 1$. For SVPWM the effective usable modulation amplitude before overmodulation is higher (see note above); verify the controller convention.

Output fundamental voltage vs. M

$$V_{1,\text{peak}} \;=\; M \cdot \frac{V_{dc}}{2}, \qquad V_{1,\text{rms}} \;=\; \frac{M\,V_{dc}}{2\sqrt{2}}.$$

and therefore

$$V_{LL,\text{rms}} \;=\; \frac{M\,V_{dc}\,\sqrt{3}}{2\sqrt{2}}.$$

Remarks: the scalar factor above assumes the common half-bridge leg convention. Different topologies (full H-bridge per phase, series H-bridges, NPC) change the coefficient; SVPWM can increase the attainable line-line RMS for the same reference amplitude (practical factor $\sim$15% improvement versus SPWM depending on normalization).

E. Harmonic Content

THD formula Total harmonic distortion of a measured quantity (voltage or current) is:

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \quad \text{or} \quad \text{THD\%} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100\%.$$

Dominant harmonics

- **Switching-related harmonics:** energy concentrated at multiples of the switching frequency kf_s and sidebands $kf_s \pm mf_o$.
- **Low-order harmonics:** in SPWM low-order harmonics near the fundamental are small in the linear region; over-modulation and dead-time introduce low-order distortion.
- **Triplen harmonics (multiples of 3):** triplen harmonics constitute zero-sequence components. In a three-wire, balanced, star-connected system without neutral these zero-sequence components cancel in the line-to-line voltages (i.e., triplen harmonics are not present in line-line voltages). However, phase-to-neutral voltages and neutral currents can contain triplen components if there are single-phase nonlinear loads or DC-link asymmetries.
- **Space-vector / multilevel effects:** SVPWM and multilevel converters reduce low-order harmonic content for a given switching frequency compared with simple bipolar SPWM.

Effect of switching frequency

- Increasing f_s shifts switching harmonics away from the fundamental and reduces the required filter size for a given THD target, at the cost of increased switching and gate-drive losses.
- Lower f_s places more harmonic energy closer to the output band and requires larger L–C filters or results in higher measured THD.
- Practical design balances thermal limits, EMI, filter size, and THD specifications. For three-phase motor drives, attention must be paid to harmonic torque pulsations (low-order harmonics are more harmful).

Practical notes

- Always state whether voltages/currents are phase (phase-to-neutral) or line values when reporting results.
- For detailed harmonic prediction, use Fourier analysis of the chosen modulation scheme (SPWM, unipolar, SVPWM) and include dead-time and device non-idealities, or perform time-domain simulation.
- For multilevel converters, replace the fundamental amplitude relations with the appropriate level-dependent coefficients (multilevel topologies increase attainable fundamental and reduce switching-step size).

4.3 Loss Analysis — Three-Phase Two-Level Inverter

A. Conduction losses Conduction losses occur when semiconductor devices or passive components carry current.

Switch conduction loss For each switching device (MOSFET/IGBT) with on-resistance $R_{ds(on)}$,

$$P_{\text{cond,sw}} \;=\; I_{\text{rms,sw}}^2 \, R_{ds(on)}$$

Total semiconductor conduction loss (accounting only for devices conducting at any instant) can be approximated by summing per-conductor losses. In a balanced three-phase two-level inverter there are three concurrently conducting switches (one per phase), so an approximate total switch conduction loss is

$$P_{\text{cond,sw,tot}} \approx 3 \, I_{1,\text{rms}}^2 \, R_{ds(on)}$$

where $I_{1,\text{rms}}$ is the phase (fundamental) RMS current.

Diode conduction loss (if applicable) When body diodes or discrete freewheeling diodes conduct,

$$P_{\text{cond,diode}} \;=\; V_F \cdot I_{\text{avg}} \;+\; r_D \cdot I_{\text{rms}}^2$$

Sum diode losses over phases/diodes to obtain the total diode conduction loss. In synchronous designs diode conduction may be small (MOSFETs conduct instead).

Total conduction loss

$$P_{\text{cond}} \;=\; P_{\text{cond,sw,tot}} \;+\; P_{\text{cond,diode,tot}}$$

B. Switching losses Switching losses arise from energy dissipated during finite-voltage/current transitions.

Turn-on / turn-off energy Per-device turn-on and turn-off energies are

$$E_{\text{on}} \;=\; \int_{t_{\text{on,start}}}^{t_{\text{on,end}}} v_{\text{sw}}(t)\, i_{\text{sw}}(t)\, \mathrm{d}t, \qquad E_{\text{off}} \;=\; \int_{t_{\text{off,start}}}^{t_{\text{off,end}}} v_{\text{sw}}(t)\, i_{\text{sw}}(t)\, \mathrm{d}t.$$

Use datasheet curves (function of V_{DC} and current) or measured waveforms.

Total switching loss For switching frequency f_s and N_{switches} devices that switch each fundamental period,

$$P_{\text{sw}} \;=\; (E_{\text{on}} + E_{\text{off}})\, f_s \, N_{\text{switches}}.$$

Note: modulation method (bipolar/unipolar/SPWM/SVPWM) affects per-device switching counts — use appropriate N_{switches}.

Dead-time effects Dead-time causes additional diode conduction and low-order distortion. Include an extra dead-time loss term P_{dead} (from simulation/measurement) if dead-time is significant.

C. Filter losses Passive filter losses reduce output power.

Inductor losses DCR (copper) loss per phase:

$$P_{L,\text{DCR}} \;=\; I_{L,\text{rms}}^2 \, \text{DCR}_L$$

Sum across three phases for total DCR loss. Core loss may be modeled with a Steinmetz form:

$$P_{\text{core}} \;=\; k \, f^{\alpha} \, B_{\text{pk}}^{\beta} \, V_{\text{core}}.$$

Capacitor ESR loss

$$P_C \;=\; I_{C,\mathrm{rms}}^2\,\mathrm{ESR}$$

Total filter loss

$$P_{\mathrm{filter}} \;=\; \sum_{\mathrm{phases}} P_{L,\mathrm{DCR}} \;+\; P_{\mathrm{core,tot}} \;+\; P_C$$

D. Gate drive losses Energy to charge/discharge gate per transition gives:

$$P_{\mathrm{gate}} \;=\; Q_g\, V_{gs}\, f_s\, N_{\mathrm{switches}}$$

If gate energy is recovered or active drivers are used, effective gate loss reduces.

E. Total efficiency Collecting all loss contributions:

$$\eta \;=\; \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} \;+\; P_{\mathrm{cond}} \;+\; P_{\mathrm{sw}} \;+\; P_{\mathrm{filter}} \;+\; P_{\mathrm{gate}}} \times 100\%.$$

F. Numerical example (worked) Given specifications (example):

- DC link voltage: $V_{dc} = 700$ V
- Target line-to-line RMS output: $V_{LL,\mathrm{rms}} = 400$ V
- Output power (balanced three-phase): $P_{\mathrm{out}} = 5000$ W
- Switching frequency: $f_s = 12$ kHz
- Device assumptions (example): $R_{ds(on)} = 20$ mΩ, $E_{on} = E_{off} = 0.8$ mJ (per device, representative), $Q_g = 60$ nC, $V_{gs} = 12$ V
- Filter / passive estimates: per-phase DCR = 0.05 Ω, core loss ≈ 1 W per phase, capacitor ESR loss ≈ 0.1 W total.
- Diode model: $V_F = 0.7$ V, dynamic resistance $r_D = 0.02$ Ω. (Estimate diode conduction duty small — use conservative fraction for average.)
- Assume unity power factor ($\cos\varphi = 1$) for simplicity.

Step 1 — Derived fundamental and modulation index Phase (phase-to-neutral) RMS fundamental:

$$V_{1,\mathrm{rms}} \;=\; \frac{V_{LL,\mathrm{rms}}}{\sqrt{3}} = \frac{400}{\sqrt{3}} \approx 230.9401\ \mathrm{V}.$$

Modulation index (SPWM linear relation)

$$V_{1,\mathrm{rms}} \;=\; \frac{M\,V_{dc}}{2\sqrt{2}} \quad\Rightarrow\quad M \;=\; \frac{2\sqrt{2}\,V_{1,\mathrm{rms}}}{V_{dc}}$$

Numerically,

$$M \approx \frac{2\sqrt{2}\cdot 230.9401}{700} \approx 0.9331 \quad (\text{within linear range } M \le 1).$$

Step 2 — Currents Phase (line) RMS current (balanced, PF = 1):

$$I_{LL,\mathrm{rms}} \;=\; \frac{P_{\mathrm{out}}}{\sqrt{3}\,V_{LL,\mathrm{rms}}} = \frac{5000}{\sqrt{3}\cdot 400} \approx 7.2169\ \mathrm{A}.$$

Phase peak:

$$I_{1,\text{peak}} = \sqrt{2}\, I_{1,\text{rms}} \approx 10.2062 \text{ A}.$$

Step 3 — Conduction losses Approximate total semiconductor conduction loss (3 concurrently conducting switches):

$$P_{\text{cond,sw,tot}} \approx 3\, I_{1,\text{rms}}^2\, R_{ds(on)} = 3 \cdot (7.2169)^2 \cdot 0.02 \approx 3.125 \text{ W}.$$

Estimated diode conduction loss (rough estimate accounting small duty / dead-time conduction):

$$P_{\text{cond,diode,tot}} \approx 4.641 \text{ W} \quad \text{(assumptions used: } I_{\text{avg}} \approx 0.1\, I_{1,\text{rms}},\ r_D = 0.02\ \Omega).$$

Total conduction:

$$P_{\text{cond}} \approx 3.125 + 4.641 \approx 7.766 \text{ W}.$$

Step 4 — Switching losses Using $E_{on} = E_{off} = 0.8$ mJ per device and $N_{\text{switches}} = 6$:

$$P_{\text{sw}} = (E_{on} + E_{off})\, f_s\, N_{\text{switches}} = (0.0008 + 0.0008) \cdot 12000 \cdot 6 \approx 115.20 \text{ W}.$$

Step 5 — Filter losses DCR loss (sum over 3 phases):

$$P_{L,\text{DCR}} = 3\, I_{1,\text{rms}}^2\, \text{DCR}_L = 3 \cdot (7.2169)^2 \cdot 0.05 \approx 8.09 \text{ W}.$$

Core loss (assumed 1 W per phase): $P_{\text{core,tot}} = 3$ W. Capacitor ESR loss (estimate): $P_C \approx 0.1$ W. Total filter:

$$P_{\text{filter}} \approx 8.09 + 3 + 0.10 \approx 11.19 \text{ W}.$$

Step 6 — Gate drive losses

$$P_{\text{gate}} = Q_g\, V_{gs}\, f_s\, N_{\text{switches}} = 60 \times 10^{-9} \cdot 12 \cdot 12000 \cdot 6 \approx 0.052 \text{ W}.$$

Step 7 — Sum of losses and efficiency Sum of losses:

$$P_{\text{losses}} \approx P_{\text{cond}} + P_{\text{sw}} + P_{\text{filter}} + P_{\text{gate}} \approx 7.766 + 115.20 + 11.19 + 0.052 \approx 133.93 \text{ W}.$$

Overall efficiency:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{losses}}} \times 100\% = \frac{5000}{5000 + 133.93} \times 100\% \approx 97.39\%.$$

Notes and recommendations

- **Assumptions:** the numerical example above uses many simplifying assumptions (per-device energy values, simplified diode conduction duty, fixed DCR and core loss estimates). Use manufacturer datasheet curves and time-domain simulation for more accurate estimates.
- **Switching losses dominate the example:** P_{sw} (=115 W) is the largest contributor. To reduce it: lower f_s, pick devices with lower switching energy at the operating V_{dc}/I, or adopt soft-switching topologies.
- **Conduction losses are small here** due to modest current and relatively low $R_{ds(on)}$. At higher currents conduction losses scale as I^2 and may dominate.
- **Thermal design:** convert per-device loss share into junction temperature rise and select heatsinking/forced cooling accordingly; include margin (20–30%).
- **Validation:** always validate analytic estimates with time-domain switching simulation (SPICE/LTspice/PLECS/Simulink) including gate waveforms, dv/dt, di/dt, dead-time and device temperature dependence.

4.4 Design cheatsheet — Three-Phase Two-Level Inverter (quick reference)

Key equations (balanced, two-level, SPWM linear region)

$$V_{1,\text{peak}} = M \cdot \frac{V_{dc}}{2} \tag{34}$$

$$V_{1,\text{rms}} = \frac{M\,V_{dc}}{2\sqrt{2}} \tag{35}$$

$$V_{LL,\text{rms}} = \sqrt{3}\,V_{1,\text{rms}} = \frac{M\,V_{dc}\,\sqrt{3}}{2\sqrt{2}} \tag{36}$$

$$M = \frac{V_{\text{control}}}{V_{\text{carrier}}}, \qquad 0 \le M \le 1 \tag{37}$$

$$I_{1,\text{rms}} = \frac{P_{\text{out}}}{3\,V_{1,\text{rms}}} \tag{38}$$

$$P_{\text{out}} = 3\,V_{1,\text{rms}}\,I_{1,\text{rms}}\,\cos\varphi \tag{39}$$

Loss equations (per device / element)

$$P_{\text{cond,sw}} = I_{\text{rms,sw}}^2\,R_{ds(on)} \tag{40}$$

$$P_{\text{cond,diode}} = V_F\,I_{\text{avg}} + r_D\,I_{\text{rms}}^2 \tag{41}$$

$$P_{\text{sw}} = (E_{\text{on}} + E_{\text{off}})\,f_s\,N_{\text{switches}} \tag{42}$$

$$P_{\text{gate}} = Q_g\,V_{gs}\,f_s\,N_{\text{switches}} \tag{43}$$

$$P_{L,\text{DCR}} = I_{L,\text{rms}}^2\,\text{DCR}_L \quad \text{(per phase)} \tag{44}$$

$$P_C = I_{C,\text{rms}}^2\,\text{ESR} \tag{45}$$

$$P_{\text{core}} = k\,f^{\alpha}\,B_{\text{pk}}^{\beta}\,V_{\text{core}} \quad \text{(Steinmetz)} \tag{46}$$

Overall efficiency

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{cond}} + P_{\text{sw}} + P_{\text{filter}} + P_{\text{gate}}} \times 100\%$$

Filter / L–C design quick rules

- **Choose cutoff:** pick filter cutoff f_c such that

  $$f_o \ll f_c \ll f_s.$$

  Practical rule: $5\,f_o \lesssim f_c \lesssim f_s/10$ (trade THD vs. size).

- **LC cutoff:** $f_c = \dfrac{1}{2\pi\sqrt{L\,C}}$.

- **Inductor ripple (approx):**

  $$\Delta I_L \approx \frac{V_{\text{step}}}{L\,f_s},$$

  where V_{step} is the maximum voltage step seen by the filter (safe conservative pick: V_{dc} or the relevant line-to-line step).

- **Choose L:** ensure ΔI_L below allowed ripple and check DCR/core loss; ensure inductor RMS current rating covers harmonic ripple.

- **Choose C:** size for voltage ripple and reactive current; ensure ESR and RMS ripple current rating.

Quick sizing rules & checks

- $\boxed{V_{dc,\min} = \dfrac{2\sqrt{2}\,V_{1,\mathrm{rms}}}{M_{\max}}}$ with $M_{\max} = 1$ in linear SPWM. For a required line voltage $V_{LL,\mathrm{rms}}$ use $V_{1,\mathrm{rms}} = V_{LL,\mathrm{rms}}/\sqrt{3}$.
- Device voltage rating: $V_{ds,\max} \geq 1.2{-}1.5 \times V_{dc,\max}$.
- Current rating: choose continuous and transient current ratings $\geq I_{1,\mathrm{rms}}$ with 20–50% margin depending on cooling.
- Thermal margin: include temperature dependence of $R_{ds(on)}$; compute per-device dissipation and heatsink requirement with safety margin.
- Neutral and triplen harmonics: for unbalanced or single-phase nonlinear loads expect triplen harmonics in phase-to-neutral voltages and possible neutral current — check neutral conductor and DC-link stress.
- Modulation strategy: use SVPWM for best DC-link utilization (higher fundamental for same V_{dc}) and lower low-order distortion versus basic SPWM.

Component selection checklist

1. **Switches:** voltage rating $\geq 1.2{-}1.5 \times V_{dc}$; low $R_{ds(on)}$ at operating $\mathrm{T_j}$; review E_{on}/E_{off} vs V_{dc}, I.
2. **Diodes / synchronous MOSFETs:** low V_F or use synchronous MOSFET to reduce diode loss.
3. **Gate drivers:** support required peak gate current, dead-time control, desat/protection and isolated gate supply if needed.
4. **Inductors:** core material with acceptable core loss at switching harmonics; DCR and thermal ratings adequate.
5. **Capacitors:** low ESR, adequate ripple current rating and energy storage for DC link / filter.
6. **Thermal management:** heatsinks, forced air, or liquid cooling sized from total per-device losses.
7. **Sensing & protection:** accurate current sensing (shunt/Hall), overcurrent, overvoltage, desaturation, and temperature monitoring.

Practical rules of thumb

- Use SVPWM to gain 10–15% more fundamental amplitude from the same V_{dc} compared with naive SPWM normalization (verify exact normalization in your controller).
- Keep switching losses below 10–30% of total losses if you need high efficiency; otherwise prioritize conduction losses at high currents.
- If triplen or zero-sequence harmonics appear (single-phase nonlinear loads), verify neutral path and DC-link balancing caps.
- When increasing f_s to reduce filter size/THD, always check device E_{on}/E_{off} and gate drive thermal limits — wide-bandgap semiconductors make high f_s more practical.
- Always state assumptions (modulation, temperature, measurement bandwidth) when reporting THD or efficiency.

5 Cascaded H-Bridge (CHB) Inverter

5.1 Circuit Topology

A cascaded H-bridge (CHB) inverter is a multilevel inverter topology composed of several single-phase full-bridge cells connected in series on the AC side. Each H-bridge cell is supplied by an isolated DC source such as a battery, capacitor, or photovoltaic panel. The overall AC output voltage is obtained by summing the individual bridge voltages.

$$V_{an} = V_{an1} + V_{an2} + \cdots + V_{ann}$$

Each H-bridge cell consists of four switches $(S_{1i}, S_{2i}, S_{3i}, S_{4i})$ and one isolated DC source V_{dci}, where $i = 1, 2, \ldots, n$ denotes the cell index.

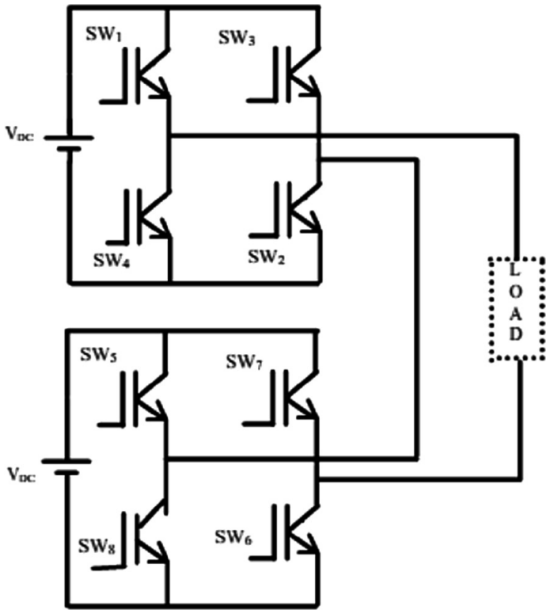

Figure 4: H-bridge inverter.

Circuit diagram (conceptual)

Description of Operation

Each individual H-bridge inverter cell can generate three voltage levels:

$$V_{oi} = +V_{dci},\ 0,\ -V_{dci}$$

By properly controlling the switching states of the series-connected bridges, a stepped multilevel waveform approximating a sinusoidal output is obtained.

For an n-cell CHB inverter, the number of output voltage levels m is:

$$m = 2n + 1$$

Switching Sequence

The switching sequence is designed so that each H-bridge contributes one voltage step to the output. At any instant, the inverter output equals the sum of selected DC source voltages depending on the modulation signal. Level-shifted or phase-shifted PWM techniques are typically used to control switching.

Key Waveforms

- **Input DC voltages:** Constant, isolated sources for each cell.
- **Output AC voltage:** Multilevel stepped waveform approximating a sinusoid.
- **Switch signals:** PWM patterns for each switch, typically phase-shifted between bridges.

Applications and Power Range

Cascaded H-bridge inverters are widely used in:

- Medium- and high-voltage grid-connected systems
- Photovoltaic farms and energy storage systems
- Electric vehicle traction drives
- FACTS (Flexible AC Transmission Systems)

Power ratings typically range from tens of kW up to several MW.

5.2 Operating Equations

A. Output Voltage

For an n-cell CHB inverter, the maximum peak output voltage per phase is:

$$V_{o,peak} = n \cdot V_{dc}$$

The RMS of the fundamental component of the phase voltage is given by:

$$V_{o,rms} = \frac{M \cdot n \cdot V_{dc}}{\sqrt{2}}$$

where M is the modulation index ($0 \leq M \leq 1$).

The line-to-line RMS voltage is:

$$V_{LL,rms} = \sqrt{3}\, V_{o,rms}$$

B. Output Current

Assuming a balanced load, the output current per phase is:

$$i_o(t) = I_{o,peak} \sin(\omega t - \varphi)$$

The RMS and peak values are related by:

$$I_{o,rms} = \frac{I_{o,peak}}{\sqrt{2}}$$

C. Power Equations

The real output power per phase is:

$$P_{out} = V_{o,rms} \cdot I_{o,rms} \cdot \cos(\varphi)$$

The apparent power is:

$$S = V_{o,rms} \cdot I_{o,rms}$$

and the power factor is:

$$\text{PF} = \cos(\varphi)$$

5.3 Modulation

PWM Principle

Cascaded H-bridge inverters commonly employ multicarrier PWM techniques such as:

- Level-Shifted PWM (LS-PWM)
- Phase-Shifted PWM (PS-PWM)

In LS-PWM, multiple carrier signals are vertically shifted, while in PS-PWM, they are phase-shifted by $\frac{180^\circ}{n}$ between adjacent cells.

Switching Frequency

Each H-bridge cell switches at a frequency f_s (typically 1–20 kHz), leading to an effective output switching frequency of $n \cdot f_s$ for the composite waveform.

Modulation Index

The modulation index is defined as the ratio of control to carrier signal amplitudes:

$$M = \frac{V_{control}}{V_{carrier}}$$

The output fundamental voltage is proportional to M:

$$V_{o,1} = M \cdot n \cdot \frac{V_{dc}}{2}$$

with $0 \leq M \leq 1$ to avoid overmodulation.

5.4 Harmonic Content

THD Formula

The Total Harmonic Distortion of the output voltage is given by:

$$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots}}{V_1} \times 100\%$$

Dominant Harmonics

For a properly modulated CHB inverter:

- Dominant harmonics appear around the carrier frequency and its multiples.
- Increasing the number of levels ($m = 2n + 1$) significantly reduces harmonic amplitude.

Effect of Switching Frequency

Higher switching frequency improves waveform quality (reduces THD) but increases switching losses. In CHB designs, moderate f_s values are preferred since harmonic suppression primarily depends on the number of voltage levels rather than high-frequency switching.

5.5 Loss Analysis

A. Conduction Losses

Each switch in the CHB inverter conducts during a portion of the fundamental period depending on the modulation scheme. The conduction loss per switch is expressed as:

$$P_{\text{cond,sw}} = I_{\text{rms,sw}}^2 \cdot R_{ds(on)}$$

where $I_{\text{rms,sw}}$ is the RMS current through the switch and $R_{ds(on)}$ is the ON-state resistance of the MOSFET or IGBT.

If freewheeling diodes are used, their conduction loss is:

$$P_{\text{cond,diode}} = V_F \cdot I_{\text{avg}} + r_D \cdot I_{\text{rms}}^2$$

where V_F is the diode forward voltage drop and r_D is its dynamic resistance.

The total conduction loss for an n-cell CHB inverter (each cell having 4 switches and 4 diodes) is:

$$P_{\text{cond,total}} = n\,(4P_{\text{cond,sw}} + 4P_{\text{cond,diode}})$$

B. Switching Losses

Each semiconductor experiences turn-on and turn-off switching transitions that dissipate energy per switching event. The total switching loss is given by:

$$P_{\text{sw}} = (E_{\text{on}} + E_{\text{off}}) \cdot f_s \cdot N_{\text{switches}}$$

where:

- $E_{\text{on}}, E_{\text{off}}$ are the turn-on and turn-off energy losses per switch.
- f_s is the switching frequency.
- $N_{\text{switches}} = 4n$ per phase for a single-phase CHB, or $12n$ for a three-phase CHB.

Dead-time effects: Dead-time is introduced between complementary switches to prevent short circuits in each leg. However, it introduces waveform distortion and affects the effective output voltage and THD, especially at light loads.

C. Filter Losses

Although the CHB inverter inherently produces a stepped waveform that reduces the need for bulky filters, small LC filters are often used to attenuate high-frequency harmonics.

Inductor losses:

$$P_{L,\text{DCR}} = I_{L,\text{rms}}^2 \cdot DCR_L$$

where DCR_L is the winding resistance of the output inductor.

Core losses are estimated using the generalized Steinmetz equation:

$$P_{\text{core}} = k \cdot f_s^{\alpha} \cdot B_{\text{max}}^{\beta} \cdot V_{\text{core}}$$

where k, α, and β are material-specific constants.

Capacitor ESR loss:

$$P_C = I_{C,\text{rms}}^2 \cdot ESR$$

The total filter loss is:

$$P_{\text{filter}} = P_{L,\text{DCR}} + P_{\text{core}} + P_C$$

D. Gate Drive Losses

Gate drivers supply charge to turn MOSFETs or IGBTs on and off. The total gate drive power is:

$$P_{\text{gate}} = Q_g \cdot V_{gs} \cdot f_s \cdot N_{\text{switches}}$$

where Q_g is the total gate charge and V_{gs} is the gate voltage swing.

E. Total Efficiency

The overall inverter efficiency accounting for conduction, switching, filter, and gate losses is:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{cond}} + P_{\text{sw}} + P_{\text{filter}} + P_{\text{gate}}} \times 100\%$$

Since CHB inverters distribute switching among multiple cells, each device experiences lower voltage and current stress, improving efficiency compared to two-level inverters.

5.6 Numerical example 6 cell Cascaded H-Bridge (three-phase)

Given / Assumptions:

- Number of cells per phase: $n = 6$.
- DC link per cell: $V_{dc} = 100$ V (each cell).
- Three-phase line-to-line RMS target: $V_{LL,\text{rms}} = 400$ V.
- Total three-phase output power: $P_{\text{out}} = 15$ kW (balanced, PF = 1).
- Switching frequency (per device): $f_s = 5$ kHz.
- Device parameters (per MOSFET/IGBT): $R_{ds(on)} = 20$ mΩ, $E_{on} = 50$ μJ, $E_{off} = 50$ μJ, $Q_g = 60$ nC, $V_{gs} = 12$ V.
- Filter / passive losses (estimate): $P_{\text{filter}} \approx 20$ W (total, all phases).
- Simple conduction/usage model: each semiconductor conducts, on average, 50% of the time (typical for complementary switching in H-bridges).
- All cells identical; every device is assumed to switch at f_s (conservative estimate).

Step 1 — Derived voltages and currents

Phase (phase-to-neutral) RMS fundamental:

$$V_{1,\text{rms}} = \frac{V_{LL,\text{rms}}}{\sqrt{3}} = \frac{400}{\sqrt{3}} \approx 230.94 \text{ V}.$$

Using the CHB relation (linear modulation):

$$V_{1,\text{rms}} = \frac{M\, n\, V_{dc}}{\sqrt{2}} \quad \Rightarrow \quad M = \frac{\sqrt{2}\, V_{1,\text{rms}}}{n\, V_{dc}}.$$

Numerically:

$$M = \frac{1.4142 \cdot 230.94}{6 \cdot 100} \approx 0.544.$$

(Linear region, $M \leq 1$, so SPWM operation is feasible.)

Per-phase power:

$$P_{\text{phase}} = \frac{P_{\text{out}}}{3} = \frac{15000}{3} = 5000 \text{ W}.$$

Phase current (RMS, PF = 1):

$$I_{1,\text{rms}} = \frac{P_{\text{phase}}}{V_{1,\text{rms}}} = \frac{5000}{230.94} \approx 21.64 \text{ A}.$$

Phase current peak:

$$I_{1,\text{peak}} = \sqrt{2}\, I_{1,\text{rms}} \approx 30.6 \text{ A}.$$

Step 2 — Conduction losses

Total number of semiconductor switches in the three-phase CHB:

$$N_{\text{sw,total}} = 12\, n = 12 \cdot 6 = 72.$$

Approximate per-device RMS current (each device carries the phase current when conducting):

$$I_{\text{rms,sw}} \approx I_{1,\text{rms}} \approx 21.64 \text{ A}.$$

Per-device conduction loss (average, assuming 50% conduction duty):

$$\overline{P}_{\text{cond,sw}} = 0.5 \cdot I_{\text{rms,sw}}^2\, R_{ds(on)} = 0.5 \cdot (21.64)^2 \cdot 0.02 \approx 4.69 \text{ W}.$$

Total switch conduction loss:

$$P_{\text{cond,sw,tot}} = N_{\text{sw,total}} \cdot \overline{P}_{\text{cond,sw}} = 72 \cdot 4.69 \approx 337.7 \text{ W}.$$

Estimate diode conduction loss (body/aux diodes, small extra loss). Assume diode contribution $\approx 5\%$ of switch conduction losses:

$$P_{\text{cond,diode,tot}} \approx 0.05 \cdot 337.7 \approx 16.9 \text{ W}.$$

Total conduction loss:

$$P_{\text{cond}} \approx 337.7 + 16.9 = 354.6 \text{ W}.$$

Step 3 — Switching losses

Per-device total switching energy per transition:

$$E_{sw} = E_{on} + E_{off} = 50\ \mu\text{J} + 50\ \mu\text{J} = 100\ \mu\text{J}.$$

Total switching devices $= N_{\text{sw,total}} = 72$.

Total switching loss:

$$P_{\text{sw}} = E_{sw} \cdot f_s \cdot N_{\text{sw,total}} = 100 \times 10^{-6} \cdot 5000 \cdot 72 = 36.0 \text{ W}.$$

Step 4 — Filter losses (given estimate)

$$P_{\text{filter}} \approx 20.0 \text{ W}.$$

Step 5 — Gate drive losses

Gate drive power (all devices):

$$P_{\text{gate}} = Q_g \cdot V_{gs} \cdot f_s \cdot N_{\text{sw,total}} = 60 \times 10^{-9} \cdot 12 \cdot 5000 \cdot 72 \approx 0.26 \text{ W}.$$

Step 6 — Sum losses and efficiency

Sum of losses:

$$P_{\text{losses}} = P_{\text{cond}} + P_{\text{sw}} + P_{\text{filter}} + P_{\text{gate}} \approx 354.6 + 36.0 + 20.0 + 0.26 \approx 410.9 \text{ W}.$$

Overall efficiency:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{losses}}} \times 100\% = \frac{15000}{15000 + 410.9} \times 100\% \approx 97.35\%.$$

Remarks and practical considerations

- The above calculation uses simplifying assumptions (every device switches at f_s, identical cells, 50% conduction duty per switch). In practice, phase-shifted carrier methods and level-sharing reduce harmonic content and can change per-device switching counts.
- The dominant loss term here is conduction loss (mainly because many devices conduct and device count is high). Per-device $R_{ds(on)}$ and device current strongly influence P_{cond} (scales with I^2).
- Switching losses remain moderate due to relatively small per-device switching energy assumed; selecting devices with lower E_{on}/E_{off} (and/or using soft-switching) further reduces P_{sw}.
- If a designer uses larger V_{dc} per cell or different modulation (SVPWM / selective harmonic elimination), the modulation index and currents change — recompute accordingly.
- For more accurate results, replace the per-device energy and conduction assumptions with device datasheet curves (E_{on}, E_{off} vs. V_{DC}, I) and run time-domain switching simulations (SPICE / PLECS / Simulink).

5.6.1 Design cheatsheet Cascaded H-Bridge (CHB), n cells per phase (quick reference)

Notation / parameters

- n : number of H-bridge cells per phase
- V_{dc} : DC-link voltage of each cell (assumed identical unless noted)
- $m = 2n + 1$: number of discrete output voltage levels per phase
- f_o : output (fundamental) frequency
- f_s : switching (carrier) frequency per cell
- M : modulation index (control amplitude / carrier amplitude)
- P_{out} : total three-phase output power (balanced)
- $V_{1,\text{rms}}$: phase (phase-to-neutral) fundamental RMS voltage
- $V_{LL,\text{rms}} = \sqrt{3}\, V_{1,\text{rms}}$: line-to-line RMS
- $I_{1,\text{rms}}$: phase RMS current

Fundamental relations (linear SPWM region)

$$m = 2n + 1 \tag{47}$$

$$V_{1,\text{peak}} = M \cdot n \cdot \frac{V_{dc}}{2} \quad \text{(common normalization)} \tag{48}$$

$$V_{1,\text{rms}} = \frac{V_{1,\text{peak}}}{\sqrt{2}} = \frac{M\, n\, V_{dc}}{2\sqrt{2}} \tag{49}$$

$$V_{LL,\text{rms}} = \sqrt{3}\, V_{1,\text{rms}} = \frac{M\, n\, V_{dc}\, \sqrt{3}}{2\sqrt{2}} \tag{50}$$

$$M = \frac{V_{\text{control}}}{V_{\text{carrier}}}, \qquad 0 \le M \le 1 \text{ (linear)} \tag{51}$$

Minimum DC per cell to achieve a required line voltage (for $M = 1$)

$$V_{dc,\text{min}} = \frac{2\sqrt{2}\, V_{1,\text{rms}}}{n} \quad \text{with } V_{1,\text{rms}} = \frac{V_{LL,\text{rms}}}{\sqrt{3}}.$$

(If V_{dc} chosen lower, either use over-modulation/SHE or increase n.)

Current and power

$$I_{1,\text{rms}} = \frac{P_{\text{phase}}}{V_{1,\text{rms}}} = \frac{P_{\text{out}}}{3\, V_{1,\text{rms}}} \tag{52}$$

$$P_{\text{out}} = 3\, V_{1,\text{rms}}\, I_{1,\text{rms}}\, \cos\varphi \tag{53}$$

$$S = 3\, V_{1,\text{rms}}\, I_{1,\text{rms}} \tag{54}$$

$$\text{PF} = \cos\varphi \tag{55}$$

Loss scaling and useful loss formulas (for quick estimates; replace with device/datasheet curves or sim results for final design)

$$P_{\text{cond,sw}} = I^2_{\text{rms,sw}}\, R_{ds(on)} \tag{56}$$

$$P_{\text{cond,diode}} = V_F\, I_{\text{avg}} + r_D\, I^2_{\text{rms}} \tag{57}$$

$$P_{\text{sw}} = (E_{on} + E_{off})\, f_s\, N_{\text{sw,total}} \tag{58}$$

$$P_{\text{gate}} = Q_g\, V_{gs}\, f_s\, N_{\text{sw,total}} \tag{59}$$

$$P_{L,\text{DCR}} = I^2_{L,\text{rms}}\, \text{DCR}_L \tag{60}$$

$$P_C = I^2_{C,\text{rms}}\, \text{ESR} \tag{61}$$

$$P_{\text{core}} = k\, f^{\alpha}\, B^{\beta}_{\text{pk}}\, V_{\text{core}} \quad \text{(Steinmetz)} \tag{62}$$

where $N_{\text{sw,total}}$ (three-phase) $= 12\, n$ (conservative upper bound).

Per-device duty and switching count notes

- With phase-shifted carriers (PS-PWM) each cell uses a carrier shifted by $360^\circ/n$, distributing switching events among cells and reducing spectral amplitude at lower orders.
- Effective per-device switching events per fundamental cycle differ with modulation method: account for reduced per-device switching when using PS-PWM or selective SHE. Conservative estimate: assume each device switches at f_s for power-loss upper bound.
- Typical per-device conduction duty depends on modulation and instantaneous phase; use time-domain integrals or simulation to obtain $I_{\text{rms,sw}}$ precisely.

Filter design (practical rules)

- **Cutoff frequency:** choose f_c such that

$$f_o \ll f_c \ll f_s.$$

  Practical guideline: $5f_o \lesssim f_c \lesssim f_s/10$ — tune to meet THD and dynamic response.

- **LC relation:** $f_c = \dfrac{1}{2\pi\sqrt{L\,C}}$.

- **Inductor ripple:** $\Delta I_L \approx \dfrac{V_{\text{step}}}{L\,f_s}$ where V_{step} is the maximum step amplitude seen by filter (choose conservative $V_{\text{step}} \approx n_{eff} V_{dc}$ or compute actual step sizes).

- Ensure inductor RMS rating includes ripple; choose core with low P_{core} at switching harmonics.

- Capacitors: ensure ESR and RMS current rating safe; size for acceptable voltage ripple and energy buffering during transients.

Cell and DC-source balancing (critical)

- Each cell DC source (cap or isolated supply) must be regulated or actively/passively balanced to prevent unequal voltages.

- For capacitor-based cells include balancing resistors, active balancing circuits, or control offsets to equalize voltages under mismatched loading.

- Monitor cell voltages and implement protection (OV/UV) per cell.

Control and modulation choices (recommendations)

- **Phase-Shifted PWM (PS-PWM):** easy to implement; distributes switching harmonics and reduces per-cell harmonic amplitude.

- **Level-Shifted PWM (LS-PWM):** straightforward; careful carrier arrangement reduces staircase steps.

- **Selective Harmonic Elimination (SHE):** for low switching frequency, compute switching angles to eliminate targeted harmonics — good for high-efficiency low-f_s designs.

- **Space-Vector / Advanced modulation:** beneficial for per-phase H-bridge cascades when using multilevel SVPWM formulations — improves DC utilization.

Protection, sensing and diagnostics

- Per-cell: DC-link over/under-voltage detection, temperature sensor, fuse or breaker.

- Per-leg: overcurrent (fast shunt or Rogowski), desaturation detection (IGBT) or MOSFET short detection.

- System: ground-fault detection, neutral current monitoring for triplen harmonics, cell voltage logging for predictive maintenance.

Thermal and packaging guidelines

- Compute per-device loss (conduction+switching+gate) and map to junction temperature rise using thermal resistance θ_{JC} and θ_{JA}; size heatsinks/airflow accordingly with 20–30% margin.
- Distribute power-dissipating devices to avoid thermal hotspots; consider staggered cell PCB layout for balanced cooling.

EMI / layout / snubbers

- Fast edges improve THD but increase EMI — use snubbers (RCD, RC) or RC+clamp only where needed.
- Careful PCB layout: minimize loop inductance of switching legs, provide low-impedance return paths, place gate drives close to devices, separate power and control grounds.
- Provide common-mode chokes and Y-capacitors as required by EMC standards.

Quick design checklist

1. Define specs: P_{out}, $V_{LL,\text{rms}}$, f_o, THD target, ambient/operating temperature.
2. Choose n such that V_{dc} practical and $M \leq 1$ (compute $V_{dc,\min}$). If higher amplitude needed, increase n.
3. Select semiconductors: check V_{ds} margin, $R_{ds(on)}$, E_{on}/E_{off} curves, Q_g, thermal limits.
4. Decide modulation: PS-PWM / LS-PWM / SHE / SVPWM depending on performance and complexity.
5. Design per-cell DC supply and balancing strategy.
6. Size filter (L, C) for THD spec and transient response.
7. Compute losses (per-device and system) and design thermal solution with margin.
8. Implement protections and per-cell monitoring.
9. Validate with time-domain switching simulation (include device datasheet switching energy curves, dead-time, parasitics) and prototype measurements.

Rules-of-thumb

- Increasing n reduces stepping amplitude and THD rapidly — doubling n roughly halves largest step size, improving waveform quality significantly.
- For given V_{dc} per cell, CHB provides higher DC utilization and lower per-device voltage stress vs two-level inverter.
- Conservative loss budgeting: assume each device switches at f_s and conducts worst-case RMS current for initial thermal sizing; refine with simulation.
- Target switching losses $\lesssim$ 10–30% of total losses for high-efficiency designs; if switching dominates, consider lower f_s or soft-switching.

6 Filter Design

In DC–AC converters, filters are essential to reduce high-frequency switching harmonics, improve power quality, and ensure compliance with grid or load standards. This section covers the design principles, typical configurations, and analytical equations for inverter output filters.

6.1 Objectives of Filter Design

The main objectives of designing an output filter are:

- Reduce Total Harmonic Distortion (THD) of the AC output waveform.
- Limit high-frequency ripple current to protect loads and improve efficiency.
- Ensure stable operation of the inverter and connected loads.
- Minimize size, weight, and cost while maintaining performance.

6.2 Types of Filters

6.2.1 Inductor Filter (L-Filter)

An inductor placed in series with the inverter output reduces high-frequency components:

$$L = \frac{V_{o,rms}}{4 f_s I_{o,rms} \cdot THD_{target}} \tag{63}$$

where f_s is the switching frequency, $I_{o,rms}$ is the load current, and THD_{target} is the desired total harmonic distortion.

6.2.2 Capacitor Filter (C-Filter)

A shunt capacitor can smooth voltage ripple:

$$C = \frac{I_{o,rms}}{2\pi f_o V_{ripple}} \tag{64}$$

where f_o is the output AC frequency and V_{ripple} is the maximum allowable voltage ripple.

6.2.3 LC Filter

An LC filter provides better attenuation of harmonics than L- or C-filters alone:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{65}$$

$$X_L = 2\pi f_o L \tag{66}$$

$$X_C = \frac{1}{2\pi f_o C} \tag{67}$$

where f_c is the filter cutoff frequency, chosen below the switching frequency but above the fundamental frequency.

6.2.4 LCL Filter (for Grid-Tied Inverters)

For three-phase grid-tied systems, LCL filters offer improved harmonic attenuation:

$$L_1 = \text{Inverter-side inductor} \tag{68}$$

$$L_2 = \text{Grid-side inductor} \tag{69}$$

$$C_f = \text{Shunt capacitor to suppress switching harmonics} \tag{70}$$

$$f_c = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{71}$$

A damping resistor R_d is often added in series with C_f to suppress resonance.

6.3 Design Considerations

- Filter components should handle peak currents and voltage stresses.
- High switching frequencies allow smaller filter components but may increase switching losses.
- Grid-tied applications may require active damping and careful resonance management.
- Component parasitics (ESR, ESL) significantly affect filter performance.

6.4 Example: Single-Phase LC Filter Design

Given:

- $V_{o,rms} = 230$ V
- $I_{o,rms} = 10$ A
- $f_o = 50$ Hz
- Switching frequency $f_s = 10$ kHz
- Target $THD = 5\%$

Select:

$$L = \frac{V_{o,rms}}{4 f_s I_{o,rms} THD} \approx 11.5 \text{ mH} \tag{72}$$

$$C = \frac{I_{o,rms}}{2\pi f_o V_{ripple}} \approx 100\ \mu\text{F} \tag{73}$$

This simple LC filter ensures that the output voltage harmonic content meets the design requirements while keeping components within practical size and cost limits.

6.5 Example Calculation: Single-Phase LC Filter Design

Consider a single-phase inverter with the following specifications:

- RMS output voltage: $V_{o,rms} = 230$ V
- RMS load current: $I_{o,rms} = 10$ A
- Output frequency: $f_o = 50$ Hz
- Switching frequency: $f_s = 10$ kHz
- Target Total Harmonic Distortion: $THD = 5\%$
- Maximum allowable voltage ripple: $V_{ripple} = 5$ V

6.5.1 Inductor Calculation

For an L-filter (series inductor), the approximate inductor value to achieve the desired THD is:

$$L = \frac{V_{o,rms}}{4 f_s I_{o,rms} \cdot THD} \tag{74}$$

Substitute the values:

$$\begin{aligned} L &= \frac{230}{4 \cdot 10{,}000 \cdot 10 \cdot 0.05} \\ L &= \frac{230}{20000} \\ L &\approx 11.5 \text{ mH} \end{aligned}$$

6.5.2 Capacitor Calculation

For the shunt capacitor in an LC filter, the required capacitance to limit voltage ripple is:

$$C = \frac{I_{o,rms}}{2\pi f_o V_{ripple}} \tag{75}$$

Substitute the values:

$$\begin{aligned} C &= \frac{10}{2\pi \cdot 50 \cdot 5} \\ C &= \frac{10}{1570.8} \\ C &\approx 6.36 \text{ mF} \end{aligned}$$

6.5.3 Filter Cutoff Frequency

The cutoff frequency of the LC filter is:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{76}$$

Substitute the calculated values:

$$\begin{aligned} f_c &= \frac{1}{2\pi\sqrt{0.0115 \cdot 0.00636}} \\ f_c &= \frac{1}{2\pi\sqrt{7.314 \times 10^{-5}}} \\ f_c &= \frac{1}{2\pi \cdot 0.00855} \\ f_c &\approx 18.6 \text{ Hz} \end{aligned}$$

6.5.4 Result and Discussion

- Series inductor: $L \approx 11.5$ mH
- Shunt capacitor: $C \approx 6.36$ mF
- Filter cutoff frequency: $f_c \approx 18.6$ Hz, safely below switching frequency and above fundamental frequency.

This LC filter design effectively reduces high-frequency harmonics from the inverter, achieving the desired $THD \leq 5\%$ while maintaining acceptable voltage ripple for the load.

Table 1: Filter Design Cheat Sheet for DC–AC Converters

Filter Type	**Configuration**	**Design Equations**	**Remarks / Typical Values**
L-Filter	Single-phase	$L = \frac{V_{o,rms}}{4 f_s I_{o,rms} \cdot THD}$	Series inductor; reduces current ripple
	Three-phase	$L = \frac{V_{o,rms}}{4 f_s I_{o,rms} \cdot THD}$	One inductor per phase; balanced load assumed
C-Filter	Single-phase	$C = \frac{I_{o,rms}}{2\pi f_o V_{ripple}}$	Shunt capacitor; reduces voltage ripple
	Three-phase	$C = \frac{I_{o,rms}}{2\pi f_o V_{ripple}}$	One capacitor per phase or Y-connected
LC-Filter	Single-phase	$f_c = \frac{1}{2\pi\sqrt{LC}}$	Cutoff frequency f_c should satisfy $f_o < f_c \ll f_s$
	Three-phase	$f_c = \frac{1}{2\pi\sqrt{LC}}$	Phase inductors + shunt capacitors
	n-level Cascaded H-Bridge	$L = \frac{V_{dc}}{4 f_s I_{o,rms} \cdot THD}$, $C = \frac{I_{o,rms}}{2\pi f_o V_{ripple}}$	Series LC per phase; scales with number of levels n
LCL-Filter	Three-phase grid-tied	$\begin{cases} f_c = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \\ R_d = \text{Damping resistor} \end{cases}$	Inverter-side L_1, grid-side L_2, shunt C_f; widely used for MV grid-connected inverters
Practical Considerations		Handle peak currents/voltages	Inductor saturation and capacitor voltage rating must be considered
		Component parasitics (ESR, ESL)	ESR increases losses; ESL affects high-frequency attenuation

Filter Design Cheat Sheet

Notes on Filter Design

- The cutoff frequency f_c should always be below the switching frequency f_s but above the fundamental f_o to maintain waveform quality.
- Increasing f_s allows smaller filter components but increases switching losses.
- For cascaded multilevel inverters, the voltage stress on each inductor and capacitor is reduced compared to single- or two-level inverters.
- LCL filters are preferred for grid-tied three-phase inverters because they provide better attenuation of high-frequency harmonics and comply with grid codes.

- Add damping resistors to suppress LCL resonance without significantly affecting fundamental output performance.

7 Conclusion

7.1 Selection Guide

- **Half-Bridge Inverter:** Suitable for low-power DC-AC conversion where cost and simplicity are key. Typically used in small UPS or DC supplies.
- **Full-Bridge Inverter:** Appropriate for medium-power single-phase applications (e.g., photovoltaic inverters, standalone UPS). Offers better voltage utilization and reduced harmonic distortion compared to Half-Bridge.
- **Three-Phase Inverter:** The preferred choice for motor drive and industrial applications requiring balanced three-phase AC output. Provides improved power delivery and efficiency.
- **Cascaded H-Bridge Inverter:** Ideal for modular, high-voltage, or renewable energy systems. Enables scalable voltage levels by increasing the number of H-bridge cells (n). Offers excellent waveform quality and high efficiency but requires isolated DC sources or complex balancing schemes.

7.2 Power Level and Cost Considerations

- **Low Power (< 1 kW):** Half-Bridge or Full-Bridge topologies are most cost-effective and simple to implement.
- **Medium Power (1–50 kW):** Three-Phase or NPC topologies provide good trade-offs between efficiency and THD.
- **High Power (> 50 kW):** Cascaded H-Bridge are preferred for their modularity, scalability, and low distortion.
- **Cost vs. Performance Trade-off:**
  - Simpler topologies (Half/Full-Bridge) $\Rightarrow$ Lower cost, higher THD.
  - Complex multilevel topologies (NPC, CHB) $\Rightarrow$ Higher cost, lower THD, better efficiency.

7.3 Final Remarks

Cascaded H-Bridge and NPC multilevel topologies represent the most promising solutions for high-efficiency and low-THD applications in renewable energy, motor drives, and grid-connected systems. The choice of inverter topology depends on power level, waveform quality requirements, and cost constraints.

7.4 Topology Comparison Table

Table 2: Comparison of inverter topologies

Topology	**Voltage Levels**	**Efficiency (%)**	**THD**	**Complexity**	**Applications**
Half-Bridge	2	∼92	High	Low	Low-power DC/AC conversion
Full-Bridge	2	∼94	Medium	Medium	UPS, Solar inverter systems
Three-Phase	2	∼96	Medium	Medium	Motor drives, Industrial systems
Cascaded H-Bridge (n cells)	$2n+1$	∼97–98	Very Low	High	Renewable, HV applications, EV drives

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