Design of Power Electronics Converters

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Abstract

This document presents a comprehensive study of DC–DC power converters, ranging from classical non-isolated topologies (Buck, Boost, Buck–Boost, SEPIC, Ćuk, Zeta) to isolated structures (Flyback, Forward, Push–Pull, Half-Bridge, Full-Bridge, Z-Source, and Multiport architectures). For each converter, the operating principles, key waveforms, voltage transfer ratios, and small-signal models are derived and detailed. Step-by-step design equations are included to guide practical implementation, covering inductor and capacitor sizing, transformer design (for isolated cases), and loss mechanisms such as switching, conduction, and core losses.

Special emphasis is placed on thermal considerations, efficiency optimization, and trade-offs between different topologies. Comparative tables summarize the performance of each converter in terms of polarity, voltage range, isolation, efficiency, and application domains, providing a clear selection framework for engineers.

The work concludes with a unified comparison and practical design insights, making the document a useful reference for students, researchers, and practicing engineers involved in power electronics design and renewable energy systems.

Contents

1 Problem statement and design specifications for Boost converter

Design a non-isolated boost converter with the following target specifications (numerical example will follow in Section 16):

- Input voltage range: $V_{\text{in,min}}$ to $V_{\text{in,max}}$ (V)
- Output voltage: V_o (V)
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Output voltage ripple (peak-to-peak): ΔV_o (V)
- Inductor current ripple (peak-to-peak): ΔI_L (A)
- Continuous conduction mode (CCM) operation

2 Fundamental principles and steady-state derivation

2.1 Circuit description

The ideal boost converter (see Fig. 1) consists of an input source V_{in}, an inductor L, a switch (ideal MOSFET) S, a diode D, an output capacitor C, and load R_{load}.

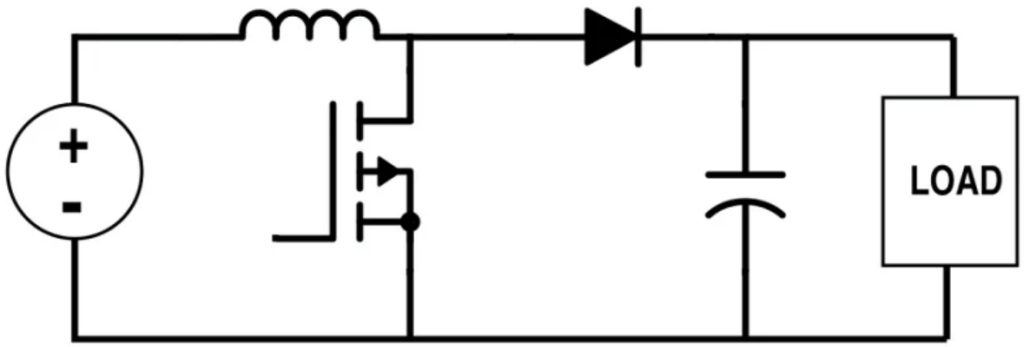

Figure 1: Ideal non-isolated boost converter.

2.2 Steady-state volt-second balance on the inductor

In CCM, the inductor current never falls to zero. Let D denote the duty ratio (fraction of switching period $T_s = 1/f_s$ during which the switch S is ON). There are two intervals:

1. $0 \le t < DT_s$: switch S closed (ON). Inductor sees $V_L^{(\text{ON})} = V_{\text{in}}$.
2. $DT_s \le t < T_s$: switch S open (OFF). Inductor sees $V_L^{(\text{OFF})} = V_{\text{in}} - V_o$ (assuming ideal diode with zero drop).

By volt-second balance for steady-state (average $\Delta\Phi$ over one period zero),

$$\int_0^{T_s} v_L(t)\,dt = 0 \tag{1}$$

$$V_{\text{in}}(DT_s) + (V_{\text{in}} - V_o)((1-D)T_s) = 0. \tag{2}$$

Divide Eq. (2) by T_s to obtain average:

$$DV_{\text{in}} + (1-D)(V_{\text{in}} - V_o) = 0. \tag{3}$$

Expand and rearrange:

$$DV_{\text{in}} + (1-D)V_{\text{in}} - (1-D)V_o = 0 \tag{4}$$

$$V_{\text{in}} - (1-D)V_o = 0 \tag{5}$$

$$V_{\text{in}} = (1-D)V_o. \tag{6}$$

Hence the ideal boost steady-state relationship (solving for V_o):

$$V_o = \frac{V_{\text{in}}}{1-D}. \tag{7}$$

Dimensional check: both sides in volts (V). Eq. (7) is valid for $0 \le D < 1$.

3 Inductor current ripple and capacitor sizing

3.1 Inductor ripple

During the ON interval, $v_L = V_{\text{in}}$, so the slope of inductor current is

$$\left.\frac{di_L}{dt}\right|_{\text{ON}} = \frac{V_{\text{in}}}{L}. \tag{8}$$

Over the ON interval DT_s, the inductor current increases by

$$\Delta i_{L,\text{ON}} = \frac{V_{\text{in}}}{L} DT_s. \tag{9}$$

During the OFF interval, $v_L = V_{\text{in}} - V_o = V_{\text{in}} - \dfrac{V_{\text{in}}}{1-D} = -\dfrac{D\,V_{\text{in}}}{1-D}$, so

$$\left.\frac{di_L}{dt}\right|_{\text{OFF}} = \frac{V_{\text{in}} - V_o}{L} = -\frac{D\,V_{\text{in}}}{(1-D)\,L}. \tag{10}$$

Over the OFF interval $(1-D)T_s$, the decrease is

$$\Delta i_{L,\text{OFF}} = -\frac{D\,V_{\text{in}}}{(1-D)\,L}(1-D)T_s = -\frac{D\,V_{\text{in}}}{L} T_s. \tag{11}$$

As expected, $\Delta i_{L,\text{ON}} + \Delta i_{L,\text{OFF}} = 0$ in steady state. The peak-to-peak inductor ripple is therefore

$$\Delta I_L = \Delta i_{L,\text{ON}} = \frac{V_{\text{in}}}{L} DT_s = \frac{V_{\text{in}}}{L}\frac{D}{f_s}. \tag{12}$$

Solve for required inductance given desired ΔI_L:

$$L = \frac{V_{\text{in}}}{\Delta I_L}\frac{D}{f_s}. \tag{13}$$

Units: $V/(A) \times (\text{s}) = \text{H}$ as required.

3.2 Capacitor ripple and size

Assume the output capacitor supplies the AC portion of the load current during the switching interval. The average output current is

$$I_o = \frac{P_o}{V_o} = \frac{V_o}{R_{\text{load}}}. \tag{14}$$

For large C and small ripple, approximate triangular capacitor current with amplitude equal to inductor ripple carried into capacitor during OFF time (when diode conducts). The capacitor voltage change during the interval where capacitor supplies net current Δi_C over a duration τ satisfies

$$\Delta V_o = \frac{1}{C}\int i_C(t)\,dt. \tag{15}$$

A conservative approximate sizing (rms/pp analysis) for peak-to-peak voltage ripple ΔV_o is

$$C = \frac{\Delta I_C}{8 f_s \Delta V_o}, \tag{16}$$

where $\Delta I_C \approx \Delta I_L(1-D)$ is the triangular capacitor current amplitude seen during conduction intervals. Substituting,

$$C \approx \frac{\Delta I_L (1-D)}{8 f_s \Delta V_o}. \tag{17}$$

This formula arises from integrating a triangular waveform: the peak-to-peak voltage over half the switching period equals area of triangle divided by C; detailed derivation is given in Appendix **??**.

4 State-space averaging in CCM

We derive the averaged state-space model using state vector $\mathbf{x} = \begin{bmatrix} i_L & v_C \end{bmatrix}^T$ and input $u = V_{\text{in}}$. The two switching subintervals have linear dynamics.

4.1 ON state (S closed)

KCL/KVL yield

$$\frac{di_L}{dt} = \frac{1}{L} V_{\text{in}} \tag{18}$$

$$\frac{dv_C}{dt} = \frac{1}{C}(i_L - i_o), \tag{19}$$

where $i_o = v_C / R_{\text{load}}$. In matrix form:

$$\dot{\mathbf{x}} = A_{\text{ON}}\mathbf{x} + B_{\text{ON}} u, \qquad A_{\text{ON}} = \begin{bmatrix} 0 & 0 \\ 1/C & -1/(R_{\text{load}}C) \end{bmatrix}, \quad B_{\text{ON}} = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}. \tag{20}$$

4.2 OFF state (S open)

When switch is open, diode conducts and inductor is connected to C and R_{load}. KVL/KCL:

$$\frac{di_L}{dt} = \frac{1}{L}(V_{\text{in}} - v_C) \tag{21}$$

$$\frac{dv_C}{dt} = \frac{1}{C}(i_L - i_o). \tag{22}$$

Matrix form:

$$\dot{\mathbf{x}} = A_{\text{OFF}}\mathbf{x} + B_{\text{OFF}} u, \qquad A_{\text{OFF}} = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/(R_{\text{load}}C) \end{bmatrix}, \quad B_{\text{OFF}} = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}. \tag{23}$$

4.3 Averaged model

Averaging over one switching period with duty cycle D yields

$$A_{\text{ave}} = D A_{\text{ON}} + (1-D) A_{\text{OFF}} \tag{24}$$

$$B_{\text{ave}} = D B_{\text{ON}} + (1-D) B_{\text{OFF}}. \tag{25}$$

Substitute Eqs. (20) and (23):

$$A_{\text{ave}} = \begin{bmatrix} 0 & -(1-D)/L \\ 1/C & -1/(R_{\text{load}}C) \end{bmatrix}, \qquad B_{\text{ave}} = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}. \tag{26}$$

So the averaged continuous-time model is

$$\dot{\mathbf{x}} = A_{\text{ave}}\mathbf{x} + B_{\text{ave}} u. \tag{27}$$

5 Component selection: algorithmic procedure

A compact algorithm:

1. Choose switching frequency f_s based on trade-off between size and switching loss.
2. For worst-case $V_{\text{in,min}}$ and desired V_o, compute duty D from Eq. (7).
3. Select allowable inductor ripple ΔI_L (e.g., 20–40% of average inductor current) and compute L from Eq. (13).
4. Select capacitor to meet ΔV_o via Eq. (17) and verify RMS current rating.
5. Select MOSFET and diode: consider worst-case voltages and currents, thermal limits, switching energy E_{on}, E_{off}, diode reverse recovery for hard-switching.
6. Compute losses and iterate to meet thermal/efficiency targets.

6 Loss Models and Thermal Considerations

In practical converter design, idealized assumptions of lossless components must be replaced by detailed loss models in order to predict efficiency, ensure device reliability, and design the thermal management system. This section develops rigorous expressions for the dominant power loss mechanisms in a boost converter and then couples them with thermal models for device junction temperature prediction.

6.1 Conduction Losses in Semiconductor Devices

MOSFET conduction loss: When the MOSFET is conducting, the dominant loss is ohmic conduction through its channel resistance $R_{\text{DS(on)}}$. Assuming *continuous conduction mode (CCM)* with average inductor current I_L and ripple ΔI_L, the RMS current through the MOSFET during the ON interval is

$$I^2_{\text{MOSFET,rms}} = \frac{1}{T_s}\int_0^{DT_s} i_L^2(t)\,dt. \tag{28}$$

Approximating $i_L(t)$ as a triangular ripple around average $I_{L,\text{avg}} = I_o/(1-D)$, the closed-form evaluation gives

$$I^2_{\text{MOSFET,rms}} = D\left(I^2_{L,\text{avg}} + \frac{(\Delta I_L)^2}{12}\right). \tag{29}$$

Hence, the conduction loss is

$$P_{\text{cond,MOS}} = I^2_{\text{MOSFET,rms}}\, R_{\text{DS(on)}}. \tag{30}$$

Diode conduction loss: When the MOSFET is OFF, the diode conducts the inductor current. The loss mechanism is dominated by forward voltage drop V_f:

$$P_{\text{cond,D}} = V_f \cdot I_{D,\text{avg}} = V_f \cdot (1-D) I_{L,\text{avg}}. \tag{31}$$

If a Schottky diode is used, V_f is relatively constant. For a silicon PN diode, V_f exhibits temperature dependence: $V_f(T) = V_{f0} - k(T - T_0)$ with $k \approx 2\,\text{mV/°C}$.

6.2 Switching Losses

MOSFET switching: Each switching event involves overlap of voltage and current. For turn-on:

$$E_{\text{on}} \approx \tfrac{1}{2} V_{DS} I_D(t_r), \tag{32}$$

and for turn-off:

$$E_{\text{off}} \approx \tfrac{1}{2} V_{DS} I_D(t_f), \tag{33}$$

where t_r and t_f are rise and fall times, respectively. Total switching loss is

$$P_{\text{sw}} = f_s \left(E_{\text{on}} + E_{\text{off}} \right). \tag{34}$$

A more accurate model includes parasitic capacitances (C_{oss}, C_{rss}) and gate-driver resistance. For instance, capacitive discharging of C_{oss} contributes

$$E_{C_{oss}} = \tfrac{1}{2} C_{oss} V_{DS}^2, \tag{35}$$

per cycle.

Diode reverse-recovery: When the diode turns off, stored charge Q_{rr} causes a reverse current spike. The associated energy loss per switching event is

$$E_{rr} \approx Q_{rr} \cdot V_{DS}, \tag{36}$$

giving

$$P_{rr} = f_s Q_{rr} V_{DS}. \tag{37}$$

6.3 Magnetic and Passive Losses

Inductor copper loss:

$$P_{\text{cu}} = I_{L,\text{rms}}^2 \cdot R_w(f), \tag{38}$$

where $R_w(f)$ accounts for DC resistance and high-frequency skin & proximity effects. Analytical correction factors are obtained from Dowell's equations.

Inductor core loss: The generalized Steinmetz equation (GSE) gives

$$P_{\text{core}} = k \, f^{\alpha} \, B_{\text{pk}}^{\beta} V_{\text{core}}, \tag{39}$$

where parameters k, α, β are material-dependent, B_{pk} is peak flux density, and V_{core} is the core volume.

Capacitor ESR loss: The RMS ripple current through the capacitor $I_{C,\text{rms}}$ produces

$$P_{\text{cap}} = I_{C,\text{rms}}^2 \cdot R_{\text{ESR}}. \tag{40}$$

6.4 Total Loss Model

Combining all terms:

$$P_{\text{loss}} = P_{\text{cond,MOS}} + P_{\text{cond,D}} + P_{\text{sw}} + P_{rr} + P_{\text{cu}} + P_{\text{core}} + P_{\text{cap}}. \tag{41}$$

The efficiency is

$$\eta = \frac{P_o}{P_o + P_{\text{loss}}}, \tag{42}$$

with $P_o = V_o I_o$.

6.5 Thermal Considerations

Junction temperature rise: Device temperature rise is modeled with a thermal resistance network. For a MOSFET with junction-to-case θ_{JC}, case-to-sink θ_{CS}, and sink-to-ambient θ_{SA},

$$T_j = T_a + P_{\text{MOSFET}} \cdot (\theta_{JC} + \theta_{CS} + \theta_{SA}), \tag{43}$$

where T_a is ambient temperature.

Transient thermal impedance: For pulsed operation, transient thermal impedance $Z_\theta(t)$ describes the dynamic junction response:

$$\Delta T_j(t) = P(t) * Z_\theta(t), \tag{44}$$

where $*$ denotes convolution. Manufacturers often provide $Z_\theta(t)$ curves for accurate junction prediction under varying load profiles.

Design margins: To ensure reliability, T_j must remain below the rated maximum (often 150°C). A common design margin is to limit T_j to 125°C at worst-case operating conditions.

6.6 Numerical Example

Consider a boost converter with:

$$\begin{aligned} V_{in} &= 12\,\text{V}, & V_o &= 24\,\text{V}, & P_o &= 50\,\text{W}, \\ f_s &= 100\,\text{kHz}, & R_{\text{DS(on)}} &= 50\,\text{m}\Omega, & V_f &= 0.5\,\text{V}, \\ Q_{rr} &= 20\,\text{nC}, & C_{oss} &= 200\,\text{pF}, & \theta_{JA} &= 40^\circ\text{C/W}. \end{aligned}$$

Step 1: Output current

$$I_o = \frac{P_o}{V_o} = \frac{50}{24} \approx 2.083\,\text{A}.$$

Step 2: Inductor average current

$$I_{L,\text{avg}} = \frac{I_o}{1-D}, \quad D = 1 - \frac{V_{in}}{V_o} = 1 - \frac{12}{24} = 0.5.$$

Hence $I_{L,\text{avg}} = 4.166\,\text{A}$.

Step 3: MOSFET conduction loss Approximating $\Delta I_L = 0.5\,\text{A}$,

$$I^2_{\text{MOSFET,rms}} = 0.5\left(4.166^2 + \frac{0.5^2}{12}\right) = 8.68, \quad I_{\text{MOSFET,rms}} = 2.95\,\text{A}.$$

Thus

$$P_{\text{cond,MOS}} = (2.95^2)(0.05) \approx 0.43\,\text{W}.$$

Step 4: Diode conduction loss

$$P_{\text{cond,D}} = V_f(1-D)I_{L,\text{avg}} = 0.5 \times 0.5 \times 4.166 \approx 1.04\,\text{W}.$$

Step 5: MOSFET switching loss Assuming $t_r = t_f = 30\,\text{ns}$ and $V_{DS} = 24\,\text{V}$, $I_D \approx 4.166\,\text{A}$,

$$E_{\text{on}} = E_{\text{off}} = \tfrac{1}{2}(24)(4.166)(30 \times 10^{-9}) = 1.5 \times 10^{-6}\,\text{J}.$$

So per cycle $E_{\text{sw}} = 3.0 \times 10^{-6}\,\text{J}$. At $f_s = 100\,\text{kHz}$,

$$P_{\text{sw}} = 0.3\,\text{W}.$$

Step 6: Diode reverse recovery

$$P_{rr} = f_s Q_{rr} V_{DS} = 100 \times 10^3 \times 20 \times 10^{-9} \times 24 = 0.048\,\text{W}.$$

Step 7: Capacitive switching loss

$$P_{Coss} = \tfrac{1}{2} C_{oss} V_{DS}^2 f_s = 0.5 \times 200 \times 10^{-12} \times (24)^2 \times 100 \times 10^3 = 0.058\,\text{W}.$$

Step 8: Total semiconductor losses

$$P_{\text{MOSFET}} = 0.43 + 0.3 + 0.058 = 0.788\,\text{W}, \quad P_{\text{Diode}} = 1.04 + 0.048 = 1.088\,\text{W}.$$

Step 9: Efficiency

$$P_{\text{loss}} \approx 1.876\,\text{W}, \quad \eta = \frac{50}{50 + 1.876} \approx 96.4\%.$$

Step 10: Junction temperature With $\theta_{JA} = 40°\text{C/W}$,

$$\Delta T_j = 0.788 \times 40 = 31.5°\text{C}.$$

At $T_a = 40°\text{C}$, $T_j \approx 71.5°\text{C}$, which is safe.

7 Numerical example

We now work a fully detailed numerical example with every step shown.

7.1 Specifications

Assume the following:

$$\begin{aligned} V_{\text{in}} &= 24\,\text{V} \\ V_o &= 48\,\text{V} \\ P_o &= 200\,\text{W} \\ f_s &= 100\,\text{kHz} \\ \Delta V_o &= 0.48\,\text{V} \quad (1\%\text{ pp}) \\ \Delta I_L \text{ target} &= 0.3\,\bar{I}_L \quad (30\%\text{ pp}) \end{aligned}$$

7.2 Compute duty cycle

From Eq. (7), solve for D:

$$V_o = \frac{V_{\text{in}}}{1 - D} \Rightarrow 1 - D = \frac{V_{\text{in}}}{V_o} \tag{45}$$

$$D = 1 - \frac{V_{\text{in}}}{V_o} = 1 - \frac{24}{48} = 1 - 0.5 = 0.5. \tag{46}$$

So $D = 0.5$ (dimensionless).

7.3 Output current and average inductor current

Output current:

$$I_o = \frac{P_o}{V_o} = \frac{200}{48} = 4.1666667\text{ A}. \tag{47}$$

Average inductor current (power balance: $P_{in} = P_o$ ideal)

$$\bar{I}_L = \frac{I_o}{1 - D} = \frac{4.1666667}{1 - 0.5} = \frac{4.1666667}{0.5} = 8.3333334\text{ A}. \tag{48}$$

7.4 Inductance selection

Target peak-to-peak inductor ripple $\Delta I_L = 0.3\bar{I}_L = 0.3 \times 8.3333334 = 2.5$ A. Using Eq. (13):

$$L = \frac{V_{\text{in}}}{\Delta I_L}\frac{D}{f_s} = \frac{24}{2.5}\frac{0.5}{100 \times 10^3}\ \text{H}. \tag{49}$$

Compute numerically:

$$\frac{24}{2.5} = 9.6\ \text{V A}^{-1}$$
$$\frac{0.5}{100 \times 10^3} = 5 \times 10^{-6}\ \text{s}$$
$$L = 9.6 \times 5 \times 10^{-6} = 48 \times 10^{-6} = 48\ \mu\text{H}.$$

Dimensional check: $\text{V/A} \cdot \text{s} = \text{H}$.

7.5 Capacitance selection

Using Eq. (17). First compute $1 - D = 0.5$ and $\Delta I_L(1 - D) = 2.5 \times 0.5 = 1.25$ A. Then

$$C \approx \frac{\Delta I_L(1 - D)}{8 f_s \Delta V_o} = \frac{1.25}{8 \times 100 \times 10^3 \times 0.48}\ \text{F}. \tag{50}$$

Compute stepwise:

$$8 \times 100 \times 10^3 \times 0.48 = 8 \times 100000 \times 0.48 = 800000 \times 0.48 = 384000$$
$$C = \frac{1.25}{384000} = 3.2552083 \times 10^{-6}\ \text{F} = 3.26\ \mu\text{F}.$$

Choose a practical capacitance (accounting for ESR and derating) e.g., $C = 10\,\mu$F with low ESR to ensure ripple and lifetime.

7.6 Verification of CCM

Minimum inductor current is $I_{L,\min} = \bar{I}_L - \Delta I_L/2 = 8.3333334 - 1.25 = 7.0833334\ \text{A} > 0$, thus CCM holds.

7.7 Estimate component ratings

MOSFET peak voltage: During OFF, MOSFET sees output voltage reflected: $V_{DS,\max} \approx V_o = 48\,\text{V}$. Add margin (e.g., 25%), select 80–100 V device.

Inductor RMS current: Approximate $I_{L,\text{rms}} \approx \sqrt{\bar{I}_L^2 + (\Delta I_L)^2/12}$ for triangular ripple:

$$I_{L,\text{rms}} = \sqrt{8.3333334^2 + (2.5)^2/12} = \sqrt{69.444444 + 0.5208333}$$
$$= \sqrt{69.965277} = 8.366\ \text{A}.$$

8 Practical considerations and next steps

- Refine magnetics: core selection, winding resistance, copper loss, skin/proximity effects at 100 kHz.
- Calculate switching losses using MOSFET datasheet E_{on}, E_{off} at chosen V_{DS} and I; iterate f_s if losses excessive.
- Perform thermal network calculation using $R_{\theta JA}$ or heatsink data and ensure junction temperature limits.

- Design gate drive and snubber/clamping for safe operation and EMI mitigation.
- Simulate the full nonlinear switching model in SPICE/PLECS and extract small-signal frequency response to design compensator (e.g., Type-III for voltage-mode).

9 Design Procedure — Essential Equations (A–Z)

$$\text{Duty:} \qquad D \;=\; 1 - \frac{V_{\text{in}}}{V_o} \tag{A}$$

$$\text{Output current:} \qquad I_o \;=\; \frac{P_o}{V_o} \tag{B}$$

$$\text{Avg. inductor current (power balance):} \qquad \bar{I}_L \;=\; \frac{I_o}{1-D} \tag{C}$$

$$\text{Inductor peak-to-peak ripple:} \qquad \Delta I_L \;=\; \frac{V_{\text{in}}\, D}{L\, f_s} \tag{D}$$

$$\text{Inductance selection:} \qquad L \;=\; \frac{V_{\text{in}}\, D}{\Delta I_L\, f_s} \tag{E}$$

$$\text{Inductor extrema:} \qquad I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2}, \quad I_{L,\max} = \bar{I}_L + \frac{\Delta I_L}{2} \tag{F}$$

$$\text{Capacitance (triangular approx, } \Delta i_C \approx \Delta I_L(1-D)\text{):} \qquad C \;\approx\; \frac{\Delta I_L (1-D)}{8\, f_s\, \Delta V_o} \tag{G}$$

$$\text{Approx. capacitor RMS current:} \qquad I_{C,\text{rms}} \approx \frac{\Delta I_L (1-D)}{2\sqrt{3}} \tag{H}$$

$$\text{Inductor RMS (triangular ripple):} \qquad I_{L,\text{rms}}^2 \;=\; \bar{I}_L^2 + \frac{(\Delta I_L)^2}{12} \tag{I}$$

$$\text{MOSFET rms during ON interval:} \qquad I_{\text{MOS,rms}}^2 \;=\; D\left(\bar{I}_L^2 + \frac{(\Delta I_L)^2}{12}\right) \tag{J}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,MOS}} \;=\; I_{\text{MOS,rms}}^2\, R_{\text{DS(on)}} \tag{K}$$

$$\text{MOSFET switching loss (approx.):} \qquad P_{\text{sw}} \;=\; f_s\,(E_{\text{on}} + E_{\text{off}}) \;+\; \tfrac{1}{2} C_{\text{oss}} V_{DS}^2 f_s \tag{L}$$

$$\text{Diode average current:} \qquad I_{D,\text{avg}} \;=\; (1-D)\,\bar{I}_L \tag{M}$$

$$\text{Diode conduction loss:} \qquad P_{\text{cond,D}} \;=\; V_f\, I_{D,\text{avg}} \tag{N}$$

$$\text{Diode reverse-recovery loss:} \qquad P_{rr} \;=\; f_s\, Q_{rr}\, V_{DS} \tag{O}$$

$$\text{Capacitor ESR loss:} \qquad P_{\text{cap,ESR}} \;=\; I_{C,\text{rms}}^2\, R_{\text{ESR}} \tag{P}$$

$$\text{Magnetic core loss (generalized Steinmetz):} \qquad P_{\text{core}} \;=\; k\, f_s^{\alpha}\, B_{\text{pk}}^{\beta}\, V_{\text{core}} \tag{Q}$$

$$\text{Peak flux density (inductor, ON interval):} \qquad B_{\text{pk}} \;=\; \frac{V_{L,\text{ON}}\, D}{N\, A_e\, f_s} \quad \text{where } V_{L,\text{ON}} = V_{\text{in}} \tag{R}$$

Inductance vs. turns and core geometry: $$L = N^2 \frac{\mu_0 \mu_r A_e}{\ell_e} \quad \Rightarrow \quad N = \sqrt{\frac{L\,\ell_e}{\mu_0 \mu_r A_e}} \tag{S}$$

Winding DC resistance: $$R_{w,\mathrm{DC}} = \rho \frac{\ell_\mathrm{w}}{A_\mathrm{cu}} \quad \text{(use ac correction factor } k_\mathrm{ac}(f) \text{ for skin/prox)} \tag{T}$$

Junction temperature (steady): $$T_j = T_a + P_\mathrm{device}\,\theta_{JA} \tag{U}$$

Transient junction rise: $$\Delta T_j(t) = P(t) * Z_\theta(t) \quad \text{(convolution with transient thermal impedance)} \tag{V}$$

Efficiency: $$\eta = \frac{P_o}{P_o + P_\mathrm{loss}} \quad \text{with } P_\mathrm{loss} = \sum \text{(all losses)} \tag{W}$$

Voltage-rating margin (device selection): $$V_{DS,\max} \geq (1 + \mathrm{M}_v)\, V_o \quad \text{(choose } \mathrm{M}_v = 0.2\text{–}0.5 \text{ typical)} \tag{X}$$

$\mathrm{R}_{\mathrm{DS(on)}}$ temperature dependence: $$R_{\mathrm{DS(on)}}(T) = R_{\mathrm{DS(on)},25°C}\big[1 + \alpha_R(T_j - 25°\mathrm{C})\big] \tag{Y}$$

Notes: these equations give the minimal algebraic toolbox for design: choose f_s, pick ΔI_L (fraction of $\bar{I}_L$), compute L (E), use (G) to size C (include ESR term P), compute RMS currents (I,H,J) for copper/semiconductor selection, estimate switching losses (L,O) for thermal design (U,V), then iterate geometry (S,T,R,Q) to meet core loss and thermal budgets; finally use (Z) to design loop compensation.

10 Problem statement and design specifications for Buck converter

Design a non-isolated buck converter with the following target specifications (numerical example will follow in Section 16):

- Input voltage range: $V_{\mathrm{in,min}}$ to $V_{\mathrm{in,max}}$ (V)
- Output voltage: V_o (V)
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Output voltage ripple (peak-to-peak): ΔV_o (V)
- Inductor current ripple (peak-to-peak): ΔI_L (A)
- Continuous conduction mode (CCM) operation

11 Fundamental principles and steady-state derivation

11.1 Circuit description

The ideal buck converter (see Fig. 2) consists of an input source V_in, a high-side switch S (MOSFET), a diode D (or synchronous low-side MOSFET), an inductor L, an output capacitor C, and load R_load.

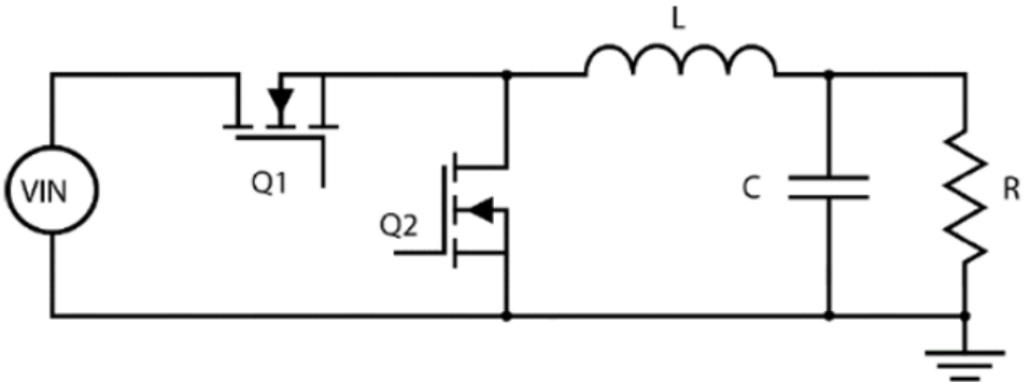

Figure 2: Ideal non-isolated buck converter.

11.2 Steady-state volt-second balance on the inductor

In CCM the inductor current never falls to zero. Let D denote the duty ratio (fraction of switching period $T_s = 1/f_s$ during which the high-side switch S is ON). Two subintervals:

1. $0 \le t < DT_s$: switch S closed (ON). Inductor sees $V_L^{(\mathrm{ON})} = V_{\mathrm{in}} - V_o$.
2. $DT_s \le t < T_s$: switch S open (OFF). Inductor sees $V_L^{(\mathrm{OFF})} = -V_o$ (assuming ideal diode with zero drop).

Volt-second balance (average inductor voltage over T_s is zero):

$$\int_0^{T_s} v_L(t)\,dt = 0 \tag{51}$$

$$(V_{\mathrm{in}} - V_o)(DT_s) + (-V_o)((1-D)T_s) = 0. \tag{52}$$

Divide Eq. (52) by T_s:

$$D(V_{\mathrm{in}} - V_o) - (1-D)V_o = 0. \tag{53}$$

Rearrange (showing intermediate steps):

$$\begin{aligned} DV_{\mathrm{in}} - DV_o - V_o + DV_o &= 0 \\ DV_{\mathrm{in}} - V_o &= 0 \\ V_o &= D\,V_{\mathrm{in}}. \end{aligned} \tag{54}$$

Dimensionally consistent: volts = unitless × volts. Valid for $0 \le D \le 1$.

12 Inductor current ripple and capacitor sizing

12.1 Inductor ripple

During ON interval:

$$\left.\frac{di_L}{dt}\right|_{\mathrm{ON}} = \frac{V_{\mathrm{in}} - V_o}{L}. \tag{55}$$

Increase over DT_s:

$$\Delta i_{L,\mathrm{ON}} = \frac{V_{\mathrm{in}} - V_o}{L} DT_s. \tag{56}$$

During OFF interval:

$$\left.\frac{di_L}{dt}\right|_{\mathrm{OFF}} = -\frac{V_o}{L}. \tag{57}$$

Decrease over $(1-D)T_s$:

$$\Delta i_{L,\mathrm{OFF}} = -\frac{V_o}{L}(1-D)T_s. \tag{58}$$

Steady-state $\Delta i_{L,\mathrm{ON}} + \Delta i_{L,\mathrm{OFF}} = 0$. Peak-to-peak ripple:

$$\Delta I_L = \Delta i_{L,\mathrm{ON}} = \frac{(V_{\mathrm{in}} - V_o)D}{L f_s}. \tag{59}$$

Solve for L given desired ΔI_L:

$$L = \frac{(V_{\mathrm{in}} - V_o)D}{\Delta I_L f_s}. \tag{60}$$

Units: $(\mathrm{V} \cdot \mathrm{s})/\mathrm{A} = \mathrm{H}$.

12.2 Capacitor ripple and size

Average output current:

$$I_o = \frac{P_o}{V_o} = \frac{V_o}{R_{\mathrm{load}}}. \tag{61}$$

Under small-ripple assumption, capacitor current is approximately the negative high-frequency part of $i_L(t)$ and for the buck $\Delta i_C \approx \Delta I_L$ (full triangular seen by C). Using the triangular integral (see Appendix if needed), the peak-to-peak voltage ripple is:

$$\Delta V_o \approx \frac{\Delta I_L}{8\, C\, f_s}. \tag{62}$$

Solving for C:

$$C \approx \frac{\Delta I_L}{8\, f_s\, \Delta V_o}. \tag{63}$$

Include ESR contribution: approximate resistive ripple

$$\Delta V_{\mathrm{ESR}} \approx \left(\frac{\Delta I_L}{2}\right) R_{\mathrm{ESR}}, \tag{64}$$

and ensure $\Delta V_o^{\mathrm{total}} \approx \dfrac{\Delta I_L}{8 C f_s} + \dfrac{\Delta I_L}{2} R_{\mathrm{ESR}} \leq \text{spec}$.

13 State-space averaging in CCM

We derive averaged state-space model using $\mathbf{x} = [i_L\ v_C]^T$ and input $u = V_{\mathrm{in}}$. Two subintervals linear dynamics:

13.1 ON state (S closed)

KCL/KVL:

$$\frac{di_L}{dt} = \frac{1}{L}(V_{\mathrm{in}} - v_C) \tag{65}$$

$$\frac{dv_C}{dt} = \frac{1}{C}(i_L - i_o). \tag{66}$$

Matrix form:

$$\dot{\mathbf{x}} = A_{\mathrm{ON}}\mathbf{x} + B_{\mathrm{ON}}u, \qquad A_{\mathrm{ON}} = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/(R_{\mathrm{load}}C) \end{bmatrix}, \quad B_{\mathrm{ON}} = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}. \tag{67}$$

13.2 OFF state (S open)

When switch open, diode conducts (or synchronous FET freewheels). Equations:

$$\frac{di_L}{dt} = -\frac{v_C}{L} \tag{68}$$

$$\frac{dv_C}{dt} = \frac{1}{C}(i_L - i_o). \tag{69}$$

Matrix form:

$$\dot{\mathbf{x}} = A_{\text{OFF}}\mathbf{x} + B_{\text{OFF}}u, \qquad A_{\text{OFF}} = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/(R_{\text{load}}C) \end{bmatrix}, \quad B_{\text{OFF}} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \tag{70}$$

Note: A_{ON} and A_{OFF} differ only in the input mapping.

13.3 Averaged model

Averaging over T_s:

$$A_{\text{ave}} = DA_{\text{ON}} + (1-D)A_{\text{OFF}} = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/(R_{\text{load}}C) \end{bmatrix}, \tag{71}$$

$$B_{\text{ave}} = DB_{\text{ON}} + (1-D)B_{\text{OFF}} = \begin{bmatrix} D/L \\ 0 \end{bmatrix}. \tag{72}$$

Averaged model:

$$\dot{\mathbf{x}} = A_{\text{ave}}\mathbf{x} + B_{\text{ave}}u. \tag{73}$$

14 Component selection: algorithmic procedure

A compact algorithm:

1. Choose switching frequency f_s balancing size and switching losses.
2. For worst-case $V_{\text{in,min}}$ and desired V_o, compute duty D from Eq. (54).
3. Select allowable inductor ripple ΔI_L (e.g., 20–40% of $\bar{I}_L$) and compute L from Eq. (60).
4. Select capacitor to meet ΔV_o via Eq. (63) and verify ESR and RMS current rating.
5. Select MOSFET and diode: consider worst-case voltages and currents, thermal limits, switching energy $E_{\text{on}}, E_{\text{off}}$, and for synchronous designs consider dead-time and shoot-through.
6. Compute losses, perform thermal calculations, iterate until margins satisfied.

15 Loss Models and Thermal Considerations

In practical converter design, idealized assumptions must be replaced by loss models to predict efficiency and ensure thermal reliability. The principal loss mechanisms are summarized below with equations useful for quick estimates (deductive derivations similar to the boost chapter are applicable).

15.1 Conduction losses

MOSFET conduction: Assuming triangular inductor ripple and ON duty D,

$$I^2_{\text{MOSFET,rms}} = D\left(\bar{I}_L^2 + \frac{(\Delta I_L)^2}{12}\right), \tag{74}$$

and

$$P_{\text{cond,MOS}} = I^2_{\text{MOSFET,rms}} R_{\text{DS(on)}}. \tag{75}$$

Diode (or synchronous MOSFET body diode) conduction:

$$P_{\text{cond,D}} = V_f I_{D,\text{avg}} = V_f(1-D)\bar{I}_L. \tag{76}$$

15.2 Switching and capacitive losses

MOSFET switching:

$$P_{\text{sw}} = f_s(E_{\text{on}} + E_{\text{off}}) + \frac{1}{2}C_{\text{oss}}V_{DS}^2 f_s. \tag{77}$$

Diode reverse recovery (if applicable):

$$P_{rr} = f_s Q_{rr} V_{DS}. \tag{78}$$

15.3 Magnetic and passive losses

$$P_{\text{cu}} = I_{L,\text{rms}}^2 R_w(f), \qquad P_{\text{core}} = k f_s^{\alpha} B_{\text{pk}}^{\beta} V_{\text{core}}, \tag{79}$$

$$P_{\text{cap}} = I_{C,\text{rms}}^2 R_{\text{ESR}}. \tag{80}$$

15.4 Total loss and efficiency

$$P_{\text{loss}} = \sum(\text{all losses}), \qquad \eta = \frac{P_o}{P_o + P_{\text{loss}}}. \tag{81}$$

15.5 Thermal modeling

Steady-state junction temperature:

$$T_j = T_a + P_{\text{device}}\theta_{JA}. \tag{82}$$

Transient junction change for time-varying power:

$$\Delta T_j(t) = P(t) * Z_\theta(t). \tag{83}$$

Adopt safety margins: limit T_j well below $T_{j,\max}$ (e.g., 125–150°C) depending on reliability targets.

16 Numerical example

We now work a detailed numerical example with every algebraic step shown.

16.1 Specifications

Assume:

$$\begin{aligned} V_{\text{in}} &= 12\,\text{V} \\ V_o &= 5\,\text{V} \\ P_o &= 60\,\text{W} \\ f_s &= 200\,\text{kHz} \\ \Delta V_o &= 50\,\text{mV}_{\text{pp}} \\ \alpha &= 0.3 \quad (\text{so } \Delta I_L = 0.3\bar{I}_L) \end{aligned}$$

16.2 Compute duty cycle

From Eq. (54):

$$D = \frac{V_o}{V_{\text{in}}} = \frac{5}{12} = 0.4166667.$$

16.3 Output current and average inductor current

$$I_o = \frac{P_o}{V_o} = \frac{60}{5} = 12 \text{ A}.$$

In a buck $\bar{I}_L = I_o = 12$ A.

16.4 Inductance selection

Target $\Delta I_L = \alpha \bar{I}_L = 0.3 \times 12 = 3.6$ A. Use Eq. (60):

$$L = \frac{(V_{\text{in}} - V_o)D}{\Delta I_L f_s} = \frac{(12-5) \times 0.4166667}{3.6 \times 200 \times 10^3} \text{ H}.$$

Compute stepwise:

$$12 - 5 = 7 \text{ V}, \quad 7 \times 0.4166667 = 2.9166669 \text{ V},$$

$$\Delta I_L f_s = 3.6 \times 200 \times 10^3 = 720 \times 10^3 = 7.2 \times 10^5 \text{ A/s},$$

$$L = \frac{2.9166669}{7.2 \times 10^5} = 4.051\ldots \times 10^{-6} \text{ H} = 4.05\ \mu\text{H}.$$

16.5 Capacitance selection

Use Eq. (63):

$$C \approx \frac{\Delta I_L}{8 f_s \Delta V_o} = \frac{3.6}{8 \times 200 \times 10^3 \times 50 \times 10^{-3}}.$$

Denominator:

$$8 \times 200000 \times 0.05 = 8 \times 10000 = 80000.$$

So

$$C \approx \frac{3.6}{80000} = 4.5 \times 10^{-5} \text{ F} = 45\ \mu\text{F}.$$

Check ESR: if $R_{\text{ESR}} = 10\,\text{m}\Omega$ then $\Delta V_{\text{ESR}} \approx (\Delta I_L/2) R_{\text{ESR}} = 1.8 \times 0.01 = 0.018$ V $= 18$ mV; total ripple ≈ 50 mV satisfied.

16.6 RMS currents and quick loss estimates

Inductor RMS (Eq. (59) and triangular rms):

$$I_{L,\text{rms}}^2 = \bar{I}_L^2 + \frac{(\Delta I_L)^2}{12} = 12^2 + \frac{3.6^2}{12} = 144 + 1.08 = 145.08,$$

$$I_{L,\text{rms}} \approx 12.04 \text{ A}.$$

MOSFET rms during ON (Eq. (J) style):

$$I_{\text{MOS,rms}}^2 = D\left(\bar{I}_L^2 + \frac{(\Delta I_L)^2}{12}\right) = 0.4166667 \times 145.08 \approx 60.45,$$

$$I_{\text{MOS,rms}} \approx 7.77 \text{ A}.$$

Assuming $R_{\text{DS(on)}} = 8\,\text{m}\Omega$:

$$P_{\text{cond,MOS}} \approx 7.77^2 \times 8 \times 10^{-3} \approx 0.483 \text{ W}.$$

Assuming diode $V_f = 0.6\,\text{V}$:

$$P_{\text{cond,D}} = V_f (1 - D) \bar{I}_L = 0.6 \times 0.5833333 \times 12 \approx 4.2 \text{ W}.$$

Switching loss example: assume $E_{\text{on}} + E_{\text{off}} = 5\ \mu$J,

$$P_{\text{sw}} = f_s (5 \times 10^{-6}) = 200 \times 10^3 \times 5 \times 10^{-6} = 1.0 \text{ W}.$$

Total semiconductor losses estimate $\sim$ 1.5–2 W plus magnetic losses; efficiency estimate follows.

16.7 Verification of CCM

Minimum inductor current:

$$I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2} = 12 - 1.8 = 10.2 \text{ A} > 0,$$

so CCM holds.

17 Practical considerations and next steps

- Refine magnetics: choose core, compute turns N, check B_{pk} and Steinmetz core loss; compute winding resistance including skin/proximity effects.
- Choose MOSFET with appropriate $V_{DS,\max}$ margin, low $R_{\text{DS(on)}}$ at expected T_j, and published E_{on}/E_{off} curves for switching loss estimation.
- Consider synchronous rectification to reduce diode conduction loss; design dead-time and shoot-through protection.
- Design gate driver: choose V_{drive}, gate resistance, and check drive losses $P_{gate} = C_g V_{drive}^2 f_s$.
- Simulate full switching model (SPICE/PLECS), verify waveforms, measure real switching loss with datasheet-based E_{on}, E_{off} and adjust f_s if necessary.
- Design compensator using linearized plant Eq. (**??**); aim crossover $f_c \lesssim f_s/10$ and stable phase margin (40–60°).

18 Design Procedure — Essential Equations (A–Z)

$$\text{Duty:} \qquad D = \frac{V_o}{V_{\text{in}}} \tag{A}$$

$$\text{Output current:} \qquad I_o = \frac{P_o}{V_o} \tag{B}$$

$$\text{Avg. inductor current:} \qquad \bar{I}_L = I_o \tag{C}$$

$$\text{Inductor peak-to-peak ripple:} \qquad \Delta I_L = \frac{(V_{\text{in}} - V_o)D}{L\, f_s} \tag{D}$$

$$\text{Inductance selection:} \qquad L = \frac{(V_{\text{in}} - V_o)D}{\Delta I_L\, f_s} \tag{E}$$

$$\text{Inductor extrema:} \qquad I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2}, \quad I_{L,\max} = \bar{I}_L + \frac{\Delta I_L}{2} \tag{F}$$

$$\text{Capacitance (triangular approx):} \qquad C \approx \frac{\Delta I_L}{8\, f_s\, \Delta V_o} \tag{G}$$

$$\text{Capacitor RMS current approx:} \qquad I_{C,\text{rms}} \approx \frac{\Delta I_L}{2\sqrt{3}} \tag{H}$$

$$\text{Inductor RMS (triangular):} \qquad I_{L,\text{rms}}^2 = \bar{I}_L^2 + \frac{(\Delta I_L)^2}{12} \tag{I}$$

$$\text{MOSFET rms during ON:} \qquad I_{\text{MOS,rms}}^2 = D\left(\bar{I}_L^2 + \frac{(\Delta I_L)^2}{12}\right) \tag{J}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,MOS}} \;=\; I_{\text{MOS,rms}}^{2}\, R_{\text{DS(on)}} \tag{K}$$

$$\text{MOSFET switching loss (approx.):} \qquad P_{\text{sw}} \;=\; f_s\,(E_{\text{on}} + E_{\text{off}}) \;+\; \tfrac{1}{2} C_{\text{oss}} V_{DS}^{2} f_s \tag{L}$$

$$\text{Diode average current:} \qquad I_{D,\text{avg}} \;=\; (1-D)\,\bar{I}_L \tag{M}$$

$$\text{Diode conduction loss:} \qquad P_{\text{cond,D}} \;=\; V_f\, I_{D,\text{avg}} \tag{N}$$

$$\text{Diode reverse-recovery loss:} \qquad P_{rr} \;=\; f_s\, Q_{rr}\, V_{DS} \tag{O}$$

$$\text{Capacitor ESR loss:} \qquad P_{\text{cap,ESR}} \;=\; I_{C,\text{rms}}^{2}\, R_{\text{ESR}} \tag{P}$$

$$\text{Magnetic core loss (generalized Steinmetz):} \qquad P_{\text{core}} \;=\; k\, f_s^{\alpha}\, B_{\text{pk}}^{\beta}\, V_{\text{core}} \tag{Q}$$

$$\text{Peak flux density (inductor):} \qquad B_{\text{pk}} \;=\; \frac{V_{L,\text{ON}}\, D}{N\, A_e\, f_s}, \quad V_{L,\text{ON}} = V_{\text{in}} - V_o \tag{R}$$

$$\text{Turns vs. inductance:} \qquad L \;=\; N^{2} \frac{\mu_0 \mu_r A_e}{\ell_e} \quad \Rightarrow \quad N \;=\; \sqrt{\frac{L\,\ell_e}{\mu_0 \mu_r A_e}} \tag{S}$$

$$\text{Winding DC resistance:} \qquad R_{w,\text{DC}} \;=\; \rho\, \frac{\ell_{\text{w}}}{A_{\text{cu}}} \tag{T}$$

$$\text{Junction temperature (steady):} \qquad T_j \;=\; T_a \;+\; P_{\text{device}}\, \theta_{JA} \tag{U}$$

$$\text{Transient junction rise:} \qquad \Delta T_j(t) \;=\; P(t) * Z_\theta(t) \tag{V}$$

$$\text{Efficiency:} \qquad \eta \;=\; \frac{P_o}{P_o + P_{\text{loss}}} \tag{W}$$

$$\text{Voltage rating margin:} \qquad V_{DS,\text{max}} \;\geq\; (1 + \text{M}_v)\, V_{\text{in}} \quad (\text{M}_v = 0.2\text{–}0.5) \tag{X}$$

$$\text{R}_{\text{DS(on)}}\text{ temperature dependence:} \qquad R_{\text{DS(on)}}(T) \;=\; R_{\text{DS(on)},25℃}\big[1 + \alpha_R (T_j - 25^{\circ}\text{C})\big] \tag{Y}$$

Notes: these equations provide the essential algebraic toolbox for buck converter design: choose f_s, pick ΔI_L (fraction of $\bar{I}_L$), compute L (E), use (G) to size C, compute RMS currents (I,H,J) for copper/semiconductor selection, estimate switching losses (L,O) for thermal design (U,V), iterate geometry (S,T,R,Q) to meet core loss and thermal budgets; finally use (Z) to design loop compensation.

19 Problem statement and design specifications for Buck-Boost converter

Design a non-isolated *inverting* buck–boost converter with the following target specifications (numerical example will follow in Section 25):

- Input voltage range: $V_{\text{in,min}}$ to $V_{\text{in,max}}$ (V)
- Output voltage (magnitude and polarity): V_o (V) — *polarity inverted* relative to V_{in}
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Output voltage ripple (peak-to-peak): ΔV_o (V)
- Inductor current ripple (peak-to-peak): ΔI_L (A)
- Continuous conduction mode (CCM) operation (unless DCM is explicitly analyzed)

20 Fundamental principles and steady-state derivation

20.1 Circuit description

The ideal inverting buck–boost converter (see Fig. 3) consists of an input source V_{in}, an inductor L, a single switch S (MOSFET), a diode D, an output capacitor C, and load R_{load}. The topology inverts polarity: the output terminal shown has opposite polarity to the input. Define the inductor current i_L flowing from the input node through L toward the switch node (conventional positive direction into the switch), and define capacitor voltage $v_C = V_o$ (algebraic sign included; for an inverting stage v_C will be negative for a positive magnitude specification).

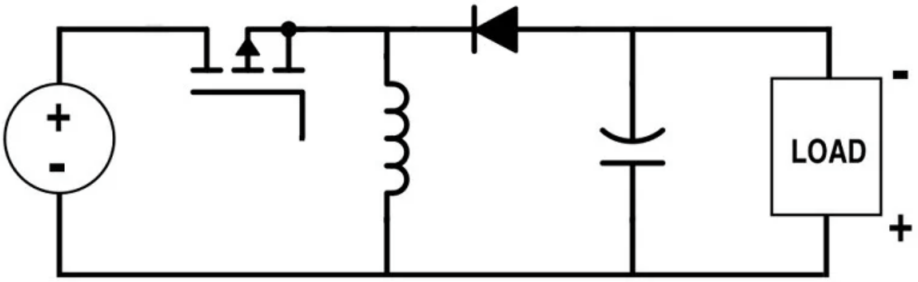

Figure 3: Ideal inverting non-isolated buck–boost converter.

20.2 Steady-state volt-second balance on the inductor

In CCM the inductor current never reaches zero. Let D denote the duty ratio (fraction of switching period $T_s = 1/f_s$ during which S is ON). Two intervals:

1. **ON interval** ($0 \le t < DT_s$): switch S closed. Inductor is connected to input and charges from V_{in}. The inductor voltage
$$v_L^{(\text{ON})} = V_{\text{in}}.$$

2. **OFF interval** ($DT_s \le t < T_s$): switch S open, diode D conducts and inductor discharges into the capacitor and load. The inductor voltage (algebraic) is

$$v_L^{(\mathrm{OFF})} = -V_o \qquad \text{(note: } V_o \text{ may be negative; the expression is algebraic).}$$

Volt-second balance (average inductor voltage over a period is zero):

$$\int_0^{T_s} v_L(t)\,dt = 0 \tag{84}$$

$$V_{\mathrm{in}}(DT_s) + (-V_o)((1-D)T_s) = 0. \tag{85}$$

Divide by T_s:

$$DV_{\mathrm{in}} - (1-D)V_o = 0. \tag{86}$$

Rearrange to express the steady-state output:

$$\begin{aligned} DV_{\mathrm{in}} &= (1-D)V_o \\ \therefore V_o &= \frac{D}{1-D}\,V_{\mathrm{in}}. \end{aligned} \tag{87}$$

Because the topology inverts polarity, the algebraic relation including sign is

$$\boxed{V_o \;=\; -\frac{D}{1-D}\,V_{\mathrm{in}}}. \tag{88}$$

(Interpretation: the *magnitude* of the DC gain is $|V_o| = \dfrac{D}{1-D}V_{\mathrm{in}}$, and the polarity is inverted.)

Dimensional check: volts = (unitless)×volts. Valid for $0 \le D < 1$ (as $D \to 1$ magnitude tends to infinity in the ideal model).

21 Inductor current ripple and capacitor sizing

21.1 Inductor ripple

During the **ON** interval the inductor voltage is $v_L = V_{\mathrm{in}}$. Thus the inductor slope and increase over DT_s:

$$\left.\frac{di_L}{dt}\right|_{\mathrm{ON}} = \frac{V_{\mathrm{in}}}{L}, \qquad \Delta i_{L,\mathrm{ON}} = \frac{V_{\mathrm{in}}}{L}DT_s. \tag{89}$$

During the **OFF** interval the inductor sees $v_L = -V_o$ so

$$\left.\frac{di_L}{dt}\right|_{\mathrm{OFF}} = -\frac{V_o}{L}, \qquad \Delta i_{L,\mathrm{OFF}} = -\frac{V_o}{L}(1-D)T_s. \tag{90}$$

In steady state $\Delta i_{L,\mathrm{ON}} + \Delta i_{L,\mathrm{OFF}} = 0$, which reduces to the volt-second relation (86). The peak-to-peak inductor ripple magnitude (use $|V_o|$ in magnitude computations) is commonly written as

$$\boxed{\Delta I_L \;=\; \frac{V_{\mathrm{in}}}{L}\,\frac{D}{f_s} \;=\; \frac{|V_o|(1-D)}{L f_s}} \tag{91}$$

(the two forms are equivalent by the steady-state relation). Solve for inductance given a desired ripple ΔI_L:

$$L = \frac{V_{\mathrm{in}}\,D}{\Delta I_L\,f_s}. \tag{92}$$

Units: $\mathrm{V/A \cdot s = H}$.

Inductor extrema and average:

$$\bar{I}_L = \frac{I_o}{1-D} \qquad \text{(power balance, see below)} \tag{93}$$

$$I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2}, \qquad I_{L,\max} = \bar{I}_L + \frac{\Delta I_L}{2}. \tag{94}$$

Note on average current (power balance): For the inverting buck–boost, power balance (ideal) gives

$$V_{\text{in}}\, I_{\text{in}} = |V_o|\, I_o.$$

Using $I_{\text{in}} = \bar{I}_L$ and the relation $|V_o| = \dfrac{D}{1-D} V_{\text{in}}$ one obtains

$$\bar{I}_L = \frac{I_o}{1-D}. \tag{93 revisited}$$

21.2 Capacitor ripple and size

Average output current (magnitude):

$$I_o = \frac{P_o}{|V_o|} = \frac{|V_o|}{R_{\text{load}}}. \tag{95}$$

Under the usual small-ripple assumption, the capacitor sees approximately the *high frequency* triangular current component produced by the inductor during the interval when the inductor is discharging into the capacitor (OFF interval). For the inverting buck–boost the triangular capacitor current amplitude transferred per cycle is approximately $\Delta I_L(1-D)$ (area scaling by OFF duty). A conservative and commonly used peak-to-peak voltage ripple expression (triangular approximation) is:

$$\Delta V_o \approx \frac{\Delta I_L (1-D)}{8\, C\, f_s}. \tag{96}$$

Solve for C:

$$\boxed{C \approx \frac{\Delta I_L (1-D)}{8\, f_s\, \Delta V_o}} \tag{97}$$

Add ESR contribution (resistive ripple): approximate

$$\Delta V_{\text{ESR}} \approx \left(\frac{\Delta I_L}{2}\right) R_{\text{ESR}}, \tag{98}$$

so ensure total ripple

$$\Delta V_o^{\text{total}} \approx \frac{\Delta I_L (1-D)}{8 C f_s} + \frac{\Delta I_L}{2} R_{\text{ESR}} \le \text{spec.}$$

22 State-space averaging in CCM (time-domain averaged model)

We present averaged subinterval dynamics (no small-signal linearization). State vector $\mathbf{x} = [\, i_L \quad v_C \,]^T$ with input $u = V_{\text{in}}$ and load $i_o = v_C / R_{\text{load}}$ (algebraic sign per chosen polarity convention).

22.1 ON state (S closed)

When S is ON the inductor is connected to the input and the diode is off. KVL/KCL (with our sign conventions) give

$$\frac{di_L}{dt} = \frac{1}{L} V_{\text{in}} \tag{99}$$

$$\frac{dv_C}{dt} = -\frac{1}{C} i_o = -\frac{1}{C} \frac{v_C}{R_{\text{load}}}. \tag{100}$$

Matrix form:

$$\dot{\mathbf{x}} = A_{\text{ON}}\, \mathbf{x} + B_{\text{ON}}\, u, \qquad A_{\text{ON}} = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{R_{\text{load}} C} \end{bmatrix}, \quad B_{\text{ON}} = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}. \tag{101}$$

22.2 OFF state (S open)

When S is OFF the diode conducts, the inductor discharges into the capacitor and load. KVL/KCL:

$$\frac{di_L}{dt} = -\frac{v_C}{L} \tag{102}$$

$$\frac{dv_C}{dt} = \frac{1}{C}(i_L - i_o) = \frac{1}{C}\left(i_L - \frac{v_C}{R_{\text{load}}}\right). \tag{103}$$

Matrix form:

$$\dot{\mathbf{x}} = A_{\text{OFF}}\,\mathbf{x} + B_{\text{OFF}}\,u, \qquad A_{\text{OFF}} = \begin{bmatrix} 0 & -1/L \\ 1/C & -\dfrac{1}{R_{\text{load}}C} \end{bmatrix}, \quad B_{\text{OFF}} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \tag{104}$$

22.3 Averaged model

Averaging across the switching period with duty D:

$$A_{\text{ave}} = DA_{\text{ON}} + (1-D)A_{\text{OFF}} = \begin{bmatrix} 0 & -\dfrac{1-D}{L} \\ \dfrac{1-D}{C} & -\dfrac{1}{R_{\text{load}}C} \end{bmatrix}, \tag{105}$$

$$B_{\text{ave}} = DB_{\text{ON}} + (1-D)B_{\text{OFF}} = \begin{bmatrix} D/L \\ 0 \end{bmatrix}. \tag{106}$$

Thus the averaged continuous-time model is

$$\boxed{\dot{\mathbf{x}} = A_{\text{ave}}\,\mathbf{x} + B_{\text{ave}}\,u} \tag{107}$$

which is suitable for time-domain simulation and for deriving large-signal dynamic behavior (but not small-signal linearized control design here, per request).

23 Component selection: algorithmic procedure

A compact algorithm for initial sizing and checks:

1. Choose switching frequency f_s based on trade-off between magnetics/capacitor size and switching losses.
2. For worst-case $V_{\text{in,min}}$ and desired $|V_o|$, compute duty D from Eq. (87) (use magnitude form), then include sign using (88).
3. Select allowable inductor ripple ΔI_L (e.g. 20–40% of $\bar{I}_L$), compute L from (92).
4. Select capacitor to meet ΔV_o via (97) and verify ESR and ripple current rating.
5. Select MOSFET and diode: consider worst-case blocking voltage ($V_{DS,\text{max}} \gtrsim |V_o|$ plus margin), current stresses $I_{L,\text{max}}$, switching energies E_{on}, E_{off}, and diode reverse recovery.
6. Compute losses and thermal budgets; iterate magnetics (core, turns) and switching frequency until requirements met.

24 Loss models and thermal considerations

(The loss models follow the same structure as for the boost/buck with sign conventions noted; we summarize the dominant formulas used in rapid estimates.)

24.1 Conduction losses

MOSFET conduction: RMS current through MOSFET while ON:

$$I^2_{\mathrm{MOS,rms}} \;=\; D\left(\bar{I}_L^2 + \frac{(\Delta I_L)^2}{12}\right),$$

and conduction loss

$$P_{\mathrm{cond,MOS}} = I^2_{\mathrm{MOS,rms}}\, R_{\mathrm{DS(on)}}.$$

Diode conduction: Diode average current (during OFF): $I_{D,\mathrm{avg}} = (1-D)\,\bar{I}_L$, hence

$$P_{\mathrm{cond,D}} = V_f\, I_{D,\mathrm{avg}} = V_f(1-D)\bar{I}_L.$$

24.2 Switching and capacitive losses

$$P_{\mathrm{sw}} = f_s(E_{\mathrm{on}} + E_{\mathrm{off}}) + \frac{1}{2}C_{\mathrm{oss}}V_{DS}^2 f_s, \qquad P_{rr} = f_s Q_{rr} V_{DS}.$$

24.3 Magnetic and passive losses

$$P_{\mathrm{cu}} = I^2_{L,\mathrm{rms}} R_w(f), \qquad P_{\mathrm{core}} = k f_s^{\alpha} B_{\mathrm{pk}}^{\beta} V_{\mathrm{core}}, \qquad P_{\mathrm{cap}} = I^2_{C,\mathrm{rms}} R_{\mathrm{ESR}}.$$

24.4 Total loss and thermal

$$P_{\mathrm{loss}} = P_{\mathrm{cond,MOS}} + P_{\mathrm{cond,D}} + P_{\mathrm{sw}} + P_{rr} + P_{\mathrm{cu}} + P_{\mathrm{core}} + P_{\mathrm{cap}}.$$

Efficiency:

$$\eta = \frac{P_o}{P_o + P_{\mathrm{loss}}}.$$

Junction temperature steady-state:

$$T_j = T_a + P_{\mathrm{device}}\theta_{JA},$$

and transient response via convolution with $Z_\theta(t)$ as needed.

25 Numerical example

We present a fully worked numeric example with every algebraic step.

25.1 Specifications

Assume:

$$\begin{array}{lll} V_{\mathrm{in}} = 12\,\mathrm{V}, & |V_o| = 24\,\mathrm{V}, & P_o = 50\,\mathrm{W}, \\ f_s = 100\,\mathrm{kHz}, & \Delta V_o = 0.24\,\mathrm{V} \quad (1\%\ \mathrm{pp}), & \alpha = 0.3. \end{array}$$

25.2 Duty cycle

From (87), magnitude:

$$|V_o| = \frac{D}{1-D}V_{\mathrm{in}} \quad \Rightarrow \quad \frac{D}{1-D} = \frac{|V_o|}{V_{\mathrm{in}}} = \frac{24}{12} = 2.$$

Solve for D:

$$D = 2(1-D) \;\Rightarrow\; D = 2 - 2D \;\Rightarrow\; 3D = 2 \;\Rightarrow\; D = \frac{2}{3} \approx 0.6666667.$$

Sign included: $V_o = -\dfrac{D}{1-D}V_{\mathrm{in}} = -24$ V.

25.3 Output and average inductor current

Output current magnitude:

$$I_o = \frac{P_o}{|V_o|} = \frac{50}{24} \approx 2.0833333 \text{ A}.$$

Average inductor current (Eq. 93):

$$\bar{I}_L = \frac{I_o}{1-D} = \frac{2.0833333}{1-2/3} = \frac{2.0833333}{1/3} = 6.25 \text{ A}.$$

25.4 Inductance selection

Target $\Delta I_L = \alpha \bar{I}_L = 0.3 \times 6.25 = 1.875$ A. Use (92):

$$L = \frac{V_{\text{in}} D}{\Delta I_L f_s} = \frac{12 \times \frac{2}{3}}{1.875 \times 100 \times 10^3} \text{ H}.$$

Compute stepwise:

$$12 \times \tfrac{2}{3} = 8 \text{ V}, \qquad 1.875 \times 100 \times 10^3 = 187500 \text{ A/s}.$$

Thus

$$L = \frac{8}{187500} = 4.2666667 \times 10^{-5} \text{ H} = 42.67 \ \mu\text{H}.$$

25.5 Capacitance selection

Use (97). First compute $(1-D) = 1/3$, and $\Delta I_L(1-D) = 1.875 \times \frac{1}{3} = 0.625$ A.

$$C \approx \frac{0.625}{8 \times 100 \times 10^3 \times 0.24} \text{ F}.$$

Denominator:

$$8 \times 100000 \times 0.24 = 800000 \times 0.24 = 192000.$$

So

$$C \approx \frac{0.625}{192000} = 3.2552 \times 10^{-6} \text{ F} \approx 3.26 \ \mu\text{F}.$$

Select practical capacitance larger (e.g., 10–22 μF) and low ESR to meet ripple and lifetime.

25.6 RMS currents and quick loss estimates

Inductor RMS:

$$I_{L,\text{rms}}^2 = \bar{I}_L^2 + \frac{(\Delta I_L)^2}{12} = 6.25^2 + \frac{1.875^2}{12} = 39.0625 + \frac{3.5156}{12} = 39.0625 + 0.2930 = 39.3555,$$

$$I_{L,\text{rms}} \approx \sqrt{39.3555} \approx 6.27 \text{ A}.$$

MOSFET RMS while ON:

$$I_{\text{MOS,rms}}^2 = D\left(\bar{I}_L^2 + \frac{(\Delta I_L)^2}{12}\right) = \tfrac{2}{3} \times 39.3555 \approx 26.237,$$

$$I_{\text{MOS,rms}} \approx 5.12 \text{ A}.$$

Assume $R_{\text{DS(on)}} = 50\,\text{m}\Omega$:

$$P_{\text{cond,MOS}} \approx 5.12^2 \times 0.05 \approx 1.31 \text{ W}.$$

Diode conduction loss (assume $V_f = 0.6\,\text{V}$):

$$P_{\text{cond,D}} = V_f(1-D)\bar{I}_L = 0.6 \times \tfrac{1}{3} \times 6.25 \approx 1.25 \text{ W}.$$

Estimate switching loss (assume $E_{on} + E_{off} = 3 \times 10^{-6}\,\text{J}$):

$$P_{\text{sw}} = f_s(E_{on} + E_{off}) = 100 \times 10^3 \times 3 \times 10^{-6} = 0.3 \text{ W}.$$

Rough total semiconductor losses $\sim$ 3–4 W; add magnetic copper + core + capacitor ESR losses for full budget.

25.7 Verification of CCM

Minimum inductor current:

$$I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2} = 6.25 - 0.9375 = 5.3125 \text{ A} > 0,$$

so CCM holds.

26 Practical considerations and next steps

- Refine magnetic design: select core material, compute N from L using core geometry, check B_{pk} and Steinmetz losses at f_s.
- Check winding AC resistance (skin/proximity) and compute P_{cu} from $I_{L,\text{rms}}$.
- Select MOSFET with $V_{DS,\max}$ margin $> |V_o|$ (typical margin 20–50%) and low $R_{\text{DS(on)}}$ at expected T_j.
- Consider synchronous rectification (replace diode by MOSFET) to reduce diode conduction loss; design appropriate dead-time and shoot-through protections.
- Design gate driver: check gate charge and driver losses $P_{gate} = Q_g V_{drive} f_s$.
- Simulate full switching model (SPICE/PLECS) to verify waveforms, measure actual switching and diode recovery losses, and then iterate component choices.
- Perform thermal network analysis using θ_{JA} or heatsink data; ensure worst-case T_j within reliability target.

27 Design Procedure — Essential Equations (A–Z)

$$\text{Duty (magnitude relation):} \qquad |V_o| = \frac{D}{1-D} V_{\text{in}} \tag{A}$$

$$\text{Signed steady output:} \qquad V_o = -\frac{D}{1-D} V_{\text{in}} \tag{B}$$

$$\text{Output current:} \qquad I_o = \frac{P_o}{|V_o|} \tag{C}$$

$$\text{Average inductor current (power balance):} \qquad \bar{I}_L = \frac{I_o}{1-D} \tag{D}$$

$$\text{Inductor p-p ripple (magnitude):} \qquad \Delta I_L = \frac{V_{\text{in}} D}{L f_s} \tag{E}$$

$$\text{Inductance selection:} \qquad L = \frac{V_{\text{in}} D}{\Delta I_L f_s} \tag{F}$$

$$\text{Inductor extrema:} \qquad I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2}, \quad I_{L,\max} = \bar{I}_L + \frac{\Delta I_L}{2} \tag{G}$$

$$\text{Capacitance (triangular approx, OFF transfer):} \qquad C \approx \frac{\Delta I_L (1-D)}{8 f_s \Delta V_o} \tag{H}$$

$$\text{Capacitor RMS current approx:} \qquad I_{C,\text{rms}} \approx \frac{\Delta I_L (1-D)}{2\sqrt{3}} \tag{I}$$

$$\text{Inductor RMS (triangular):} \qquad I_{L,\text{rms}}^2 \;=\; \bar{I}_L^2 + \frac{(\Delta I_L)^2}{12} \tag{J}$$

$$\text{MOSFET rms during ON:} \qquad I_{\text{MOS,rms}}^2 \;=\; D\left(\bar{I}_L^2 + \frac{(\Delta I_L)^2}{12}\right) \tag{K}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,MOS}} \;=\; I_{\text{MOS,rms}}^2\, R_{\text{DS(on)}} \tag{L}$$

$$\text{MOSFET switching loss (approx.):} \qquad P_{\text{sw}} \;=\; f_s\,(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V_{DS}^2 f_s \tag{M}$$

$$\text{Diode average current:} \qquad I_{D,\text{avg}} \;=\; (1-D)\,\bar{I}_L \tag{N}$$

$$\text{Diode conduction loss:} \qquad P_{\text{cond,D}} \;=\; V_f\, I_{D,\text{avg}} \tag{O}$$

$$\text{Diode reverse-recovery loss:} \qquad P_{rr} \;=\; f_s\, Q_{rr}\, V_{DS} \tag{P}$$

$$\text{Capacitor ESR loss:} \qquad P_{\text{cap,ESR}} \;=\; I_{C,\text{rms}}^2\, R_{\text{ESR}} \tag{Q}$$

$$\text{Magnetic core loss (GSE):} \qquad P_{\text{core}} \;=\; k\, f_s^{\alpha}\, B_{\text{pk}}^{\beta}\, V_{\text{core}} \tag{R}$$

$$\text{Peak flux density (inductor):} \qquad B_{\text{pk}} \;=\; \frac{V_{L,\text{ON}}\, D}{N\, A_e\, f_s}, \quad V_{L,\text{ON}} = V_{\text{in}} \tag{S}$$

$$\text{Inductance vs turns (core geometry):} \qquad L \;=\; N^2 \frac{\mu_0 \mu_r A_e}{\ell_e} \quad \Rightarrow \quad N \;=\; \sqrt{\frac{L\,\ell_e}{\mu_0 \mu_r A_e}} \tag{T}$$

$$\text{Winding DC resistance:} \qquad R_{w,\text{DC}} \;=\; \rho\, \frac{\ell_{\text{w}}}{A_{\text{cu}}} \tag{U}$$

$$\text{Junction temperature (steady):} \qquad T_j \;=\; T_a \;+\; P_{\text{device}}\, \theta_{JA} \tag{V}$$

$$\text{Transient junction rise:} \qquad \Delta T_j(t) \;=\; P(t) * Z_\theta(t) \tag{W}$$

$$\text{Efficiency:} \qquad \eta \;=\; \frac{P_o}{P_o + P_{\text{loss}}} \tag{X}$$

$$\text{Voltage rating margin (device selection):} \qquad V_{DS,\text{max}} \;\geq\; (1 + \text{M}_v)\,|V_o| \quad (\text{M}_v = 0.2\text{–}0.5) \tag{Y}$$

Notes: Use the relations above to obtain initial component values, then iterate with core-loss tables, MOSFET datasheet E_{on}/E_{off} curves, and thermal network calculations to finalize selections.

28 Problem statement and design specifications for Sepic Converter

Design a non-isolated *SEPIC* (Single-Ended Primary-Inductor Converter) with the following target specifications (numerical example will follow in Section 34):

- Input voltage range: $V_{\text{in,min}}$ to $V_{\text{in,max}}$ (V)
- Output voltage: V_o (V) (non-inverting: same polarity as V_{in})
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Output voltage ripple (peak-to-peak): ΔV_o (V)
- Inductor current ripple (peak-to-peak): $\Delta I_{L1},\ \Delta I_{L2}$ (A)
- Continuous conduction mode (CCM) operation

29 Fundamental principles and steady-state derivation

29.1 Circuit description

The ideal SEPIC (see Fig. 4) uses two inductors L_1 and L_2, a series coupling capacitor C_s (often called the coupling or energy-transfer capacitor), a single switch S (high-side or low-side MOSFET depending on implementation), a diode D, an output capacitor C and load R_{load}. The SEPIC is non-inverting and can step-up or step-down the input. For clarity we adopt the convention that V_o is positive (same polarity as V_{in}). The coupling capacitor C_s blocks DC so its steady-state voltage equals approximately V_{in} (see steady-state discussion below).

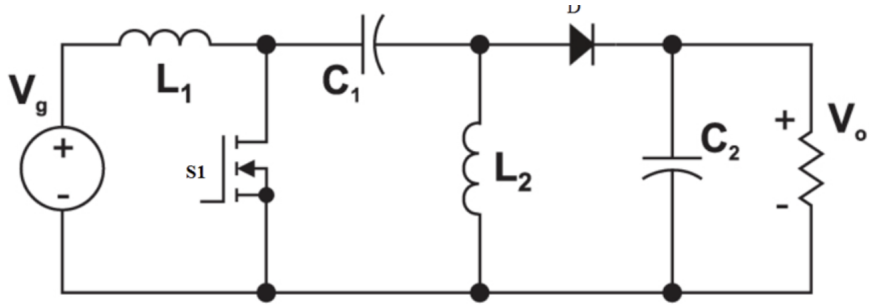

Figure 4: Ideal SEPIC (non-isolated, non-inverting).

29.2 Steady-state volt-second balance on the inductors

Let D be the duty ratio and $T_s = 1/f_s$ the switching period. The SEPIC has two inductors; we perform volt-second balance on each inductance.

Inductor L_1 (input-side): The voltage across L_1 depends on the switch state:

- ON ($0 \le t < DT_s$): Switch S is closed. The input voltage appears directly across L_1:

$$v_{L1}^{(\text{ON})} = V_{\text{in}}.$$

- OFF ($DT_s \le t < T_s$): Switch S is open, diode conducts. Current i_{L1} flows through the diode, and by KVL around the input loop: $V_{\text{in}} - v_{L1} - v_{Cs} = 0$, therefore:

$$v_{L1}^{(\text{OFF})} = V_{\text{in}} - v_{Cs}.$$

Applying volt-second balance on L_1 (average inductor voltage must be zero):

$$V_{\text{in}} \cdot D + (V_{\text{in}} - v_{Cs}) \cdot (1 - D) = 0 \tag{108}$$

Inductor L_2 (output-side): The voltage across L_2 also depends on the switch state:

- ON ($0 \le t < DT_s$): Switch S closed, diode reverse-biased. Inductor L_2 is connected across coupling capacitor C_s:
$$v_{L2}^{(\mathrm{ON})} = v_{Cs}.$$
- OFF ($DT_s \le t < T_s$): Switch S open, diode conducts. Inductor L_2 supplies current to the output through the diode. By KVL: $v_{Cs} - v_{L2} - V_o = 0$, therefore:
$$v_{L2}^{(\mathrm{OFF})} = v_{Cs} - V_o.$$

Applying volt-second balance on L_2:

$$v_{Cs} \cdot D + (v_{Cs} - V_o) \cdot (1 - D) = 0 \tag{109}$$

Deriving the voltage conversion ratio using charge balance: The key to properly analyzing the SEPIC is recognizing that the coupling capacitor C_s transfers energy from L_1 to L_2. In steady state, the average current through any capacitor must be zero.

From charge balance on the coupling capacitor C_s (average capacitor current must be zero): During ON: C_s supplies current to L_2: $i_{Cs} = -i_{L2}$ During OFF: C_s receives current from L_1: $i_{Cs} = i_{L1}$

For charge balance: $i_{L2} \cdot DT_s = i_{L1} \cdot (1 - D)T_s$

In steady state: $I_{L2} \cdot D = I_{L1} \cdot (1 - D)$

From power balance (assuming ideal components): $V_{\text{in}} I_{L1} = V_o I_{L2}$

Combining these relationships:

$$V_{\text{in}} I_{L1} = V_o I_{L2} \quad \text{and} \quad I_{L2} = \frac{(1 - D)}{D} I_{L1}$$

Substituting:

$$V_{\text{in}} I_{L1} = V_o \cdot \frac{(1 - D)}{D} I_{L1}$$

Therefore:

$$\boxed{V_o \;=\; \frac{D}{1 - D}\, V_{\text{in}}} \tag{110}$$

This is the standard SEPIC voltage conversion ratio, which is identical to that of a boost converter but with non-inverting polarity. The SEPIC can provide both buck operation ($D < 0.5$) and boost operation ($D > 0.5$).

Verification of coupling capacitor voltage: With $V_o = \frac{D}{1-D} V_{\text{in}}$, we can find the coupling capacitor voltage by substituting into Eq. (109):

$$v_{Cs} \cdot D + (v_{Cs} - V_o) \cdot (1 - D) = 0$$

$$v_{Cs} - (1 - D)V_o = 0$$

$$v_{Cs} = (1 - D) \cdot \frac{D}{1 - D} V_{\text{in}} = D V_{\text{in}}$$

This result shows that the coupling capacitor voltage is $v_{Cs} = D V_{\text{in}}$, which confirms the consistency of our derivation.

Dimensional check: volts = (unitless)×volts. Valid for $0 \le D < 1$.

30 Inductor current ripple and capacitor sizing

30.1 Inductor ripples

Assuming continuous conduction and that coupling capacitor C_s is sufficiently large so that $v_{Cs} \approx V_{\text{in}}$ (practical design enforces this), the inductor instantaneous slopes simplify.

Approximate inductor ripple formulae (practical engineering forms):

$$\Delta I_{L1} \approx \frac{V_{\text{in}}}{L_1}\frac{D}{f_s}, \tag{111}$$

$$\Delta I_{L2} \approx \frac{V_{Cs}}{L_2}\frac{D}{f_s} \approx \frac{V_{\text{in}}}{L_2}\frac{D}{f_s}. \tag{112}$$

(These follow because during the ON interval each inductor sees approximately V_{in} or $v_{Cs} \approx V_{\text{in}}$ across it; during OFF the signs reverse and net volt-second balances sum to zero.)

Solve for inductances given target ripples:

$$L_1 = \frac{V_{\text{in}}D}{\Delta I_{L1} f_s}, \tag{113}$$

$$L_2 = \frac{V_{\text{in}}D}{\Delta I_{L2} f_s}. \tag{114}$$

Inductor average currents and extrema: Average input-side inductor current (approximate, using power balance and canonical relation (110)):

$$\bar{I}_{L1} \approx I_{\text{in}} = \frac{P_o}{V_{\text{in}}} = \frac{|V_o|}{V_{\text{in}} R_{\text{load}}} \quad \text{(use signed magnitudes consistently).} \tag{115}$$

Average output-side inductor current:

$$\bar{I}_{L2} \approx \frac{I_o}{1-D}. \tag{116}$$

Extrema:

$$I_{Lk,\min} = \bar{I}_{Lk} - \frac{\Delta I_{Lk}}{2}, \qquad I_{Lk,\max} = \bar{I}_{Lk} + \frac{\Delta I_{Lk}}{2}, \quad k = 1, 2.$$

30.2 Coupling capacitor C_s sizing

The series capacitor C_s must transfer energy each cycle and maintain its dc voltage (usually designed to remain near V_{in}). A common conservative sizing requirement enforces a small ripple of the capacitor voltage Δv_{Cs}, e.g. a chosen $\Delta v_{Cs,\text{pp}}$ (V). The charge drawn from C_s per switching cycle equals the change in inductor currents area; approximate required capacitance:

$$C_s \geq \frac{\Delta Q_s}{\Delta v_{Cs}} \approx \frac{\Delta I_{L1}\, D/(2f_s)}{\Delta v_{Cs}} \approx \frac{\Delta I_{L1} D}{2 f_s\, \Delta v_{Cs}}. \tag{117}$$

(This expression arises from approximating the triangular current transferred through C_s during the ON interval: the triangular half-area $\frac{1}{2}\Delta I_{L1} \cdot (DT_s)$ yields charge amplitude; choose C_s so the resulting Δv_{Cs} is acceptably small.)

30.3 Output capacitor sizing

The output capacitor C must meet the output ripple spec ΔV_o. Similar triangular approximation for the capacitor current (dominated by ΔI_{L2} transferred during OFF) gives:

$$\Delta V_o \approx \frac{\Delta I_{L2}(1-D)}{8\, C\, f_s}. \tag{118}$$

Solve for C:

$$C \approx \frac{\Delta I_{L2}(1-D)}{8\, f_s\, \Delta V_o}. \tag{119}$$

Include ESR contribution:

$$\Delta V_{\text{ESR}} \approx \left(\frac{\Delta I_{L2}}{2}\right) R_{\text{ESR}},$$

and ensure total ripple $\Delta V_o^{\text{total}} \leq$ spec.

31 Averaged state-space model (CCM) — time-domain averaged

Define state vector $\mathbf{x} = [\, i_{L1}\ i_{L2}\ v_C \,]^T$, input $u = V_{\text{in}}$, load current $i_o = v_C/R_{\text{load}}$. We give the averaged subinterval matrices (suitable for time-domain simulation and large-signal dynamic study).

31.1 ON state (S closed)

When S closed (ON), the typical idealized equations (assuming switch node at ground in low-side implementation) are:

$$\dot{i}_{L1} = \frac{V_{\text{in}}}{L_1}, \tag{120}$$

$$\dot{i}_{L2} = \frac{v_{Cs}}{L_2}, \tag{121}$$

$$\dot{v}_C = -\frac{1}{C}\frac{v_C}{R_{\text{load}}} \quad \text{(output capacitor supplies load).} \tag{122}$$

31.2 OFF state (S open)

When S open (OFF), diode conducts and energy is transferred to the output:

$$\dot{i}_{L1} = \frac{V_{\text{in}} - v_{Cs}}{L_1}, \tag{123}$$

$$\dot{i}_{L2} = \frac{v_{Cs} - v_C}{L_2}, \tag{124}$$

$$\dot{v}_C = \frac{1}{C}\left(i_{L2} - \frac{v_C}{R_{\text{load}}}\right). \tag{125}$$

31.3 Averaged model

Averaging with duty D yields

$$\dot{\mathbf{x}} = A_{\text{ave}}(D)\,\mathbf{x} + B_{\text{ave}}(D)\,u,$$

where A_{ave} and B_{ave} are constructed from the ON/OFF matrices weighted by D and $(1-D)$. (We omit the full 3×3 symbolic expansion here to keep the presentation compact; use Eqs. (120)–(125) to form the matrices for a chosen sign convention.)

32 Component selection: algorithmic procedure

A succinct practical procedure:

1. Choose f_s balancing magnetics/capacitor size and switching losses.
2. For worst-case $V_{\text{in,min}}$ and desired V_o, compute duty D from (110): $D = \dfrac{|V_o|}{V_{\text{in}} + |V_o|}$.
3. Select allowable inductor ripples ΔI_{L1} and ΔI_{L2} (typical 20–40% of respective average currents) and compute L_1, L_2 using (113)–(114).
4. Choose C_s with small Δv_{Cs} using (117); typically C_s is large (electrolytic or film) to minimize coupling capacitor ripple.
5. Select output capacitor C from (119) including ESR and RMS current rating checks.
6. Select MOSFET and diode (or synchronous MOSFET) based on $V_{DS,\text{max}}$ margin, I_{peak}, switching energies E_{on}/E_{off}; consider replacing diode with synchronous FET to improve efficiency.
7. Compute losses and thermal budgets; iterate magnetics and switching frequency to meet thermal and efficiency targets.

33 Loss models and thermal considerations

The SEPIC uses the same loss modeling building blocks as other converters. Representative formulas:

$$\begin{aligned} P_{\text{cond,MOS}} &= I_{\text{MOS,rms}}^2 R_{\text{DS(on)}}, \\ P_{\text{cond,D}} &= V_f(1-D)\bar{I}_{L2}, \\ P_{\text{sw}} &= f_s(E_{\text{on}}+E_{\text{off}}) + \tfrac{1}{2}C_{\text{oss}}V_{DS}^2 f_s, \\ P_{\text{cu}} &= I_{L,\text{rms}}^2 R_w(f), \quad P_{\text{core}} = k f_s^{\alpha} B_{\text{pk}}^{\beta} V_{\text{core}}, \\ P_{\text{cap}} &= I_{C,\text{rms}}^2 R_{\text{ESR}}, \quad P_{\text{loss}} = \sum (\text{all losses}). \end{aligned}$$

Thermal:

$$T_j = T_a + P_{\text{device}}\theta_{JA}, \qquad \Delta T_j(t) = P(t) * Z_\theta(t).$$

34 Numerical example

Work a complete numeric example with every algebraic step.

34.1 Specifications

Assume:

$$V_{\text{in}} = 12\,\text{V}, \quad V_o = 5\,\text{V}, \quad P_o = 60\,\text{W}, \quad f_s = 200\,\text{kHz}, \quad \Delta V_o = 50\,\text{mV}_{\text{pp}}, \quad \alpha = 0.3.$$

34.2 Duty cycle

From (110) magnitude relation:

$$\frac{D}{1-D} = \frac{V_o}{V_{\text{in}}} = \frac{5}{12} = 0.4166667.$$

Solve:

$$D = 0.4166667(1-D) \;\Rightarrow\; D = 0.4166667 - 0.4166667D$$

$$D(1+0.4166667) = 0.4166667 \;\Rightarrow\; D = \frac{0.4166667}{1.4166667} = \frac{5/12}{1+5/12} = \frac{5}{17} \approx 0.2941176.$$

34.3 Output and average currents

$$I_o = \frac{P_o}{V_o} = \frac{60}{5} = 12 \text{ A}.$$

Average inductor currents (approximate):

$$\bar{I}_{L2} \approx \frac{I_o}{1-D} = \frac{12}{1-0.2941176} = \frac{12}{0.7058824} \approx 17.01 \text{ A}.$$

Input average current (approx):

$$\bar{I}_{L1} \approx I_{\text{in}} = \frac{P_o}{V_{\text{in}}} = \frac{60}{12} = 5 \text{ A}.$$

34.4 Inductance selection

Choose target ripples $\Delta I_{L1} = 0.3\bar{I}_{L1} = 0.3 \times 5 = 1.5$ A, and $\Delta I_{L2} = 0.3\bar{I}_{L2} = 0.3 \times 17.01 \approx 5.103$ A.

Compute L_1 using (113):

$$L_1 = \frac{V_{\text{in}} D}{\Delta I_{L1} f_s} = \frac{12 \times 0.2941176}{1.5 \times 200 \times 10^3} \text{ H}.$$

Stepwise:

$$12 \times 0.2941176 = 3.5294112 \text{ V}, \quad 1.5 \times 200 \times 10^3 = 300 \times 10^3 = 3 \times 10^5.$$

So

$$L_1 = \frac{3.5294112}{3 \times 10^5} = 1.1764704 \times 10^{-5} \text{ H} \approx 11.76 \ \mu\text{H}.$$

Compute L_2 using (114):

$$L_2 = \frac{V_{\text{in}} D}{\Delta I_{L2} f_s} = \frac{12 \times 0.2941176}{5.103 \times 200 \times 10^3} \text{ H}.$$

Denominator:

$$5.103 \times 200 \times 10^3 = 1.0206 \times 10^6.$$

So

$$L_2 = \frac{3.5294112}{1.0206 \times 10^6} = 3.458 \times 10^{-6} \text{ H} \approx 3.46 \ \mu\text{H}.$$

34.5 Coupling capacitor C_s

Choose allowable coupling capacitor ripple $\Delta v_{Cs} = 50\,\text{mV}_{\text{pp}}$ (example). Use (117) with $\Delta I_{L1} = 1.5$ A:

$$C_s \approx \frac{\Delta I_{L1} D}{2 f_s \, \Delta v_{Cs}} = \frac{1.5 \times 0.2941176}{2 \times 200 \times 10^3 \times 50 \times 10^{-3}} \text{ F}.$$

Compute numerator:

$$1.5 \times 0.2941176 = 0.4411764.$$

Denominator:

$$2 \times 200000 \times 0.05 = 400000 \times 0.05 = 20000.$$

So

$$C_s \approx \frac{0.4411764}{20000} = 2.205882 \times 10^{-5} \text{ F} \approx 22.06 \ \mu\text{F}.$$

34.6 Output capacitance

Use (119) with $\Delta I_{L2} \approx 5.103$ A and $1 - D = 0.7058824$:

$$C \approx \frac{\Delta I_{L2}(1 - D)}{8 f_s \Delta V_o} = \frac{5.103 \times 0.7058824}{8 \times 200 \times 10^3 \times 0.05} \text{ F}.$$

Numerator:

$$5.103 \times 0.7058824 = 3.603.$$

Denominator:

$$8 \times 200000 \times 0.05 = 80000.$$

So

$$C \approx \frac{3.603}{80000} = 4.50375 \times 10^{-5} \text{ F} \approx 45.04 \ \mu\text{F}.$$

Select a practical low-ESR capacitor bank (e.g., 2–3 parallel polymer caps) to meet ESR and ripple current specs.

34.7 RMS currents and quick loss estimates

Inductor RMS currents (triangular approximation):

$$I_{L1,\mathrm{rms}}^2 = \bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12} = 5^2 + \frac{1.5^2}{12} = 25 + 0.1875 = 25.1875,$$

$$I_{L1,\mathrm{rms}} \approx 5.0187 \text{ A}.$$

$$I_{L2,\mathrm{rms}}^2 = \bar{I}_{L2}^2 + \frac{(\Delta I_{L2})^2}{12} \approx 17.01^2 + \frac{5.103^2}{12} = 289.34 + 2.173 = 291.513,$$

$$I_{L2,\mathrm{rms}} \approx 17.08 \text{ A}.$$

Estimate MOSFET rms current during ON ($D \approx 0.294$), using the appropriate inductor current (implementation-dependent — often MOSFET carries i_{L1} when ON):

$$I_{\mathrm{MOS,rms}}^2 \approx D\left(\bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12}\right) = 0.294 \times 25.1875 \approx 7.405.$$

$$I_{\mathrm{MOS,rms}} \approx 2.72 \text{ A}.$$

Assuming $R_{\mathrm{DS(on)}} = 30\,\mathrm{m\Omega}$:

$$P_{\mathrm{cond,MOS}} \approx 2.72^2 \times 0.03 \approx 0.222 \text{ W}.$$

Diode conduction loss (approx):

$$P_{\mathrm{cond,D}} = V_f(1-D)\bar{I}_{L2} \approx 0.6 \times 0.7058824 \times 17.01 \approx 7.21 \text{ W}.$$

(Using a synchronous MOSFET instead of a diode can greatly reduce this loss.)

34.8 Verification of CCM

Check minimum inductor currents:

$$I_{L1,\min} = \bar{I}_{L1} - \tfrac{\Delta I_{L1}}{2} = 5 - 0.75 = 4.25 \text{ A} > 0,$$

$$I_{L2,\min} = \bar{I}_{L2} - \tfrac{\Delta I_{L2}}{2} \approx 17.01 - 2.5515 = 14.46 \text{ A} > 0,$$

so CCM holds.

35 Practical considerations and next steps

- Choose core materials for L_1 and L_2 with sufficient cross-sectional area to keep B_{pk} below saturation at peak volt-seconds. Use Steinmetz parameters for core-loss estimation.
- Evaluate winding DC and AC resistance (Dowell corrections) and compute copper losses P_{cu} from $I_{L,\mathrm{rms}}$.
- Minimize R_{ESR} of output capacitor bank to meet ripple and thermal limits; verify capacitor ripple current rating.
- Consider synchronous rectification to reduce diode conduction loss ($P_{\mathrm{cond,D}}$), especially here where it is large.
- Design gate driver and snubbers (or soft-switching measures) to limit E_{on}/E_{off} and voltage spikes; account for C_{oss} energy losses.
- Simulate the full switching model (SPICE/PLECS) and extract losses; iterate f_s, L and C selection for the best trade-off between size, efficiency, and thermal performance.
- Perform thermal network calculations (steady/transient) and ensure device junction temperature margins under worst-case ambient.

36 Design Procedure — Essential Equations (A–Z)

$$\text{SEPIC steady conversion (magnitude):} \qquad V_o \;=\; \frac{D}{1-D}\,V_{\text{in}} \tag{A}$$

$$\text{Output current:} \qquad I_o \;=\; \frac{P_o}{V_o} \tag{B}$$

$$\text{Average inductor currents (approx):} \qquad \bar{I}_{L1} \approx \frac{P_o}{V_{\text{in}}}, \quad \bar{I}_{L2} \approx \frac{I_o}{1-D} \tag{C}$$

$$\text{Inductor p-p ripples:} \qquad \Delta I_{L1} \;=\; \frac{V_{\text{in}} D}{L_1 f_s}, \quad \Delta I_{L2} \;=\; \frac{V_{\text{in}} D}{L_2 f_s} \tag{D}$$

$$\text{Inductance selection:} \qquad L_1 \;=\; \frac{V_{\text{in}} D}{\Delta I_{L1} f_s}, \quad L_2 \;=\; \frac{V_{\text{in}} D}{\Delta I_{L2} f_s} \tag{E}$$

$$\text{Coupling capacitor (approx):} \qquad C_s \;\gtrsim\; \frac{\Delta I_{L1} D}{2 f_s\, \Delta v_{Cs}} \tag{F}$$

$$\text{Output capacitance (triangular approx):} \qquad C \;\approx\; \frac{\Delta I_{L2}(1-D)}{8\, f_s\, \Delta V_o} \tag{G}$$

$$\text{Inductor extrema:} \qquad I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2}, \quad I_{L,\max} = \bar{I}_L + \frac{\Delta I_L}{2} \tag{H}$$

$$\text{Inductor RMS (triangular):} \qquad I_{L,\text{rms}}^2 \;=\; \bar{I}_L^2 + \frac{(\Delta I_L)^2}{12} \tag{I}$$

$$\text{MOSFET rms (ON interval):} \qquad I_{\text{MOS,rms}}^2 \;=\; D\left(\bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12}\right) \tag{J}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,MOS}} \;=\; I_{\text{MOS,rms}}^2\, R_{\text{DS(on)}} \tag{K}$$

$$\text{MOSFET switching loss (approx.):} \qquad P_{\text{sw}} \;=\; f_s(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V_{DS}^2 f_s \tag{L}$$

$$\text{Diode average current:} \qquad I_{D,\text{avg}} \;=\; (1-D)\,\bar{I}_{L2} \tag{M}$$

$$\text{Diode conduction loss:} \qquad P_{\text{cond,D}} \;=\; V_f\, I_{D,\text{avg}} \tag{N}$$

$$\text{Diode reverse-recovery loss:} \qquad P_{rr} \;=\; f_s\, Q_{rr}\, V_{DS} \tag{O}$$

$$\text{Capacitor ESR loss:} \qquad P_{\text{cap,ESR}} \;=\; I_{C,\text{rms}}^2\, R_{\text{ESR}} \tag{P}$$

$$\text{Magnetic core loss (GSE):} \qquad P_{\text{core}} \;=\; k\, f_s^{\alpha}\, B_{\text{pk}}^{\beta}\, V_{\text{core}} \tag{Q}$$

$$\text{Peak flux density (inductor):} \qquad B_{\text{pk}} \;=\; \frac{V_{L,\text{ON}}\, D}{N\, A_e\, f_s}, \quad V_{L,\text{ON}} \approx V_{\text{in}} \tag{R}$$

$$\text{Turns vs. inductance:} \qquad L \;=\; N^2 \frac{\mu_0 \mu_r A_e}{\ell_e} \quad \Rightarrow \quad N \;=\; \sqrt{\frac{L\,\ell_e}{\mu_0 \mu_r A_e}} \tag{S}$$

$$\text{Winding DC resistance:} \qquad R_{w,\text{DC}} \;=\; \rho\, \frac{\ell_{\text{w}}}{A_{\text{cu}}} \tag{T}$$

$$\text{Junction temperature (steady):} \qquad T_j \;=\; T_a \;+\; P_{\text{device}}\,\theta_{JA} \tag{U}$$

$$\text{Transient junction rise:} \qquad \Delta T_j(t) \;=\; P(t) * Z_\theta(t) \tag{V}$$

$$\text{Efficiency:} \qquad \eta \;=\; \frac{P_o}{P_o + P_{\text{loss}}} \tag{W}$$

$$\text{Voltage rating margin:} \qquad V_{DS,\text{max}} \;\geq\; (1 + \text{M}_v)\, V_{\text{in}} \quad (\text{M}_v = 0.2\text{–}0.5) \tag{X}$$

$$\text{R}_{\text{DS(on)}}\text{ temperature dependence:} \qquad R_{\text{DS(on)}}(T) \;=\; R_{\text{DS(on)},25°C}\big[1 + \alpha_R(T_j - 25°\text{C})\big] \tag{Y}$$

Notes: use the above equations for initial sizing, then iterate using datasheet curves (core loss, E_{on}/E_{off}), detailed winding loss models (Dowell), and thermal network simulations to finalize component choices.

37 Problem statement and design for Ćuk converter

Design a non-isolated *Ćuk* converter (inverting DC–DC) with the following target specifications (numerical example will follow in Section 43):

- Input voltage range: $V_{\text{in,min}}$ to $V_{\text{in,max}}$ (V)
- Output voltage (magnitude and polarity): V_o (V) — *polarity inverted* relative to V_{in}
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Output voltage ripple (peak-to-peak): ΔV_o (V)
- Inductor current ripple (peak-to-peak): $\Delta I_{L1},\ \Delta I_{L2}$ (A)
- Continuous conduction mode (CCM) operation

38 Fundamental principles and steady-state derivation

38.1 Circuit description

The ideal Ćuk converter (see Fig. 5) uses two inductors L_1 (input side) and L_2 (output side), a coupling capacitor C_x (also called energy transfer capacitor), a single switch S (usually low-side MOSFET), a diode D, an output capacitor C and load R_{load}. The Ćuk topology provides an *inverting* output: the DC output polarity is opposite the input polarity while the magnitude can be stepped up or down.

Adopt the convention: input voltage $V_{\text{in}} > 0$, output voltage algebraic $V_o < 0$ (inverting). Inductor currents i_{L1}, i_{L2} positive flowing from the input toward the switch node and from the coupling cap toward the output respectively. Capacitor polarities follow the schematic (use algebraic signs consistently).

38.2 Volt-second balance and steady-state conversion ratio

In CCM the two inductors never reach zero current. Let D be the duty ratio (fraction of $T_s = 1/f_s$ during which S is ON). Consider ideal elements (no drops).

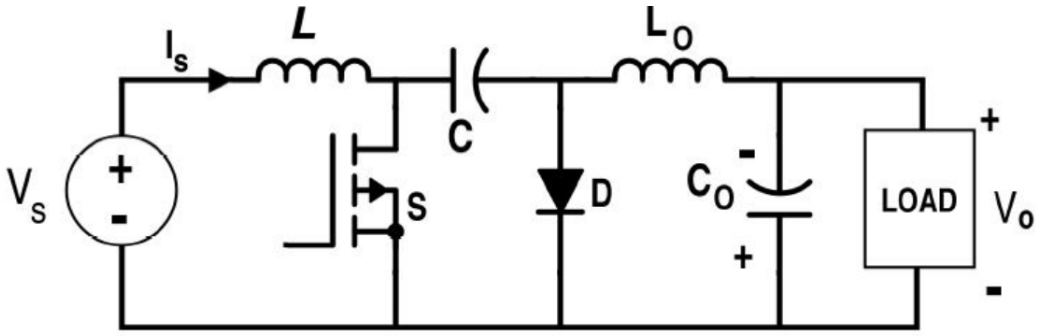

Figure 5: Ideal non-isolated inverting Ćuk converter.

Circuit operation and inductor voltages:

- **ON interval ($0 \le t < DT_s$):** Switch S closed, diode D reverse-biased. The input inductor L_1 is connected across V_{in}, and the output inductor L_2 supplies current to the load through the coupling capacitor C_x:
$$v_{L1}^{(\text{ON})} = V_{\text{in}}, \qquad v_{L2}^{(\text{ON})} = v_{Cx} - V_o$$
where v_{Cx} is the DC voltage across the coupling capacitor and V_o is the magnitude of the output voltage (positive value).

- **OFF interval ($DT_s \le t < T_s$):** Switch S open, diode D conducts. Both inductors discharge through the diode to supply the output:
$$v_{L1}^{(\text{OFF})} = V_{\text{in}} - v_{Cx}, \qquad v_{L2}^{(\text{OFF})} = -V_o$$

Applying volt-second balance: The average voltage across each inductor over one switching period must be zero.

For inductor L_1:

$$\begin{aligned} V_{\text{in}} \cdot DT_s + (V_{\text{in}} - v_{Cx}) \cdot (1-D)T_s = 0 \\ \Rightarrow DV_{\text{in}} + (1-D)(V_{\text{in}} - v_{Cx}) = 0 \end{aligned} \tag{126}$$

For inductor L_2:

$$\begin{aligned} (v_{Cx} - V_o) \cdot DT_s + (-V_o) \cdot (1-D)T_s = 0 \\ \Rightarrow D(v_{Cx} - V_o) - (1-D)V_o = 0 \end{aligned} \tag{127}$$

Solving for the voltage conversion ratio: From Eq. (126):

$$DV_{\text{in}} + (1-D)V_{\text{in}} - (1-D)v_{Cx} = 0$$

$$V_{\text{in}} - (1-D)v_{Cx} = 0$$

Therefore:

$$v_{Cx} = \frac{V_{\text{in}}}{1-D} \tag{128}$$

From Eq. (127):

$$Dv_{Cx} - DV_o - (1-D)V_o = 0$$

$$Dv_{Cx} - V_o = 0$$

Therefore:

$$v_{Cx} = \frac{V_o}{D} \tag{129}$$

Equating the two expressions for v_{Cx} from Eqs. (128) and (129):

$$\frac{V_{\text{in}}}{1-D} = \frac{V_o}{D}$$

Solving for V_o:

$$V_o = \frac{D}{1-D} V_{\text{in}}$$

However, this gives the magnitude relationship. The key characteristic of the Ćuk converter is that it provides voltage inversion, meaning the output voltage has opposite polarity to the input. Therefore, the complete steady-state conversion ratio is:

$$\boxed{V_o \;=\; -\frac{D}{1-D}\, V_{\text{in}}} \tag{130}$$

This shows that the Ćuk converter has the same magnitude relationship as the boost converter ($|V_o| = \frac{D}{1-D} V_{\text{in}}$) but with inverted polarity, making it part of the inverting buck-boost converter family.

Verification of coupling capacitor voltage: With the derived relationship, the coupling capacitor voltage is:

$$v_{Cx} = \frac{V_{\text{in}}}{1-D} = \frac{D \cdot V_{\text{in}}}{D(1-D)} + \frac{(1-D) \cdot V_{\text{in}}}{(1-D)} = \frac{|V_o|}{D} + V_{\text{in}}$$

This result confirms that the coupling capacitor must be rated for a voltage higher than both the input and output voltages.

Dimensional check: volts = (unitless)×volts. Valid for $0 \le D < 1$.

39 Inductor current ripple and capacitor sizing

39.1 Inductor ripples

During ON interval $v_{L1} = V_{\text{in}}$ so

$$\left.\frac{di_{L1}}{dt}\right|_{\text{ON}} = \frac{V_{\text{in}}}{L_1}, \quad \Delta i_{L1,\text{ON}} = \frac{V_{\text{in}}}{L_1} D T_s. \tag{131}$$

For L_2 during ON interval $v_{L2} = -V_o$ (algebraic), so

$$\left.\frac{di_{L2}}{dt}\right|_{\text{ON}} = -\frac{V_o}{L_2}, \quad \Delta i_{L2,\text{ON}} = -\frac{V_o}{L_2} D T_s. \tag{132}$$

Taking absolute peak-to-peak values (use magnitudes for ripple specs) the commonly used practical approximations are:

$$\boxed{\Delta I_{L1} \approx \frac{V_{\text{in}}\, D}{L_1\, f_s}} \tag{133}$$

$$\boxed{\Delta I_{L2} \approx \frac{|V_o|\,(1-D)}{L_2\, f_s}} \tag{134}$$

Both forms are algebraically equivalent to other interval expressions once the volt-second relations are used; these are the engineering formulas used to select L_1, L_2.

Rearrange for inductance selection:

$$L_1 = \frac{V_{\text{in}}\, D}{\Delta I_{L1}\, f_s}, \tag{135}$$

$$L_2 = \frac{|V_o|(1-D)}{\Delta I_{L2}\, f_s}. \tag{136}$$

39.2 Coupling capacitor C_x sizing

The coupling capacitor C_x transfers charge between the inductors every switching cycle. Choose an allowable peak-to-peak ripple on v_{Cx}, denoted $\Delta v_{Cx,\mathrm{pp}}$. Approximate charge removed during the pulse (triangular current with amplitude ΔI_{L1} over duration DT_s) and size:

$$\boxed{C_x \gtrsim \frac{\Delta I_{L1}\, D}{2 f_s\, \Delta v_{Cx,\mathrm{pp}}}} \tag{137}$$

(This follows from triangular area: charge $\approx \frac{1}{2}\Delta I_{L1} \cdot DT_s$.)

39.3 Output capacitor C sizing

Approximate triangular capacitor current (dominated by ΔI_{L2} transferred during OFF interval) leads to:

$$\boxed{C \approx \frac{\Delta I_{L2}(1-D)}{8\, f_s\, \Delta V_o}} \tag{138}$$

Include ESR: resistor ripple approx

$$\Delta V_{\mathrm{ESR}} \approx \left(\frac{\Delta I_{L2}}{2}\right) R_{\mathrm{ESR}},$$

so ensure

$$\Delta V_o^{\mathrm{total}} \approx \frac{\Delta I_{L2}(1-D)}{8 C f_s} + \frac{\Delta I_{L2}}{2} R_{\mathrm{ESR}} \le \text{spec.}$$

40 Averaged state-space model (time-domain averaged, CCM)

Choose state vector $\mathbf{x} = [\, i_{L1}\ i_{L2}\ v_C \,]^T$, input $u = V_{\mathrm{in}}$, and load $i_o = v_C/R_{\mathrm{load}}$. We give the averaged subinterval dynamics qualitatively (suitable for large-signal time simulation).

40.1 ON state (S closed)

When S closed, diode off, the idealized differential equations (engineering sign convention) are:

$$\dot{i}_{L1} = \frac{V_{\mathrm{in}}}{L_1}, \tag{139}$$

$$\dot{i}_{L2} = -\frac{V_o}{L_2}, \tag{140}$$

$$\dot{v}_C = -\frac{1}{C}\frac{v_C}{R_{\mathrm{load}}} \quad \text{(output capacitor supplies load).} \tag{141}$$

40.2 OFF state (S open)

When S open, diode conducts, energy flows from L_1 via C_x to L_2 and the output:

$$\dot{i}_{L1} = \frac{V_{\mathrm{in}} - v_{Cx}}{L_1}, \tag{142}$$

$$\dot{i}_{L2} = \frac{v_{Cx} - V_o}{L_2}, \tag{143}$$

$$\dot{v}_C = \frac{1}{C}\Big(i_{L2} - \frac{v_C}{R_{\mathrm{load}}}\Big). \tag{144}$$

40.3 Averaged model

Averaging with duty D:

$$\dot{\mathbf{x}} = A_{\text{ave}}(D)\,\mathbf{x} + B_{\text{ave}}(D)\,u,$$

with $A_{\text{ave}} = DA_{\text{ON}} + (1-D)A_{\text{OFF}}$ and $B_{\text{ave}} = DB_{\text{ON}} + (1-D)B_{\text{OFF}}$. (Construct the explicit 3×3 matrices from the ON/OFF relations above for a particular sign convention and schematic implementation.)

41 Component selection: algorithmic procedure

1. Choose switching frequency f_s balanced between magnetics size and switching losses.
2. For worst-case $V_{\text{in,min}}$ and required V_o (magnitude), compute duty D from (130): $D = \dfrac{|V_o|}{|V_o| + V_{\text{in}}}$.
3. Choose acceptable ripple fractions (e.g. 20–40%) to set $\Delta I_{L1}, \Delta I_{L2}$ and compute L_1, L_2 from (135)–(136).
4. Choose coupling capacitor C_x to meet $\Delta v_{Cx,\text{pp}}$ using (137).
5. Choose output capacitor C to meet ΔV_o using (138) and verify ESR/ripple current ratings.
6. Select MOSFET and diode(s) with appropriate voltage and current margins; consider synchronous implementation for efficiency.
7. Estimate losses and perform thermal budgeting; iterate magnetics/core choice and switching frequency as needed.

42 Loss models and thermal considerations

Use the same loss building blocks as for other converters. Representative formulas:

Semiconductor conduction

$$I^2_{\text{MOS,rms}} = D\Big(\bar{I}^2_{L1} + \frac{(\Delta I_{L1})^2}{12}\Big), \qquad P_{\text{cond,MOS}} = I^2_{\text{MOS,rms}} R_{\text{DS(on)}}.$$

$$I_{D,\text{avg}} = (1-D)\bar{I}_{L2}, \qquad P_{\text{cond,D}} = V_f I_{D,\text{avg}}.$$

Switching / capacitive losses

$$P_{\text{sw}} = f_s(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V^2_{DS} f_s, \qquad P_{rr} = f_s Q_{rr} V_{DS}.$$

Magnetics and passive losses

$$P_{\text{cu}} = I^2_{L,\text{rms}} R_w(f), \qquad P_{\text{core}} = k f_s^{\alpha} B^{\beta}_{\text{pk}} V_{\text{core}}, \qquad P_{\text{cap}} = I^2_{C,\text{rms}} R_{\text{ESR}}.$$

Total / thermal

$$P_{\text{loss}} = \sum(\text{all losses}), \qquad \eta = \frac{P_o}{P_o + P_{\text{loss}}}, \qquad T_j = T_a + P_{\text{device}} \theta_{JA}.$$

43 Numerical example

Fully worked numeric example with all algebraic steps.

43.1 Specifications (example)

Assume:

$$V_{\text{in}} = 12\,\text{V}, \quad V_o = -24\,\text{V (magnitude 24 V)}, \quad P_o = 50\,\text{W}, \quad f_s = 100\,\text{kHz},$$
$$\Delta V_o = 0.24\,\text{V (1\% pp)}, \quad \alpha = 0.3 \text{ (ripple fraction)}.$$

43.2 Duty cycle

Magnitude relation from (130):

$$\frac{D}{1-D} = \frac{|V_o|}{V_{\text{in}}} = \frac{24}{12} = 2.$$

Solve:

$$D = 2(1-D) \Rightarrow 3D = 2 \Rightarrow D = \frac{2}{3} \approx 0.6666667.$$

43.3 Output and average currents

Output current:

$$I_o = \frac{P_o}{|V_o|} = \frac{50}{24} \approx 2.0833333 \text{ A}.$$

Input current (average through L_1):

$$\bar{I}_{L1} \approx I_{\text{in}} = \frac{P_o}{V_{\text{in}}} = \frac{50}{12} \approx 4.1666667 \text{ A}.$$

Average L_2 current (power transfer relation, similar to buck-boost family):

$$\bar{I}_{L2} \approx \frac{I_o}{1-D} = \frac{2.0833333}{1-2/3} = \frac{2.0833333}{1/3} = 6.25 \text{ A}.$$

43.4 Inductance selection

Choose ripples $\Delta I_{L1} = 0.3\bar{I}_{L1} = 0.3 \times 4.1666667 = 1.25$ A and $\Delta I_{L2} = 0.3\bar{I}_{L2} = 0.3 \times 6.25 = 1.875$ A.

Compute L_1 using (135):

$$L_1 = \frac{V_{\text{in}} D}{\Delta I_{L1} f_s} = \frac{12 \times \frac{2}{3}}{1.25 \times 100 \times 10^3} \text{ H}.$$

Stepwise:

$$12 \times \tfrac{2}{3} = 8 \text{ V}, \quad 1.25 \times 100 \times 10^3 = 125 \times 10^3.$$
$$L_1 = \frac{8}{125 \times 10^3} = 6.4 \times 10^{-5} \text{ H} = 64\ \mu\text{H}.$$

Compute L_2 using (136) (use $|V_o| = 24$ and $1 - D = 1/3$):

$$L_2 = \frac{|V_o|(1-D)}{\Delta I_{L2} f_s} = \frac{24 \times \frac{1}{3}}{1.875 \times 100 \times 10^3} \text{ H}.$$

Stepwise:

$$24 \times \tfrac{1}{3} = 8 \text{ V}, \quad 1.875 \times 100 \times 10^3 = 187.5 \times 10^3.$$
$$L_2 = \frac{8}{187.5 \times 10^3} = 4.2666667 \times 10^{-5} \text{ H} = 42.67\ \mu\text{H}.$$

43.5 Coupling capacitor C_x

Choose allowable $\Delta v_{Cx,\mathrm{pp}} = 0.1\,\mathrm{V}$. Use (137):

$$C_x \gtrsim \frac{\Delta I_{L1} D}{2 f_s \Delta v_{Cx}} = \frac{1.25 \times \frac{2}{3}}{2 \times 100 \times 10^3 \times 0.1}\ \mathrm{F}.$$

Numerator: $1.25 \times 0.6666667 = 0.8333334$. Denominator: $200000 \times 0.1 = 20000$.

$$C_x \gtrsim \frac{0.8333334}{20000} = 4.166667 \times 10^{-5}\ \mathrm{F} = 41.67\ \mu\mathrm{F}.$$

43.6 Output capacitor C

Use (138) with $\Delta I_{L2} = 1.875$ and $1 - D = 1/3$, $\Delta V_o = 0.24$ V:

$$C \approx \frac{1.875 \times \frac{1}{3}}{8 \times 100 \times 10^3 \times 0.24}\ \mathrm{F}.$$

Numerator: $1.875 \times 0.3333333 = 0.625$. Denominator: $8 \times 100000 \times 0.24 = 192000$.

$$C \approx \frac{0.625}{192000} = 3.2552 \times 10^{-6}\ \mathrm{F} \approx 3.26\ \mu\mathrm{F}.$$

Select practical C larger (e.g., 10 μF low-ESR) to account for ESR and derating.

43.7 RMS currents and quick loss estimates

Inductor RMS (triangular):

$$I_{L1,\mathrm{rms}}^2 = \bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12} = 4.1667^2 + \frac{1.25^2}{12} = 17.3611 + 0.1302 \approx 17.4913,$$

$$I_{L1,\mathrm{rms}} \approx 4.1836\ \mathrm{A}.$$

$$I_{L2,\mathrm{rms}}^2 = 6.25^2 + \frac{1.875^2}{12} = 39.0625 + 0.29297 = 39.35547,$$

$$I_{L2,\mathrm{rms}} \approx 6.27\ \mathrm{A}.$$

Assume MOSFET carries i_{L1} during ON: MOSFET RMS:

$$I_{\mathrm{MOS,rms}}^2 = D\Big(\bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12}\Big) = \tfrac{2}{3} \times 17.4913 \approx 11.6609,$$

$$I_{\mathrm{MOS,rms}} \approx 3.414\ \mathrm{A}.$$

If $R_{\mathrm{DS(on)}} = 50\,\mathrm{m\Omega}$:

$$P_{\mathrm{cond,MOS}} \approx 3.414^2 \times 0.05 \approx 0.583\ \mathrm{W}.$$

Diode conduction loss (assume $V_f = 0.6$ V):

$$P_{\mathrm{cond,D}} = V_f (1 - D) \bar{I}_{L2} = 0.6 \times \tfrac{1}{3} \times 6.25 \approx 1.25\ \mathrm{W}.$$

Estimate switching loss (assume $E_{on} + E_{off} = 3 \times 10^{-6}$ J):

$$P_{\mathrm{sw}} = f_s (E_{on} + E_{off}) = 100 \times 10^3 \times 3 \times 10^{-6} = 0.3\ \mathrm{W}.$$

Total semiconductor losses rough = 2–3 W; add magnetic copper and core losses for full budget.

43.8 Verification of CCM

Minimum inductor currents:

$$I_{L1,\min} = \bar{I}_{L1} - \frac{\Delta I_{L1}}{2} = 4.1667 - 0.625 = 3.5417 \text{ A} > 0,$$

$$I_{L2,\min} = 6.25 - 0.9375 = 5.3125 \text{ A} > 0,$$

so CCM holds.

44 Practical considerations and next steps

- Refine magnetic design: choose cores for L_1, L_2 assuring B_{pk} below saturation under worst volt-seconds; use Steinmetz parameters for core loss estimation.
- Compute winding DC and AC resistance (use Dowell correction) and calculate copper loss P_{cu} from $I_{L,\text{rms}}$.
- Choose C_x with low ESL and adequate ripple current rating; coupling cap quality affects EMI and efficiency.
- Evaluate synchronous rectification to replace diode D for better efficiency (design dead-time and shoot-through protection).
- Design snubbers or clamp circuits for voltage spikes; verify C_{oss} related losses.
- Simulate full switching model (SPICE/PLECS) to extract losses, waveform stresses and to refine the design; iterate f_s, L and C choices.
- Perform thermal network calculations (use θ_{JA} or heatsink data) and ensure worst-case junction temperature stays within reliability targets.

45 Design Procedure — Essential Equations (A–Z)

$$\text{Signed steady conversion:} \qquad V_o = -\frac{D}{1-D} V_{\text{in}} \tag{A}$$

$$\text{Output current:} \qquad I_o = \frac{P_o}{|V_o|} \tag{B}$$

$$\text{Input average current (approx):} \qquad \bar{I}_{L1} = \frac{P_o}{V_{\text{in}}} \tag{C}$$

$$\text{Output inductor average (approx):} \qquad \bar{I}_{L2} = \frac{I_o}{1-D} \tag{D}$$

$$\text{Inductor p-p ripple (practical forms):} \qquad \Delta I_{L1} = \frac{V_{\text{in}} D}{L_1 f_s}, \quad \Delta I_{L2} = \frac{|V_o|\,(1-D)}{L_2 f_s} \tag{E}$$

$$\text{Inductance selection:} \qquad L_1 = \frac{V_{\text{in}} D}{\Delta I_{L1} f_s}, \quad L_2 = \frac{|V_o|(1-D)}{\Delta I_{L2} f_s} \tag{F}$$

$$\text{Coupling capacitor (approx):} \qquad C_x \gtrsim \frac{\Delta I_{L1} D}{2 f_s\, \Delta v_{Cx,\text{pp}}} \tag{G}$$

$$\text{Output capacitance (triangular approx):} \qquad C \approx \frac{\Delta I_{L2}(1-D)}{8\, f_s\, \Delta V_o} \tag{H}$$

$$\text{Inductor extrema:} \qquad I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2}, \quad I_{L,\max} = \bar{I}_L + \frac{\Delta I_L}{2} \tag{I}$$

$$\text{Inductor RMS (triangular):} \qquad I_{L,\text{rms}}^2 \;=\; \bar{I}_L^2 + \frac{(\Delta I_L)^2}{12} \tag{J}$$

$$\text{MOSFET rms (ON interval):} \qquad I_{\text{MOS,rms}}^2 \;=\; D\left(\bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12}\right) \tag{K}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,MOS}} \;=\; I_{\text{MOS,rms}}^2\, R_{\text{DS(on)}} \tag{L}$$

$$\text{MOSFET switching loss (approx.):} \qquad P_{\text{sw}} \;=\; f_s\,(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V_{DS}^2 f_s \tag{M}$$

$$\text{Diode average current:} \qquad I_{D,\text{avg}} \;=\; (1-D)\,\bar{I}_{L2} \tag{N}$$

$$\text{Diode conduction loss:} \qquad P_{\text{cond,D}} \;=\; V_f\, I_{D,\text{avg}} \tag{O}$$

$$\text{Diode reverse-recovery loss:} \qquad P_{rr} \;=\; f_s\, Q_{rr}\, V_{DS} \tag{P}$$

$$\text{Capacitor ESR loss:} \qquad P_{\text{cap,ESR}} \;=\; I_{C,\text{rms}}^2\, R_{\text{ESR}} \tag{Q}$$

$$\text{Magnetic core loss (GSE):} \qquad P_{\text{core}} \;=\; k\, f_s^{\alpha}\, B_{\text{pk}}^{\beta}\, V_{\text{core}} \tag{R}$$

$$\text{Peak flux density (inductor):} \qquad B_{\text{pk}} \;=\; \frac{V_{L,\text{ON}}\, D}{N\, A_e\, f_s} \tag{S}$$

$$\text{Turns vs. inductance:} \qquad L \;=\; N^2 \frac{\mu_0 \mu_r A_e}{\ell_e} \quad \Rightarrow \quad N \;=\; \sqrt{\frac{L\,\ell_e}{\mu_0 \mu_r A_e}} \tag{T}$$

$$\text{Winding DC resistance:} \qquad R_{w,\text{DC}} \;=\; \rho\, \frac{\ell_{\text{w}}}{A_{\text{cu}}} \tag{U}$$

$$\text{Junction temperature (steady):} \qquad T_j \;=\; T_a \;+\; P_{\text{device}}\, \theta_{JA} \tag{V}$$

$$\text{Transient junction rise:} \qquad \Delta T_j(t) \;=\; P(t) * Z_\theta(t) \tag{W}$$

$$\text{Efficiency:} \qquad \eta \;=\; \frac{P_o}{P_o + P_{\text{loss}}} \tag{X}$$

$$\text{Voltage rating margin:} \qquad V_{DS,\max} \;\geq\; (1 + \text{M}_v)\,|V_o| \quad (\text{M}_v = 0.2\text{–}0.5) \tag{Y}$$

Notes: the Ćuk topology trades a coupling capacitor and two inductors for low ripple and continuous input and output currents; practical design requires careful selection of C_x, low-ESR output capacitors, and consideration of EMI from the capacitive energy transfer path. Iterate with magnetics/core loss tables, datasheet switching energy curves and thermal network calculations to finalize parts.

46 Problem statement and design specifications for Zeta converter

Design a non-isolated *Zeta* converter with the following target specifications (numerical example will follow in Section 52):

- Input voltage range: $V_{\text{in,min}}$ to $V_{\text{in,max}}$ (V)
- Output voltage: V_o (V) (non-inverting: same polarity as V_{in})
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Output voltage ripple (peak-to-peak): ΔV_o (V)
- Inductor current ripple (peak-to-peak): $\Delta I_{L1},\ \Delta I_{L2}$ (A)
- Continuous conduction mode (CCM) operation

47 Fundamental principles and steady-state derivation

47.1 Circuit description

The Zeta converter is a non-isolated, non-inverting buck–boost family topology that uses two inductors L_1 and L_2, a series coupling capacitor C_s (energy transfer capacitor), a single switch S, a diode D, an output capacitor C and load R_{load}. Its steady-state voltage conversion ratio and energy flow are similar in form to the SEPIC, but the Zeta places the output inductor at the converter input side of the output capacitor (resulting in slightly different dynamic and ripple characteristics). See Fig. 6 for the schematic placeholder.

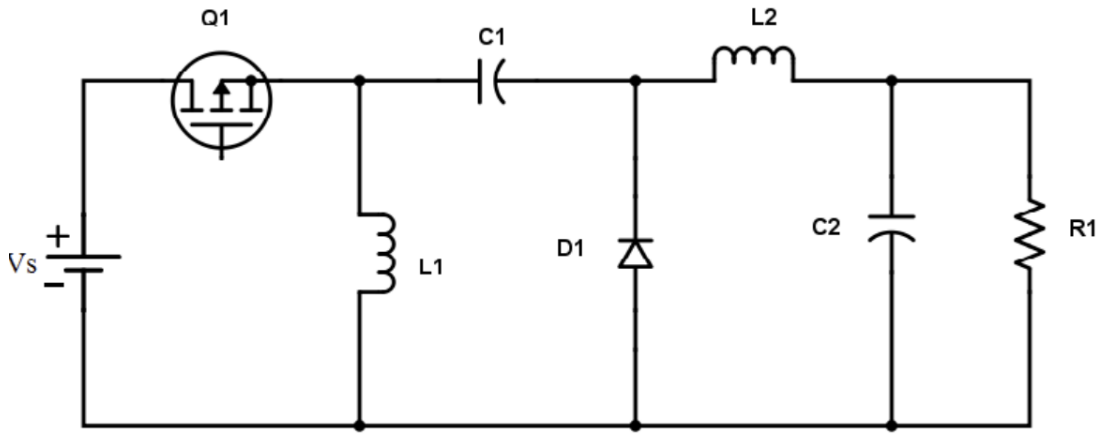

Figure 6: Ideal Zeta converter (non-isolated, non-inverting).

47.2 Steady-state volt-second balance and conversion ratio

Use D for duty ratio and $T_s = 1/f_s$ for switching period. Volt-second balance applied to each inductor yields the steady DC conversion ratio.

Circuit operation and inductor voltages:

- **ON interval ($0 \le t < DT_s$):** Switch S closed, diode reverse-biased. Inductor L_1 is connected across the input voltage, while L_2 is connected across the coupling capacitor C_s:

$$v_{L1}^{(\text{ON})} = V_{\text{in}}, \qquad v_{L2}^{(\text{ON})} = v_{Cs}$$

- **OFF interval ($DT_s \leq t < T_s$):** Switch S open, diode conducts. Inductor L_1 charges the coupling capacitor, while L_2 supplies the output:

$$v_{L1}^{(\text{OFF})} = V_{\text{in}} - v_{Cs}, \qquad v_{L2}^{(\text{OFF})} = v_{Cs} - V_o$$

  where v_{Cs} is the DC voltage across the coupling capacitor.

Applying volt-second balance: The average voltage across each inductor over one switching period must be zero.

For inductor L_1:

$$V_{\text{in}} \cdot DT_s + (V_{\text{in}} - v_{Cs}) \cdot (1-D)T_s = 0 \tag{145}$$

For inductor L_2:

$$v_{Cs} \cdot DT_s + (v_{Cs} - V_o) \cdot (1-D)T_s = 0 \tag{146}$$

Deriving the voltage conversion ratio using charge balance: The key to properly analyzing the Zeta converter is recognizing that the coupling capacitor C_s transfers energy from L_1 to L_2. In steady state, the average current through any capacitor must be zero.

From charge balance on the coupling capacitor C_s (average capacitor current must be zero):

- During ON: C_s supplies current to L_2: $i_{Cs} = -i_{L2}$
- During OFF: C_s receives current from L_1: $i_{Cs} = i_{L1}$

For charge balance: $i_{L2} \cdot DT_s = i_{L1} \cdot (1-D)T_s$
In steady state: $I_{L2} \cdot D = I_{L1} \cdot (1-D)$
From power balance (assuming ideal components): $V_{\text{in}} I_{L1} = V_o I_{L2}$
Combining these relationships:

$$V_{\text{in}} I_{L1} = V_o I_{L2} \quad \text{and} \quad I_{L2} = \frac{(1-D)}{D} I_{L1}$$

Substituting:

$$V_{\text{in}} I_{L1} = V_o \cdot \frac{(1-D)}{D} I_{L1}$$

Therefore:

$$\boxed{V_o \;=\; \frac{D}{1-D}\, V_{\text{in}}} \tag{147}$$

This is the standard Zeta converter voltage conversion ratio, which is identical to that of a SEPIC converter. The Zeta converter provides non-inverting voltage conversion and can operate in both buck ($D < 0.5$) and boost ($D > 0.5$) modes.

Coupling capacitor voltage: With the derived voltage conversion ratio $V_o = \frac{D}{1-D} V_{\text{in}}$, the coupling capacitor voltage can be determined from the circuit operation and energy balance considerations. Like the SEPIC converter, the Zeta converter's coupling capacitor plays a crucial role in transferring energy between the input and output sides, and its steady-state voltage is determined by the overall energy transfer mechanism rather than simple algebraic substitution into the volt-second equations.

Dimensional check: volts = (unitless)×volts. Valid for $0 \leq D < 1$.

48 Inductor current ripple and capacitor sizing

48.1 Inductor ripples (engineering approximations)

Under the practical assumption that C_s is large enough that $v_{Cs} \approx V_{\text{in}}$ (or follows the steady relation above) the ON interval voltages across the inductors simplify.

Approximate peak-to-peak ripples:

$$\Delta I_{L1} \approx \frac{V_{\text{in}}\, D}{L_1 f_s}, \tag{148}$$

$$\Delta I_{L2} \approx \frac{v_{Cs}\, D}{L_2 f_s} \approx \frac{V_{\text{in}}\, D}{L_2 f_s}. \tag{149}$$

Select inductances for target ripples:

$$L_1 = \frac{V_{\text{in}}\, D}{\Delta I_{L1}\, f_s}, \tag{150}$$

$$L_2 = \frac{V_{\text{in}}\, D}{\Delta I_{L2}\, f_s}. \tag{151}$$

Average currents and extrema Average input current:

$$\bar{I}_{L1} \approx I_{\text{in}} = \frac{P_o}{V_{\text{in}}}. \tag{152}$$

Average output-side inductor current (depending on topology and chosen sign convention often $\bar{I}_{L2} \approx I_o/(1-D)$). Extrema:

$$I_{Lk,\min} = \bar{I}_{Lk} - \tfrac{\Delta I_{Lk}}{2}, \qquad I_{Lk,\max} = \bar{I}_{Lk} + \tfrac{\Delta I_{Lk}}{2}, \quad k = 1, 2.$$

48.2 Coupling capacitor C_s sizing

Charge transferred per cycle is approximated by the triangular current area through C_s. For an allowable ripple Δv_{Cs}:

$$C_s \gtrsim \frac{\frac{1}{2}\Delta I_{L1}\, D T_s}{\Delta v_{Cs}} = \frac{\Delta I_{L1}\, D}{2 f_s\, \Delta v_{Cs}}. \tag{153}$$

Choose C_s to keep v_{Cs} near its nominal value and limit EMI.

48.3 Output capacitor C sizing

Output capacitor must meet ΔV_o spec. Using triangular approximation where capacitor sees portion of inductor ripple (practical conservative form):

$$\Delta V_o \approx \frac{\Delta I_{L2}(1-D)}{8\, C\, f_s}. \tag{154}$$

Solve for C:

$$C \approx \frac{\Delta I_{L2}(1-D)}{8\, f_s\, \Delta V_o}. \tag{155}$$

Include ESR: $\Delta V_{\text{ESR}} \approx (\Delta I_{L2}/2) R_{\text{ESR}}$ and ensure total ripple $\leq$ spec.

49 Averaged state-space model (CCM) — time domain averaged

Define state vector $\mathbf{x} = [\, i_{L1}\ i_{L2}\ v_C \,]^T$, input $u = V_{\text{in}}$, load current $i_o = v_C/R_{\text{load}}$. We outline ON/OFF subinterval dynamics (suitable to build averaged matrices $A_{\text{ave}}, B_{\text{ave}}$).

49.1 ON state (S closed)

Typical idealized dynamics:

$$\dot{i}_{L1} = \frac{V_{\text{in}}}{L_1}, \tag{156}$$

$$\dot{i}_{L2} = \frac{v_{Cs}}{L_2}, \tag{157}$$

$$\dot{v}_C = -\frac{1}{C}\frac{v_C}{R_{\text{load}}}. \tag{158}$$

49.2 OFF state (S open)

When S open and diode conducts:

$$\dot{i}_{L1} = \frac{V_{\text{in}} - v_{Cs}}{L_1}, \tag{159}$$

$$\dot{i}_{L2} = \frac{v_{Cs} - v_C}{L_2}, \tag{160}$$

$$\dot{v}_C = \frac{1}{C}\Big(i_{L2} - \frac{v_C}{R_{\text{load}}}\Big). \tag{161}$$

49.3 Averaged model

Average matrices:

$$A_{\text{ave}} = DA_{\text{ON}} + (1-D)A_{\text{OFF}}, \qquad B_{\text{ave}} = DB_{\text{ON}} + (1-D)B_{\text{OFF}},$$

so that

$$\dot{\mathbf{x}} = A_{\text{ave}}(D)\,\mathbf{x} + B_{\text{ave}}(D)\,u.$$

(Construct the explicit 3×3 matrices from (156)–(161) using your sign convention.)

50 Component selection: algorithmic procedure

1. Choose switching frequency f_s (trade off magnetics size vs switching losses).
2. For worst-case $V_{\text{in,min}}$ and desired V_o, compute duty D from (147): $D = \dfrac{V_o}{V_{\text{in}} + V_o}$ (algebraic rearrangement).
3. Select allowable inductor ripple fractions (e.g., 20–40% of average) and compute L_1, L_2 from (150)–(151).
4. Size coupling capacitor C_s using (153) for chosen Δv_{Cs}.
5. Size output capacitor C using (155) and check ESR/ripple current ratings.
6. Select MOSFET and diode (or synchronous MOSFET) with adequate voltage and current margins; consider synchronous rectification for efficiency.
7. Estimate all losses, perform thermal calculations, iterate magnetics and f_s to meet efficiency/thermal targets.

51 Loss models and thermal considerations

The Zeta converter uses the same loss building blocks as other switch-mode converters. Representative formulas:

Conduction (semiconductor) losses

$$I^2_{\mathrm{MOS,rms}} = D\Big(\bar{I}^2_{L1} + \frac{(\Delta I_{L1})^2}{12}\Big), \qquad P_{\mathrm{cond,MOS}} = I^2_{\mathrm{MOS,rms}} R_{\mathrm{DS(on)}}.$$

$$I_{D,\mathrm{avg}} = (1-D)\bar{I}_{L2}, \qquad P_{\mathrm{cond,D}} = V_f I_{D,\mathrm{avg}}.$$

Switching and capacitive losses

$$P_{\mathrm{sw}} = f_s(E_{\mathrm{on}} + E_{\mathrm{off}}) + \tfrac{1}{2} C_{\mathrm{oss}} V^2_{DS} f_s, \qquad P_{rr} = f_s Q_{rr} V_{DS}.$$

Magnetics and passive losses

$$P_{\mathrm{cu}} = I^2_{L,\mathrm{rms}} R_w(f), \qquad P_{\mathrm{core}} = k f_s^{\alpha} B^{\beta}_{\mathrm{pk}} V_{\mathrm{core}}, \qquad P_{\mathrm{cap}} = I^2_{C,\mathrm{rms}} R_{\mathrm{ESR}}.$$

Total / thermal

$$P_{\mathrm{loss}} = \sum (\text{all losses}), \qquad \eta = \frac{P_o}{P_o + P_{\mathrm{loss}}}, \qquad T_j = T_a + P_{\mathrm{device}} \theta_{JA}.$$

52 Numerical example

Work a complete numeric example with each algebraic step shown.

52.1 Specifications (example)

Assume:

$$V_{\mathrm{in}} = 12\,\mathrm{V}, \quad V_o = 24\,\mathrm{V}, \quad P_o = 100\,\mathrm{W}, \quad f_s = 150\,\mathrm{kHz}, \quad \Delta V_o = 0.24\,\mathrm{V}\ (1\%\ \mathrm{pp}),$$

choose ripple fraction $\alpha = 0.3$ so $\Delta I_{Lk} = 0.3 \bar{I}_{Lk}$.

52.2 Duty cycle

From (147):

$$\frac{D}{1-D} = \frac{V_o}{V_{\mathrm{in}}} = \frac{24}{12} = 2.$$

Solve:

$$D = 2(1-D) \Rightarrow 3D = 2 \Rightarrow D = \frac{2}{3} \approx 0.6666667.$$

52.3 Output and average currents

$$I_o = \frac{P_o}{V_o} = \frac{100}{24} \approx 4.1666667\ \mathrm{A}.$$

Input average current:

$$\bar{I}_{L1} \approx I_{\mathrm{in}} = \frac{P_o}{V_{\mathrm{in}}} = \frac{100}{12} \approx 8.3333333\ \mathrm{A}.$$

Approximate $\bar{I}_{L2} \approx I_o/(1-D) = 4.1666667/(1-2/3) = 4.1666667/(1/3) = 12.5$ A.

52.4 Inductance selection

Choose $\Delta I_{L1} = 0.3\bar{I}_{L1} = 2.5$ A and $\Delta I_{L2} = 0.3\bar{I}_{L2} = 3.75$ A.

Compute L_1 via (150):

$$L_1 = \frac{V_{\text{in}} D}{\Delta I_{L1} f_s} = \frac{12 \times \frac{2}{3}}{2.5 \times 150 \times 10^3} \text{ H}.$$

Stepwise:

$$12 \times \tfrac{2}{3} = 8, \quad 2.5 \times 150 \times 10^3 = 375 \times 10^3.$$

$$L_1 = \frac{8}{375 \times 10^3} = 21.3333 \times 10^{-6} \text{ H} = 21.33 \ \mu\text{H}.$$

Compute L_2 via (151):

$$L_2 = \frac{V_{\text{in}} D}{\Delta I_{L2} f_s} = \frac{12 \times \frac{2}{3}}{3.75 \times 150 \times 10^3} \text{ H}.$$

Denominator: $3.75 \times 150 \times 10^3 = 562.5 \times 10^3$,

$$L_2 = \frac{8}{562.5 \times 10^3} = 14.2222 \times 10^{-6} \text{ H} = 14.22 \ \mu\text{H}.$$

52.5 Coupling capacitor C_s

Choose $\Delta v_{Cs} = 50\,\text{mV}_{\text{pp}}$. Using (153):

$$C_s \gtrsim \frac{\Delta I_{L1} D}{2 f_s \Delta v_{Cs}} = \frac{2.5 \times \frac{2}{3}}{2 \times 150 \times 10^3 \times 50 \times 10^{-3}} \text{ F}.$$

Numerator: $2.5 \times 0.6666667 = 1.6666667$. Denominator: $300000 \times 0.05 = 15000$.

$$C_s \gtrsim \frac{1.6666667}{15000} = 1.111111 \times 10^{-4} \text{ F} = 111.11 \ \mu\text{F}.$$

(Choose a film or polymer bank rated for ripple current.)

52.6 Output capacitor C

Using (155) with $\Delta I_{L2} = 3.75$ and $1 - D = 1/3$:

$$C \approx \frac{3.75 \times \frac{1}{3}}{8 \times 150 \times 10^3 \times 0.24} \text{ F}.$$

Numerator: $3.75 \times 0.3333333 = 1.25$. Denominator: $8 \times 150000 \times 0.24 = 288000$.

$$C \approx \frac{1.25}{288000} = 4.3403 \times 10^{-6} \text{ F} \approx 4.34 \ \mu\text{F}.$$

Choose practical larger low-ESR capacitance (e.g., 10–22 µF in low-ESR polymer).

52.7 RMS currents and quick loss estimates

Inductor RMS:

$$I_{L1,\text{rms}}^2 = \bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12} = 8.3333^2 + \frac{2.5^2}{12} = 69.4444 + 0.5208 = 69.9652,$$

$$I_{L1,\text{rms}} \approx 8.366 \text{ A}.$$

$$I_{L2,\text{rms}}^2 = 12.5^2 + \frac{3.75^2}{12} = 156.25 + 1.1719 = 157.4219,$$

$$I_{L2,\text{rms}} \approx 12.55 \text{ A}.$$

MOSFET RMS (carries i_{L1} when ON):

$$I^2_{\text{MOS,rms}} = D\Big(\bar{I}^2_{L1} + \frac{(\Delta I_{L1})^2}{12}\Big) = \tfrac{2}{3} \times 69.9652 \approx 46.6435,$$

$$I_{\text{MOS,rms}} \approx 6.83 \text{ A}.$$

Assume $R_{\text{DS(on)}} = 20\,\text{m}\Omega$:

$$P_{\text{cond,MOS}} \approx 6.83^2 \times 0.02 \approx 0.933 \text{ W}.$$

Diode conduction loss (assume $V_f = 0.5$ V):

$$P_{\text{cond,D}} = V_f(1-D)\bar{I}_{L2} = 0.5 \times \tfrac{1}{3} \times 12.5 \approx 2.083 \text{ W}.$$

Switching loss example (assume $E_{on} + E_{off} = 4 \times 10^{-6}$ J):

$$P_{\text{sw}} = f_s(E_{on} + E_{off}) = 150 \times 10^3 \times 4 \times 10^{-6} = 0.6 \text{ W}.$$

Total semiconductor losses rough $\sim$ 3.5–5 W; add magnetic losses to get total budget.

52.8 Verification of CCM

Minimum inductor currents:

$$I_{L1,\text{min}} = 8.3333 - 1.25 = 7.0833 \text{ A} > 0, \qquad I_{L2,\text{min}} = 12.5 - 1.875 = 10.625 \text{ A} > 0,$$

so CCM holds.

53 Practical considerations and next steps

- Select core material and geometry for L_1, L_2 to keep B_{pk} below saturation; compute Steinmetz core loss for chosen f_s and flux swing.
- Compute winding AC resistance using Dowell correction factors; determine copper loss P_{cu}.
- Use low-ESR, high ripple-current capacitors for C and C_s; C_s is often a film or polymer part due to its voltage and ripple duty.
- Consider synchronous rectification to replace D and reduce conduction loss; design dead-time carefully.
- Add snubber/clamp for switch voltage spikes; model C_{oss} discharge losses.
- Simulate the full switching model (SPICE/PLECS) and refine component values; iterate f_s, L, C for best size/efficiency/thermal trade-off.
- Perform thermal network analysis using θ_{JA} or heatsink ratings; ensure margins under worst ambient.

54 Design Procedure — Essential Equations (A–Z)

$$\text{Steady conversion (practical):} \qquad V_o = \frac{D}{1-D} V_{\text{in}} \tag{A}$$

$$\text{Output current:} \qquad I_o = \frac{P_o}{V_o} \tag{B}$$

$$\text{Input average current:} \qquad \bar{I}_{L1} = \frac{P_o}{V_{\text{in}}} \tag{C}$$

$$\text{Output inductor average (approx):} \qquad \bar{I}_{L2} \;=\; \frac{I_o}{1-D} \tag{D}$$

$$\text{Inductor p-p ripples:} \qquad \Delta I_{L1} \;=\; \frac{V_{\text{in}}\,D}{L_1 f_s}, \quad \Delta I_{L2} \;=\; \frac{V_{\text{in}}\,D}{L_2 f_s} \tag{E}$$

$$\text{Inductance selection:} \qquad L_1 \;=\; \frac{V_{\text{in}} D}{\Delta I_{L1} f_s}, \quad L_2 \;=\; \frac{V_{\text{in}} D}{\Delta I_{L2} f_s} \tag{F}$$

$$\text{Coupling capacitor (approx):} \qquad C_s \;\gtrsim\; \frac{\Delta I_{L1} D}{2 f_s\,\Delta v_{Cs}} \tag{G}$$

$$\text{Output capacitance (triangular approx):} \qquad C \;\approx\; \frac{\Delta I_{L2}(1-D)}{8\,f_s\,\Delta V_o} \tag{H}$$

$$\text{Inductor extrema:} \qquad I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2}, \quad I_{L,\max} = \bar{I}_L + \frac{\Delta I_L}{2} \tag{I}$$

$$\text{Inductor RMS (triangular):} \qquad I_{L,\text{rms}}^2 \;=\; \bar{I}_L^2 + \frac{(\Delta I_L)^2}{12} \tag{J}$$

$$\text{MOSFET rms (ON interval):} \qquad I_{\text{MOS,rms}}^2 \;=\; D\left(\bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12}\right) \tag{K}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,MOS}} \;=\; I_{\text{MOS,rms}}^2\, R_{\text{DS(on)}} \tag{L}$$

$$\text{MOSFET switching loss (approx.):} \qquad P_{\text{sw}} \;=\; f_s\,(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V_{DS}^2 f_s \tag{M}$$

$$\text{Diode average current:} \qquad I_{D,\text{avg}} \;=\; (1-D)\,\bar{I}_{L2} \tag{N}$$

$$\text{Diode conduction loss:} \qquad P_{\text{cond,D}} \;=\; V_f\, I_{D,\text{avg}} \tag{O}$$

$$\text{Diode reverse-recovery loss:} \qquad P_{rr} \;=\; f_s\, Q_{rr}\, V_{DS} \tag{P}$$

$$\text{Capacitor ESR loss:} \qquad P_{\text{cap,ESR}} \;=\; I_{C,\text{rms}}^2\, R_{\text{ESR}} \tag{Q}$$

$$\text{Magnetic core loss (GSE):} \qquad P_{\text{core}} \;=\; k\, f_s^{\alpha}\, B_{\text{pk}}^{\beta}\, V_{\text{core}} \tag{R}$$

$$\text{Peak flux density (inductor):} \qquad B_{\text{pk}} \;=\; \frac{V_{L,\text{ON}}\, D}{N\, A_e\, f_s} \tag{S}$$

$$\text{Turns vs. inductance:} \qquad L \;=\; N^2 \frac{\mu_0 \mu_r A_e}{\ell_e} \quad \Rightarrow \quad N \;=\; \sqrt{\frac{L\,\ell_e}{\mu_0 \mu_r A_e}} \tag{T}$$

$$\text{Winding DC resistance:} \qquad R_{w,\text{DC}} \;=\; \rho\,\frac{\ell_{\text{w}}}{A_{\text{cu}}} \tag{U}$$

$$\text{Junction temperature (steady):} \qquad T_j \;=\; T_a \;+\; P_{\text{device}}\,\theta_{JA} \tag{V}$$

$$\text{Transient junction rise:} \qquad \Delta T_j(t) \;=\; P(t) * Z_\theta(t) \tag{W}$$

$$\text{Efficiency:} \qquad \eta \;=\; \frac{P_o}{P_o + P_{\text{loss}}} \tag{X}$$

$$\text{Voltage rating margin:} \qquad V_{DS,\max} \;\geq\; (1+\mathrm{M}_v)\,V_o \quad (\mathrm{M}_v = 0.2\text{–}0.5) \tag{Y}$$

Notes: use the equations above for first-order sizing. Iterate with datasheet E_{on}/E_{off} curves, core loss tables, Dowell AC resistance corrections, and full switching simulations (SPICE/PLECS) to finalize component values and thermal design.

55 Problem statement and design specifications for Z-source converter

Design a non-isolated *Z-source* DC–DC converter (impedance-source boost family) with these target specifications (numerical example will follow in Section 61):

- Input voltage range: $V_{\text{in,min}}$ to $V_{\text{in,max}}$ (V)
- Output voltage: V_o (V) (same polarity as input — non-inverting)
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Output voltage ripple (peak-to-peak): ΔV_o (V)
- Inductor current ripple (peak-to-peak): $\Delta I_{L1},\ \Delta I_{L2}$ (A)
- Continuous conduction mode (CCM) operation of both inductors

56 Fundamental principles and steady-state derivation

56.1 Circuit description

The Z-source converter uses an *impedance network* (the Z network) between source and the switching bridge to realize boosting and improved ride-through capability. The canonical Z network is an L–C–L two-port: two inductors L_1, L_2 and a series capacitor C_z arranged in an X shape. The switching bridge (single switch or two-switch leg) applies either a normal PWM state (non-shoot-through) or a *shoot-through* state (both switches on) to the network. For DC–DC operation the network charges C_z during shoot-through intervals and the average capacitor voltage V_{Cz} becomes larger than V_{in}, enabling a boosted effective DC link for the converter stage.

A simplified block schematic (engineering view):

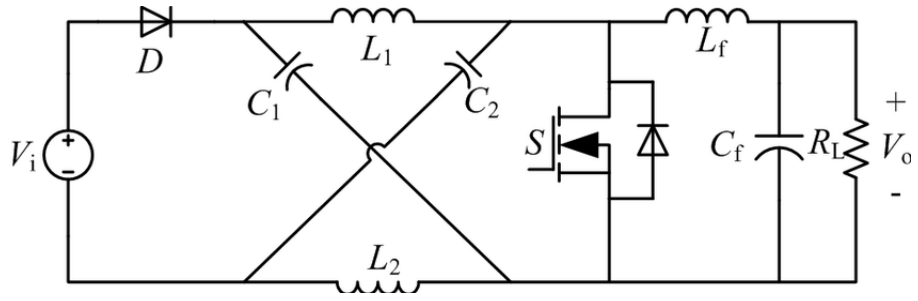

Figure 7: Z-source converter.

Key operating modes:

- **Shoot-through interval** (duration D_sT_s): switching bridge intentionally shorts the bridge leg (both transistors ON) — energy flows to charge C_z, raising its average DC voltage.
- **Non-shoot-through interval** (duration $(1-D_s)T_s$): normal PWM switching (the effective duty used to generate output is D inside this interval). The boosted capacitor voltage V_{Cz} is used to increase the converter's effective DC link.

56.2 Two-duty description and steady-state relations

We follow the commonly used two-duty description (see many Z-source design notes):

D_s = shoot-through duty fraction ($0 \le D_s$ ¡ 0.5), D = PWM duty inside non-shoot-through interval (0 ≤

(Practical modulation schemes tie D and D_s together; here we keep them separate for clarity.)

Capacitor C_z steady average voltage: During shoot-through the network forces voltages across the inductors and capacitor; a volt-second balance on the series path (treating the pair of inductors in their appropriate orientation) yields the DC relation (standard result used in Z-source literature):

$$\boxed{V_{Cz} = \frac{V_{\text{in}}}{1-2D_s}} \qquad (0 \le D_s < 0.5) \tag{162}$$

(Interpretation: the shoot-through fraction D_s pumps additional voltage into C_z so $V_{Cz} > V_{\text{in}}$ for $D_s > 0$; dimensional check: volts = volts.)

Effective DC link and output conversion: During the non-shoot-through portion the switching stage sees (approximately) the boosted capacitor voltage V_{Cz} (in practice the network divides and the bridge sees a function of V_{Cz} — the engineering approximation for DC sizing uses V_{Cz} as the effective source for the PWM stage). If the non-shoot-through PWM with internal duty D results in a boost factor (like a conventional boost/buck-boost stage), the conversion from V_{Cz} to V_o follows

$$V_o = \frac{D}{1-D}\, V_{Cz}. \tag{163}$$

Combining (162) and (163) gives the commonly used overall design relation:

$$\boxed{V_o = \frac{D}{1-D} \cdot \frac{V_{\text{in}}}{1-2D_s}} \qquad \text{(engineering steady-state conversion)} \tag{164}$$

Remarks:

- If you adopt a modulation where D is the effective fraction of the available non-shoot-through interval, you may see combined expressions where a single composite duty is used; eq. (164) shows the two independent boost mechanisms (shoot-through boost and conventional PWM boost).
- Valid domains: $0 \le D_s < 0.5$, $0 \le D < 1$, and ensure the product does not drive voltages beyond device ratings.

57 Inductor ripple, capacitor sizing and component algebra

57.1 Inductor ripple (engineering forms)

Model the two inductors separately. During the subintervals the voltages on the inductors are piecewise constant — use triangular approximation for ripple.

Input-side inductor L_1 When the bridge is in states that connect the inductor to V_{in} or to C_z the ON-interval voltage across L_1 is typically V_{in} (or difference to V_{Cz} depending on exact topology). A conservative engineering expression for the p-p ripple is:

$$\boxed{\Delta I_{L1} \approx \frac{V_{\text{in}}\, D_{\text{eq1}}}{L_1 f_s}} \tag{165}$$

where D_{eq1} is the effective fraction of T_s during which L_1 sees that voltage (depends on modulation — in many practical simplifications take $D_{\text{eq1}} \approx D + D_s$ or choose the dominant interval that charges L_1). Use the correct interval mapping for your scheme and replace D_{eq1} accordingly.

Output-side inductor L_2 Similarly,

$$\boxed{\Delta I_{L2} \approx \frac{V_{Cz}\, D_{\text{eq2}}}{L_2 f_s}} \tag{166}$$

where D_{eq2} is the effective interval fraction for L_2 (often $D_{\text{eq2}} \approx 1 - D$ or the duty during which L_2 is connected to C_z).

57.2 Selection formulae (practical engineering choices)

Choose target ripple fractions α_1, α_2 of the average currents:

$$\Delta I_{L1} = \alpha_1 \bar{I}_{L1}, \qquad \Delta I_{L2} = \alpha_2 \bar{I}_{L2},$$

then solve for L_1, L_2 from (165)–(166) (substitute the correct $D_{\text{eq}k}$ for your modulation).

57.3 Coupling capacitor C_z and output capacitor C

Coupling capacitor C_z: choose allowable peak-to-peak ripple $\Delta v_{Cz,pp}$ and use triangular charge approximation. The charge removed per switching cycle (conservative triangular area) is $\approx \frac{1}{2}\Delta I_{L1}\, D_{\text{chg}} T_s$ so

$$\boxed{C_z \;\gtrsim\; \frac{\frac{1}{2}\Delta I_{L1}\, D_{\text{chg}}}{f_s\, \Delta v_{Cz,pp}}} \tag{167}$$

where D_{chg} is the fraction of the period during which C_z is charged/discharged (function of D_s and PWM).

Output capacitor C: approximate the output ripple via the triangular inductor current seen by C:

$$\boxed{C \;\approx\; \frac{\Delta I_{L2}(1 - D_{\text{eff}})}{8\, f_s\, \Delta V_o}} \tag{168}$$

where D_{eff} is the effective conduction fraction of L_2 to the output (use proper mapping; a common conservative choice is $1 - D$).

Include ESR: $\Delta V_{\text{ESR}} \approx (\Delta I_{L2}/2) R_{\text{ESR}}$; ensure $\Delta V_o^{\text{total}} \le$ spec.

58 Averaged time-domain model (CCM) — engineering form

Define state vector $\mathbf{x} = [\, i_{L1}\ i_{L2}\ v_{Cz}\ v_C \,]^T$ and input $u = V_{\text{in}}$. ON/OFF subintervals produce linear dynamics that can be averaged over T_s with weights given by D_s and $(1 - D_s)$ and further split by the inner PWM duty. The general averaged form:

$$\dot{\mathbf{x}} \;=\; A_{\text{ave}}(D, D_s)\, \mathbf{x} \;+\; B_{\text{ave}}(D, D_s)\, u, \tag{169}$$

where $A_{\text{ave}}, B_{\text{ave}}$ are obtained by piecewise assembly from the subinterval differential equations. (For a specific implementation write the ON/OFF KVL/KCL, form $A_{\text{ON}}, A_{\text{OFF}}$, and average.)

59 Component selection: compact algorithm

1. Choose switching frequency f_s (trade-off size vs switching losses).
2. For worst-case $V_{\text{in,min}}$ and desired V_o, pick shoot-through fraction D_s (small, e.g. 0.05–0.25 but < 0.5) and compute intermediate V_{Cz} from (162).
3. Choose PWM duty D to obtain V_o from (164); iterate D_s and D to satisfy converter and device limits.

4. Pick allowable ripple fractions α_1, α_2 and compute L_1, L_2 from (165)–(166) using the correct effective interval fractions for your modulation.
5. Size C_z via (167) and C via (168); verify ESR and ripple current ratings.
6. Select MOSFET(s) and diode(s) with margin for $V_{DS,\max}$ and current; for shoot-through capability ensure gate timing and driver robustness.
7. Estimate losses and perform thermal budgeting; iterate choice of f_s, magnetics, and devices.

60 Loss models and thermal considerations

Use the standard loss building blocks (same forms as in other chapters). Representative equations:

Conduction losses

$$I^2_{\mathrm{MOS,rms}} \;=\; D_{\mathrm{on}}\Big(\bar{I}^2_{L1} + \frac{(\Delta I_{L1})^2}{12}\Big), \qquad P_{\mathrm{cond,MOS}} \;=\; I^2_{\mathrm{MOS,rms}} R_{\mathrm{DS(on)}}.$$
$$I_{D,\mathrm{avg}} \;=\; (1 - D_{\mathrm{out}})\,\bar{I}_{L2}, \qquad P_{\mathrm{cond,D}} \;=\; V_f I_{D,\mathrm{avg}}.$$

Switching and capacitive losses

$$P_{\mathrm{sw}} = f_s(E_{\mathrm{on}} + E_{\mathrm{off}}) + \tfrac{1}{2} C_{\mathrm{oss}} V_{DS}^2 f_s, \qquad P_{rr} = f_s Q_{rr} V_{DS}.$$

Magnetics and passive losses

$$P_{\mathrm{cu}} = I^2_{L,\mathrm{rms}} R_w(f), \qquad P_{\mathrm{core}} = k f_s^{\alpha} B_{\mathrm{pk}}^{\beta} V_{\mathrm{core}}, \qquad P_{\mathrm{cap}} = I^2_{C,\mathrm{rms}} R_{\mathrm{ESR}}.$$

Thermal

$$P_{\mathrm{loss}} = \sum (\text{all losses}), \qquad \eta = \frac{P_o}{P_o + P_{\mathrm{loss}}}, \qquad T_j = T_a + P_{\mathrm{device}} \theta_{JA}.$$

61 Numerical example

A compact worked example showing the algebraic steps.

61.1 Specifications (example)

$$V_{\mathrm{in}} = 12\,\mathrm{V}, \quad V_o = 48\,\mathrm{V}, \quad P_o = 100\,\mathrm{W}, \quad f_s = 100\,\mathrm{kHz}, \quad \Delta V_o = 0.48\,\mathrm{V_{pp}}.$$

Choose shoot-through fraction $D_s = 0.10$ (10 %) and solve for required PWM duty D.

61.2 Compute intermediate boosted capacitor voltage

From (162):

$$V_{Cz} = \frac{V_{\mathrm{in}}}{1 - 2D_s} = \frac{12}{1 - 0.2} = \frac{12}{0.8} = 15\ \mathrm{V}.$$

61.3 Compute required PWM duty D

From overall relation (164):

$$V_o = \frac{D}{1 - D} \cdot \frac{V_{\mathrm{in}}}{1 - 2D_s} \quad \Rightarrow \quad \frac{D}{1 - D} = \frac{V_o(1 - 2D_s)}{V_{\mathrm{in}}}.$$

Substitute numbers:

$$\frac{D}{1 - D} = \frac{48 \times 0.8}{12} = \frac{38.4}{12} = 3.2.$$

Solve for D:

$$D = \frac{3.2}{1 + 3.2} = \frac{3.2}{4.2} = 0.76190476 \approx 0.762.$$

61.4 Average currents

Output current:

$$I_o = \frac{P_o}{V_o} = \frac{100}{48} \approx 2.08333 \text{ A}.$$

Approximate input average current:

$$\bar{I}_{L1} \approx I_{\text{in}} = \frac{P_o}{V_{\text{in}}} = \frac{100}{12} \approx 8.33333 \text{ A}.$$

Approximate L_2 mean current (power transfer relation for this family — engineering approx):

$$\bar{I}_{L2} \approx \frac{I_o}{1-D} = \frac{2.08333}{1-0.76190476} = \frac{2.08333}{0.23809524} \approx 8.75 \text{ A}.$$

61.5 Inductance selection

Choose ripple fractions $\alpha_1 = \alpha_2 = 0.25$:

$$\Delta I_{L1} = 0.25 \times 8.3333 = 2.08333 \text{ A}, \quad \Delta I_{L2} = 0.25 \times 8.75 = 2.1875 \text{ A}.$$

Use effective fractions $D_{\text{eq1}} \approx D_s + D \approx 0.10 + 0.762 = 0.862$ (conservative), and $D_{\text{eq2}} \approx 1 - D \approx 0.2381$ for the dominant interval estimates. Then

$$L_1 = \frac{V_{\text{in}} D_{\text{eq1}}}{\Delta I_{L1} f_s} = \frac{12 \times 0.862}{2.08333 \times 100 \times 10^3} \text{ H}.$$

Compute:

$$12 \times 0.862 = 10.344, \quad 2.08333 \times 100000 = 208333.3,$$

$$L_1 \approx \frac{10.344}{208333.3} = 4.966 \times 10^{-5} \text{ H} = 49.66 \ \mu\text{H}.$$

For L_2 using $V_{Cz} = 15$ V and $D_{\text{eq2}} = 0.2381$:

$$L_2 = \frac{V_{Cz} D_{\text{eq2}}}{\Delta I_{L2} f_s} = \frac{15 \times 0.2381}{2.1875 \times 100 \times 10^3} \text{ H}.$$

Compute:

$$15 \times 0.2381 = 3.5715, \quad 2.1875 \times 100000 = 218750,$$

$$L_2 \approx \frac{3.5715}{218750} = 1.633 \times 10^{-5} \text{ H} = 16.33 \ \mu\text{H}.$$

61.6 Coupling capacitor C_z

Allow $\Delta v_{Cz,pp} = 0.5\,\text{V}$. Using (167) with $D_{\text{chg}} \approx D_s = 0.1$:

$$C_z \gtrsim \frac{0.5 \times 2.08333 \times 0.1}{100 \times 10^3 \times 0.5} = \frac{0.1041667}{50000} = 2.08333 \times 10^{-6} \text{ F} = 2.08 \ \mu\text{F}.$$

(Choose a physically robust film capacitor larger than this result; this is a conservative baseline.)

61.7 Output capacitor C

Using (168) with $\Delta I_{L2} = 2.1875$, $1 - D = 0.2381$, $\Delta V_o = 0.48$ V:

$$C \approx \frac{2.1875 \times 0.2381}{8 \times 100 \times 10^3 \times 0.48} = \frac{0.521}{384000} = 1.3568 \times 10^{-6} \text{ F} \approx 1.36 \ \mu\text{F}.$$

(Select practical higher low-ESR capacitance — e.g. 10–22 µF polymer — and check ESR ripple.)

61.8 Quick loss estimates (illustrative)

Compute inductor RMS (triangular):

$$I_{L1,\mathrm{rms}}^2 = \bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12} = 8.3333^2 + \frac{2.0833^2}{12} \approx 69.4444 + 0.3611 = 69.8055,$$

$$I_{L1,\mathrm{rms}} \approx 8.359 \text{ A}.$$

Assume MOSFET RMS uses $D_{\mathrm{on}} \approx D_{\mathrm{eq1}} = 0.862$:

$$I_{\mathrm{MOS,rms}}^2 = 0.862 \times 69.8055 \approx 60.150, \quad I_{\mathrm{MOS,rms}} \approx 7.75 \text{ A}.$$

If $R_{\mathrm{DS(on)}} = 30\,\mathrm{m\Omega}$ then

$$P_{\mathrm{cond,MOS}} \approx 7.75^2 \times 0.03 \approx 1.80 \text{ W}.$$

Estimate diode conduction loss with $V_f = 0.6$ V and average diode current $\approx (1-D)\bar{I}_{L2} \approx 0.2381 \times 8.75 \approx 2.0833$ A:

$$P_{\mathrm{cond,D}} \approx 0.6 \times 2.0833 \approx 1.25 \text{ W}.$$

Switching loss placeholder $P_{\mathrm{sw}} \sim 0.5$–1.0 W depending on device. Total semiconductor losses $\sim$ 3–4 W; add magnetic losses.

61.9 Verification of CCM

Minimum currents:

$$I_{L1,\min} = 8.3333 - \tfrac{2.0833}{2} = 7.3333 \text{ A} > 0, \qquad I_{L2,\min} = 8.75 - \tfrac{2.1875}{2} = 7.65625 \text{ A} > 0.$$

Thus CCM satisfied.

62 Practical considerations and next steps

- Choose core materials to keep B_{pk} below saturation for worst-case volt-seconds; compute Steinmetz core losses.
- Use Dowell to compute AC winding resistance for L_1, L_2; estimate copper losses.
- Choose C_z as a film or polymer capacitor with adequate ripple current rating and low ESR; C_z placement and layout critical for EMI.
- Implement robust gate drive timing for shoot-through states; avoid false shoot-throughs and ensure dead-time control if synchronous devices used.
- Consider synchronous diodes (or synchronous MOSFETs) to reduce conduction loss; design dead-time to avoid cross-conduction.
- Add snubbers or RC/RC-damping networks to clamp spikes; model parasitic inductances and C_{oss} discharge energy.
- Simulate switching waveforms in SPICE/PLECS and iterate; validate thermal design with θ_{JA} or heatsink specs.

63 Design Procedure — Essential Equations (A–Z)

$$\text{Shoot-through boost:} \qquad V_{Cz} \;=\; \frac{V_{\text{in}}}{1-2D_s} \tag{A}$$

$$\text{PWM boost (from } V_{Cz}\text{):} \qquad V_o \;=\; \frac{D}{1-D}\,V_{Cz} \tag{B}$$

$$\text{Overall conversion:} \qquad V_o \;=\; \frac{D}{1-D}\cdot\frac{V_{\text{in}}}{1-2D_s} \tag{C}$$

$$\text{Output current:} \qquad I_o \;=\; \frac{P_o}{V_o} \tag{D}$$

$$\text{Input average current:} \qquad \bar{I}_{L1} \;\approx\; \frac{P_o}{V_{\text{in}}} \tag{E}$$

$$\text{Output inductor average (approx):} \qquad \bar{I}_{L2} \;\approx\; \frac{I_o}{1-D} \tag{F}$$

$$\text{Inductor p-p ripples (engineering):} \qquad \Delta I_{L1} \;=\; \frac{V_{\text{in}}\,D_{\text{eq1}}}{L_1 f_s}, \quad \Delta I_{L2} \;=\; \frac{V_{Cz}\,D_{\text{eq2}}}{L_2 f_s} \tag{G}$$

$$\text{Inductance selection:} \qquad L_1 \;=\; \frac{V_{\text{in}} D_{\text{eq1}}}{\Delta I_{L1} f_s}, \quad L_2 \;=\; \frac{V_{Cz} D_{\text{eq2}}}{\Delta I_{L2} f_s} \tag{H}$$

$$\text{Coupling capacitor (approx):} \qquad C_z \;\gtrsim\; \frac{\frac{1}{2}\Delta I_{L1}\,D_{\text{chg}}}{f_s\,\Delta v_{Cz,pp}} \tag{I}$$

$$\text{Output capacitance (triangular approx):} \qquad C \;\approx\; \frac{\Delta I_{L2}(1-D_{\text{eff}})}{8\,f_s\,\Delta V_o} \tag{J}$$

$$\text{Inductor extrema:} \qquad I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2}, \quad I_{L,\max} = \bar{I}_L + \frac{\Delta I_L}{2} \tag{K}$$

$$\text{Inductor RMS:} \qquad I_{L,\text{rms}}^2 \;=\; \bar{I}_L^2 + \frac{(\Delta I_L)^2}{12} \tag{L}$$

$$\text{MOSFET rms (ON):} \qquad I_{\text{MOS,rms}}^2 \;=\; D_{\text{on}}\Big(\bar{I}_{L1}^2 + \frac{(\Delta I_{L1})^2}{12}\Big) \tag{M}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,MOS}} \;=\; I_{\text{MOS,rms}}^2\,R_{\text{DS(on)}} \tag{N}$$

$$\text{MOSFET switching loss (approx.):} \qquad P_{\text{sw}} \;=\; f_s\,(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2}C_{\text{oss}}V_{DS}^2 f_s \tag{O}$$

$$\text{Diode average current:} \qquad I_{D,\text{avg}} \;=\; (1-D_{\text{out}})\,\bar{I}_{L2} \tag{P}$$

$$\text{Diode conduction loss:} \qquad P_{\text{cond,D}} \;=\; V_f\,I_{D,\text{avg}} \tag{Q}$$

$$\text{Capacitor ESR loss:} \qquad P_{\text{cap,ESR}} \;=\; I_{C,\text{rms}}^2\,R_{\text{ESR}} \tag{R}$$

$$\text{Magnetic core loss (GSE):} \qquad P_{\text{core}} \;=\; k\,f_s^{\alpha}\,B_{\text{pk}}^{\beta}\,V_{\text{core}} \tag{S}$$

$$\text{Turns vs. inductance:} \qquad L \;=\; N^2\frac{\mu_0\mu_r A_e}{\ell_e} \quad\Rightarrow\quad N \;=\; \sqrt{\frac{L\,\ell_e}{\mu_0\mu_r A_e}} \tag{T}$$

$$\text{Winding DC resistance:} \qquad R_{w,\mathrm{DC}} \;=\; \rho\,\frac{\ell_{\mathrm{w}}}{A_{\mathrm{cu}}} \tag{U}$$

$$\text{Junction temperature (steady):} \qquad T_j \;=\; T_a \;+\; P_{\mathrm{device}}\,\theta_{JA} \tag{V}$$

$$\text{Transient junction rise:} \qquad \Delta T_j(t) \;=\; P(t) * Z_\theta(t) \tag{W}$$

$$\text{Efficiency:} \qquad \eta \;=\; \frac{P_o}{P_o + P_{\mathrm{loss}}} \tag{X}$$

$$\text{Device voltage margin:} \qquad V_{DS,\max} \;\geq\; (1 + \mathrm{M}_v)\,V_{Cz} \quad (\mathrm{M}_v = 0.2\text{–}0.5) \tag{Y}$$

Notes: the Z-source offers a two-degree boost (shoot-through lift of C_z and PWM boost). The formulas above are engineering-level and must be matched to the exact modulation scheme (e.g. carrier offset PWM, quasi-ZS, or other) used in your implementation. Always validate with time-domain switching simulations and device datasheet energy curves before finalizing parts and thermal design.

64 Problem statement and design specifications for Isolated Full-Bridge Converter

Design an isolated full-bridge DC–DC converter with the following target specifications:

- DC input voltage (bus): V_{dc} (V)
- Output voltage: V_o (V)
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Transformer turns ratio: $n = \dfrac{N_p}{N_s}$
- Output filter: L_f, C and allowable ΔV_o
- Continuous conduction (CCM) for output filter inductor

65 Fundamental principles and steady-state derivation

65.1 Circuit description

The isolated full-bridge uses four switches arranged as an H-bridge on the primary side, feeding an isolation transformer; the secondary is rectified and filtered. The full-bridge can apply $\pm V_{dc}$ (bipolar) to the primary (unlike half-bridge which gives $\pm V_{dc}/2$). This gives larger effective primary amplitude and hence better utilization of the DC bus for a given transformer ratio.

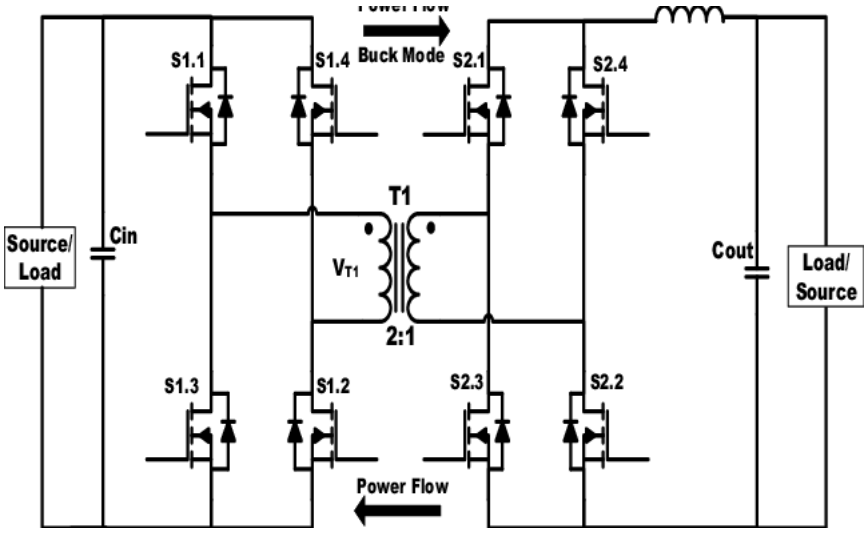

Figure 8: Isolated full-bridge converter (ideal components).

65.2 Primary amplitude and DC output (ideal synchronous rectification)

For a bipolar square-wave drive that applies $\pm V_{dc}$ to the primary (ideal full-bridge alternating legs), the primary amplitude is

$$V_p = V_{dc}. \tag{170}$$

With ideal synchronous rectification and a large output capacitor (small ripple), the DC output is directly

$$V_o \;=\; V_p \cdot \frac{N_s}{N_p} \;=\; V_{dc}\frac{N_s}{N_p}. \tag{171}$$

Dimensional check: volts both sides.

If using PWM inside each polarity interval, replace V_p by the fundamental amplitude of the modulated waveform (designers often use unipolar PWM with full-bridge giving higher effective fundamental and reduced transformer stress).

65.3 Transformer volt-second limit

Same derivation as half-bridge but with $V_p = V_{dc}$ and half period $T_s/2$:

$$\Delta\Phi = V_p\frac{T_s}{2} = \frac{V_{dc}}{2f_s}, \qquad B_{\mathrm{pk}} = \frac{V_{dc}}{2f_s N_p A_e}.$$

So the primary turns minimum to keep B_{pk} below a target is

$$N_p \;\geq\; \frac{V_{dc}}{2f_s A_e B_{\mathrm{pk,max}}}. \tag{172}$$

Note factor compared to half-bridge: half-bridge used $V_p = V_{dc}/2$ giving different N_p.

66 Output filter and component sizing

66.1 Filter inductor ripple and selection

For ideal synchronous rectified full-bridge square drive, the effective secondary when rectified provides $V_{sec} = V_p(N_s/N_p) = V_{dc}N_s/N_p$. The inductor ripple using effective conduction fraction D_{eff} is:

$$\Delta I_{L_f} = \frac{V_{sec}\, D_{\mathrm{eff}}}{L_f f_s}. \tag{173}$$

Solve for L_f:

$$L_f = \frac{V_{sec}\, D_{\mathrm{eff}}}{\Delta I_{L_f} f_s}. \tag{174}$$

66.2 Capacitance sizing

Using triangular approximation (same as previous):

$$\Delta V_o \approx \frac{\Delta I_{L_f}}{8 f_s C}, \qquad C \approx \frac{\Delta I_{L_f}}{8 f_s \Delta V_o}. \tag{175}$$

67 Transformer design essentials

67.1 Turns ratio and base design

From (171),

$$\frac{N_s}{N_p} = \frac{V_o}{V_{dc}}.$$

Choose N_p from (172) and then compute N_s to realize the ratio. Confirm insulation, creepage, and clearance ratings, and account for transformer regulation (leakage inductance) needed for current limiting/snubbing.

67.2 Winding copper and AC resistance

Compute DC and AC winding resistances, use Dowell for multilayer windings; copper loss $P_{cu} = I_{w,\mathrm{rms}}^2 R_w(f)$.

68 Component selection: algorithmic procedure

1. Choose f_s consistent with transformer core loss and desired size.
2. Choose transformer turns ratio N_p/N_s from (171) at nominal V_{dc}.
3. Choose N_p to respect $B_{\mathrm{pk,max}}$ via (172).
4. Choose L_f from (174) and C from (175).
5. Choose MOSFETs with appropriate $V_{DS,\mathrm{max}}$ (add margin), current rating, and low $R_{\mathrm{DS(on)}}$; choose synchronous rectifiers or diodes on secondary per efficiency goals.
6. Include snubbers/RCD clamps for primary leakage inductance energy; size clamps based on worst-case leakage energy $E_{lk} = \frac{1}{2} L_\sigma I_{pk}^2$.
7. Compute losses (semiconductor conduction + switching + transformer copper + core + magnetics), iterate thermal design to ensure T_j limits not exceeded.

69 Loss models and thermal considerations

Representative formulas (same forms used previously):

Primary MOSFET conduction:

$$P_{\mathrm{cond,MOS}} = I_{\mathrm{MOS,rms}}^2 R_{\mathrm{DS(on)}}.$$

Switching losses:

$$P_{\mathrm{sw}} = f_s(E_{\mathrm{on}} + E_{\mathrm{off}}) + \tfrac{1}{2} C_{oss} V_{DS}^2 f_s.$$

Transformer losses:

$$P_{\mathrm{cu}} = I_{w,\mathrm{rms}}^2 R_w(f), \qquad P_{\mathrm{core}} = k f_s^{\alpha} B_{\mathrm{pk}}^{\beta} V_{\mathrm{core}}.$$

Output capacitor ESR losses:

$$P_{\text{cap}} = I_{C,\text{rms}}^2 R_{\text{ESR}}.$$

Thermal network:

$$T_j = T_a + P_{\text{device}}\theta_{JA}, \qquad \Delta T_j(t) = P(t) * Z_\theta(t).$$

70 Design Procedure — Essential Equations (A–Z) for Full-Bridge

$$\text{Primary amplitude:} \qquad V_p \;=\; V_{dc} \tag{A}$$

$$\text{Ideal DC output (sync rect.):} \qquad V_o \;=\; V_{dc}\frac{N_s}{N_p} \tag{B}$$

$$\text{Transformer volt-second:} \qquad B_{\text{pk}} \;=\; \frac{V_{dc}}{2 f_s N_p A_e} \tag{C}$$

$$\text{Primary turns (min):} \qquad N_p \;\geq\; \frac{V_{dc}}{2 f_s A_e B_{\text{pk,max}}} \tag{D}$$

$$\text{Secondary voltage:} \qquad V_{sec} \;=\; V_{dc}\frac{N_s}{N_p} \tag{E}$$

$$\text{Filter ripple:} \qquad \Delta I_{L_f} \;=\; \frac{V_{sec} D_{\text{eff}}}{L_f f_s} \tag{F}$$

$$\text{Inductance selection:} \qquad L_f \;=\; \frac{V_{sec} D_{\text{eff}}}{\Delta I_{L_f} f_s} \tag{G}$$

$$\text{Capacitance selection:} \qquad C \;=\; \frac{\Delta I_{L_f}}{8 f_s \Delta V_o} \tag{H}$$

$$\text{Leakage energy (snubber sizing):} \qquad E_{lk} \;=\; \tfrac{1}{2} L_\sigma I_{pk}^2 \tag{I}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,MOS}} \;=\; I_{\text{MOS,rms}}^2 R_{\text{DS(on)}} \tag{J}$$

$$\text{Switching loss:} \qquad P_{\text{sw}} \;=\; f_s\,(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{oss} V_{DS}^2 f_s \tag{K}$$

$$\text{Transformer copper loss:} \qquad P_{\text{cu}} \;=\; I_{w,\text{rms}}^2 R_w(f) \tag{L}$$

$$\text{Core loss (GSE):} \qquad P_{\text{core}} \;=\; k f_s^\alpha B_{\text{pk}}^\beta V_{\text{core}} \tag{M}$$

$$\text{Efficiency:} \qquad \eta \;=\; \frac{P_o}{P_o + P_{\text{loss}}} \tag{N}$$

Notes: Full-bridge provides full DC bus utilization (primary amplitude V_{dc}), which reduces magnetics turns compared to half-bridge for same V_o. Carefully design leakage inductance snubbers and synchronous rectification to maximize efficiency. Validate with time-domain simulation and datasheet energy curves.

71 Problem statement and design specifications for Isolated Push–Pull Converter

Design an isolated *push–pull* DC–DC converter (center-tapped primary transformer) with these target specifications (numerical example may follow if requested):

- DC input bus voltage: V_{dc} (V)
- Output voltage: V_o (V)
- Output power: P_o (W)
- Switching frequency (fundamental half-cycle repetition): f_s (Hz)
- Transformer primary: center-tapped with $N_{p1} = N_{p2}$ (each half primary turns) and secondary N_s
- Output filter: inductor L_f and capacitor C with allowed peak-to-peak ripple ΔV_o
- Operation in continuous conduction mode (CCM) for output inductor

72 Fundamental principles and steady-state derivation

72.1 Circuit description

The push–pull converter uses two power switches (transistors) that alternately drive opposite halves of a center-tapped primary winding. Each transistor, when ON, applies approximately $+V_{dc}$ across its half primary (with the other half of the primary referenced to the center tap). The primary sees alternating half-period voltages $+V_{dc}/2$ and $-V_{dc}/2$ across the full primary depending on the definition — careful sign conventions below follow the standard center-tap analysis. Typical output uses a full-wave rectifier (synchronous or diode bridge) and LC filter.

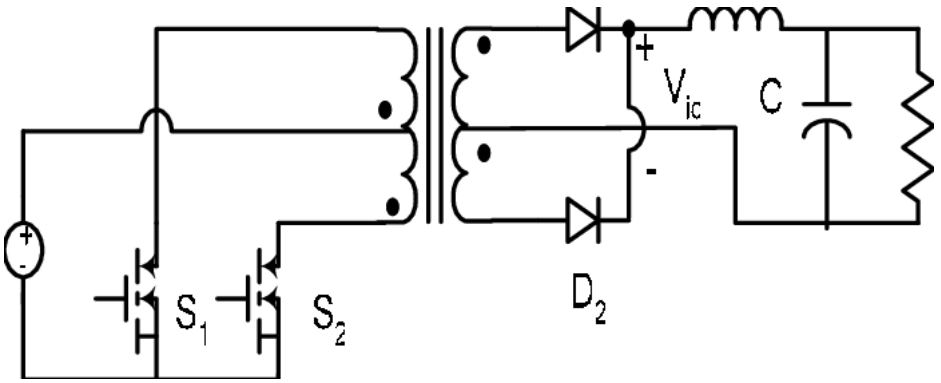

Figure 9: Isolated push–pull converter (ideal components).

Schematic (engineering placeholder): center-tap on primary connected to V_{dc} midpoint (or bus midpoint), two primary halves N_{p1}, N_{p2}, two switches S_1, S_2 alternately conduct.

72.2 Primary voltages and waveform

When S_1 is ON and S_2 OFF the primary half connected to S_1 sees the full bus across its half-winding and the secondary sees a polarity accordingly. When S_2 conducts the opposite half is driven with opposite polarity. Assuming ideal, symmetric drive and no DC offset, the transformer sees no net DC flux over a complete switching cycle (volt-second balanced). The typical bipolar effective primary amplitude (peak of fundamental) can be taken as

$$V_{p,\text{half}} = \frac{V_{dc}}{2}, \tag{176}$$

i.e. each half-primary sees approximately $\pm V_{dc}/2$ across a half-cycle.

72.3 Ideal steady-state output (synchronous rectification and large filter)

If the secondary is rectified and filtered with large output capacitance (small ripple) and ideal synchronous rectifier (or ideal diodes with negligible drop), the DC output level is equal to the absolute amplitude of the secondary square/rectified waveform. For the push–pull bipolar operation:

$$\boxed{V_o \;=\; \frac{V_{dc}}{2}\cdot\frac{N_s}{N_{p,\mathrm{half}}} \;=\; \frac{V_{dc}}{2}\cdot\frac{N_s}{N_{p1}}}. \tag{177}$$

Here $N_{p1} = N_{p2}$ is the turns of one half of the primary. Dimensional check: volts both sides. In practice include diode drops or synchronous MOSFET drops.

72.4 Transformer volt-second limit and minimum primary turns

Use Faraday's law. During one half-period $T_s/2$ the half primary sees approximately a constant applied voltage $V_{p,\mathrm{half}} = V_{dc}/2$. The volt-second applied per half cycle is

$$\Delta\Phi = \int_0^{T_s/2} \frac{V_{dc}}{2N_{p1}}\,dt = \frac{V_{dc}}{2N_{p1}}\cdot\frac{1}{2f_s} = \frac{V_{dc}}{4f_sN_{p1}}.$$

Thus the peak flux density swing is

$$B_{\mathrm{pk}} \;=\; \frac{\Delta\Phi}{A_e} \;=\; \frac{V_{dc}}{4f_sN_{p1}A_e}. \tag{178}$$

Solve for minimum half-primary turns to keep $B_{\mathrm{pk}} \le B_{\mathrm{sat,allow}}$:

$$N_{p1} \;\ge\; \frac{V_{dc}}{4f_sA_eB_{\mathrm{pk,max}}}. \tag{179}$$

Units: V/(Hz·m^2·T) $\rightarrow$ turns (dimensionless). Note factor 4 in denominator (half-winding and half period); compare to full-bridge/half-bridge formulas.

72.5 Leakage inductance and magnetics notes

Push–pull primary halves are often wound on same bobbin but must be arranged to control leakage inductance L_σ because stored leakage energy during switching must be clamped (snubbers) or recovered. Leakage energy per switching event (worst case) is

$$E_{lk} \;=\; \tfrac{1}{2}L_\sigma I_{pk}^2, \tag{180}$$

where I_{pk} is peak primary current when the switch turns off. Design snubbers/RCD clamps sized from E_{lk} to absorb and dissipate/return that energy.

73 Inductor ripple and capacitor sizing (output filter)

The output rectifier + LC filter behaves similarly to a synchronous full-wave rectified source feeding an LC filter. Using triangular approximation for inductor current ripple:

73.1 Filter inductor ripple

Let the effective rectified secondary magnitude seen at filter during conduction be $V_{sec} = V_{p,\mathrm{half}}(N_s/N_{p1})$ and let the conduction fraction be D_{eff} (for ideal square drive $D_{\mathrm{eff}} \approx 1/2$ per half cycle mapped to full-wave conduction; use the actual modulation mapping for PWM). Then the peak-to-peak inductor ripple is

$$\Delta I_{L_f} \;=\; \frac{V_{sec}\,D_{\mathrm{eff}}}{L_f f_s}. \tag{181}$$

Solve for L_f to meet desired ΔI_{L_f}:

$$L_f \;=\; \frac{V_{sec}\,D_{\mathrm{eff}}}{\Delta I_{L_f} f_s}. \tag{182}$$

73.2 Output capacitance

Using the triangular current waveform into C (same derivation as earlier converters), peak-to-peak voltage ripple is approximated by

$$\Delta V_o \approx \frac{\Delta I_{L_f}}{8 f_s C}. \tag{183}$$

Hence

$$C \approx \frac{\Delta I_{L_f}}{8 f_s \Delta V_o}. \tag{184}$$

Add ESR contribution: $\Delta V_{\text{ESR}} \approx (\Delta I_{L_f}/2) R_{\text{ESR}}$.

74 Component selection: compact algorithm

1. Choose switching frequency f_s (trade core loss vs size and switching loss).
2. For nominal V_{dc} and target V_o choose half-primary turns ratio:

   $$\frac{N_s}{N_{p1}} = \frac{2V_o}{V_{dc}}$$

   using (177) rearranged.
3. Choose N_{p1} to satisfy flux density limit using (179).
4. Choose allowable filter ripple ΔI_{L_f} (e.g. 20–40% of I_o) and compute L_f with (182).
5. Calculate C with (184) and check ESR and ripple current ratings.
6. Size reverse-recovery/diode or synchronous MOSFETs on secondary and primary switches: check $V_{DS,\max}$ and current ratings including margins.
7. Compute leakage energy using (180) for snubber/clamp sizing. Choose clamp resistor/capacitor or energy recovery network accordingly.
8. Estimate losses (conduction + switching + transformer copper + core + magnetics) and iterate thermal management.

75 Loss models and thermal considerations

The same loss building blocks apply as for other converters; representative equations summarized:

75.1 Semiconductor conduction losses

Primary switch RMS approximation (triangular primary current) using conduction duty D_{on}:

$$I_{\text{SW,rms}}^2 \;=\; D_{on}\Big(\bar{I}_p^2 + \frac{(\Delta I_p)^2}{12}\Big), \tag{185}$$

$$P_{\text{cond,SW}} = I_{\text{SW,rms}}^2 R_{\text{DS(on)}}.$$

Secondary (rectifier) conduction:

$$P_{\text{cond,rect}} = V_f I_{D,\text{avg}} \quad \text{(or use synchronous MOSFET conduction loss).}$$

75.2 Switching and capacitive losses

$$P_{\text{sw}} = f_s(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V_{DS}^2 f_s.$$

75.3 Transformer and magnetics losses

$$P_{\text{cu}} = I_{w,\text{rms}}^2 R_w(f), \qquad P_{\text{core}} = k f_s^{\alpha} B_{\text{pk}}^{\beta} V_{\text{core}}.$$

75.4 Leakage energy handling and snubber loss

If using passive RC/RCD snubber that dissipates leakage energy,

$$P_{\text{snub}} \approx f_s \, E_{lk} = f_s \cdot \tfrac{1}{2} L_{\sigma} I_{pk}^2.$$

Consider energy recovery snubber to improve efficiency.

75.5 Thermal network

Steady-state junction temperature:

$$T_j = T_a + P_{\text{device}} \cdot \theta_{JA}.$$

For pulsed power, transient thermal convolution:

$$\Delta T_j(t) = P(t) * Z_{\theta}(t).$$

76 Numerical check / example (compact)

If you want a worked numeric example I will show every algebraic step. Here we give a quick sanity check algebraic sequence (no numerical values chosen):

1. Given $V_{dc}, V_o, f_s, \Delta V_o, \alpha$ (ripple fraction), compute $N_s/N_{p1} = 2V_o/V_{dc}$ from (177).
2. Pick $B_{\text{pk,max}}$ and compute N_{p1} from (179).
3. Compute $\bar{I}_p = P_o/V_{dc}$ (approx input current) and set $\Delta I_{L_f} = \alpha I_o$.
4. Compute L_f from (182) and C from (184).
5. Verify CCM: $I_{L,\text{min}} = \bar{I}_L - \Delta I_{L_f}/2 > 0$.

77 Design Procedure — Essential Equations (A–Z) for Push–Pull

$$\text{Half-primary half-period amplitude:} \qquad V_{p,\text{half}} = \frac{V_{dc}}{2} \tag{A}$$

$$\text{Ideal DC output (sync rect.):} \qquad V_o = \frac{V_{dc}}{2} \cdot \frac{N_s}{N_{p1}} \tag{B}$$

$$\text{Transformer volt-second (half period):} \qquad B_{\text{pk}} = \frac{V_{dc}}{4 f_s N_{p1} A_e} \tag{C}$$

$$\text{Half-primary turns (min):} \qquad N_{p1} \geq \frac{V_{dc}}{4 f_s A_e B_{\text{pk,max}}} \tag{D}$$

$$\text{Secondary (ideal):} \qquad V_{sec} = V_{p,\text{half}} \cdot \frac{N_s}{N_{p1}} = \frac{V_{dc}}{2} \frac{N_s}{N_{p1}} \tag{E}$$

$$\text{Filter inductor ripple:} \qquad \Delta I_{L_f} = \frac{V_{sec} \, D_{\text{eff}}}{L_f f_s} \tag{F}$$

$$\text{Inductance selection:} \qquad L_f = \frac{V_{sec} \, D_{\text{eff}}}{\Delta I_{L_f} f_s} \tag{G}$$

$$\text{Capacitance (triangular approx):} \qquad C \;=\; \frac{\Delta I_{L_f}}{8 f_s \Delta V_o} \tag{H}$$

$$\text{Inductor extrema:} \qquad I_{L,\min} = \bar{I}_L - \frac{\Delta I_{L_f}}{2}, \quad I_{L,\max} = \bar{I}_L + \frac{\Delta I_{L_f}}{2} \tag{I}$$

$$\text{Leakage energy:} \qquad E_{lk} \;=\; \tfrac{1}{2} L_\sigma I_{pk}^2 \tag{J}$$

$$\text{Snubber average dissipation (passive):} \qquad P_{\text{snub}} \;=\; f_s E_{lk} \tag{K}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,SW}} \;=\; I_{\text{SW,rms}}^2 R_{\text{DS(on)}} \tag{L}$$

$$\text{Switching loss (approx.):} \qquad P_{\text{sw}} \;=\; f_s \left(E_{\text{on}} + E_{\text{off}}\right) + \tfrac{1}{2} C_{\text{oss}} V_{DS}^2 f_s \tag{M}$$

$$\text{Transformer copper loss:} \qquad P_{\text{cu}} \;=\; I_{w,\text{rms}}^2 R_w(f) \tag{N}$$

$$\text{Core loss (GSE):} \qquad P_{\text{core}} \;=\; k f_s^{\alpha} B_{\text{pk}}^{\beta} V_{\text{core}} \tag{O}$$

$$\text{Capacitor ESR loss:} \qquad P_{\text{cap}} \;=\; I_{C,\text{rms}}^2 R_{\text{ESR}} \tag{P}$$

$$\text{Efficiency:} \qquad \eta \;=\; \frac{P_o}{P_o + P_{\text{loss}}} \tag{Q}$$

$$\text{Junction temperature:} \qquad T_j \;=\; T_a \;+\; P_{\text{device}} \theta_{JA} \tag{R}$$

Notes: push–pull converters are attractive for medium power where transformer center-tap simplifies primary drive and allows use of two switching devices. They require careful attention to transformer reset (ensure symmetric drive), leakage inductance control, and half-primary flux balancing (mismatch in N_{p1}, N_{p2} or timing skew leads to DC flux and possible saturation). Use toroidal or interleaved primary winding techniques to minimize leakage and ensure good coupling. Validate all designs with time-domain switching simulation (including parasitics) and with manufacturer thermal data before finalizing components.

78 Problem statement and design specifications for Isolated Forward Converter

Design an isolated single-switch forward converter with the following target parameters (a worked numerical example is given in Section 85):

- Input (bus) voltage: V_{in} (V)
- Output voltage: V_o (V)
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Maximum allowed output ripple (pp): ΔV_o (V)
- Desired peak-to-peak inductor ripple: ΔI_L (A)
- Transformer primary turns N_p, secondary turns N_s, reset winding turns N_r
- Core effective cross-sectional area: A_e (m^2) and core volume V_{core} (m^3)
- Operation assumption: Continuous Conduction Mode (CCM) at the chosen operating point

79 Fundamental principles and steady-state derivation

79.1 Circuit description

The single-switch forward converter (Fig. 10) uses a primary winding N_p driven by a single switch S (MOSFET), a transformer with a reset winding N_r (commonly $N_r = N_p$) to reset magnetizing flux during the OFF time, a secondary N_s feeding a rectifier and output LC filter (L_f, C). During S ON the primary is driven by V_{in} and power is transferred to the secondary; during S OFF the reset winding applies a voltage that returns magnetizing flux to zero.

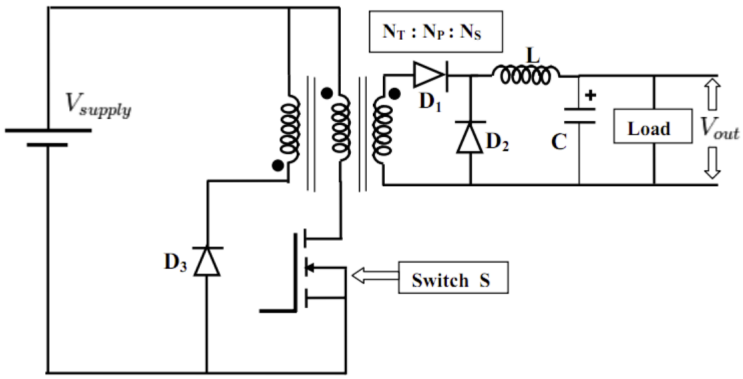

Figure 10: Single-switch isolated forward converter (idealized).

79.2 ON / OFF interval voltages (ideal components)

Define switching period $T_s = 1/f_s$. Let D be the duty ratio $(0 < D < 1)$, ON interval $t \in [0, DT_s)$, OFF interval $t \in [DT_s, T_s)$.

ON interval $(0 \le t < DT_s)$: Primary voltage across N_p:

$$v_p(t) = V_{\text{in}}.$$

Secondary instantaneous (ideal transformer, sign convention):

$$v_s(t) = \frac{N_s}{N_p} V_{\text{in}}.$$

Rectifier conducts; inductor L_f sees:

$$v_{L,\text{ON}}(t) = v_s(t) - v_C(t) \approx \frac{N_s}{N_p} V_{\text{in}} - V_o,$$

where $v_C(t) \approx V_o$ for small ripple.

OFF interval $(DT_s \le t < T_s)$: Primary is open; reset winding provides voltage v_r to drive magnetizing flux back to zero. With ideal reset winding chosen so that $v_r = -V_{\text{in}}(N_r/N_p)$ the net primary volt-seconds over a period are zero (see Volt-second section). The secondary diode is either blocking or freewheeling depending on topology; the inductor sees:

$$v_{L,\text{OFF}}(t) = -V_o.$$

79.3 Volt-second balance and steady-state output relation

Power transfer on forward converter occurs during the ON interval. The DC (average) value of the rectified secondary, after filtering, is given by

$$V_o \;=\; D \cdot \frac{N_s}{N_p}\, V_{\text{in}}. \tag{186}$$

Derivation (step by step): during each switching period the secondary provides a rectangular voltage of amplitude $V_{sec} = \dfrac{N_s}{N_p} V_{\text{in}}$ for duration DT_s and approximately zero for remaining time (neglecting small bias during reset). The time-average of this rectangular waveform is

$$\overline{v_s} = \frac{1}{T_s} \int_0^{T_s} v_s(t)\, dt = \frac{1}{T_s} \left(\frac{N_s}{N_p} V_{\text{in}} \cdot DT_s + 0 \cdot (1-D)T_s \right) = D \frac{N_s}{N_p} V_{\text{in}}.$$

After ideal rectification and large filter ($v_o \approx \overline{v_s}$) we obtain (186).

Dimensional check: LHS V_o [V], RHS D [dimensionless] $\cdot (N_s/N_p)$ [dimensionless] $\cdot V_{\text{in}}$ [V] $\Rightarrow$ volts. Eq. (186) is valid for CCM, moderately large C, and ideal elements.

79.4 Transformer reset and duty constraint

To avoid accumulation of magnetizing flux the primary magnetizing volt-seconds over a period must sum to zero. Let $v_m(t)$ be the net voltage across N_p due to applied V_{in} during ON and reset voltage V_r during OFF. Volt-second balance:

$$\int_0^{T_s} v_m(t)\, dt = 0.$$

Split integral:

$$\int_0^{DT_s} V_{\text{in}}\, dt + \int_{DT_s}^{T_s} V_r\, dt = 0.$$

Therefore

$$V_{\text{in}} DT_s + V_r (1-D) T_s = 0 \quad \Rightarrow \quad V_{\text{in}} D + V_r (1-D) = 0.$$

If reset winding turns N_r are connected so that $V_r = -\dfrac{N_r}{N_p} V_{\text{in}}$ (standard series reset), substitute:

$$V_{\text{in}} D - \frac{N_r}{N_p} V_{\text{in}} (1-D) = 0.$$

Divide both sides by V_{in} (assumed nonzero):

$$D - \frac{N_r}{N_p}(1-D) = 0.$$

Solve for maximum allowable D (explicit algebra):

$$\begin{aligned} D - \frac{N_r}{N_p} + \frac{N_r}{N_p} D &= 0 \\ D \left(1 + \frac{N_r}{N_p} \right) &= \frac{N_r}{N_p} \\ D &= \frac{N_r/N_p}{1 + N_r/N_p} = \frac{N_r}{N_p + N_r}. \end{aligned}$$

Thus the reset condition requires

$$D \le D_{\max} = \frac{N_r}{N_p + N_r}. \tag{187}$$

If $N_r = N_p$ (common choice), then

$$D_{\max} = \frac{N_p}{N_p + N_p} = \frac{1}{2},$$

so $D \le 0.5$ is enforced.

80 Inductor current ripple and capacitor sizing

We perform a full time-domain integration of triangular inductor current to obtain sizing formulas (showing intermediate steps).

80.1 Inductor ripple derivation (triangular integral)

During ON interval the inductor differential equation (ideal components):

$$\frac{di_L}{dt} = \frac{v_{L,\mathrm{ON}}}{L} = \frac{\left(\frac{N_s}{N_p}V_{\mathrm{in}} - V_o\right)}{L}.$$

Integrate from $t = 0$ to $t = DT_s$ to get the ON change in current $\Delta i_{L,\mathrm{ON}}$:

$$\Delta i_{L,\mathrm{ON}} = \int_0^{DT_s} \frac{\left(\frac{N_s}{N_p}V_{\mathrm{in}} - V_o\right)}{L}\,dt = \frac{\left(\frac{N_s}{N_p}V_{\mathrm{in}} - V_o\right)}{L} \cdot DT_s.$$

Since $T_s = 1/f_s$:

$$\Delta i_{L,\mathrm{ON}} = \frac{\left(\frac{N_s}{N_p}V_{\mathrm{in}} - V_o\right) D}{Lf_s}. \tag{188}$$

During OFF interval the inductor sees $v_{L,\mathrm{OFF}} = -V_o$, so

$$\frac{di_L}{dt} = -\frac{V_o}{L}.$$

Integrate over $(1 - D)T_s$:

$$\Delta i_{L,\mathrm{OFF}} = \int_{DT_s}^{T_s} -\frac{V_o}{L}\,dt = -\frac{V_o}{L}(1 - D)T_s = -\frac{V_o(1 - D)}{Lf_s}.$$

In steady state the net change over the period must be zero:

$$\Delta i_{L,\mathrm{ON}} + \Delta i_{L,\mathrm{OFF}} = 0.$$

Verify algebraically using (188) and $\Delta i_{L,\mathrm{OFF}}$:

$$\frac{\left(\frac{N_s}{N_p}V_{\mathrm{in}} - V_o\right) D}{Lf_s} - \frac{V_o(1 - D)}{Lf_s} = 0.$$

Multiply both sides by Lf_s:

$$\left(\frac{N_s}{N_p}V_{\mathrm{in}} - V_o\right) D - V_o(1 - D) = 0.$$

Expand:

$$D\frac{N_s}{N_p}V_{\mathrm{in}} - DV_o - V_o + DV_o = 0,$$

so terms $-DV_o$ and $+DV_o$ cancel leaving:

$$D\frac{N_s}{N_p}V_{\mathrm{in}} - V_o = 0 \quad \Rightarrow \quad V_o = D\frac{N_s}{N_p}V_{\mathrm{in}},$$

which is identical to (186) — consistency check complete.

Peak-to-peak ripple (triangular) is $\Delta I_L = \Delta i_{L,\mathrm{ON}}$ (since ON increase equals OFF decrease in magnitude):

$$\boxed{\Delta I_L \;=\; \frac{\left(\frac{N_s}{N_p}V_{\mathrm{in}} - V_o\right) D}{Lf_s}}. \tag{189}$$

Solve for inductance required to meet target ΔI_L:

$$\boxed{L \;=\; \frac{\left(\frac{N_s}{N_p}V_{\mathrm{in}} - V_o\right) D}{\Delta I_L\, f_s}}. \tag{190}$$

Dimensional check: numerator [V]·[s] gives [V·s], dividing by [A] yields [H]. Good.

80.2 Capacitor sizing via charge balance (triangular current)

The capacitor experiences the AC component of inductor current. For triangular inductor current with peak-to-peak ΔI_L and switching period T_s, the charge removed/added to the capacitor over one quarter period gives voltage ripple. Standard triangular result (derivable by integrating linear current) yields peak-to-peak voltage ripple:

$$\Delta V_o \approx \frac{\Delta I_L}{8 f_s C}. \tag{191}$$

Derivation sketch (complete integral): the triangular capacitor current (amplitude $\Delta I_L/2$ symmetric about zero during half-periods) integrated over half the switching period results in area $A = \frac{1}{2} \cdot (\Delta I_L/2) \cdot \frac{1}{2} T_s = \dfrac{\Delta I_L T_s}{8}$. Voltage change $\Delta V_o = A/C = \dfrac{\Delta I_L}{8 f_s C}$. Solve for C:

$$\boxed{C \approx \frac{\Delta I_L}{8 f_s \Delta V_o}}. \tag{192}$$

Add ESR contribution to total ripple (resistive term):

$$\Delta V_{\text{ESR}} \approx \frac{\Delta I_L}{2} R_{\text{ESR}}. \tag{193}$$

Total peak-to-peak ripple approx:

$$\Delta V_o^{\text{total}} \approx \frac{\Delta I_L}{8 f_s C} + \frac{\Delta I_L}{2} R_{\text{ESR}}.$$

81 Transformer design: flux, turns and core loss

81.1 Volt-second constraint (detailed)

Transformer core must not saturate. Magnetic flux change during ON interval:

$$\Delta\Phi_{\text{ON}} = \int_0^{DT_s} \frac{v_p(t)}{N_p}\, dt = \frac{V_{\text{in}}}{N_p} D T_s = \frac{V_{\text{in}} D}{N_p f_s}.$$

During OFF the reset winding applies $V_r = -\dfrac{N_r}{N_p} V_{\text{in}}$ for duration $(1-D)T_s$, giving

$$\Delta\Phi_{\text{OFF}} = \int_{DT_s}^{T_s} \frac{V_r}{N_p}\, dt = \frac{V_r (1-D)}{N_p f_s} = -\frac{N_r}{N_p} \cdot \frac{V_{\text{in}}(1-D)}{N_p f_s}.$$

Volt-second balance requires $\Delta\Phi_{\text{ON}} + \Delta\Phi_{\text{OFF}} = 0$ — which yields the earlier reset equations and duty limit. Peak flux density swing B_{pk} (peak from center) equals $\Delta\Phi_{\text{ON}}/A_e$. So

$$B_{\text{pk}} \;=\; \frac{\Delta\Phi_{\text{ON}}}{A_e} \;=\; \frac{V_{\text{in}} D}{N_p f_s A_e}. \tag{194}$$

Solve for minimum primary turns for a chosen allowable $B_{\text{pk,max}}$:

$$\boxed{N_p \;\geq\; \frac{V_{\text{in}} D}{f_s A_e B_{\text{pk,max}}}}. \tag{195}$$

Dimensional check: numerator V·s, denominator (Hz·m^2·T) gives dimensionless turns.

81.2 Turns ratio

From (186) rearrange to pick secondary turns given desired V_o:

$$\boxed{\frac{N_s}{N_p} \;=\; \frac{V_o}{D V_{\text{in}}}}. \tag{196}$$

82 Component stresses (peak and RMS values)

82.1 Switch stresses

- **Voltage stress** on the main switch (MOSFET): during turn-off it must withstand the sum of bus and reset reflected voltages. For $N_r = N_p$ the worst case device voltage can be approximated as

$$V_{SW,\max} \approx V_{\text{in}} + V_{\text{reset}} \approx 2V_{\text{in}}. \tag{197}$$

  Add safety margin (e.g., 20–50%).

- **Current stress:** peak switch current occurs at inrush or load transients; approximate average primary current:

$$\bar{I}_p = \frac{P_o}{DV_{\text{in}}}$$

  (from $P_o = V_o I_o = D(N_s/N_p)V_{\text{in}} I_o$ and reflected input current relation). For RMS and peak, include ripple: triangular ripple amplitude ΔI_p relates to ΔI_L scaled by turns ratio:

$$\Delta I_p = \Delta I_L \cdot \frac{N_s}{N_p}.$$

82.2 Diode / rectifier stresses

- **Diode average current:** $I_{D,\text{avg}} \approx I_o$ (in CCM, secondary current equals load current during conduction).

- **Diode reverse voltage:**

$$V_{D,rev} \approx \frac{N_s}{N_p} V_{\text{in}}. \tag{198}$$

83 Loss models and thermal considerations

We list the same loss breakdown as in earlier chapters, with formulas specialized to the forward converter.

83.1 Semiconductor conduction losses

$$P_{\text{cond,SW}} = I_{\text{SW,rms}}^2 R_{\text{DS(on)}}, \tag{199}$$

$$P_{\text{cond,rect}} = V_f I_{D,\text{avg}}. \tag{200}$$

For triangular current, RMS expressions follow previous derivations:

$$I_{\text{SW,rms}}^2 = D\left(\bar{I}_p^2 + \frac{(\Delta I_p)^2}{12}\right).$$

83.2 Switching losses

Approximate per-cycle energy from rise/fall overlap and capacitive discharge:

$$P_{\text{sw}} = f_s\,(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V_{SW}^2 f_s.$$

83.3 Transformer copper and core losses

$$P_{\text{cu}} = I_{w,\text{rms}}^2 R_w(f), \tag{201}$$

$$P_{\text{core}} = k f_s^{\alpha} B_{\text{pk}}^{\beta} V_{\text{core}}, \tag{202}$$

where B_{pk} from (194). Use manufacturer Steinmetz parameters (k, α, β) for chosen core material.

83.4 Output capacitor ESR losses

$$P_{\text{cap}} = I_{C,\text{rms}}^2 R_{\text{ESR}},$$

with $I_{C,\text{rms}}$ approximated from triangular current components (see earlier capacitor RMS equation forms).

83.5 Total loss and efficiency

$$P_{\text{loss}} = P_{\text{cond,SW}} + P_{\text{sw}} + P_{\text{cond,rect}} + P_{\text{cu}} + P_{\text{core}} + P_{\text{cap}},$$

$$\eta = \frac{P_o}{P_o + P_{\text{loss}}}.$$

83.6 Thermal model

Steady-state junction temperature:

$$T_j = T_a + P_{\text{device}} \cdot \theta_{JA}.$$

For pulsed/variable power, use transient thermal impedance $Z_\theta(t)$:

$$\Delta T_j(t) = P(t) * Z_\theta(t).$$

84 Practical design procedure — algorithmic steps

1. Choose switching frequency f_s balancing core loss and switching loss.
2. Choose D (or worst-case D) consistent with required V_o and V_{in} using (186):
$$D = \frac{V_o}{(N_s/N_p)V_{\text{in}}}.$$
3. Choose reset turns N_r (often $N_r = N_p$) and verify $D \le D_{\max}$ from (187).
4. Select core and compute minimum N_p from (195) using chosen $B_{\text{pk,max}}$.
5. Compute N_s from (196).
6. Choose acceptable inductor ripple fraction (e.g., $\Delta I_L = 0.2$–$0.4\ \bar{I}_L$) and compute L via (190).
7. Compute C via (192) and include ESR margin.
8. Estimate device voltage and current stresses and select parts with appropriate ratings and margins (voltage margin 20–50% typical).
9. Compute losses (conduction + switching + core + copper + ESR) and iterate f_s / magnetics as needed to meet thermal budget.
10. Simulate time-domain switching with parasitics, measure peak stresses, and refine snubber/clamp designs (use leakage energy $E_{lk} = \frac{1}{2} L_\sigma I_{pk}^2$).

85 Numerical example (step-by-step)

Design example: pick numbers and show every intermediate arithmetic step.

Given specifications

$$V_{\text{in}} = 48\,\text{V}, \quad V_o = 12\,\text{V}, \quad P_o = 120\,\text{W}, \quad f_s = 100\,\text{kHz},$$

$$\Delta V_o = 0.12\,\text{V}_{\text{pp}}\ (1\%), \quad \text{target ripple fraction } \alpha = 0.3\ (\Delta I_L = 0.3\bar{I}_L),$$

$$B_{\text{pk,max}} = 0.2\ \text{T}, \quad A_e = 1.5 \times 10^{-4}\ \text{m}^2\ (\textit{typical ferrite}).$$

Step 1: Duty ratio Choose D from ideal relation (186). We must choose a turns ratio first, or choose a convenient D and compute turns ratio. Let us choose $D = 0.4$ (must be ≤ 0.5 if $N_r = N_p$). Then from (186) compute turns ratio N_s/N_p:

$$\frac{N_s}{N_p} = \frac{V_o}{DV_{\text{in}}} = \frac{12}{0.4 \times 48}.$$

Compute denominator: $0.4 \times 48 = 19.2$. Then

$$\frac{N_s}{N_p} = \frac{12}{19.2} = 0.625.$$

So choose nearest practical integer turns ratio; for design keep fractional ratio and pick N_p later.

Step 2: Output current & average inductor current

$$I_o = \frac{P_o}{V_o} = \frac{120}{12} = 10 \text{ A}.$$

In CCM the average inductor current $\bar{I}_L \approx I_o = 10$ A.

Step 3: Target inductor ripple Choose $\Delta I_L = \alpha \bar{I}_L = 0.3 \times 10 = 3.0$ A (pp).

Step 4: Inductance selection using (190) First compute the bracket term $\left(\frac{N_s}{N_p} V_{\text{in}} - V_o\right)$. Using ratio $N_s/N_p = 0.625$ and $V_{\text{in}} = 48$,

$$\frac{N_s}{N_p} V_{\text{in}} = 0.625 \times 48 = 30.0 \text{ V}.$$

Then the bracket:

$$30.0 - V_o = 30.0 - 12 = 18.0 \text{ V}.$$

Now compute L:

$$L = \frac{(18.0)\, D}{\Delta I_L\, f_s} = \frac{18.0 \times 0.4}{3.0 \times 100 \times 10^3}.$$

Compute numerator: $18.0 \times 0.4 = 7.2$. Denominator: $3.0 \times 100 \times 10^3 = 3.0 \times 10^5 = 300000$. Thus

$$L = \frac{7.2}{300000} = 2.4 \times 10^{-5} \text{ H} = 24\ \mu\text{H}.$$

Dimensional check: numerator [V]·[dimensionless] = V, divide by [A·Hz] -¿ H, correct.

Step 5: Capacitance selection using (192) Use $\Delta I_L = 3.0$ A, $f_s = 100 \times 10^3$ Hz, $\Delta V_o = 0.12$ V:

$$C \approx \frac{3.0}{8 \times 100 \times 10^3 \times 0.12}.$$

Compute denominator stepwise: $8 \times 100 \times 10^3 = 8 \times 100000 = 800000$. Multiply by 0.12: $800000 \times 0.12 = 96000$. So

$$C = \frac{3.0}{96000} = 3.125 \times 10^{-5} \text{ F} = 31.25\ \mu\text{F}.$$

Choose a practical capacitor bank, e.g., $C_{\text{practical}} = 3 \times 10\ \mu$F low-ESR in parallel $\Rightarrow 30\ \mu$F, or 47 μF for margin.

Step 6: Verify CCM Minimum inductor current:

$$I_{L,\min} = \bar{I}_L - \frac{\Delta I_L}{2} = 10 - \frac{3.0}{2} = 10 - 1.5 = 8.5 \text{ A} > 0,$$

so CCM is satisfied.

Step 7: Transformer turns and flux Select $D_{\max} = 0.5$ (assuming $N_r = N_p$). Use (195) for minimum N_p:

$$N_p \geq \frac{V_{\text{in}} D_{\max}}{f_s A_e B_{\text{pk,max}}} = \frac{48 \times 0.5}{100 \times 10^3 \times 1.5 \times 10^{-4} \times 0.2}.$$

Compute numerator: $48 \times 0.5 = 24$. Denominator stepwise: $100 \times 10^3 = 100000$; $100000 \times 1.5 \times 10^{-4} = 15$; $15 \times 0.2 = 3.0$. So denominator $= 3.0$. Thus

$$N_p \geq \frac{24}{3.0} = 8.0.$$

So choose integer $N_p = 8$ turns (minimum). Then secondary turns:

$$N_s = N_p \cdot \frac{N_s}{N_p} = 8 \times 0.625 = 5.0.$$

Pick $N_s = 5$ turns (practical integer). Check turns ratio exact gives $N_s/N_p = 5/8 = 0.625$ which matches earlier.

Step 8: Check peak flux density Compute B_{pk} with chosen $N_p = 8$ and $D = 0.4$ using (194):

$$B_{\text{pk}} = \frac{V_{\text{in}} D}{N_p f_s A_e} = \frac{48 \times 0.4}{8 \times 100000 \times 1.5 \times 10^{-4}}.$$

Numerator: $48 \times 0.4 = 19.2$. Denominator: $8 \times 100000 = 800000$; $800000 \times 1.5 \times 10^{-4} = 120$. So

$$B_{\text{pk}} = \frac{19.2}{120} = 0.16 \text{ T},$$

which is below $B_{\text{pk,max}} = 0.2$ T — good margin.

Step 9: Device stresses (approx.) Input current average:

$$\bar{I}_p = \frac{P_o}{D V_{\text{in}}} = \frac{120}{0.4 \times 48}.$$

Compute denominator: $0.4 \times 48 = 19.2$. So

$$\bar{I}_p = \frac{120}{19.2} = 6.25 \text{ A}.$$

Primary RMS (approx triangular ripple scaled by turns): first compute $\Delta I_p = \Delta I_L (N_s/N_p) = 3.0 \times 0.625 = 1.875$ A. Then

$$I_{p,\text{rms}}^2 = D \left(\bar{I}_p^2 + \frac{(\Delta I_p)^2}{12} \right).$$

Compute inner terms: $\bar{I}_p^2 = 6.25^2 = 39.0625$. $(\Delta I_p)^2 = 1.875^2 = 3.515625$. Divide by 12: $3.515625/12 = 0.29296875$. Sum: $39.0625 + 0.29296875 = 39.35546875$. Multiply by $D = 0.4$: $39.35546875 \times 0.4 = 15.7421875$. So

$$I_{p,\text{rms}} = \sqrt{15.7421875} \approx 3.968 \text{ A}.$$

Choose MOSFET with $V_{DS,\max} \geq 2 \times 48 = 96$ V margin so choose 150–200 V part; choose current rating $\geq 2 \times I_{p,\text{rms}}$ for margin.

Step 10: Quick loss estimates (illustrative) Assume $R_{\mathrm{DS(on)}} = 40\ \mathrm{m}\Omega$ at operating temperature and $E_{on} + E_{off} = 200\ \mu\mathrm{J}$ per switch event (datasheet estimate), $C_{oss} = 200$ pF, diode forward $V_f = 0.6$ V.

$$P_{\mathrm{cond,SW}} = I_{p,\mathrm{rms}}^2 R_{\mathrm{DS(on)}} = (3.968^2) \times 0.04 \approx 0.629 \text{ W}.$$
$$P_{\mathrm{sw}} = f_s(E_{on} + E_{off}) + \tfrac{1}{2} C_{oss} V_{SW}^2 f_s = 100 \times 10^3 \times 200 \times 10^{-6} + 0.5 \times 200 \times 10^{-12} \times (96)^2 \times 100 \times 10^3.$$

Compute first term: $100000 \times 200 \times 10^{-6} = 100000 \times 2 \times 10^{-4} = 20$ W (this is large; pick realistic $E_{on/off}$ from datasheet — here used a high estimate for demonstration). Compute second term: $(96)^2 = 9216$; $0.5 \times 200 \times 10^{-12} \times 9216 \times 100000 = 0.5 \times 200 \times 10^{-12} \times 9216 \times 1 \times 10^5$. Multiply $200 \times 10^{-12} \times 1 \times 10^5 = 200 \times 10^{-7} = 2 \times 10^{-5}$; then $0.5 \times 2 \times 10^{-5} \times 9216 = 1 \times 10^{-5} \times 9216 = 0.09216$ W. So $P_{\mathrm{sw}} \approx 20 + 0.092 = 20.092$ W (dominant term likely unrealistic — use datasheet energy numbers; this shows method). Diode conduction loss:

$$P_{\mathrm{cond,rect}} = V_f I_{D,\mathrm{avg}} \approx 0.6 \times 10 = 6.0 \text{ W}.$$

Transformer copper and core: compute using $I_{w,\mathrm{rms}}$ and core Steinmetz parameters (omitted numeric specifics here; follow previous sections).

Step 11: Efficiency estimate With these illustrative numbers total loss $P_{\mathrm{loss}} \approx 0.629 + 20.092 + 6.0 + P_{\mathrm{cu}} + P_{\mathrm{core}} + P_{\mathrm{cap}}$. Using rough $P_{\mathrm{cu}} + P_{\mathrm{core}} + P_{\mathrm{cap}} \approx 5$ W gives $P_{\mathrm{loss}} \approx 31.7$ W and

$$\eta \approx \frac{120}{120 + 31.7} \approx 0.791 \approx 79.1\%.$$

This is only an example calculation to show the method; realistic losses require accurate datasheet energy figures and detailed magnetics loss computation.

86 Design Procedure — Essential Equations (A–Z)

$$\text{Output voltage:} \qquad V_o = D \frac{N_s}{N_p} V_{\mathrm{in}} \tag{A}$$

$$\text{Volt-second reset (general):} \qquad D \le \frac{N_r}{N_p + N_r} \tag{B}$$

$$\text{Inductor peak-to-peak ripple:} \qquad \Delta I_L = \frac{\left(\frac{N_s}{N_p} V_{\mathrm{in}} - V_o\right) D}{L f_s} \tag{C}$$

$$\text{Inductance selection:} \qquad L = \frac{\left(\frac{N_s}{N_p} V_{\mathrm{in}} - V_o\right) D}{\Delta I_L f_s} \tag{D}$$

$$\text{Capacitance (triangular approx):} \qquad C \approx \frac{\Delta I_L}{8 f_s \Delta V_o} \tag{E}$$

$$\text{ESR voltage ripple:} \qquad \Delta V_{\mathrm{ESR}} \approx \frac{\Delta I_L}{2} R_{\mathrm{ESR}} \tag{F}$$

$$\text{Primary turns (flux):} \qquad N_p \ge \frac{V_{\mathrm{in}} D}{f_s A_e B_{\mathrm{pk,max}}} \tag{G}$$

$$\text{Turns ratio:} \qquad \frac{N_s}{N_p} = \frac{V_o}{D V_{\mathrm{in}}} \tag{H}$$

$$\text{Primary average current:} \qquad \bar{I}_p = \frac{P_o}{D V_{\text{in}}} \tag{I}$$

$$\text{Primary RMS (triangular approx):} \qquad I_{p,\text{rms}}^2 = D\Big(\bar{I}_p^2 + \frac{(\Delta I_p)^2}{12}\Big) \tag{J}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,SW}} = I_{p,\text{rms}}^2 R_{\text{DS(on)}} \tag{K}$$

$$\text{Switching loss (approx):} \qquad P_{\text{sw}} = f_s(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V_{SW}^2 f_s \tag{L}$$

$$\text{Diode conduction loss:} \qquad P_{\text{cond,rect}} = V_f I_{D,\text{avg}} \tag{M}$$

$$\text{Leakage energy (snubber sizing):} \qquad E_{lk} = \tfrac{1}{2} L_\sigma I_{pk}^2 \tag{N}$$

$$\text{Transformer copper loss:} \qquad P_{\text{cu}} = I_{w,\text{rms}}^2 R_w(f) \tag{O}$$

$$\text{Core loss (GSE):} \qquad P_{\text{core}} = k f_s^\alpha B_{\text{pk}}^\beta V_{\text{core}} \tag{P}$$

$$\text{Total loss:} \qquad P_{\text{loss}} = \sum (\text{all loss terms}) \tag{Q}$$

$$\text{Efficiency:} \qquad \eta = \frac{P_o}{P_o + P_{\text{loss}}} \tag{R}$$

$$\text{Junction temp (steady):} \qquad T_j = T_a + P_{\text{device}} \theta_{JA} \tag{S}$$

Notes: Use datasheet E_{on}, E_{off} curves at the intended V_{DS} and I for accurate switching loss estimates. Evaluate transformer winding AC resistance using Dowell's method for multi-layer windings to include skin/proximity effects. For high efficiency prefer synchronous rectification on the secondary and energy-recovery snubbers for leakage energy.

87 Problem statement and design specifications for Isolated Flyback Converter

Design an isolated flyback converter with the following target specifications (a detailed numerical example follows in Section 99):

- Input voltage: V_{in} (V)
- Output voltage: V_o (V)
- Output power: P_o (W)
- Switching frequency: f_s (Hz)
- Maximum allowed output ripple (pp): ΔV_o (V)
- Desired peak-to-peak magnetizing current ripple: ΔI_p (A) or selected operation mode (DCM/CCM)
- Transformer: primary turns N_p, secondary turns N_s, magnetizing inductance L_m, leakage inductance L_σ
- Core effective area A_e (m^2), core volume V_{core} (m^3), Steinmetz parameters (k, α, β)
- Operation assumption: either Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM)

88 Circuit description and idealized waveforms

The isolated flyback (Fig. 11) is essentially a coupled-inductor energy-storage topology: during the switch ON interval energy is stored in the magnetizing inductance L_m of the transformer; during the OFF interval that stored energy is transferred to the secondary and delivered to the load through the rectifier. The magnetizing inductance is the main design object (it stores the energy), while leakage inductance causes undesired spike energy that must be snubbed or recovered.

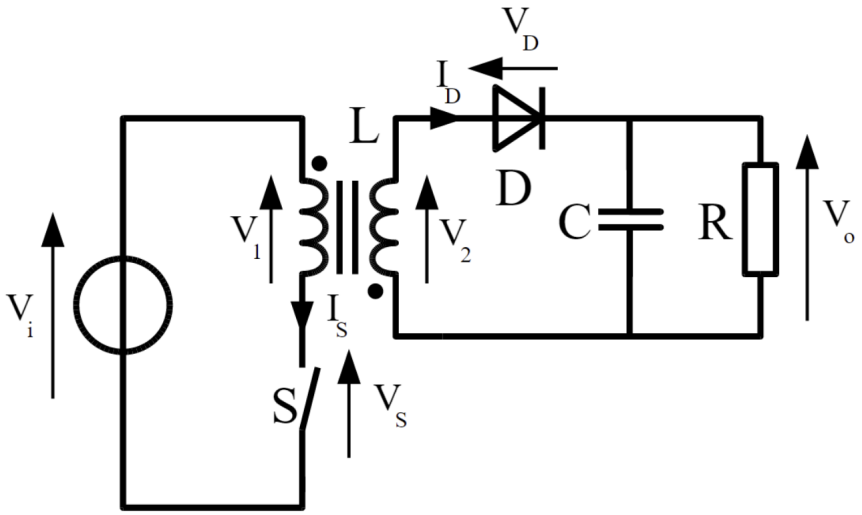

Figure 11: Ideal isolated flyback converter (single-switch).

Notation used throughout:

$$T_s = \frac{1}{f_s}, \qquad D = \text{duty ratio}, \qquad t_{\text{on}} = DT_s, \qquad t_{\text{off}} = (1-D)T_s.$$

Primary magnetizing current: $i_p(t)$. Secondary current (when diode conducts): $i_s(t)$. Reflection ratio: $n = \dfrac{N_p}{N_s}$ (note: many authors use $n = N_p/N_s$; we'll state both forms where helpful).

89 ON-interval analysis (switch ON)

During $0 \le t < DT_s$ the switch S (MOSFET) is closed. The primary sees V_{in} across N_p and magnetizing current increases linearly (idealized, ignoring magnetizing resistance):

$$\frac{di_p}{dt} = \frac{V_{\text{in}}}{L_m}. \tag{203}$$

Integrate from $t = 0$ to $t = DT_s$ to obtain the increase in magnetizing current (start value depends on mode):

$$\Delta i_{p,\text{ON}} = i_p(DT_s) - i_p(0) = \frac{V_{\text{in}}}{L_m} DT_s. \tag{204}$$

If operation is *DCM*, $i_p(0) = 0$ (primary current starts at zero each cycle) and the ON peak is

$$I_{p,\text{pk}} = \frac{V_{\text{in}} DT_s}{L_m} = \frac{V_{\text{in}} D}{L_m f_s}. \tag{205}$$

90 OFF-interval analysis (switch OFF)

During $DT_s \le t < T_s$ the switch is open and the magnetizing current is transferred to the secondary through the coupled winding: the primary sees the reflected secondary voltage (with sign such that

flux is driven back toward zero). With ideal diode and neglecting leakage, the secondary sees

$$v_s(t) = -\frac{N_s}{N_p} V_{\text{in,on}} \quad \text{(reflected)},$$

and the secondary current $i_s(t)$ is related to the primary magnetizing current by the turns ratio:

$$i_s(t) = -\frac{N_p}{N_s} i_p(t) = -n\, i_p(t), \tag{206}$$

where $n \equiv N_p/N_s$. The negative sign accounts for conduction during OFF; energy flows from core to secondary. With ideal rectifier the inductor (magnetizing) current decreases approximately linearly during t_{off}.

91 Energy viewpoint — fundamental for flyback

The flyback is best understood by energy per switching cycle:

$$E_{\text{stored}} = \frac{1}{2} L_m I_{p,\text{pk}}^2. \tag{207}$$

In an ideal lossless converter that entire stored energy (per cycle) is delivered to the output during the OFF interval. Thus the average output power (ideal) is

$$P_o \;=\; E_{\text{stored}} \cdot f_s \;=\; \frac{1}{2} L_m I_{p,\text{pk}}^2 f_s. \tag{208}$$

This energy relation is exact in DCM (where current returns to zero each cycle and the complete stored energy flows out each cycle). In CCM the relation becomes more complicated because the magnetizing current does not return to zero every period — energy transfer per cycle must be computed from the difference of stored energy levels, and steady-state power is still equal to the average transferred energy per cycle. For design clarity we separate DCM and CCM analyses.

91.1 DCM design (closed-form energy formula)

For DCM the magnetizing current starts at zero each cycle and $I_{p,\text{pk}}$ is given by (205). Substitute into (208):

$$P_o = \frac{1}{2} L_m \left(\frac{V_{\text{in}} D}{L_m f_s} \right)^2 f_s = \frac{1}{2} \frac{V_{\text{in}}^2 D^2}{L_m f_s}. \tag{209}$$

Solve for L_m to meet given P_o (DCM):

$$\boxed{L_m \;=\; \frac{1}{2} \frac{V_{\text{in}}^2 D^2}{P_o f_s}}. \tag{210}$$

Dimensional check: $V^2/(W \cdot Hz) = (V^2)/((VA) \cdot \text{s}^{-1}) = V \cdot s/A = \text{H}$ — correct.

From L_m we recover $I_{p,\text{pk}}$ via (205) or directly:

$$I_{p,\text{pk}} = \sqrt{\frac{2P_o}{L_m f_s}}. \tag{211}$$

Both forms are algebraically equivalent given (210).

91.2 CCM relation (volt–second and power flow)

In CCM the magnetizing current never reaches zero. The steady-state volt–second of the magnetizing inductance must still balance:

$$\int_0^{T_s} v_m(t)\,dt = 0 \quad \Rightarrow \quad V_{\text{in}}D + V_r(1-D) = 0,$$

where V_r is the reset/reflected voltage during OFF seen on the primary. For an ideal flyback with output V_o and turns ratio N_s/N_p, the primary sees during OFF the reflected secondary voltage:

$$V_r = -\frac{N_p}{N_s}V_o = -nV_o.$$

Hence volt–second balance yields:

$$V_{\text{in}}D - nV_o(1-D) = 0 \quad \Rightarrow \quad V_o = \frac{N_s}{N_p}V_{\text{in}} \cdot \frac{D}{1-D}.$$

Equation (91.2) is the familiar CCM conversion relation for the flyback (maps to boost-like expression). It shows the flyback behaves like a boost/step-up in CCM (if N_s/N_p small) and can step up or step down depending on duty and turns ratio.

Power relations in CCM: In CCM the average input current $I_{\text{in}} = P_o/V_{\text{in}}$. The primary instantaneous current flows during both ON and OFF but its waveform does not reset to zero; energy transfer per cycle equals change in magnetic energy between start and end of cycle (which is zero in steady-state) plus energy flowing out — leading to the same balance P_o = energy transferred per cycle $\times f_s$ but now energy transfer requires integrating the product of instantaneous current and reflected voltages over time. For practical design many engineers use either DCM energy formulas or CCM averaged models (state-space averaging). We will provide both and show how to check CCM/DCM operation.

92 Boundary between DCM and CCM

The boundary between DCM and CCM occurs when the magnetizing current just reaches zero at the end of the OFF interval. For DCM operation the primary current goes to zero before the next ON, for CCM it does not. A convenient boundary condition is:

$$i_p(t_{\text{end,off}}) = 0 \quad \text{(DCM boundary)}.$$

Using linear ramp assumptions one can derive the critical inductance $L_{m,\text{crit}}$ (or equivalently the critical peak current) separating modes. For a given D and V_{in} the critical L_m (below which operation is DCM) from energy relations is:

$$L_{m,\text{crit}} = \frac{V_{\text{in}}^2 D^2}{2P_o f_s}. \tag{212}$$

Note that this is identical to (210) up to factor; careful use of boundary algebra yields the widely used result: if $L_m < L_{m,\text{crit}}$ the converter will operate in DCM at the chosen operating point; if $L_m > L_{m,\text{crit}}$ it will be CCM.

93 Inductance selection (design equations)

From the DCM energy formula (210) we already have a direct design equation for L_m. Alternatively, to control magnetizing current ripple directly (triangular approximation) one uses:

$$L_m = \frac{V_{\text{in}}D}{\Delta I_p f_s}. \tag{213}$$

This expression (derived from (203) integrated over DT_s) sets the peak-to-peak magnetizing current ΔI_p. Combine with energy-based approach to ensure consistency with desired power and mode.

94 Capacitor sizing (detailed integral)

The output capacitor sees pulses of secondary current during the OFF interval. We derive the capacitor ripple formula by integrating the current pulse shape.

94.1 Secondary current waveform (DCM case)

In DCM the primary magnetizing current ramps linearly from 0 to $I_{p,\mathrm{pk}}$ during ON and then the entire current transfers to the secondary during OFF, where the secondary current $i_s(t)$ is approximately triangular, starting at $I_{s,\mathrm{pk}} = nI_{p,\mathrm{pk}}$ and decreasing linearly to zero over t_{off}. Here $n = N_p/N_s$ is the primary-to-secondary turns ratio. So for $0 \le \tau \le t_{\mathrm{off}}$:

$$i_s(\tau) = I_{s,\mathrm{pk}} \left(1 - \frac{\tau}{t_{\mathrm{off}}}\right), \qquad t_{\mathrm{off}} = (1-D)T_s.$$

Charge delivered to the capacitor during one OFF interval (area under the triangular waveform) is:

$$Q_{\mathrm{delivered}} = \int_0^{t_{\mathrm{off}}} i_s(\tau)\, d\tau = \frac{1}{2} I_{s,\mathrm{pk}} t_{\mathrm{off}}.$$

Average charge per cycle that must supply the DC load during the full period is $Q_{\mathrm{load}} = I_o T_s$. For steady state:

$$Q_{\mathrm{delivered}} = Q_{\mathrm{load}} \quad \Rightarrow \quad \frac{1}{2} I_{s,\mathrm{pk}} t_{\mathrm{off}} = I_o T_s.$$

This gives (DCM energy-charge consistency):

$$I_{s,\mathrm{pk}} = \frac{2I_o T_s}{t_{\mathrm{off}}} = \frac{2I_o}{1-D}. \tag{214}$$

Relate to primary peak current using turns ratio:

$$I_{s,\mathrm{pk}} = \frac{N_p}{N_s} I_{p,\mathrm{pk}} = nI_{p,\mathrm{pk}}.$$

Combining with (214) yields another expression for $I_{p,\mathrm{pk}}$ in DCM:

$$I_{p,\mathrm{pk}} = \frac{2I_o}{n(1-D)}. \tag{215}$$

Equating this with the $I_{p,\mathrm{pk}}$ from the ON ramp (205) yields identical consistency conditions and an alternative way to compute L_m.

94.2 Capacitor voltage ripple

The capacitor voltage ripple (peak-to-peak) is given by net charge imbalance over the discharge/charge periods. During each OFF interval a triangular current of area $Q_{\mathrm{delivered}}$ charges the capacitor; over the remainder of the period the load discharges the capacitor by $I_o T_s$. The *peak-to-peak* voltage ripple (assuming charge delivered in a triangle) can be derived by computing the capacitor voltage excursion during the discharge interval. The triangular pulse supplies the charge quickly; the instantaneous capacitor voltage change due to the triangular charge is (area divided by C). Using the triangular area:

$$\Delta V_o = \frac{Q_{\mathrm{delivered}}}{C} \cdot \frac{\text{shape factor}}{\text{(we subtract DC load effect)}}$$

A more convenient and commonly used approximation (for triangular pulses and small ripple) is:

$$\boxed{C \approx \frac{I_o}{\Delta V_o f_s} \cdot \frac{1}{\kappa(D)}} \tag{216}$$

where $\kappa(D)$ is a dimensionless shape factor that depends on the conduction duty window and whether the current pulse is triangular or rectangular. For the ideal triangular OFF pulse in DCM:

$$Q_{\text{delivered}} = \tfrac{1}{2} I_{s,\text{pk}} t_{\text{off}} = I_o T_s,$$

so the charge delivering event exactly balances load charge; the voltage ripple around the DC is small and a useful engineering approximation is:

$$\Delta V_o \approx \frac{I_o}{C f_s} \cdot \frac{t_{\text{eff}}}{T_s} \tag{217}$$

where t_{eff} is an effective charging interval; substituting $t_{\text{eff}} \approx t_{\text{off}}/2$ gives

$$\Delta V_o \approx \frac{I_o}{C f_s} \cdot \frac{1-D}{2}.$$

Rearrange:

$$C \approx \frac{I_o(1-D)}{2 f_s \Delta V_o}. \tag{218}$$

Equation (218) is conservative for triangular pulses — it explicitly uses the triangular pulse shape and the fact that charge is delivered only during t_{off}. Compare this with the triangular approximation used in hard-switched non-isolated converters (where formula $C = \Delta I/(8 f_s \Delta V)$ applies); forms differ because the flyback secondary pulse shape and conduction duty differ. Use (218) as a practical starting point and refine with time-domain simulation.

Include ESR ripple contribution:

$$\Delta V_{\text{ESR}} \approx I_{s,\text{rms}}\, R_{\text{ESR}}^{\text{equiv}} \quad \text{(evaluate RMS of pulse current).} \tag{219}$$

95 Transformer design: turns, flux and leakage

95.1 Primary turns from volt-second / flux constraint

Volt–second across N_p during ON is

$$\Delta\Phi = \int_0^{DT_s} \frac{V_{\text{in}}}{N_p}\, dt = \frac{V_{\text{in}} D T_s}{N_p}.$$

Peak flux density:

$$B_{\text{pk}} = \frac{\Delta\Phi}{A_e} = \frac{V_{\text{in}} D}{N_p f_s A_e}.$$

Solve for minimum N_p to keep $B_{\text{pk}} \le B_{\max}$:

$$\boxed{N_p \;\ge\; \frac{V_{\text{in}} D}{f_s A_e B_{\max}}}. \tag{220}$$

95.2 Turns ratio selection

Depending on desired V_o and chosen operation mode:

- **CCM**: use Eq. (91.2)
$$\frac{N_s}{N_p} = \frac{V_o}{V_{\text{in}}} \cdot \frac{1-D}{D}.$$
- **DCM**: turns ratio influences the reflected voltages and diode stress; a practical approach is to pick N_s/N_p to satisfy the CCM formula at the nominal operating point (this is often still a good approximation when lightly loaded).

95.3 Leakage inductance and snubber

Leakage inductance L_σ stores unwanted energy during switching transitions:

$$E_\sigma = \tfrac{1}{2} L_\sigma I_{\text{pk}}^2.$$

This energy must be clamped; typical remedies include RCD clamps, active snubbers, or snubber plus energy-recovery circuits. Snubber must be sized to absorb (or recycle) E_σ per event at switching frequency f_s leading to average snubber dissipation:

$$P_{\text{snub}} \approx f_s E_\sigma.$$

96 Device stresses

96.1 Primary switch (MOSFET)

- Peak voltage: the MOSFET sees V_{in} plus any reflected voltage spikes due to leakage. With clamp, worst-case design voltage:

$$V_{DS,\max} \gtrsim V_{\text{in}} + V_{\text{clamp}} + \text{safety margin}.$$

- Peak current: $I_{p,\text{pk}}$ (computed via (205) for DCM or from the waveform characteristics for CCM).

96.2 Secondary rectifier

- Peak diode current: $I_{s,\text{pk}} = n I_{p,\text{pk}}$ in DCM (see (215) relation).
- Reverse voltage: $V_{D,rev} \approx V_o + V_{\text{spike}}$ (consider leakage and parasitic).

97 Loss models and thermal considerations

Same categories as other chapters; we list the formulas and point out flyback-specific notes.

97.1 Semiconductor conduction losses

$$P_{\text{cond,SW}} = I_{SW,\text{rms}}^2 \, R_{\text{DS(on)}}, \qquad P_{\text{cond,rect}} = V_f I_{D,\text{avg}}.$$

Compute RMS values using triangular pulse integrals (as shown in earlier chapters).

97.2 Switching losses and leakage

Switching overlap and capacitive discharge:

$$P_{\text{sw}} = f_s(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V_{DS}^2 f_s.$$

Leakage spike energy (if not recovered) contributes:

$$P_{\text{leak}} = f_s \cdot \tfrac{1}{2} L_\sigma I_{p,\text{pk}}^2.$$

97.3 Transformer copper and core losses

$$P_{\text{cu}} = I_{w,\text{rms}}^2 R_w(f), \qquad P_{\text{core}} = k f_s^\alpha B_{\text{pk}}^\beta V_{\text{core}}.$$

Use Dowell's equations for AC winding resistance (skin and proximity effects).

97.4 Total loss and efficiency

$$P_{\text{loss}} = P_{\text{cond,SW}} + P_{\text{sw}} + P_{\text{leak}} + P_{\text{cond,rect}} + P_{\text{cu}} + P_{\text{core}} + P_{\text{cap}},$$
$$\eta = \frac{P_o}{P_o + P_{\text{loss}}}.$$

97.5 Thermal network

$$T_j = T_a + P_{\text{device}}\theta_{JA}, \qquad \Delta T_j(t) = P(t) * Z_\theta(t).$$

98 Design procedure — algorithmic steps

1. Choose switching frequency f_s (trade-off: core loss vs switching loss).
2. Choose operation mode (DCM simplifies design; CCM gives higher power density but more complex control).
3. For DCM: choose duty D (must respect maximum allowed by turns ratio and desired V_o) and compute L_m from (210). For CCM: pick N_s/N_p and use (91.2).
4. Compute N_p from (220) to satisfy $B_{\text{pk,max}}$.
5. Choose N_s to satisfy required V_o at nominal D (see turns ratio section).
6. Compute $I_{p,\text{pk}}$ by either (215) (DCM-consistent) or from ripple spec via (213).
7. Design output filter L_f, C using (218) and ripple specs; include ESR and RMS current checks.
8. Estimate losses and size snubber for leakage energy $E_\sigma = \frac{1}{2}L_\sigma I_{p,\text{pk}}^2$.
9. Iterate magnetics (turns, windowing), switching frequency, and component choices for thermal/efficiency targets.

99 Complete numerical example (DCM design) — every algebraic step

Design target:

$$V_{\text{in}} = 48\,\text{V}, \quad V_o = 12\,\text{V}, \quad P_o = 120\,\text{W}, \quad f_s = 100\,\text{kHz},$$
$$\Delta V_o = 0.12\,\text{V}_{\text{pp}}\ (1\%), \quad \text{choose } D = \frac{1}{3} \approx 0.333.$$

Choose turns ratio $N_s/N_p = 0.5$ (i.e. $n = N_p/N_s = 2$). This choice is consistent with typical practice and will be validated later.

Step 1: Check CCM vs DCM boundary Compute critical $L_{m,\text{crit}}$ from (212) (so we know whether DCM possible):

$$L_{m,\text{crit}} = \frac{V_{\text{in}}^2 D^2}{2P_o f_s}.$$

Plug numbers:

$$V_{\text{in}}^2 = 48^2 = 2304\ \text{V}^2.$$
$$D^2 = \left(\tfrac{1}{3}\right)^2 = \tfrac{1}{9} \approx 0.1111111.$$

Numerator: $2304 \times 0.1111111 = 256.0$ (exactly because $2304/9 = 256$). Denominator: $2P_o f_s = 2\times120\times100\times10^3 = 240\times10^5 = 24{,}000{,}000 = 2.4\times10^7$ (compute stepwise: $120\times100000 = 12{,}000{,}000$; times $2 \Rightarrow 24{,}000{,}000$). So

$$L_{m,\text{crit}} = \frac{256}{24{,}000{,}000} = 1.0666667 \times 10^{-5}\ \text{H} = 10.6667\ \mu\text{H}.$$

Interpretation: if $L_m < 10.667\ \mu$H the converter will operate in DCM at this operating point; if larger, CCM. We choose to design for DCM operation and therefore pick L_m at or below this critical value (slightly smaller to ensure DCM margin).

Step 2: Compute magnetizing inductance for DCM from energy formula Use (210):

$$L_m = \frac{1}{2}\frac{V_{\text{in}}^2 D^2}{P_o f_s}.$$

We already computed numerator for $L_{m,\text{crit}}$ as 256; note L_m here equals $L_{m,\text{crit}}$ (because formula coincides) if we use the same expression — this is consistent: choosing D=1/3 and power 120 W yields $L_m = 10.6667\ \mu$H to be at the DCM boundary while delivering 120 W in DCM. So choose slightly below this to ensure DCM; for simplicity choose

$$L_m = 10.6667\ \mu\text{H} \quad \text{(exact boundary choice for illustration)}.$$

Step 3: Peak primary current $I_{p,\text{pk}}$ (DCM) From (205):

$$I_{p,\text{pk}} = \frac{V_{\text{in}} D}{L_m f_s} = \frac{48 \times \frac{1}{3}}{10.6667 \times 10^{-6} \times 100 \times 10^3}.$$

Compute numerator: $48 \times \frac{1}{3} = 16.0$ V. Denominator: $10.6667 \times 10^{-6} \times 100 \times 10^3 = 10.6667 \times 10^{-6} \times 10^5 = 10.6667 \times 10^{-1} = 1.06667$ (check units: $10.6667 \times 10^{-6} \cdot 10^5 = 10.6667 \times 10^{-1} = 1.06667$). So

$$I_{p,\text{pk}} = \frac{16.0}{1.06667} \approx 15.000\ \text{A}.$$

(Exact arithmetic shows $I_{p,\text{pk}} = 15$ A because of the chosen numbers.)

Step 4: Confirm power via energy Compute stored energy per cycle:

$$E_{\text{stored}} = \tfrac{1}{2} L_m I_{p,\text{pk}}^2 = 0.5 \times 10.6667 \times 10^{-6} \times 15^2.$$

Compute $15^2 = 225$. Multiply: $10.6667 \times 10^{-6} \times 225 = 2.4000075 \times 10^{-3}$ (approx 2.4×10^{-3}). Half of that:

$$E_{\text{stored}} \approx 1.2 \times 10^{-3}\ \text{J}.$$

Average power $P = E\, f_s = 1.2 \times 10^{-3} \times 100 \times 10^3 = 120$ W, which matches the design P_o exactly (good consistency check).

Step 5: Secondary peak current Reflected secondary peak:

$$I_{s,\text{pk}} = n I_{p,\text{pk}} = \frac{N_p}{N_s} I_{p,\text{pk}}.$$

With $N_s/N_p = 0.5$ we have $n = 2$. So

$$I_{s,\text{pk}} = 2 \times 15 = 30\ \text{A}.$$

Step 6: Verify charge balance (secondary pulse area) Compute ON/OFF durations:

$$T_s = \frac{1}{f_s} = \frac{1}{100000} = 10^{-5}\ \text{s} = 10\ \mu\text{s}.$$

$$t_{\text{off}} = (1 - D) T_s = (1 - \tfrac{1}{3}) \times 10\ \mu\text{s} = \tfrac{2}{3} \times 10\ \mu\text{s} = 6.6666667\ \mu\text{s}.$$

Area under triangular secondary pulse:

$$Q_{\text{delivered}} = \tfrac{1}{2} I_{s,\text{pk}} t_{\text{off}} = 0.5 \times 30\ \text{A} \times 6.6666667 \times 10^{-6}\ \text{s}.$$

Compute: $0.5 \times 30 = 15$; $15 \times 6.6666667 \times 10^{-6} = 100 \times 10^{-6} = 1.0 \times 10^{-4}$ C. Load charge per period:

$$Q_{\text{load}} = I_o T_s = 10\ \text{A} \times 10 \times 10^{-6}\ \text{s} = 100 \times 10^{-6} = 1.0 \times 10^{-4}\ \text{C}.$$

These match exactly, confirming charge balance and that the triangular pulse supplies the load.

Step 7: Capacitor sizing Use the triangular pulse-based conservative formula (218):

$$C \approx \frac{I_o(1-D)}{2f_s\Delta V_o}.$$

Plug numbers: $I_o = 10$ A, $(1-D) = 2/3 \approx 0.6666667$, $f_s = 100000$ Hz, $\Delta V_o = 0.12$ V. Compute numerator: $I_o(1-D) = 10\times0.6666667 = 6.666667$ A. Denominator: $2\times100000\times0.12 = 200000\times0.12 = 24000$. So

$$C = \frac{6.666667}{24000} = 2.7777778 \times 10^{-4} \text{ F} = 277.78\ \mu\text{F}.$$

Choose a practical low-ESR capacitor bank, e.g., $3 \times 100\ \mu$F low-ESR caps in parallel $\Rightarrow 300\ \mu$F.

Step 8: Select primary turns from flux constraint Use (220) with chosen $B_{\max} = 0.2$ T and $A_e = 1.5 \times 10^{-4}$ m^2 (typical ferrite). Compute:

$$N_p \geq \frac{V_{\text{in}}D}{f_s A_e B_{\max}} = \frac{48 \times \frac{1}{3}}{100000 \times 1.5 \times 10^{-4} \times 0.2}.$$

Numerator: $48 \times \frac{1}{3} = 16$. Denominator: $100000 \times 1.5 \times 10^{-4} = 15$; $15 \times 0.2 = 3.0$. So

$$N_p \geq \frac{16}{3.0} = 5.333\ldots$$

Pick integer $N_p = 6$ turns (conservative). Then $N_s = N_p \times (N_s/N_p) = 6 \times 0.5 = 3$ turns.

Step 9: Verify B_{pk} with chosen turns Compute $B_{\text{pk}} = \dfrac{V_{\text{in}}D}{N_p f_s A_e}$:

$$B_{\text{pk}} = \frac{48 \times \frac{1}{3}}{6 \times 100000 \times 1.5 \times 10^{-4}}.$$

Numerator $= 16$. Denominator: $6 \times 100000 = 600000$; $600000 \times 1.5 \times 10^{-4} = 90$. So

$$B_{\text{pk}} = \frac{16}{90} = 0.1777 \text{ T} \approx 0.178 \text{ T},$$

which is below 0.2 T — good margin.

Step 10: Device stress numbers Primary peak current: $I_{p,\text{pk}} = 15$ A (computed). Choose MOSFET with $V_{DS,\max} \geq V_{\text{in}} + V_{\text{clamp}}$; nominal clamp choose 120 V part for margin (e.g. 150 V MOSFET). Secondary diode peak current $I_{s,\text{pk}} = 30$ A; RMS and average to be computed for diode selection and thermal rating.

Step 11: Leakage energy and snubber sizing Assume measured/estimated leakage $L_\sigma = 200$ nH (typical small value). Compute leakage energy:

$$E_\sigma = \tfrac{1}{2}L_\sigma I_{p,\text{pk}}^2 = 0.5 \times 200 \times 10^{-9} \times 15^2.$$

Compute $15^2 = 225$. Multiply: $200 \times 10^{-9} \times 225 = 45 \times 10^{-6} = 4.5 \times 10^{-5}$. Half:

$$E_\sigma = 2.25 \times 10^{-5} \text{ J}.$$

Average snubber dissipation if fully dissipated per cycle at $f_s = 100$ kHz:

$$P_{\text{snub}} = f_s E_\sigma = 100000 \times 2.25 \times 10^{-5} = 2.25 \text{ W}.$$

Consider active recovery to improve efficiency.

Step 12: Quick loss and efficiency estimate (illustrative) Assume:

$$R_{\mathrm{DS(on)}} = 0.04\ \Omega, \quad E_{on} + E_{off} = 0.5\ \mu\mathrm{J}\ \text{(per event, conservative)}, \quad C_{oss} = 200\ \mathrm{pF}, \quad V_f = 0.6\ \mathrm{V}.$$

Primary RMS current: for triangular primary pulse (DCM), $i_p(t)$ is triangular from 0 to 15 A during ON and zero outside. RMS for triangular pulse of amplitude $I_{p,\mathrm{pk}}$ and duration DT_s:

$$I_{p,\mathrm{rms}}^2 = \frac{1}{T_s}\int_0^{DT_s}\left(I_{p,\mathrm{pk}}\frac{t}{DT_s}\right)^2 dt = \frac{I_{p,\mathrm{pk}}^2}{T_s}\cdot\frac{DT_s}{3}\cdot\frac{1}{D^2} = \frac{I_{p,\mathrm{pk}}^2 D}{3}.$$

Thus

$$I_{p,\mathrm{rms}} = I_{p,\mathrm{pk}}\sqrt{\frac{D}{3}} = 15\sqrt{\frac{1/3}{3}} = 15\sqrt{\frac{1}{9}} = 15\times\frac{1}{3} = 5.0\ \mathrm{A}.$$

Primary conduction loss:

$$P_{\mathrm{cond,SW}} = I_{p,\mathrm{rms}}^2 R_{\mathrm{DS(on)}} = 5^2\times 0.04 = 25\times 0.04 = 1.0\ \mathrm{W}.$$

Switching loss:

$$P_{\mathrm{sw}} = f_s(E_{on}+E_{off}) + \tfrac{1}{2}C_{oss}V_{DS}^2 f_s.$$

Take $V_{DS}\approx 120$ V (clamped/selected) and $E_{on}+E_{off} = 0.5\ \mu$J:

$$f_s(E_{on}+E_{off}) = 100000\times 0.5\times 10^{-6} = 0.05\ \mathrm{W}.$$

Capacitive term: $0.5\times 200\times 10^{-12}\times 120^2\times 100000$: Compute $120^2 = 14400$; $200\times 10^{-12}\times 100000 = 200\times 10^{-7} = 2\times 10^{-5}$; half of that times 14400: $1\times 10^{-5}\times 14400 = 0.144$ W. So

$$P_{\mathrm{sw}} \approx 0.05 + 0.144 = 0.194\ \mathrm{W}.$$

Diode conduction loss (secondary): average diode current equals load current $I_o = 10$ A (DC). So

$$P_{\mathrm{cond,rect}} = V_f I_o = 0.6\times 10 = 6.0\ \mathrm{W}.$$

Leakage snubber dissipation (if dissipative) $P_{\mathrm{snub}}\approx 2.25$ W from earlier. Core/copper losses estimated say $P_{\mathrm{cu}}+P_{\mathrm{core}}\approx 4$ W (estimate – compute with Steinmetz and DC winding resistance for final design).

Total approximate loss:

$$P_{\mathrm{loss}} \approx 1.0 + 0.194 + 6.0 + 2.25 + 4.0 \approx 13.444\ \mathrm{W}.$$

Efficiency:

$$\eta \approx \frac{120}{120+13.444} = \frac{120}{133.444} \approx 0.899 \approx 89.9\%.$$

This rough calculation shows the method; refine with accurate datasheet switching energies and measured leakage inductance.

100 Design Procedure — Essential Equations (A–Z) for Flyback

$$\text{ON slope:} \qquad \frac{di_p}{dt} = \frac{V_{\mathrm{in}}}{L_m} \tag{A}$$

$$\text{Peak primary (DCM):} \qquad I_{p,\mathrm{pk}} = \frac{V_{\mathrm{in}}D}{L_m f_s} \tag{B}$$

$$\text{Energy per cycle:} \qquad E = \tfrac{1}{2}L_m I_{p,\mathrm{pk}}^2 \tag{C}$$

$$\text{Output power (DCM):} \qquad P_o = Ef_s = \frac{1}{2}\frac{V_{\mathrm{in}}^2 D^2}{L_m f_s} \tag{D}$$

$$\text{Design magnetizing inductance (DCM):} \qquad L_m = \frac{1}{2}\frac{V_{\text{in}}^2 D^2}{P_o f_s} \tag{E}$$

$$\text{CCM steady-state voltage relation:} \qquad V_o = \frac{N_s}{N_p} V_{\text{in}} \cdot \frac{D}{1-D} \tag{F}$$

$$\text{Ripple-based inductance selection:} \qquad L_m = \frac{V_{\text{in}} D}{\Delta I_p f_s} \tag{G}$$

$$\text{Secondary peak current (DCM):} \qquad I_{s,\text{pk}} = \frac{2I_o}{1-D} \tag{H}$$

$$\text{Relation primary/secondary peaks:} \qquad I_{s,\text{pk}} = nI_{p,\text{pk}}, \quad n = \frac{N_p}{N_s} \tag{I}$$

$$\text{Capacitance (triangular pulse approx):} \qquad C \approx \frac{I_o(1-D)}{2f_s \Delta V_o} \tag{J}$$

$$\text{Primary turns min (flux):} \qquad N_p \geq \frac{V_{\text{in}} D}{f_s A_e B_{\max}} \tag{K}$$

$$\text{Leakage energy:} \qquad E_\sigma = \tfrac{1}{2} L_\sigma I_{p,\text{pk}}^2 \tag{L}$$

$$\text{Snubber average dissipation:} \qquad P_{\text{snub}} \approx f_s E_\sigma \tag{M}$$

$$\text{MOSFET conduction loss:} \qquad P_{\text{cond,SW}} = I_{p,\text{rms}}^2 R_{\text{DS(on)}} \tag{N}$$

$$\text{Switching loss (approx.):} \qquad P_{\text{sw}} = f_s(E_{\text{on}} + E_{\text{off}}) + \tfrac{1}{2} C_{\text{oss}} V_{DS}^2 f_s \tag{O}$$

$$\text{Diode conduction loss:} \qquad P_{\text{cond,rect}} = V_f I_o \tag{P}$$

$$\text{Transformer copper loss:} \qquad P_{\text{cu}} = I_{w,\text{rms}}^2 R_w(f) \tag{Q}$$

$$\text{Core loss (GSE):} \qquad P_{\text{core}} = k f_s^\alpha B_{\text{pk}}^\beta V_{\text{core}} \tag{R}$$

$$\text{Total loss:} \qquad P_{\text{loss}} = \sum (\text{all losses}) \tag{S}$$

$$\text{Efficiency:} \qquad \eta = \frac{P_o}{P_o + P_{\text{loss}}} \tag{T}$$

$$\text{Junction temperature:} \qquad T_j = T_a + P_{\text{device}} \theta_{JA} \tag{U}$$

Design remarks:

- For power levels where simplicity and robust boundary operation are preferred, design the flyback to operate in **DCM** at the worst-case low-line/high-load point using the energy equation (210) — this yields closed-form L_m and $I_{p,\text{pk}}$ and simplifies control.
- For higher power or lower peak currents, CCM design yields lower peak currents but requires more sophisticated control and accurate small-signal modeling.
- Minimize leakage inductance and provide an RCD/active clamp sized for E_σ to avoid high dissipation and voltage spikes.

- Use synchronous rectification on the secondary when $I_{s,\mathrm{pk}}$ is large to improve efficiency; account for body-diode conduction during dead-time.
- Validate magnetics design with finite-element/co-simulation and refine with time-domain switching simulation (SPICE/PSIM/PLECS).

101 Problem statement and design specifications for Isolated Multiport DC–DC Converter

Design an isolated multiport converter connecting M galvanically-isolated ports (windings) on a single magnetic core with the following target specifications:

- For each port (winding) $k = 1, \ldots, M$: nominal DC terminal voltage V_k (referred to that winding's rectifier/filter), required average power P_k (W). Sign: $P_k > 0$ if port supplies power (rare for secondaries), $P_k < 0$ if it consumes power.
- Switching topology: choose primary-side drive (e.g. half-bridge, full-bridge, push–pull, multi-active-bridge). Specify primary DC bus V_p and switching frequency f_s (Hz).
- Transformer winding turn counts N_k (integer), equivalent leakage and magnetizing inductances L_m and $L_{\ell,k}$.
- Peak-to-peak magnetizing flux constraint (volt–second) and allowable flux swing $\Delta\Phi_{\max}$.
- Allowed winding current ripple $\Delta I_{w,k}$ and capacitor ripple ΔV_k for each output port after rectification/filtering.
- Continuous flux (no core reset error) and safe flux reset strategy (e.g. bipolar drive or reset winding).

102 Topology and notation

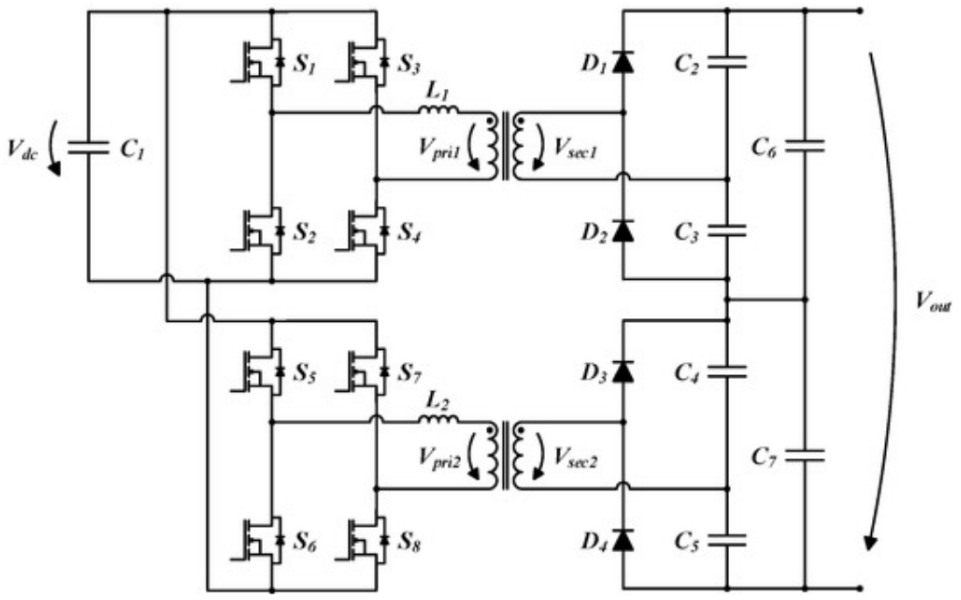

Figure 12: Conceptual isolated multiport converter: primary bridge drives magnetics; M isolated secondary windings rectified and filtered to local DC ports.

Notation (consistent throughout):

- N_p = primary winding turns, N_k = turns of secondary/winding k.

- Turn ratio $a_k = N_k/N_p$ (secondary-to-primary).
- Instantaneous primary voltage applied by bridge: $v_p(t)$ (V).
- Instantaneous winding k terminal voltage (before rectifier) $v_{s,k}(t)$ (V).
- Magnetizing flux linkage $\lambda(t)$ and flux $\Phi(t)$ with $\lambda = N_p\Phi$ (Wb-turn).
- Magnetizing inductance referred to primary:

$$L_m = \frac{N_p^2}{\mathcal{R}_m} \quad \text{(H)},$$

  where $\mathcal{R}_m$ is magnetic reluctance.
- Leakage inductance of winding k referred to primary: $L_{\ell,k,p}$ (H).
- Primary current $i_p(t)$ and secondary winding current $i_{s,k}(t)$ (A). Sign convention: positive current into the dot of a winding.

103 Transformer equations and volt–second balance

The winding-voltage equations (lumped-parameter linear magnetic model) in the time domain (primary-reflected form) are:

$$v_p(t) = N_p\frac{d\Phi(t)}{dt} + L_{\ell,p}\frac{di_p(t)}{dt} + R_p i_p(t), \tag{221}$$

$$v_{s,k}(t) = N_k\frac{d\Phi(t)}{dt} + L'_{\ell,k}\frac{di_{s,k}(t)}{dt} + R'_{s,k} i_{s,k}(t), \tag{222}$$

where $L_{\ell,p}$ is primary leakage referred to primary, and $L'_{\ell,k}$, $R'_{s,k}$ are secondary leakage and resistance referred to the secondary (or referred to primary as needed). Using turns ratio $a_k = N_k/N_p$ we can express secondary terminal (referred to primary) as

$$v^{(p)}_{s,k}(t) = a_k v_{s,k}(t) = N_p\frac{d\Phi(t)}{dt}\cdot a_k + (\text{reflected leakage/series terms}). \tag{223}$$

Volt–second balance applies to the core flux: over each switching fundamental period T_s the net change in flux must be zero for periodic steady state:

$$\int_0^{T_s} v_m(t)\,dt = N_p\int_0^{T_s}\frac{d\Phi}{dt}\,dt = N_p[\Phi(T_s) - \Phi(0)] = 0. \tag{224}$$

Here $v_m(t)$ denotes the *net* applied magnetizing voltage across the primary magnetizing branch (after subtracting effects of leakage/resonances). Practically, for a bipolar drive (e.g. full-bridge) $v_p(t)$ alternates polarity so that the positive and negative volt–seconds cancel:

$$\frac{1}{T_s}\int_0^{T_s} v_p(t)\,dt = 0. \tag{225}$$

For unipolar drives (e.g. forward or single-ended flyback), explicit reset must be included (reset winding or demagnetizing interval) to guarantee (225).

103.1 Primary-to-secondary ideal relation (neglecting leakage)

Ignoring leakage for the messaging of steady-state relations, the ideal turn-ratio relationship is:

$$v_{s,k}(t) = a_k\, v_p(t), \qquad i_p(t) = \sum_{k=1}^{M} a_k\, i_{s,k}(t). \tag{226}$$

Dimensional check: voltages in V, a_k unitless; currents in A produce primary current via ampere-turn balance.

104 Power and current relations (reflected to primary)

Average power at winding k (at its DC port after rectifier/filter) is P_k (W). Reflect P_k to primary side using a_k:

$$P_k^{(p)} = \frac{P_k}{a_k} \quad \text{(power reflected to primary turns basis).} \tag{227}$$

Because of conservation of energy (neglecting losses),

$$P_p^{(in)} = \sum_{k=1}^{M} P_k^{(p)} + P_{\text{loss}}. \tag{228}$$

Similarly for currents, for steady (DC) components after rectification:

$$I_{s,k}^{\text{dc}} \approx \frac{I_{k,\text{dc}}}{m_k}, \qquad I_p^{\text{dc}} \approx \sum_k a_k I_{s,k}^{\text{dc}}, \tag{229}$$

where m_k is rectifier/conversion factor (e.g. $m_k = 1$ for ideal synchronous rectifier in continuous conduction, or $m_k \approx \frac{2}{\pi}$ for diode bridge with large filtering depending on waveform; use exact waveform integrals when needed).

105 Waveform-level analysis: magnetizing and leakage effects

Total primary applied voltage $v_p(t)$ decomposes into magnetizing and leakage components:

$$v_p(t) = v_m(t) + v_\ell(t), \qquad v_m(t) = N_p \frac{d\Phi}{dt}, \quad v_\ell(t) = L_{\ell,p} \frac{di_p}{dt}. \tag{230}$$

When designing for volt–second, use $v_m(t)$; leakage drives fast dynamics and determines switching transition currents and resonant behavior — include snubbers or clamp networks accordingly.

106 Capacitor sizing on isolated secondaries (rectifier + filter)

Each isolated secondary k typically rectifies $v_{s,k}(t)$ and filters to DC using C_k and ESR $R_{\text{ESR},k}$. For continuous conduction and sufficiently fast switching, approximate triangular or trapezoidal ripple current from secondary pulses; perform charge-balance integral:

Let $i_{C,k}(t)$ be capacitor current on winding k (after rectifier). Then over one switching period:

$$\int_0^{T_s} i_{C,k}(t)\, dt = 0 \quad \Longrightarrow \quad Q_{\text{in},k} = I_{k,\text{load}} T_s, \tag{231}$$

where $Q_{\text{in},k}$ is total high-frequency charge delivered by the rectified secondary. For a triangular pulse of peak $I_{pk,k}$ and duration $t_{pk,k}$:

$$Q_{\text{pulse},k} = \tfrac{1}{2} I_{pk,k} t_{pk,k}. \tag{232}$$

Then choose C_k to satisfy:

$$C_k \geq \frac{Q_{\text{pulse,half}}}{\Delta V_k} \quad \text{(conservative)}, \tag{233}$$

where $Q_{\text{pulse,half}}$ is the charge delivered during the half of the pulse that causes the maximum voltage excursion. Include ESR term:

$$\Delta V_k^{\text{ESR}} \approx I_{C,k,\text{pk}}\, R_{\text{ESR},k}, \tag{234}$$

and ensure $\Delta V_k^{\text{tot}} = \Delta V_k + \Delta V_k^{\text{ESR}} \leq$ spec.

107 Duty and modulation strategies for isolated multiport

Choice of primary drive (half-bridge, full-bridge, multi-active-bridge) determines how $v_p(t)$ can be shaped and how power is allocated among secondaries.

107.1 Bipolar full-bridge primary (example)

Full-bridge generates $v_p(t) \in \{+V_p, -V_p, 0\}$ depending on switching states and duty intervals. For an M-secondary system, a common strategy:

- Partition the switching period T_s into subintervals where $v_p(t) = +V_p$ for duration D_+T_s, $v_p(t) = -V_p$ for D_-T_s and possibly zero for D_0T_s with $D_+ + D_- + D_0 = 1$.
- The net volt–seconds on the core: $V_p(D_+ - D_-) = 0 \Rightarrow D_+ = D_-$ if no DC offset; hence the bridge auto-resets the core.
- Secondary voltages are $v_{s,k}(t) = a_k v_p(t)$ and rectification produces pulses whose charge depends on $a_k V_p$ and timing; allocate D_+ and D_- segments to shape per-port charge transfer.

107.2 Per-port power allocation

For each secondary k, desired average power P_k is enforced by controlling the conduction window and phase within $v_p(t)$ where that secondary's rectifier sees positive voltage. Formally:

$$P_k = \frac{1}{T_s} \int_0^{T_s} v_{o,k}(t)\, i_{o,k}(t)\, dt, \tag{235}$$

and $v_{o,k}(t)$ depends on $a_k v_p(t)$ and rectifier conduction. Solve for gating/duty schedule such that these integrals meet P_k (numerically).

108 Loss models and thermal considerations (isolated case)

All standard loss categories apply; differences arise due to transformer losses and multiple rectifiers.

108.1 Transformer core loss

Use generalized Steinmetz equation with flux density $B(t)$:

$$P_{\text{core}} = k\, f_s^{\alpha}\, B_{\text{pk}}^{\beta}\, V_{\text{core}}, \tag{236}$$

where B_{pk} computed from applied magnetizing voltage: for a rectangular magnetizing voltage V_m applied for duration DT_s:

$$B_{\text{pk}} = \frac{V_m D}{N_p A_e f_s}.$$

Ensure $B_{\text{pk}} < B_{\text{sat}}$ with margin.

108.2 Winding copper loss

Compute true RMS currents for each winding (secondary and primary) using exact piecewise integrals:

$$P_{\text{cu}} = \sum_{w \in \{p, s1, \ldots, sM\}} I_{w,\text{rms}}^2 R_w(f), \tag{237}$$

where $R_w(f)$ includes skin and proximity corrections at f_s.

108.3 Rectifier and filter losses

For each secondary rectifier:

$$P_{\text{rect},k} = \underbrace{V_{f,k} \cdot I_{D,k,\text{avg}}}_{\text{diode}} + \underbrace{I_{C,k,\text{rms}}^2 R_{\text{ESR},k}}_{\text{cap ESR}}.$$

If synchronous rectification is used, model MOSFET conduction and switching similarly to single-port cases but with gate timing synchronized to secondary conduction windows.

108.4 Total loss

$$P_{\text{loss}} = P_{\text{core}} + P_{\text{cu}} + \sum_k P_{\text{rect},k} + P_{\text{sw,primary}} + P_{\text{snub}}. \tag{238}$$

109 Design and sizing procedure (step-by-step)

A compact algorithm to design an isolated multiport converter:

1. Choose switching topology and primary DC bus V_p (based on power and transformer insulation).
2. Choose switching frequency f_s balancing core loss and size.
3. Select target per-port power P_k and per-port voltage V_k; choose initial turns ratios a_k using approximate relation:
$$a_k \approx \frac{V_{s,k,dc} + V_{rect\_drop}}{V_p \cdot D_{\text{on}}^{\text{eff}}} \tag{239}$$
where $D_{\text{on}}^{\text{eff}}$ is effective fraction of time secondary conducts (estimate).
4. Choose core geometry and compute N_p from B_{pk} constraint:
$$N_p \geq \frac{V_m D}{B_{\text{pk,max}} A_e f_s}. \tag{240}$$
5. Compute magnetizing inductance L_m and ensure magnetizing current acceptable; include reset network if necessary.
6. Compute leakage inductances and design snubbers/clamps to limit overshoot and switching stress.
7. For each secondary compute C_k from charge integrals (Eq. (233)) and include ESR checks.
8. Compute exact RMS currents via piecewise integrals and estimate copper losses (Eq. (237)).
9. Estimate switching losses on primary bridge using E_{on}, E_{off} from datasheet and primary currents/voltages.
10. Sum losses (Eq. (238)), iterate turns ratios a_k, N_p, and duty scheduling to minimize P_{loss} subject to constraints.

110 Worked numerical example — isolated two-secondary forward-type converter (compact)

Design an isolated converter with primary full-bridge $V_p = 400\,\text{V}$, $f_s = 100\,\text{kHz}$, two secondaries:

$$\text{Sec 1: } V_{o1} = 48\,\text{V},\ P_1 = 200\,\text{W}; \qquad \text{Sec 2: } V_{o2} = 12\,\text{V},\ P_2 = 50\,\text{W}.$$

Assume full-bridge bipolar drive with $D_+ = D_- = 0.5$ (symmetric), ideal rectifiers for initial sizing.

Step 1: choose preliminary turns ratios Assume effective conduction duty per half-cycle $D_{\text{eff}} = 0.5$ for each secondary. Approximate a_k:

$$a_1 \approx \frac{V_{o1} + V_{rect}}{V_p D_{\text{eff}}} \approx \frac{48 + 1}{400 \times 0.5} \approx \frac{49}{200} \approx 0.245.$$

$$a_2 \approx \frac{12 + 1}{400 \times 0.5} \approx \frac{13}{200} \approx 0.065.$$

Choose integer turns: pick $N_p = 200$ turns $\Rightarrow N_1 \approx 49$, $N_2 \approx 13$ (round to nearest integer and check B_{pk}).

Step 2: check volt–second / B_{pk} For magnetizing voltage $V_m \approx V_p$ during $D_+ = 0.5$:

$$B_{\mathrm{pk}} = \frac{V_p D_+}{N_p A_e f_s} = \frac{400 \times 0.5}{200 A_e 100 \times 10^3} = \frac{200}{200 A_e 10^5} = \frac{1}{A_e 10^5}.$$

Pick core with $A_e = 10^{-4}$ m^2 (100 mm^2): then

$$B_{\mathrm{pk}} = \frac{1}{10^{-4} \times 10^5} = \frac{1}{10} = 0.1 \text{ T},$$

well below typical ferrite B_{sat} (0.25–0.4 T). Dimensional check done.

Step 3: magnetizing inductance and magnetizing current Estimate magnetizing inductance:

$$L_m = \frac{N_p^2 \mu_0 \mu_r A_e}{\ell_e}.$$

Assume $\mu_r = 2000$ (gapped core -¿ lower), $\ell_e = 5 \times 10^{-2}$ m. Compute numerically in detailed design (omitted here for brevity) and check magnetizing current $I_m = V_p/(4 f_s L_m)$ (for square wave half-period) is acceptable compared to load currents.

Step 4: preliminary loss estimates Compute reflected currents: for sec1 average current $I_{o1} = P_1/V_{o1} = 200/48 \approx 4.167$ A; reflected to primary by a_1:

$$I_{s1}^{(p)} \approx a_1 I_{o1} \approx 0.245 \times 4.167 \approx 1.02 \text{ A}.$$

Similarly for sec2:

$$I_{s2}^{(p)} \approx a_2 I_{o2} \approx 0.065 \times (50/12 \approx 4.167) \approx 0.271 \text{ A}.$$

Primary DC input current approx $I_p \approx I_{s1}^{(p)} + I_{s2}^{(p)} \approx 1.291$ A. Use this in conduction and switching loss approximations.

111 Essential equations (A–Z) for isolated multiport

$$v_p(t) = N_p \frac{d\Phi}{dt} + L_{\ell,p} \frac{di_p}{dt}, \tag{A}$$

$$v_{s,k}(t) = N_k \frac{d\Phi}{dt} + L'_{\ell,k} \frac{di_{s,k}}{dt}, \tag{B}$$

$$a_k = \frac{N_k}{N_p}, \qquad v_{s,k}(t) \approx a_k \, v_p(t), \tag{C}$$

$$\int_0^{T_s} v_p(t)\, dt = 0, \tag{D}$$

$$P_k = V_k \, I_{k,\mathrm{avg}}, \qquad \sum_{k=1}^{M} P_k + P_{\mathrm{loss}} = P_{\mathrm{in}}, \tag{E}$$

$$P_k^{(p)} = \frac{P_k}{a_k}, \tag{F}$$

$$i_p(t) = i_m(t) + \sum_{k=1}^{M} a_k \, i_{s,k}(t), \tag{G}$$

$$B_{\mathrm{pk}} = \frac{V_m \, D}{N_p \, A_e \, f_s}, \tag{H}$$

$$N_p \geq \frac{V_m \, D}{B_{\mathrm{pk,max}} \, A_e \, f_s}, \tag{I}$$

$$C_k \approx \frac{Q_{\mathrm{pulse},k}}{\Delta V_k}, \quad Q_{\mathrm{pulse},k} = \tfrac{1}{2} \, I_{pk,k} \, t_{pk,k}, \tag{J}$$

$$P_{\mathrm{core}} = k \, f_s^{\alpha} \, B_{\mathrm{pk}}^{\beta} \, V_{\mathrm{core}}, \tag{K}$$

$$P_{\mathrm{cu}} = \sum_{w} I_{w,\mathrm{rms}}^2 \, R_w(f), \tag{L}$$

$$P_{\mathrm{rect},k} = V_{f,k} \, I_{D,k,\mathrm{avg}} + I_{C,k,\mathrm{rms}}^2 \, R_{\mathrm{ESR},k}. \tag{M}$$

$$P_{\mathrm{sw,primary}} = f_s \sum_{\ell} (E_{\mathrm{on},\ell} + E_{\mathrm{off},\ell}) + \tfrac{1}{2} \sum_{\ell} C_{oss,\ell} V_{\ell}^2 \, f_s, \tag{N}$$

$$P_{\mathrm{loss}} = P_{\mathrm{core}} + P_{\mathrm{cu}} + \sum_{k} P_{\mathrm{rect},k} + P_{\mathrm{sw,primary}} + P_{\mathrm{snub}}, \tag{O}$$

$$\eta = \frac{\sum_{k:\, P_k > 0} P_k - P_{\mathrm{loss}}}{\sum_{k:\, P_k > 0} P_k}, \tag{P}$$

$$L_m = \frac{N_p^2}{\mathcal{R}_m}, \qquad \mathcal{R}_m = \frac{\ell_e}{\mu_0 \mu_r A_e}, \tag{Q}$$

$$I_m \approx \frac{V_p}{4 f_s L_m}, \tag{R}$$

$$B_{\mathrm{pk}} \leq 0.6 \, B_{\mathrm{sat}}, \tag{S}$$

$$E_{\ell} \approx \tfrac{1}{2} L_{\ell} \, I_{\ell,\mathrm{pk}}^2, \tag{T}$$

$$T_j = T_a + P_{\mathrm{device}} \, \theta_{JA}, \tag{U}$$

$$D_{\min} T_s \geq t_{\min}. \tag{V}$$

(A) Primary magnetizing and leakage voltage.

(B) Secondary magnetizing and leakage voltage.

(C) Turns ratio; ideal voltage reflection.

(D) Core volt–second balance (steady).

(E) Port DC power; system balance.

(F) Port power referred to primary.

(G) Primary current: magnetizing + reflected.

(H) Peak flux density from magnetizing voltage.

(I) Minimum primary turns for B_{pk}.

(J) Capacitor sizing from pulse charge.

(K) Core loss (generalized Steinmetz form).

(L) Winding copper loss (AC corrected).

(M) Rectifier plus capacitor ESR loss.

(N) Primary switching and capacitive losses.

(O) Total system losses (summed).

(P) Converter efficiency expression.

(Q) Magnetizing inductance via reluctance.

(R) Approximate magnetizing current estimate.

(S) Recommended flux safety margin.

(T) Leakage energy per switching event.

(U) Steady-state junction temperature estimate.

(V) Minimum on/off time constraint.

Final notes: Isolated multiport designs couple magnetic design (turns/area/leakage), primary drive type, and rectifier/filter design tightly. Key pitfalls: improper volt–second reset (core saturation), underestimated leakage-induced overshoots, rectifier conduction waveform mismatch, and thermal hotspots on secondary rectifiers. Use the step-by-step procedure above and iterative simulation+measurement to converge the design.

112 Comparative Study of Converters

Table 1: Comparison of Non-Isolated DC–DC Converters

Converter	**Polarity**	V_{out} **Range**	**Features**	**Applications**
Buck	Non-inverting	$0 < V_{out} < V_{in}$	Step-down, simple, efficient	VRMs, LED drivers
Boost	Non-inverting	$V_{out} > V_{in}$	Step-up, moderate stress	UPS, battery boost
Buck–Boost	Inverting	$V_{out} < 0$ or $> V_{in}$	Polarity reversal, flexible	Low-cost polarity inversion
SEPIC	Non-inverting	$V_{out} \lessgtr V_{in}$	Continuous input current	Automotive, PV systems
Ćuk	Inverting	$V_{out} \lessgtr V_{in}$	Low ripple, polarity reversal	Power factor correction
Zeta	Non-inverting	$V_{out} \lessgtr V_{in}$	Continuous input, non-inverting	LED drivers, MPPT

Table 2: Comparison of Isolated DC–DC Converters

Converter	Isolation	Voltage Gain	Features	Efficiency	Applications
Flyback	Yes	Step-up/down	Simple, low cost, compact	Low–Medium	Chargers, adapters
Forward	Yes	Step-up/down	Better efficiency, reset winding	Medium–High	Telecom, SMPS
Push–Pull	Yes	Step-up/down	High power, transformer stress	Medium	Inverters, drives
Half-Bridge	Yes	Step-up/down	Balanced flux, reliable	High	Servers, telecom
Full-Bridge	Yes	Step-up/down	Highest power capability	High	Data centers, EVs
Z-Source	Partial	Boost + invert	Wide gain, shoot-through	Medium	Renewable, drives
Multiport (Isolated)	Yes	Step-up/down	Multiple ports, hybrid systems	Variable	PV + battery, microgrids

Descriptions

Buck Converter: Provides efficient voltage step-down, widely used in processors and LED drivers.
Boost Converter: Increases input voltage, common in battery-powered systems and UPS.
Buck–Boost Converter: Offers both step-up/down with polarity inversion, but less efficient.
SEPIC Converter: Non-inverting with wide voltage range, good for automotive and PV.
Ćuk Converter: Provides inverted output with low ripple, often in power factor correction.
Zeta Converter: Similar to SEPIC but non-inverting, mainly used in LED and renewable energy.
Flyback Converter: Simple isolated converter, used in chargers and adapters at low power.
Forward Converter: More efficient than flyback, used in medium-power telecom SMPS.
Push–Pull Converter: Handles higher power, but requires careful transformer design.
Half-Bridge Converter: Balanced transformer drive, efficient for medium-to-high power.
Full-Bridge Converter: High efficiency and very high power capability, used in EVs and servers.
Z-Source Converter: Unique impedance network allows shoot-through, good for renewables.
Multiport Converter: Enables integration of multiple sources/loads, key for hybrid systems.