Errata for the PCI Express® Base Specification Revision 5.0

December 3, 2020

Revision History

REVISION	REVISION HISTORY	DATE
1.0	First Release: Errata B2, A3, B5, A6, B7, B9, B10, B11, A14, B15, A17	2019-09-05
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Note on Errata Titles and Errata Numbering

Red text in the errata title indicates the affected document(s). Absence of red text means *PCI Express Base Specification Revision 5.0*.

Errata numbering is arbitrary and reflects numbers used during the development process.

B2 Deadlocks Caused by Port Acceptance Requirements

In Section 2.4.1, make the following changes:

2.4.1 Transaction Ordering Rules

…

To ensure deadlock-free operation, devices should not forward traffic from one Virtual Channel to another. The specification of constraints used to avoid deadlock in systems where devices forward or translate transactions between Virtual Channels is outside the scope of this document (see Appendix D for a discussion of relevant issues).

IMPLEMENTATION NOTE

Deadlocks Caused by Port Acceptance Dependencies

With certain configurations and communication paradigms, systems whose Ports have acceptance dependencies may experience deadlocks. In this context, Port acceptance dependencies refer to the Ingress Port making the acceptance of a Posted Request or Completion dependent upon the Egress Port first being able to transmit one or more TLPs. As stated earlier in this section, Endpoints, Bridges, and Switch Upstream Ports are forbidden to have these dependences. However, Downstream Ports are allowed to have these dependencies.

In certain cases, Downstream Port acceptance dependencies are unavoidable. For example, the ACS P2P Request Redirect mechanism may be redirecting some peer-to-peer Posted Requests Upstream through an RP for validation in the Root Complex. Validated Posted Requests are then reflected back down through the same RP so they can make their way to their original targets. The validated Posted Requests set up the acceptance dependency due to this internal looping. For traffic within one system, Downstream Port acceptance dependencies do not contribute to deadlocks. However, for certain types of traffic between systems, Downstream Port acceptance dependencies can contribute to deadlocks.

One general case where this may contribute to deadlocks is when two or more systems have an interconnect that enables each host to map host memory in other hosts for Programmed I/O (PIO) access, as shown on the left side of Figure x. A specific example is when two systems each have a PCIe Switch with one or more integrated by Non-Transparent Bridges (NTBs), and the two systems are connected as shown on the right side of the figure.

Deadlock can occur if each host CPU is doing a heavy stream of Posted Requests to host memory in the opposite host. If Posted Request traffic in each direction gets congested, and the Root Port (RP) in each host stops accepting Posted Requests because the RP can’t transmit outbound TLPs, deadlock occurs. The root cause of deadlock in this case is actually the adapter to the system-to-system interconnect setting up an acceptance dependency, which is forbidden for Endpoints. For the example case of PCIe Switches with integrated NTBs, the NTBs are Endpoints, and the Switch Upstream Port has the acceptance dependency. While the Root Port’s acceptance dependency is not the root cause of the deadlock, it contributes to the deadlock.

Solutions using this paradigm for intersystem communications will either need to determine that their systems don't have these acceptance dependencies or rely on other mechanisms to avoid these potential deadlocks. Such mechanisms are outside the scope of this specification.

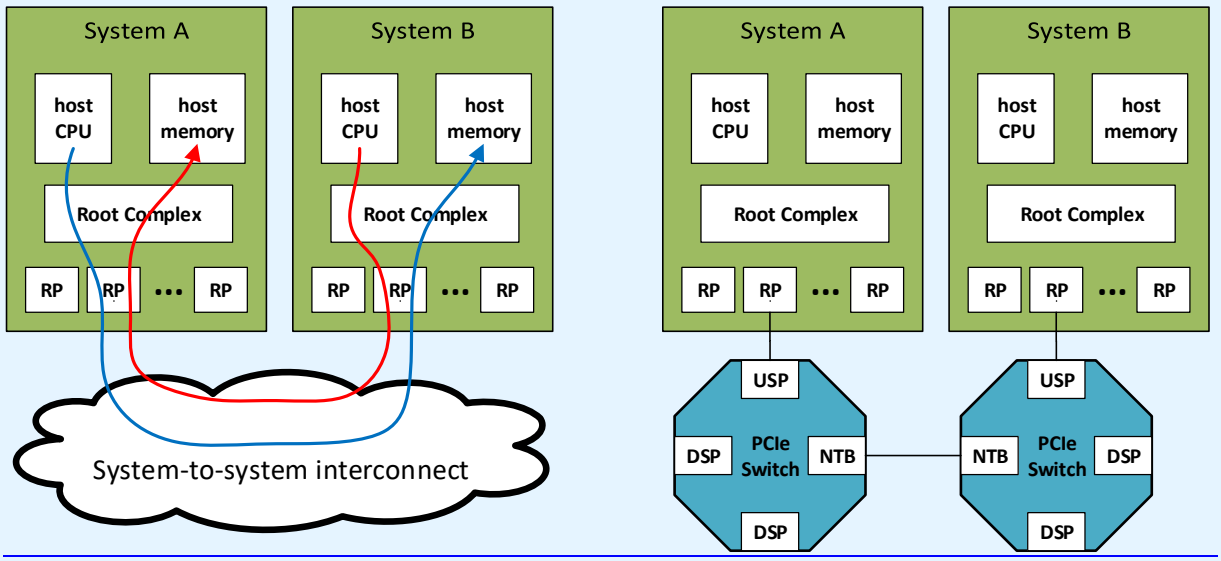

Figure X: Deadlock Examples with Intersystem Interconnects

IMPLEMENTATION NOTE
Large Memory Reads vs. Multiple Smaller Memory Reads

…

A3 Precision Time Management Byte Ordering

In Section 2.2.8.10, Page 153, Figure 2-37, change the caption as shown and add a new Implementation Note:

2.2.8.10 Precision Time Measurement (PTM) Messages

…

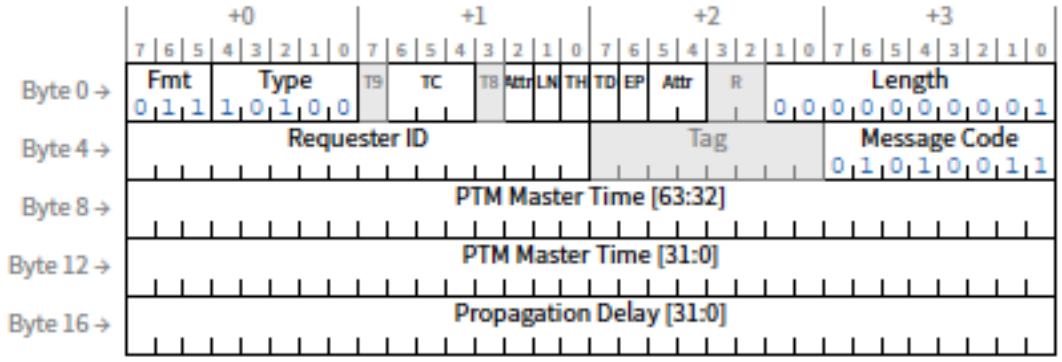

Figure 2-37 PTM ResponseD Message ~~(4 DW header and 1 DW payload)~~

IMPLEMENTATION NOTE:
Propagation Delay[31:0] Endianness

The bytes within the Propagation Delay[31:0] field (shown in Figure 2-37) are such that:

- Data Byte 0 contains Propagation Delay [31:24]
- Data Byte 1 contains Propagation Delay [23:16]
- Data Byte 2 contains Propagation Delay [15:08]
- Data Byte 3 contains Propagation Delay [07:00]

Due to ambiguity in previous versions of this document, some implementations made this interpretation:

- Data Byte 0 contains Propagation Delay [07:00]
- Data Byte 1 contains Propagation Delay [15:08]
- Data Byte 2 contains Propagation Delay [23:16]
- Data Byte 3 contains Propagation Delay [31:24]

As a result, it is recommended that implementations provide mechanisms for adapting to either byte interpretation.

B5 Translation Completion Messages

In Section 10.2.3.8, add the following Implementation Note:

10.2.3 Translation Completion

…

10.2.3.8 Global Mapping (Global)

If Global is Set, the requesting Function is permitted to create a Global Mapping entry in the ATC for this translation. If Global is Clear, the requesting Function is not permitted to create a Global Mapping entry in the ATC for this translation. Global Mapping entries apply to all PASIDs of the Function. They permit the ATC to reduce the number of translation requests needed and to reduce the memory needed for caching the results.

A Function is permitted to ignore this bit and always create non-Global Mapping entries in the ATC. This could result in multiple translations being requested for the same Untranslated Address under different PASIDs.

Functions that use this bit must also have the Global Invalidate Supported bit Set (see Section 10.5.1.2).

IMPLEMENTATION NOTE

TLP Length, Address, and Byte Offset Values for Translation Request Completions

The intention behind the rules for Translation Completions containing multiple translations is to make the TLPs look similar to those contained in a Memory Read Completion.

For single TLP Translation Completions, the goal is to make the Completion look as though it is a Memory Read Completion that ends on an RCB. As such, the Length and Byte Count will indicate the same value, and the Lower Address will contain the value that makes the TLP appear to end on an RCB.

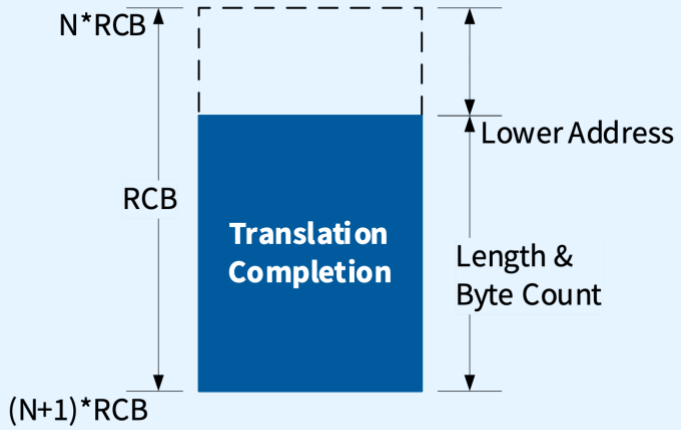

Figure 10-x1 Example Translation Completion with 1 TLP

To intermediate components (which do not track the transaction) this TLP will be indistinguishable from a Memory Read Completion ending on an RCB.

For Translation Completions consisting of two TLPs, the goal is to make the Completion look as though it is a Memory Read Completion that crosses an RCB. As Such, the first Completion TLP will contain Lower Address & Length values which make the TLP appear to end on an RCB. The Byte Count of the first TLP will indicate the total length of all the Translation Completions sent in this transaction. For the second TLP, the Length and Byte Count fields will indicate the same value, and the Lower Address value will be 0.

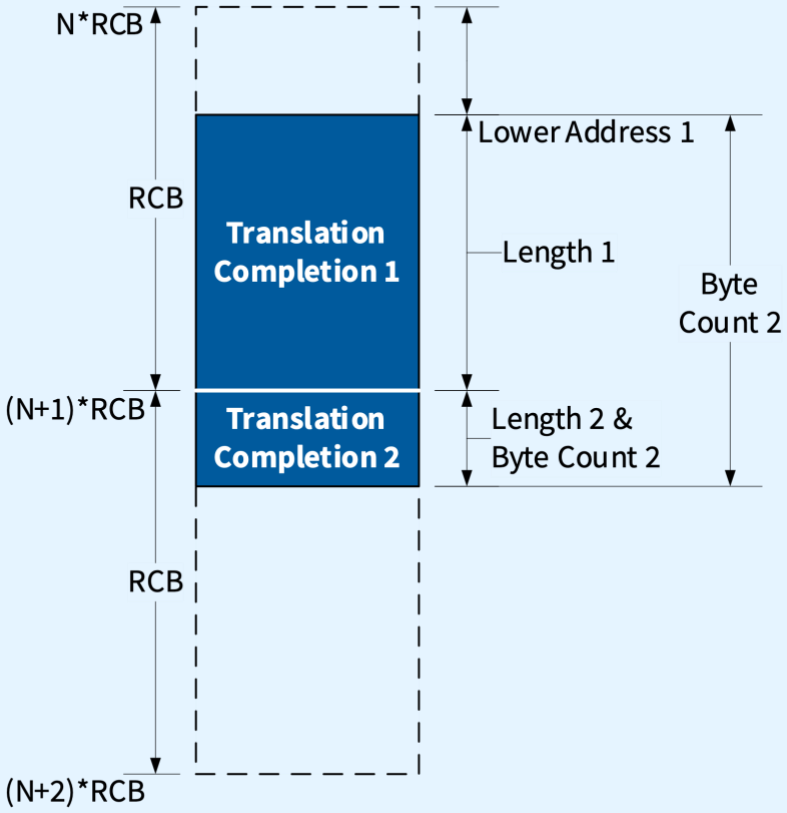

Figure 10-x2 Example Translation Completion with 2 TLPs

To intermediate components (which do not track the transaction) this Completion transaction will be indistinguishable from a Memory Read Completion that crosses an RCB.

Note that the Length field is measures DWORDs, whereas the Lower Address and Byte Offset fields are measured in Bytes.

Provided the TLPs are properly formatted, A TA may choose to split the Translation Completion between any 2 Translation Completion Data Entries. Because an ATC cannot request more translations than can fit within a single RCB, the architectural maximum number of Translation Completion Data Entries can be sent in a single Completion TLP.

A6 Precision Time Management Equation 6-2

In Section 6.22.2, in Equation 6-2 add term t2' and correct spelling of PTM. This equation was inadvertently changed in Revision 5.0. Revision 4.0 was correct.

6.22.2 PTM Link Protocol

…

$$\text{PTM}\sout{\text{PMT}}\ \text{Master Time at } t1' = t2' - \frac{\left((t4 - t1) - (t3 - t2)\right)}{2}$$

Equation 6-2 PTM Master Time

B7 Vital Product Data Capability

In Section 7.9.16, Figure 7-281, change the name of the field at Byte Offset +004h from Message Address to VPD Data Register.

7.9.19 Vital Product Data Capability (VPD Capability)

…

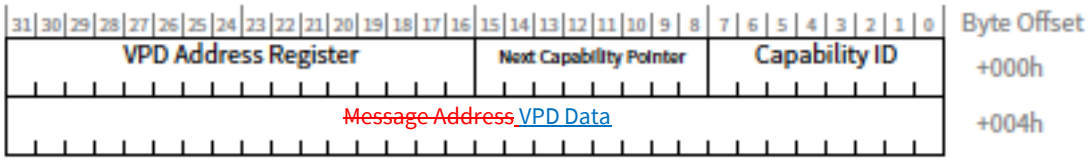

Figure 7-281 VPD Capability Structure

…

B9 ACS Redirect and Guest Physical Addresses (GPAs)

In Section 6.12.4, move text to a new paragraph as follows:

6.12.4 ACS Enhanced Capability

…

IMPLEMENTATION NOTE
ACS Redirect and Guest Physical Addresses (GPAs)
ACS redirect mechanisms were originally architected to enable fine-grained access control for P2P Memory Requests, by redirecting selected Requests Upstream to the RC, where validation logic determines whether to allow or deny access. However, ACS redirect mechanisms can also ensure that Functions under the direct control of VMs have their DMA Requests routed correctly to the Translation Agent in the host, which then translates their guest physical addresses (GPAs) into host physical addresses (HPAs).

GPA ranges used for Memory Space vs. DMA are not guaranteed to coincide with HPA ranges, which the PCIe fabric uses for Memory Request routing and access control. If any GPAs used for DMA fall with within the HPA ranges used for Memory Space, legitimate or malicious packet misrouting can result.

ACS redirect mechanisms can ensure that Upstream Memory Requests with GPAs intended for DMA never get routed to HPA Memory ranges. ACS P2P Request Redirect handles this for (1) peer accesses between Functions within a Multi-Function Device and (2) peer accesses between Downstream Ports within a Switch or RC. ACS P2P Egress Control with redirect handles this in a more fine-grained manner for the same two cases.

Redirect mechanisms introduced with ACS Enhanced Capability handle this for additional cases. ACS DSP Memory Target Access with redirect handles this for Downstream Port Memory Resource ranges. ACS USP Memory Target Access with redirect handles this for Switch Upstream Port Memory Resource ranges. In Switches, ACS Unclaimed Request Redirect handles this for any areas within Upstream Port Memory apertures that are not handled by the other ACS redirect mechanisms. ~~Together these ACS redirect mechanisms can ensure that Upstream Memory Requests with GPAs intended for DMA are always routed or redirected to the Translation Agent in the host, and those with GPAs intended for P2P are still routed as originally architected.~~

Together these ACS redirect mechanisms can ensure that Upstream Memory Requests with GPAs intended for DMA are always routed or redirected to the Translation Agent in the host, and those with GPAs intended for P2P are still routed as originally architected.

B10 ACS Capability Register

In Section 7.7.8.2, Table 7-85, make the following changes:

7.7.8.2 ACS Capability Register (Offset 04h)

…

Table 7-85 ACS Capability Register

Bit Location	Register Description	Attributes
7	**ACS Enhanced Capability** - Required for Root Ports and Switch Downstream Ports that support the ACS Enhanced Capability mechanisms. If Set, indicates that the component supports all of the following mechanisms that are applicable: ~~any of the following mechanisms:~~ • ACS I/O Request Blocking • ACS DSP Memory Target Access • ACS USP Memory Target Access • ACS Unclaimed Request Redirect	RO

B11 ACS Control Register

In Section 7.7.8.3, Table 7-86, make the following changes:

7.7.8.3 ACS Control Register (Offset 06h)

…

Table 7-86 ACS Control Register

Bit Location	Register Description	Attributes
11:10	**ACS USP Memory Target Access Control** - This field controls how a Switch Downstream Port handles Upstream Memory Requests attempting to access any Memory BAR Space on the Switch Upstream Port. See Section 6.12.1.1 . Defined Encodings are: 00b Direct Request access enabled 01b Request blocking enabled 10b Request redirect enabled 11b Reserved This field is required for ~~Root Ports and~~ Switch Downstream Ports if the ACS Enhanced Capability bit is Set and there is applicable Memory BAR Space to protect; otherwise it must be RsvdP. The default value of this field is 00b.	RW/RsvdP

A14 L1 ASPM State

In Section 5.4.1.2, make the following changes:

5.4.1.2 L1 ASPM State

…

When supported, L1 entry is controlled ~~disabled~~ by ~~default in~~ the ASPM Control field. Software must enable ASPM L1 on the Downstream component only if it is supported by both components on a Link. Software must sequence the enabling and disabling of ASPM L1 such that the Upstream component is enabled before the Downstream component and disabled after the Downstream component.

B15a Flattening Portal Bridge Configuration Forwarding (Updated B15)

In Section 6.27.2, make the following changes:
(B15a is an updated version of the earlier B15.
The highlighted change in the 2nd paragraph is new.)

6.27.2 Hardware and Software Requirements

…

When ARI Forwarding is not supported, or when the ARI Forwarding Enable bit in the Device Control 2 Register is Clear, FPB hardware must convert a Type 1 Configuration Request received on the Primary side

of the FPB to a Type 0 Configuration Request on the Secondary side of the FPB when bits 15:3 of the Routing ID of the Type 1 Configuration Request matches the value in the RID Secondary Start field in the FPB RID Vector Control 2 Register, and system software must configure the FPB accordingly

When the ARI Forwarding Enable bit in the Device Control 2 Register is Set, FPB hardware must convert a Type 1 Configuration Request received on the Primary side of the FPB to a Type 0 Configuration Request on the Secondary side of the FPB when the Bus Number portion of the Routing ID of the Type 1 Configuration Request matches the value in the Bus Number address (bits 15:8 only) of the RID Secondary Start field in the FPB RID Vector Control 2 Register, and system software must configure the FPB accordingly.

…

For FPBs associated with Upstream Ports of Switches only, when the FPB RID Decode Mechanism Enable bit is Set, FPB hardware must use the FPB Num Sec Dev field of the FPB Capabilities register to indicate the quantity of Device Numbers associated with the Secondary Side of the Upstream Port bridge, which must be used by the FPB in addition to the RID Secondary Start field in the FPB RID Vector Control 2 Register to determine when a Configuration Request received on the Primary side of the FPB targets one of the Downstream Ports of the Switch, determining in effect when such a Request must be converted ~~form~~ from a Type 1 Configuration Request to a Type 0 Configuration Request, and system software must configure the FPB appropriately

A17 DL_Feature Corrections

In Section 3.2.1, make the following changes:

3.2.1 Data Link Control and Management State Machine Rules

…

Exit to DL_Feature if:

- The Port supports the optional Data Link Feature Exchange, the Data Link Feature Exchange Enable bit is Set or the Data Link Feature Capability is not implemented, the Transaction Layer indicates that the Link is not disabled by software, and the Physical Layer reports Physical LinkUp = 1b

…

In Section 3.3, make the following changes:

3.3 Data Link Feature Exchange

The Data Link Feature Exchange protocol is required for Ports that support 16.0 GT/s and higher data rates. It is optional for other Ports. Ports that implement this protocol …

B18 SRIS Retimer Latency Limits

In Table 4-30, Section 4.3.9, make the following changes:

4.3.9 SRIS

…

Table 4-30 Retimer Latency Limit SRIS (Symbol times)

Max_Payload_Size	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s
128 Bytes	34 (max)	34 (max)	66 (max)	130 (max)	~~194~~ 258 (max)
256 Bytes	36 (max)	36 (max)	68 (max)	132 (max)	~~196~~ 260 (max)
512 Bytes	39 (max)	39 (max)	71 (max)	135 (max)	~~199~~ 263 (max)
1024 Bytes	46 (max)	46 (max)	78 (max)	142 (max)	~~206~~ 270 (max)
2048 Bytes	59 (max)	59 (max)	91 (max)	155 (max)	~~219~~ 283 (max)
4096 Bytes	86 (max)	86 (max)	118 (max)	182 (max)	~~246~~ 310 (max)

B19 Received Target Abort and Received Master Abort

In Table 7-4, modify bits 12 and 13 as follows:

Table 7-4 Status Register

Bit Location	Register Description	Attributes
12	***Received Target Abort*** - See Section 7.5.1.1.14. On a Function with a Type 0 Configuration Space Header, ~~T~~this bit is Set when a Requester receives a Completion with Completer Abort Completion Status. On a Function with a Type 1 Configuration Space Header, ~~the~~ this bit is Set when ~~the Completer Abort is received by~~ its Primary Side receives a Completion with Completer Abort Completion Status. Functions with a Type 0 Configuration Space Header that do not make Non-Posted Requests on their own behalf are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	RW1C
13	***Received Master Abort*** - See Section 7.5.1.1.14. On a Function with a Type 0 Configuration Space Header, ~~T~~this bit is Set when a Requester receives a Completion with Unsupported Request Completion Status. On a Function with a Type 1 Configuration Space Header, ~~the~~ this bit is Set when ~~the Unsupported Request is received by~~ its Primary Side receives a Completion with Unsupported Request Completion Status. Functions with a Type 0 Configuration Space Header that do not make Non-Posted Requests on their own behalf are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	RW1C

B20 Expansion ROM Base Address Register

In Section 7.5.1.2.4, make the following changes:

7.5.1.2.4 Expansion ROM Base Address Register (Offset 30h)

Some Functions, especially those that are intended for use on add-in cards, require local EPROMs for Expansion ROM (refer to the [PCI-Firmware] for a definition of ROM contents). This register is defined to

handle the base address and size information for this Expansion ROM. The register layout is shown in Figure 7-13 and Table 7-9 describes the bits in the register.

Functions that support an expansion ROM must allow that ROM to be accessed with any combination of byte enables.

B21 Transition to DL_Inactive via DPC

In Section 3.2.1, make the following changes:

3.2.1 Data Link Control and Management State Machine Rules

…

- DL_Active:
  - …
  - Exit to DL_Inactive if:
    - Physical Layer reports Physical LinkUp = 0b
    - Downstream Ports that are Surprise Down Error Reporting Capable (see Section 7.5.3.6) must treat this transition from DL_Active to DL_Inactive as a Surprise Down error, except in the following cases where this error detection is blocked:
      - If the Secondary Bus Reset bit in the Bridge Control register has been Set by software, then the subsequent transition to DL_Inactive must not be considered an error.
      - If the Link Disable bit has been Set by software or if DPC has been triggered, then the subsequent transition to DL_Inactive must not be considered an error.
      - If a Switch Downstream Port transitions to DL_Inactive due to an event above that Port, that transition to DL_Inactive must not be considered an error. Example events include the Switch Upstream Port propagating Hot Reset, the Switch Upstream Link transitioning to DL_Down, and the Secondary Bus Reset bit in the Switch Upstream Port being Set.

B28 Transaction Ordering Rules and IDO

In Section 2.4.1, make the following changes:

2.4.1 Transaction Ordering Rules

…

A2b

A Posted Request with RO29 Set is permitted to pass another Posted Request.30 A Posted Request with IDO Set is permitted to pass another Posted Request if the two Requester IDs are different. Additionally, a Posted Request with IDO Set is permitted to pass another Posted Request with the same Requester ID ~~or~~ if both Requests contain a PASID TLP Prefix and the two PASID values are different.

…

B2b

A Read Request with IDO Set is permitted to pass a Posted Request if the two Requester IDs are

different. Additionally, a Read Request with IDO Set is permitted to pass a Posted Request with the same Requester ID ~~or~~ if both Requests contain a PASID TLP Prefix and the two PASID values are different.

…

C2b

An NPR with Data and with RO Set31 is permitted to pass Posted Requests. An NPR with Data and with IDO Set is permitted to pass a Posted Request if the two Requester IDs are different. Additionally, an NPR with Data and with IDO Set is permitted to pass a Posted Request with the same Requester ID ~~or~~ if both Requests contain a PASID TLP Prefix and the two PASID values are different.

B29 Recovery.Equalization

In Section 4.2.6.4.2, make the following changes:

4.2.6.4.2 *Recovery.Equalization*

If this state was entered from Recovery.RcvrLock, Transmitter sends TS1 Ordered Sets on all configured Lanes using the same Link and Lane numbers that were set after leaving Configuration ~~if this state was entered from Recovery.RcvrLock~~.

If this state was entered from Loopback.Entry:

- Transmitter sends TS1 Ordered Sets on all Lanes that detected a Receiver during Detect ~~the Lane under test~~ using the Link and Lane numbers defined in Loopback.Entry.
- ~~If this state was entered from Loopback.Entry,~~ The Lane under test is the only Lane that participates in the equalization procedure; the Lanes that are not under test ~~must be treated as not configured for the duration of Recovery.Equalization, and they~~ must not be included in the equalization procedure and anything received by them is permitted to be ignored. The Lanes that are not under test must have their Transmitter preset values set to P4. The sole purpose of the lanes that are not under test is to create the noise that is needed in Loopback.Active.

B30 Phase 3 of Transmitter Equalization

In Section 4.2.6.4.2.1.3, make the following changes:

4.2.6.4.2.1.3 Phase 3 of Transmitter Equalization

…

- Next state is Loopback.Entry if the data rate of operation is 32.0 GT/s, perform_equalization_for_loopback is 1b and one of the following conditions is satisfied:
  a. The Lane under test is operating at its optimal setting and ~~all Lanes receive~~ it received two consecutive TS1 Ordered Sets with the Retimer Equalization Extend bit set to 0b ~~are received~~.
  b. A 24 ms timeout with a tolerance of -0 ms and +2 ms.

B31 Loopback.Active

In Section 4.2.6.10.2, make the following changes:

4.2.6.10.2 Loopback.Active

…

- A Loopback Slave that entered Loopback~~.Active~~ from Recovery.Equalization must transmit the Modified Compliance Pattern on all Lanes that detected Receivers in Detect.Active but are not under test if the transmit_modified_compliance_pattern_in_loopback variable is set to 1b, otherwise those Lanes must be transitioned into Electrical Idle. The Lane under test must follow Loopback Slave rules described below.

B32 Alternate Protocol Control Register

In Table 7-236, Section 7.9.21.3, make the following changes:

7.9.21.3 Alternate Protocol Control Register (Offset 08h)

Table 7-236 Alternate Protocol Control Register

Bit Location	Register Description	Attributes
8	***Alternate Protocol Negotiation Global Enable*** - When this bit is Set, Alternate Protocol Negotiation is enabled for this Link. When this bit is Clear, Alternate Protocol Negotiation is disabled for this Link. This bit is RW for Downstream Ports. It is HwInit for Upstream Ports. Default is 0b.	RW/HwInit (see description)

B32a Flattening Portal Bridges

In Section 6.27.2, make the following changes:

6.27.2 Hardware and Software Requirements

…

The following rules apply to the FPB Routing ID (RID) mechanism:

- FPB hardware must consider a specific range of RIDs to be associated with the Secondary side of the FPB if the Bus Number portion falls within the Bus Number range indicated by the values programmed in the Secondary and Subordinate Bus Number registers logically OR'd with the value programmed into the corresponding entry in the FPB RID Vector.
- System software must configure the Configuration Request Type 1 to Type 0 conversion mechanisms in a Bridge Function before attempting to pass Configuration Requests through that Bridge.
- System software must either program the legacy and FPB mechanisms for Configuration Request Type 1 to Type 0 conversion in a Bridge Function such that they give identical results, or such that one of the two mechanisms is disabled.

  - If it is intended to use only the FPB RID mechanism for BDF decoding, then system software must ensure that both the Secondary and Subordinate Bus Number registers are 0. {editors note – demoted this existing bullet}
  - If it is intended to enable the FPB RID Decode Mechanism, but to use only the legacy mechanism for Configuration Request Type 1 to Type 0 conversion, then system software must write bits 7:3 of the RID Secondary Start field to 0 0000b.
- System software must ensure that the FPB routing mechanisms are configured such that Configuration Requests targeting Functions Secondary side of the FPB will be routed by the FPB from the Primary to Secondary side of the FPB.

…

- For FPBs associated with Upstream Ports of Switches only, when the FPB RID Decode Mechanism Enable bit is Set, FPB hardware must use the FPB Num Sec Dev field of the FPB Capabilities register to indicate the quantity of Device Numbers associated with the Secondary Side of the Upstream Port bridge, which must be used by the FPB in addition to the RID Secondary Start field in the FPB RID Vector Control 2 Register to determine when a Configuration Request received on the Primary side of the FPB targets one of the Downstream Ports of the Switch, determining in effect when such a Request must be converted form a Type 1 Configuration Request to a Type 0 Configuration Request, and system software must configure the FPB appropriately.
  - System software configuring FPB must comprehend that the logical internal structure of a Switch will change depending on the value of the FPB RID Decode Mechanism Enable bit in the Upstream Port of a Switch.
  - Downstream Ports must use their corresponding RID values, and their Requester IDs and Completer IDs, as determined by the Upstream Port's FPB Num Sec Dev and RID Secondary Start values
  - All implemented Functions in the range determined by the Switch Upstream Port Function's RID Secondary Start and FPB Num Sec Dev must be Switch Downstream Ports associated with that Switch Upstream Port; System Software is required to scan all Functions in this range to determine which are Implemented.
  - It is strongly recommended that System Software assign the RID Secondary Start such that the Bus and Device Numbers are not the same as for the Switch Upstream Port; otherwise, the resulting hardware behavior is undefined
- For FPBs associated with Upstream Ports of Switches only, hardware must comprehend that Configuration Requests targeting the Upstream Port itself and any Downstream Ports of the Switch flattened into the range of Function Numbers with the same Bus and Device Numbers as the Upstream Port itself will be converted from Type 1 to Type 0 by the Downstream Port above the Switch, but any other Downstream Ports of the Switch flattened into successive Device Numbers will not be converted from Type 1 to Type 0 by the Downstream Port above the Switch and so must effectively be converted from Type1 to Type0 by the Switch Upstream Port itself.

  This is a special case, but the concept is not unique to FPB, and is a reflection of the definition of the relationship between Bus/Device Numbers and Function Numbers – Function Numbers are always determined by the hardware of the Upstream Port, whereas the Bus and Device Numbers for an Upstream Port are always determined by the Downstream Port immediately above the Upstream Port.
- FPBs must implement bridge mapping for INTx virtual wires (see Section 2.2.8.1)

B33 Device/Port Type

In Table 7-18, Section 7.5.3.2, add the following footnote:

Table 7-18 PCI Express Capabilities Register

Bit Location	Register Description	Attributes

7:4	**Device/Port Type** footnote – Indicates the specific type of this PCI Express Function. Note that different Functions in a Multi-Function Device can generally be of different types. Defined encodings for Functions that implement a Type 00h PCI Configuration Space header are:	RO

…

footnote This field would be better named 'Function Type' but for historical reasons is named Device/Port Type.

B34 Readiness Time Reporting

In Table 7-218 Section 7.19.17.2, make the following changes:

7.9.17.2 Readiness Time Reporting 1 Register (Offset 04h)

…

Table 7-218 Readiness Time Reporting 1 Register

Bit Location	Register Description	Attributes
11:0	***Reset Time*** – is the time ~~the~~ a non-VF Function requires to become Configuration-Ready after the completion of Conventional Reset. For VF semantics, see Section 9.3.3.3.1 <VF Enable>. This field is RsvdP if the Immediate Readiness bit is Set. This field is undefined when the Valid bit is Clear. This field must be less than or equal to the encoded value A1Eh.	HwInit/RsvdP
23:12	***DL_Up Time*** - is the time the Function requires to become Configuration-Ready after the Downstream Port above the Function reports Data Link Layer Link Active. This field is RsvdP in Functions that are not associated with an Upstream Port. For VFs, this field is not applicable and is RsvdP. This field is undefined when the Valid bit is Clear. This field must be less than or equal to the encoded value A1Eh.	HwInit/RsvdP
…	…	…

In Table 7-219 Section 7.19.17.3, make the following changes:

7.9.17.3 Readiness Time Reporting 2 Register (Offset 08h)

…

Table 7-219 Readiness Time Reporting 2 Register

Bit Location	Register Description	Attributes
11:0	***FLR Time*** - is the time that the Function requires to become Configuration-Ready after it was issued an FLR.	HwInit/RsvdP

	This field is RsvdP when the Function Level Reset Capability bit is Clear (see Section 7.5.3.3). This field is undefined when the Valid bit is Clear. This field must be less than or equal to the encoded value A1Eh.	
23:12	***D3$_{Hot}$ to D0 Time*** - If Immediate_Readiness_on_Return_to_D0 is Clear, D3Hot to D0 Time is the time that ~~the~~ a non-VF Function requires after it is directed from D3Hot to D0 before it is Configuration-Ready and has returned to either D0uninitialized or D0active state ~~(see the *PCI Bus Power Management Interface Specification*)~~. For VF semantics, see Section 9.6.1 <VF Device Power Management States>. This field is RsvdP if the Immediate_Readiness_on_Return_to_D0 bit is Set. For a VF that does not implement the PCI Power Management Capability, this field is undefined. This field is undefined when the Valid bit is Clear. This field must be less than or equal to the encoded value 80Ah.	HwInit/RsvdP

B35 Poisoned TLP

In Section 6.2.3.2.4.3, make the following changes:

6.2.3.2.4.3 Ultimate PCI Express Receiver of a Poisoned TLP

When a poisoned TLP is received by its ultimate PCI Express destination, if the severity is non-fatal and the Receiver ~~deals with the poisoned data in a manner that permits continued operation~~ legitimately chooses not to handle this case as an uncorrectable error (see below), the Receiver must handle this case[95] as an Advisory Non-Fatal Error.[96] A Receiver with AER signals the error (if enabled) by sending an ERR_COR Message. A Receiver without AER sends no error Message for this case. ~~Refer to Section 2.7.2.2 for special rules that apply for poisoned Memory Write Requests.~~

A Receiver must not handle this case as an Advisory Non-Fatal Error if either of the following apply:

- Handling the error as a Correctable Error and continuing operation when configured correctly could lead to silent data corruption.
- Rules in Section 2.7.2.2 require this case to be handled as an uncorrectable error.

An example is a Root Complex that receives a poisoned Memory Write TLP that targets host memory. If the Root Complex propagates the poisoned data along with its indication to host memory, it signals the error (if enabled) with an ERR_COR. If the Root Complex does not propagate the poison to host memory, it signals the error (if enabled) with ERR_NONFATAL.

…

{Editor's Note: Footnote:}

[95] ~~However, see Section 2.7.2.2 regarding certain Requests with Poisoned data that must be handled as uncorrectable errors.~~

B36 Alternate Protocol Negotiation Status

In Table 7-75, Section 7.7.6.6, and in Table 7-77, Section 7.7.6.8, make the following changes (both tables get the same change):

7.7.6.6 Received Modified TS Data 2 Register (Offset 14h)

7.7.6.8 Transmitted Modified TS Data 2 Register (Offset 1Ch)

…

Table 7-75 Received Modified TS Data 2 Register

Table 7-77 Transmitted Modified TS Data 2 Register

Bit Location	Description	Attributes
25:24	***Alternate Protocol Negotiation Status*** - Indicates the status of the Alternate Protocol Negotiation. Encodings are: **00b** Alternate Protocol Negotiation not supported~~ - Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear~~. **01b** Alternate Protocol Negotiation disabled~~ - Modified TS Usage Mode 2 Supported - Alternate Protocol is Set but Modified TS Usage Mode Selected was not 2 during the appropriate LTSSM State.~~ **10b** Alternate Protocol Negotiation failed - Alternate Protocol Negotiation was attempted and did not locate a protocol that was supported on both ends of the Link. **11b** Alternate Protocol Negotiation succeeded - Alternate Protocol Negotiation located one or more protocols that were supported on both ends of the Link and the Downstream Port selected one of those protocols for use. If ~~Set~~ 11b, Alternate Protocol Negotiation completed ~~succesfully~~ successfully. If ~~Clear~~ not 11b, Alternate Protocol Negotiation ~~negotiation~~ has not completed ~~succesfully~~ successfully. If Modified TS Usage Mode 1 Supported - Training Set Message and Modified TS Usage Mode 2 Supported - Alternate Protocol are both Clear, this ~~register~~ field is permitted to be hardwired to ~~0000 0000h~~ 00b. If Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear, this ~~bit~~ field is hardwired to ~~0b~~ 00b. If Modified TS Usage Mode 2 Supported - Alternate Protocol is Set and Modified TS Usage Mode Selected does not equal 2, this ~~bit contains 0b~~ field must return 01b. This ~~bit~~ field is ~~Cleared~~ cleared to 00b on entering Detect ~~LTSSM State~~. Default is ~~0b~~ 00b.	RO

B37 Configuration.Linkwidth.Accept

In Section 4.2.6.3.2, make the following changes:

4.2.6.3.2 Configuration.Linkwidth.Accept

4.2.6.3.2.1 Downstream Lanes

- If a configured Link can be formed with at least one group of Lanes that received two consecutive TS1 Ordered Sets with the same received Link number (non-PAD and matching one that was transmitted by the Downstream Lanes), TS1 Ordered Sets are transmitted with the same Link number and unique non-PAD Lane numbers are assigned to all these same Lanes. The next state is Configuration.Lanenum.Wait.
    - The assigned non-PAD Lane numbers must range from 0 to n-1, be assigned sequentially to the same grouping of Lanes that are receiving the same Link number, and Downstream Lanes which are not receiving TS1 Ordered Sets must not disrupt the initial sequential numbering of the widest possible Link. Any left over Lanes must transmit TS1 Ordered Sets with the Link and Lane number set to PAD.
    - It is recommended that any possible multi-Lane Link that received an error in a TS1 Ordered Set or lost 128b/130b Block Alignment on a subset of the received Lanes delay the evaluation listed above by an additional two, or more, TS1 Ordered Sets when using 8b/10b encoding, or by an additional 34, or more, TS1 Ordered Sets when using 128b/130b encoding, but must not exceed 1 ms, so as not to prematurely configure a smaller Link than possible.
    - The use_modified_TS1_TS2_Ordered_Set variable must be set to 1b if all of the following conditions are true:
        - LinkUp = 0b
        - The component had transmitted Modified TS1/TS2 Ordered Sets supported value (11b) in the Enhanced Link Behavior Control field in Symbol 5 of TS1 and TS2 Ordered Sets in Polling and Configuration states since entering the Polling State
        - The received eight consecutive TS2 Ordered Sets on all Lanes of the ~~currently~~ configured Link that could be formed (see 1st bullet of Section 4.2.6.3.2.1) that were part of the group that caused the transition from Polling.Configuration to Configuration state had the Modified TS1/TS2 Ordered Sets supported value (11b) in the Enhanced Link Behavior Control field in Symbol 5 and 32.0 GT/s data rate is supported bit is set to 1b in the ~~receieved~~ received eight consecutive TS2 Ordered Sets
- The next state is Detect after a 2 ms timeout or if no Link can be configured or if all Lanes receive two consecutive TS1 Ordered Sets with Link and Lane numbers set to PAD.

4.2.6.3.2.2 Upstream Lanes

- If a configured Link can be formed using Lanes that transmitted a non-PAD Link number which are receiving two consecutive TS1 Ordered Sets with the same non-PAD Link number and any non-PAD Lane number, TS1 Ordered Sets are transmitted with the same non-PAD Link number and Lane numbers that, if possible, match the received Lane numbers or are different, if necessary, (i.e., Lane reversed). The next state is Configuration.Lanenum.Wait.
    - The received consecutive TS1 Ordered Sets may be either standard TS1 Ordered Sets or Modified TS1 Ordered Sets. Modified TS1 Ordered Sets will only be received if the conditions to Set the use_modified_TS1_TS2_Ordered_Set variable (as described below) are met.
    - The newly assigned Lane numbers must range from 0 to m-1, be assigned sequentially only to some continuous grouping of Lanes that are receiving non-PAD Lane numbers (i.e., Lanes which are not receiving any TS1 Ordered Sets always disrupt a continuous grouping and must not be included in this grouping), must include either Lane 0 or Lane n-1 (largest received Lane number), and m-1 must be equal to or smaller than the largest received Lane number (n-1). Remaining Lanes must transmit TS1 Ordered Sets with Link and Lane numbers set to PAD.

- It is recommended that any possible multi-Lane Link that received an error in a TS1 Ordered Set or lost 128b/130b Block Alignment on a subset of the received Lanes delay the evaluation listed above by an additional two, or more, TS1 Ordered Sets when using 8b/10b encoding, or by an additional 34, or more, TS1 Ordered Sets when using 128b/130b encoding, but must not exceed 1 ms, so as not to prematurely configure a smaller Link than possible.
- The use_modified_TS1_TS2_Ordered_Set variable must be set to 1b if all of the following conditions are true:
  - LinkUp = 0b
  - The component has transmitted Modified TS1/TS2 Ordered Sets supported value (11b) in the Enhanced Link Behavior Control field in Symbol 5 of all TS1 and TS2 Ordered Sets in Polling and Configuration states since entering the Polling State
  - The received eight consecutive TS2 Ordered Sets on all Lanes of the ~~currently~~ configured Link that could be formed (see 1st bullet of Section 4.2.6.3.2.2) that were part of the group that caused the transition …

B39 SR-IOV Usage of PCI Express Extended Capabilities

In Table 9-23, Section 9.3.7, make the following changes:

9.3.7 PCI Express Extended Capabilities Changes

Table 9-23 SR-IOV Usage of PCI Express Extended Capabilities

Extended Capability ID	Description	PF Attributes	VF Attributes
…	…	…	…
002Ah	Physical Layer 32.0 GT/s Extended Capability	Base	Must not implement
002Bh	Alternate Protocol Extended Capability	Base	Must not implement
002Ch	SFI Extended Capability (System Firmware Intermediary)	Base	Must not implement
002Dh	Shadow Functions	Base	Base

B42 Routing ID

In Terms and Acronyms, make the following changes:

…

Routing ID, RID
: Either the Requester ID or Completer ID that identifies a PCI Express Function.

In Section 10.1.1, make the following changes:

10.1.1 Address Translation Services (ATS) Overview

…

ATS TLPs are routed using either address-based or ~~Requester ID (RID)~~ ID-based routing

In Section 10.4.2, make the following changes:

10.4.2 Page Request Group Response Message

…

All other fields are standard PCIe message fields. (Note: these messages are routed based on the ID in bytes 8 and 9; with bytes 4 and 5 containing the host's Requester ID ~~RID~~.)

B43 Aux_Current

In Table 7-13, Section 7.5.2.1, make the following changes:

7.5.2.1 Power Management Capabilities Register (Offset 00h)

…

Table 7-13 Power Management Capabilities Register

Bit Location	Description	Attributes
24:22	**Aux_Current** - This 3 bit field reports the Vaux auxiliary current requirements for the Function. If this Function implements the Data register ~~Register~~, this field must be hardwired to 000b. If PME_Support is 0 xxxxb (PME assertion from D3Cold is not supported) and the Aux Power PM Enable feature is not implemented, this field must be hardwired to 000b ~~0000b~~. For Functions where PME_Support is 1 xxxxb (PME assertion from $D3_{Cold}$ is supported), and which do not implement the Data register, the following encodings apply : …	RO

B45a Multiple Message Enable

In Table 7-39, Section 7.7.1.2, make the following changes:

7.7.1.2 Message Control Register for MSI (Offset 02h)

…

Table 7-39 Message Control Register for MSI

Bit Location	Description	Attributes
6:4	***Multiple Message Enable*** - software writes to this field to indicate the number of allocated vectors ~~(equal to or less than the number of requested vectors)~~. The number of allocated vectors is aligned to a power of two. ~~If~~ As an example, if a Function requests four vectors (indicated by a Multiple Message Capable encoding of 010b), ~~system~~ software can allocate either four, two, or one vector by writing a 010b, 001b, or 000b to this field, respectively. Behavior is undefined if the number of vectors allocated is greater than the number of vectors requested. When MSI Enable is Set, a Function will be allocated at least 1 vector. The encoding is defined as: 000b 1 vector allocated 001b 2 vectors allocated 010b 4 vectors allocated 011b 8 vectors allocated 100b 16 vectors allocated 101b 32 vectors allocated 110b Reserved 111b Reserved Default value of this field is 000b.	RW

B46 Power Management Control/Status Register

In Table 7-14, Section 7.5.2.2, make the following changes:

7.5.2.2 Power Management Control/Status Register (Offset 04h)

Table 7-14 Power Management Control/Status Register

Bit Location	Register Description	Attributes
8	**PME_En** - When Set, the Function is permitted to generate a PME. When Clear, the Function is not permitted to generate a PME. If PME_Support is 1 xxxxb (PME generation from $D3_{Cold}$) or the Function consumes auxiliary power and auxiliary power is available this bit is RWS and the bit is not modified by Conventional Reset or FLR If PME_Support is 0 xxxxb, this field is not sticky (RW) and defaults to 0b in response to a Conventional Reset or an FLR.	RW/RWS

	If PME_Support is 0 0000b, this bit is permitted to be hardwired to 0b.	

B48 Loopback.Active

In Section 4.2.6.10.2, make the following changes:

4.2.6.10.2 Loopback.Active

…

A Loopback Slave that entered Loopback.Active from Recovery.Equalization must transmit the Modified Compliance Pattern on all Lanes that detected Receivers in Detect.Active but are not under test if the transmit_modified_compliance_pattern_in_loopback variable is set to 1b, otherwise those Lanes must be transitioned into Electrical Idle. The Lane under test must follow Loopback Slave rules described below. State transitions must be based only on Link activity on the Lane under test.

B50 Configuration.Lanenum.Accept

In Section 4.2.6.3.3, make the following changes:

4.2.6.3.3 Configuration.Lanenum.Accept

…

4.2.6.3.3.1 Downstream Lanes

- If two consecutive TS1 Ordered Sets are received with non-PAD Link and non-PAD Lane numbers that match all the non-PAD Link and non-PAD Lane numbers (or reversed Lane numbers if Lane reversal is optionally supported) that are being transmitted in Downstream Lane TS1 Ordered Sets, the next state is Configuration.Complete. If the use_modified_TS1_TS2_Ordered_Set variable is Set and an Alternate Protocol Negotiation is being performed, the transition to Configuration.Complete must be delayed for 10 µs or until the Downstream Port receives the Upstream Port's response to that protocol request (whichever happens first). See Section 4.2.4.2 for Alternate Protocol Negotiation details. Note that Retimers are permitted to delay the transition to Configuration.Complete, as described in Section 4.3.8 .

…

4.2.6.3.3.2 Upstream Lanes

- If two consecutive TS2 Ordered Sets are received with non-PAD Link and non-PAD Lane numbers that match all non-PAD Link and non-PAD Lane numbers that are being transmitted in Upstream Lane TS1 Ordered Sets, the next state is Configuration.Complete. If the use_modified_TS1_TS2_Ordered_Set variable is Set, an Alternate Protocol Negotiation was performed, and the Downstream Port decided not to use any Alternate Protocol, the received TS2 Ordered Sets will have Modified TS Usage set to a value as defined in Table 4-9. See Section 4.2.4.2 for Alternate Protocol Negotiation details. Note that Retimers are permitted to delay the transition to Configuration.Complete, as described in Section 4.3.8 .

B52 Alternate Protocol Negotiation

In Table 4-9, Section 4.2.4.2, make the following changes:

4.2.4.2 Alternate Protocol Negotiation

…

Table 4-9 Modified TS Information 1 field in Modified TS1/TS2 Ordered Sets if Modified TS Usage = 010b (Alternate Protocol)

Bits	Field	Description
4:3	Alternate Protocol Negotiation Status	For Modified TS1 Ordered Sets: … For Modified TS2 Ordered Sets: **00b** Indicates a protocol confirmation from the Downstream Port as well as the Upstream Port. Behavior is undefined if the Downstream Port had not earlier received status 10b for this protocol in this instance of protocol negotiation during the Modified TS1 Ordered Sets. Similarly, behavior is undefined if the Upstream Port had not earlier transmitted status 10b for this protocol in this instance of protocol negotiation during the Modified TS1 Ordered Sets. No protocol is selected unless the Downstream Port sends and receives a protocol confirmation in the Modified TS2 Ordered Sets. If the Downstream Port decides not to use any Alternate Protocol, it ~~may optionally~~ must indicate this by transmitting Modified TS2 Ordered Set with Modified TS Usage of 000b or 001b. **01b, 10b, 11b** Reserved

B53 Loopback.Entry

In Section 4.2.6.10.1, make the following changes:

4.2.6.10.1 Loopback.Entry

…

- Loopback Master requirements:
  - If Loopback.Entry was entered from Configuration.Linkwidth.Start, determine the highest common data rate of the data rates supported by the master and the data rates received in two consecutive TS1 or TS2 Ordered Sets on any active Lane at the time the transition to Loopback.Entry occurred. If the current data rate is not the highest common data rate:
    - Transmit 16 consecutive TS1 Ordered Sets with the Loopback bit asserted, followed by an EIOSQ, and then transition to Electrical Idle for 1 ms. During the period of Electrical Idle, change the data rate to the highest common data rate.

- The Loopback Master may be directed, in an implementation specific manner, to perform a 32.0 GT/s equalization procedure on one active Lane, to be referred to as the 'Lane under test', before entering Loopback.Entry. If the highest common data rate is 32.0 GT/s, the equalization_done_32GT_data_rate variable is 0b, and the equalization procedure is to be executed, the 16 consecutive TS1 Ordered Sets transmitted on the Lane under test prior to the data rate change to the highest common data rate must have the bits listed below as follows:
  - The Enhanced Link Behavior Control bits must be set to 01b.
  - The Transmit Modified Compliance Pattern in Loopback bit must be set to 1b if the Loopback Slave is required to transmit the Modified Compliance Pattern on the Lanes that are not under test.

IMPLEMENTATION NOTE:
Lane Under Test Usage Expectations
The method whereby one active Lane is defined as the 'Lane under test' and is affected by the NEXT/FEXT aggressor Lanes (see Section 8.5.1.1) so that measurements are performed on the Lane under test (after a speed change and completion of an equalization procedure at a rate of 32.0 GT/s or above) is defined for system configurations where a test apparatus, such as (but not limited to) a BERT, acts as the Loopback Master. In such a system configuration, the expectation of this test method is that the Loopback Master is able to provide the necessary stimulus for the state traversals and protocol negotiations required to establish and exercise the 'Lane under test' without any specific guidance from this specification.

- If the highest common data rate is 5.0 GT/s, the slave's transmitter de-emphasis is controlled by setting the Selectable De-emphasis bit of the transmitted TS1 Ordered Sets to the desired value (1b = -3.5 dB, 0b = -6 dB).
- For data rates of 5.0 GT/s and above, the master is permitted to choose its own transmitter settings in an implementation-specific manner, regardless of the settings it transmitted to the slave.
- Note: If Loopback is entered after LinkUp has been set to 1b, it is possible for one Port to enter Loopback from Recovery and the other to enter Loopback from Configuration. The Port that entered from Configuration might attempt to change data rate while the other Port does not. If this occurs, the results are undefined. The test set-up must avoid such conflicting directed clauses.

- Transmit TS1 Ordered Sets with the Loopback bit asserted.
  - If Loopback.Entry was entered from Recovery.Equalization, the EC field of the transmitted TS1 Ordered Sets must be set to 00b.
  - The master is also permitted to assert the Compliance Receive bit of TS1 Ordered Sets transmitted in Loopback.Entry, including those transmitted before a data rate change. If it asserts the Compliance Receive bit, it must not deassert it again while in the Loopback.Entry state. This usage model might be helpful for test and validation purposes when one or both Ports have difficulty obtaining bit lock, Symbol lock, or Block alignment after a data rate change. The ability to set the Compliance Receive bit is implementation-specific.
- ~~Next state is Loopback.Active after 2 ms if the Compliance Receive bit of the transmitted TS1 Ordered Sets is asserted.~~
- Next state is Recovery.Equalization if the data rate was changed to 32.0 GT/s and 16 consecutive TS1 Ordered Sets were sent on any Lane with the Enhanced Link Behavior Control bits set to 01b.
  - The perform_equalization_for_loopback variable is set to 1b.

- Next state is Loopback.Active after 2 ms if the Compliance Receive bit of the transmitted TS1 Ordered Sets is asserted.
- Next state is Loopback.Active if Loopback.Entry was entered from Recovery.Equalization and the Lane under test receives two consecutive TS1 Ordered Sets with the Loopback bit asserted.

B55 Page Request Group Response Message

In Section 14.4.2, make the following changes:

10.4.2 Page Request Group Response Message

…

Receipt of a PRG Response Message that contains a PRG Index that is not currently outstanding at a Function shall result in the UPRGI flag in the PRI Extended Capability being Set, contingent upon the TLP otherwise being error free. Because of ambiguous language in earlier versions of this specification, it is permitted (though discouraged) to handle this case as an Unsupported Request (UR) or Unexpected Completion (UC) ~~and in the issuance of an Unexpected Response (UR)~~ by the Function containing the PRI Extended Capability, but otherwise no other error is permitted to be logged or signaled. ~~With the exception of setting the UPRGI flag, a Function treats receipt of an unexpected PRG Index in exactly the same manner that it treats receipt of a standard PCIe read completion for which there is no outstanding request.~~

B56 Page Request Enable

In Table 10-12, Section 10.5.2.2, make the following changes:

10.5.2.2 Page Request Control Register (Offset 04h)

…

Table 10-12 Page Request Control Register

Bit Location	Description	Attributes
0	**Enable (E)** – This field, when set, indicates that the Page Request Interface is allowed to make page requests. If this field is Clear, the Page Request Interface is not allowed to issue page requests. If both this field and the Stopped field are Clear, then the Page Request Interface will not issue new page requests, but has outstanding page requests that have been transmitted or are queued for transmission. When the Page Request Interface is transitioned from not-Enabled to Enabled, its status flags (Stopped, Response Failure, and Unexpected Page Request Group Index (UPRGI) ~~Unexpected Response~~ flags) are cleared. Enabling a Page Request Interface that has not successfully Stopped has indeterminate results. Default is 0b.	RW

B57 Invalidate Request

In Section 10.3.1, make the following changes:

10.3.1 Invalidate Request

…

The address range specified in an Invalidate Request may span one or more STU 4096-byte pages. Invalidation ranges are required to be naturally aligned and ~~may~~ should not be smaller than STU 4096-byte pages. Upon receiving an Invalidate Request with a range less than STU an ATC may either (1) signal an Unsupported Request (not recommended) or (2) round the range of the request up to a value greater than or equal to the STU.

…

The Global Invalidate bit indicates that the Invalidation Request Message affects all PASID values (see Section 10.3.8). This bit is Reserved unless the Invalidation Request has a PASID TLP Prefix. The bit is ignored by the ATC if Global Invalidate Supported bit is Clear (see Section 10.3.8).

IMPLEMENTATION NOTE

Invalidation Requests and Function Level Reset & Device Power State Transitions

Invalidation requests received while a Function is undergoing Function Level Reset, or is in (or transitioning to) non-D0 device state, may be dropped by the Function. Similarly, invalidation requests already received but pending at the time of receiving an initiate FLR or D-state transition request may be dropped by the Function.

System software can avoid ATS invalidation race conditions on Function Level Reset and Device Power State transitions in a variety of ways. For example:

1. When disabling ATS on a Function, system software quiesces ATS invalidations to the Function (i.e. either responses are received for all invalidation requests issued to the Function, or any pending invalidation requests to the Function have timed out).
2. Software ensures no invalidations are issued to a Function when its ATS capability is disabled.
3. Before initiating the FLR (or Device power state transitions), software disables ATS as described in item 1. above.

10.3.2 Invalidate Completion

B58 L02 ASPM State

In Section 5.4.1.1, make the following changes:

5.4.1.1 L0s ASPM State

…

IMPLEMENTATION NOTE

Potential Issues With Legacy Software When L0s is Not Supported

…

In earlier versions of this specification, device support of L0s was mandatory, and software could legitimately assume that all devices support L0s. Newer hardware components that do not support L0s may encounter issues with such “legacy software”. Such software might not even check the ASPM Support field in the Link Capabilities register, might not recognize the subsequently defined values (00b and 10b) for the ASPM Support field, or might not follow the policy of enabling L0s only if components on both sides of the Link each support L0s. Legacy software (either operating system or firmware) that encounters the previously reserved value 00b (No ASPM Support), will most likely refrain from enabling L1, which is intended behavior. Legacy software will also most likely refrain from enabling L0s for that component's Transmitter (also intended behavior), but it is unclear if such software will also refrain from enabling L0s for the component on the other side of the Link. If software enables L0s on one side when the component on the other side does not indicate that it supports L0s, the result is undefined. Situations where the resulting behavior is unacceptable may need to be handled by updating the legacy software, ~~resorting to “blacklists” or similar mechanisms directing~~ establishing a list of configurations for which the legacy software is directed not to enable L0s, or simply not supporting the problematic system configurations.

…

B60 Fmt Field

In Figure 10-8, Section 10.2.2, change the Fmt field to 001b
In Figure 10-9, Section 10.2.2, change the Fmt field to 000b

10.2.2 Translation Requests

…

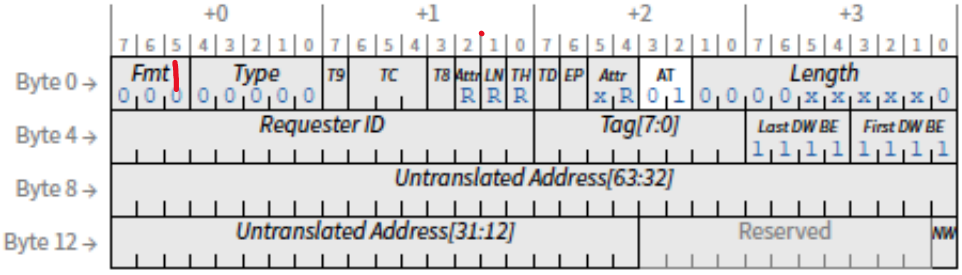

Figure 10-8 64-bit Translation Request Header

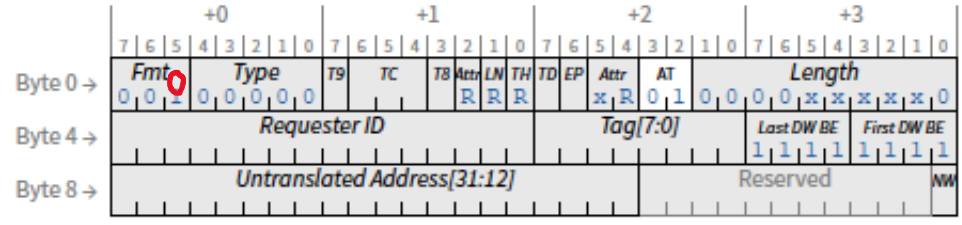

Figure 10-9 32-bit Translation Request Header

In Figure 10-10, Section 10.2.3, change the Fmt field value to 010b

10.2.3 Translation Completion

…

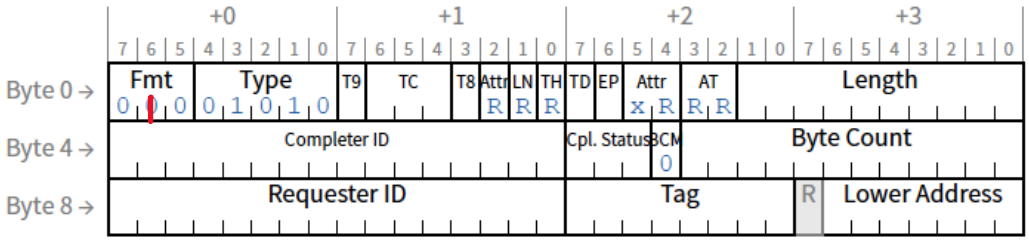

Figure 10-10 Translation Completion with No Data

B63 DMWr

In Section 2.2.5, make the following changes:

2.2.5 First/Last DW Byte Enables Rules

Byte Enables are included with Memory, I/O, and Configuration Requests. This section defines the corresponding rules. Byte Enables, when present in the Request header, are located in byte 7 of the header (see Figure 2-13). For Memory Read Requests and DMWr Requests that have the TH bit Set, the Byte Enable fields are repurposed to carry the ST[7:0] field (refer to Section 2.2.7.1 for details), and values for the Byte Enables are implied as defined below. The TH bit must only be Set in Memory Read Requests and DMWr Requests when it is acceptable to complete those Requests as if all bytes for the requested data were enabled.

- For Memory Read Requests and DMWr Requests that have the TH bit Set, the following values are implied for the Byte Enables. See Section 2.2.7 for additional requirements.
  - If the Length field for this Request indicates a length of 1 DW, then the value for the First DW Byte Enables is implied to be 1111b and the value for the Last DW Byte Enables is implied to be 0000b
  - If the Length field for this Request indicates a length of greater than 1 DW, then the value for the First DW Byte Enables and the Last DW Byte Enables is implied to be 1111b.

…

In Section 2.2.7, make the following changes:

2.2.7 Memory, I/O, and Configuration Request Rules

The following rule applies to all Memory, I/O, and Configuration Requests. Additional rules specific to each type of Request follow.

- All Memory, I/O, and Configuration Requests include the following fields in addition to the common header fields:
  - Requester ID[15:0] and Tag[9:0], forming the Transaction ID.
  - Last DW BE[3:0] and First DW BE[3:0].

- For Memory Read Requests, DMWr Requests, and AtomicOp Requests with the TH bit Set, the byte location for the Last DW BE[3:0] and First DW BE [3:0] fields in the header are repurposed to carry ST[7:0] field.
- For Memory Read Requests and DMWr Requests with the TH bit Clear, see Section 2.2.5 for First/Last DW Byte Enable Rules.
- For AtomicOp Requests and DMWr Requests with TH bit Set, the values for the DW BE fields are implied to be Reserved. For AtomicOp Requests with TH bit Clear, the DW BE fields are Reserved.

…

B65 Data Return for Read Requests

In Section 2.3.1.1, make the following changes:

2.3.1.1 Data Return for Read Requests

…

- If all the Memory Read Completions for a single Read Request have a Successful Completion Status, the sum of their payloads must equal the size requested. See Section 10.2.4 for an exception for Memory Reads that are ATS Translation Requests.

B68 $T_{perstslew}$

In Section 6.6.1, make the following changes:

6.6.1 Conventional Reset

…

In all cases where power and PERST# are supplied, the following parameters must be defined:

- T_{pvperl} - PERST# must remain asserted ~~active~~ at least this long after power becomes valid
- T_{perst} - When asserted, PERST# must remain asserted at least this long
- T_{fail} - When power becomes invalid, PERST# must be asserted within this time
- $T_{perstslew}$ – The slew rate of PERST# transition to deasserted through its logic input switching range. Tperstslew is specified as a minimum of 50 mV/ns unless the form factor specification states otherwise.

Additional parameters may be specified.

In all cases where a reference clock is supplied, the following parameter must be defined:

- $T_{perst\text{-}clk}$ - PERST# must remain asserted ~~active~~ at least this long after any supplied reference clock is stable

Additional parameters may be specified.

B69 Data Object Exchange (DOE ECN)

In the Data Object ECN, make the following changes:

6.xx.1 Data Objects

…

If the Length is greater than expected for a specific data object, then the portion of the data object up to the expected length must be processed normally and the remainder of the data object must be silently discarded.

6.xx.1.1 DOE Discovery Data Object Protocol

The DOE Discovery data object protocol must be implemented. It consists of the request and response data objects, 3 DW in total length each, with the 3rd DW of the data object content as defined in Table 7-x3 and Table 7-4x respectively. …

B70 Completion Handling Rules

In Section 2.3.2, make the following changes:

2.3.2 Completion Handling Rules

- When a device receives a Completion that does not match the Transaction ID for any of the outstanding Requests issued by that device, the Completion is called an “Unexpected Completion”.
- If a received Completion matches the Transaction ID of an outstanding Request, but in some other way does not match the corresponding Request (e.g., a problem with Attributes, Traffic Class, Byte Count, Lower Address, etc.), it is strongly recommended for the Receiver to handle the Completion as a Malformed TLP.
    - The ~~Completer~~ Requester must not check the IDO Attribute (Attribute Bit 2) in the Completion, since the ~~Requester~~ Completer is not required to copy the value of IDO from the Request into the Completion for that request as stated in Section 2.2.6.4 and Section 2.2.9 .
    - However, if the Completion is otherwise properly formed, it is permitted28 for the Receiver to handle the Completion as an Unexpected Completion.

…

B72 SR-IOV and DMWr

In Table 9-19, Section 9.3.5.9, make the following changes:

9.3.5.9 Device Capabilities 2 Register Changes (Offset 24h)

PF and VF functionality is defined in Section 7.5.3.15 except as noted in Table 9-19 .

Table 9 19: Device Capabilities 2 Register Changes

Bit Location	PF and VF Register Differences From Base	PF Attributes	VF Attributes
…	…	…	…

26	**Emergency Power Reduction Initialization Required** VF value must be identical to PF value.	Base	Base
28	**DMWr Completer Supported**	Base	Base
30:29	**DMWr Lengths Supported**	Base	Base

B73 LCRC Error Reporting

In Section 3.6.3.1, make the following changes:

- If the TLP Sequence Number is not equal to the expected value, stored in NEXT_RCV_SEQ:
  - Discard the TLP and free any storage allocated for the TLP
  - If the TLP Sequence Number satisfies the following equation:

    (NEXT_RCV_SEQ - TLP Sequence Number) mod 4096 <= 2048

    the TLP is a duplicate, and an Ack DLLP is scheduled for transmission (per transmission priority rules)
  - Otherwise, the TLP is out of sequence (indicating one or more lost TLPs):
    - if the NAK_SCHEDULED flag is ~~c~~Clear,
      - schedule a Nak DLLP for transmission immediately
      - set the NAK_SCHEDULED flag
      - This is a Bad TLP error and is a reported error associated with the Port (see Section 6.2).

    ~~This is a Bad TLP error and is a reported error associated with the Port (see Section 6.2).~~

      - if the NAK_SCHEDULED flag is Set, the Port is permitted to, but is not recommended to, report a Bad TLP error associated with the Port (see Section 6.2) and this permission is shown in Figure 3-17.

    ~~Regardless of the state of the NAK_SCHEDULED flag, it is permitted for this to be a reported error associated with the Port (see Section 6.2), and this permitted behavior is illustrated in Figure 3-17 . However, in order to prevent error pollution it is recommended that the Port only report such an error when the NAK_SCHEDULED flag is clear.~~

- If the TLP Sequence Number is equal to the expected value stored in NEXT_RCV_SEQ: