

# OLED

## 注意事项：

用的驱动芯片是SSD1306

D/C#决定写入的是写到GDDRAM还是COMMAND寄存器

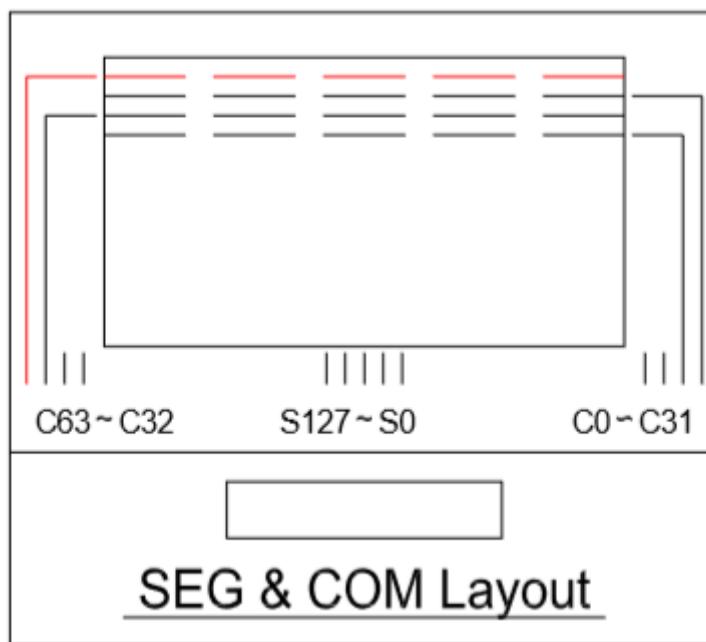
中景园版本的I2C从地址是0x78

$b_7 \ b_6 \ b_5 \ b_4 \ b_3 \ b_2 \ b_1 \ b_0$   
0 1 1 1 1 0 SA0 R/W#

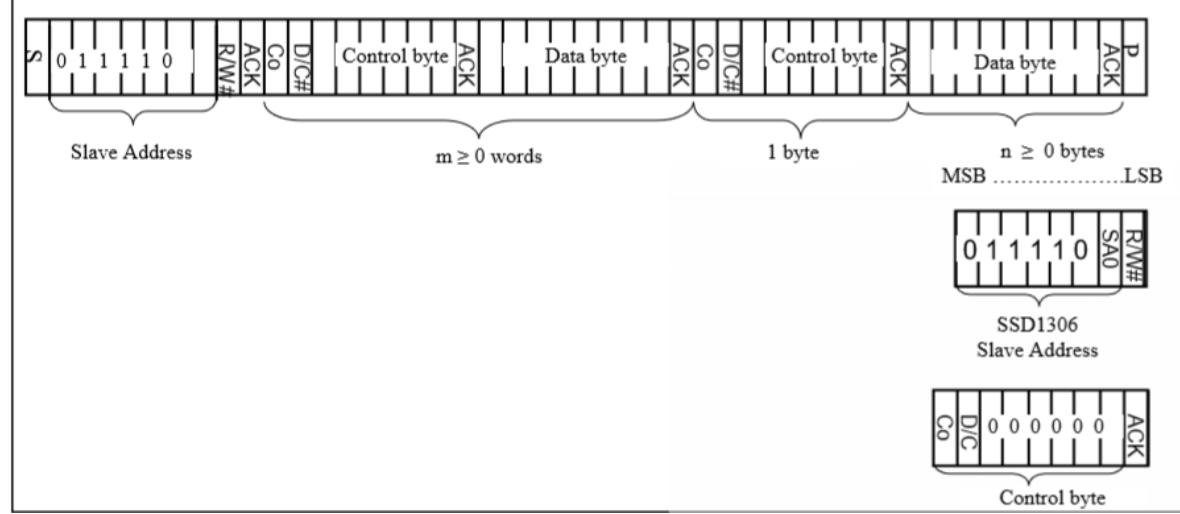
且他的COM到ROW的映射是交叉的，不是顺序叠放。且0在下63在上。所以上下是反的。S0在右，所以左右也是反的。

这样要注意在

- 设置Segment重映射的时候0XA1进行翻转左右 sge0是映射到column0还是127
- 设置扫描COM方向的时候设置0XC8倒序扫描COM即 COM[N-1] to COM0
- 设置DA的时候要失能左右重映射且失能顺序COM配置 即选择0x12 (A5=0,A4=1)



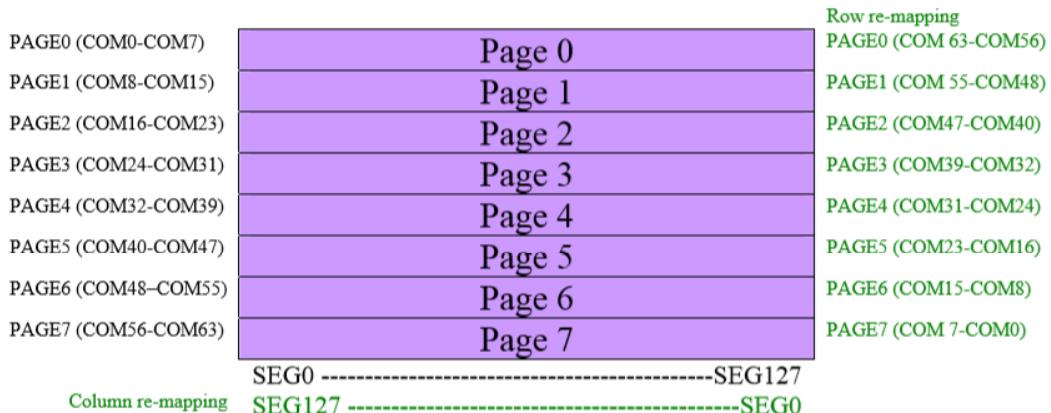
## 格式帧



这里的data byte是指接下来的数据信息，这里的control byte 不是command byte 的意思。是指I2C没有 D/C# 通过这个byte来控制接下来了的是那个byte 是什么。data byte 可以是command 也可以是 data。

<file:///D:/Data/学习/12.RobotCon/电控/成果/oled12864驱动/0.96OLED显示屏资料/中景园电子0.96OLED显示屏资料/02-显示屏数据手册/0.96插接-短排.pdf>

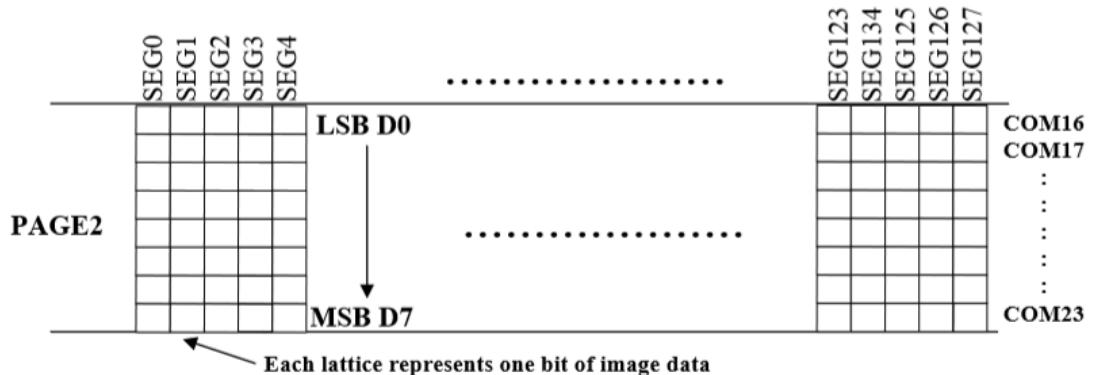
<file:///D:/Data/学习/12.RobotCon/电控/成果/oled12864驱动/0.96OLED显示屏资料/中景园电子0.96OLED显示屏资料/02-显示屏数据手册/经典款0.96OLED驱动芯片手册SSD1306规格书.pdf>



页的表示。没页128\*8 一共8大行(页)

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 8-14.

Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)



每改变GDDRAM1个字节会使得对应页的1列8行全部改变。

使用

Pin	Symbol	
1	N.C. (GND)	
2	C2P	
3	C2N	
4	C1P	
5	C1N	
6	VBAT	
7	N.C.	
8	VSS	
9	VDD	P
10	BS0	
11	BS1	
12	NC	
13	CS#	
14	RES#	
15	D/C#	
16	NC	
17	NC	
18	D0	
19	D1	
20	D2	
21	NC	
22	NC	
23	NC	
24	NC	
25	NC	
26	IREF	
27	VCOMH	
28	VCC	
29	VLSS	
30	N.C. (GND)	

POWER

9	VDD	P	<b>Power Supply for Logic</b> This is a voltage supply pin. It must be connected to external source.
8	VSS	P	<b>Ground of Logic Circuit</b> This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
28	VCC	P	<b>Power Supply for OEL Panel</b> This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V <sub>SS</sub> when the converter is used. It must be connected to external source when the converter is not used.
29	VLSS	P	<b>Ground of Analog Circuit</b> This is an analog ground pin. It should be connected to V <sub>SS</sub> externally.

Driver

26	IREF	I	<b>Current Reference for Brightness Adjustment</b> This pin is segment current reference pin. A resistor should be connected between this pin and V <sub>SS</sub> . Set the current at 12.5 $\mu$ A maximum.
27	VCOMH	O	<b>Voltage Output High Level for COM Signal</b> This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V <sub>SS</sub> .

DC/DC converter

6	VBAT	P	<b>Power Supply for DC/DC Converter Circuit</b> This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to V <sub>DD</sub> when the converter is not used.
4 / 5 2 / 3	C1P / C1N C2P / C2N	I	<b>Positive Terminal of the Flying Inverting Capacitor</b> <b>Negative Terminal of the Flying Boost Capacitor</b> The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.

## Interface

10 11	BS0 BS1	I	<b>Communicating Protocol Select</b> These pins are MCU interface selection input. See the following table:																
			<table border="1"> <thead> <tr> <th></th> <th>BS0</th> <th>BS1</th> <th></th> </tr> </thead> <tbody> <tr> <td>I<sup>2</sup>C</td> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>3-wire SPI</td> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>4-wire SPI</td> <td>0</td> <td>0</td> <td></td> </tr> </tbody> </table>		BS0	BS1		I <sup>2</sup> C	0	1		3-wire SPI	1	0		4-wire SPI	0	0	
	BS0	BS1																	
I <sup>2</sup> C	0	1																	
3-wire SPI	1	0																	
4-wire SPI	0	0																	
14	RES#	I	<b>Power Reset for Controller and Driver</b> This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.																
13	CS#	I	<b>Chip Select</b> This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.																
15	D/C#	I	<b>Data/Command Control</b> This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I <sup>2</sup> C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.																
18~20	D0~D2		These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D2 should be either tied LOW or tied together with D1 as the serial data input: SDIN and D0 will be the serial clock input: SCLK. When I <sup>2</sup> C mode is selected, D2, D1 should be tied together and serve as SDA <sub>out</sub> , SDA <sub>in</sub> in application and D0 is the serial clock input, SCL.																
7,12,16,17, 21~25	N.C.	-	<b>Reserved Pin</b> The N.C. pin between function pins are reserved for compatible and flexible design.																
1, 30	N.C. (GND)	-	<b>Reserved Pin (Supporting Pin)</b> The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.																

亮度影响寿命

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V <sub>DD</sub>	-0.3	4	V	1, 2
Supply Voltage for Display	V <sub>CC</sub>	0	16.5	V	1, 2
Supply Voltage for DC/DC	V <sub>BAT</sub>	-0.3	4.5	V	1, 2
Operating Temperature	T <sub>OP</sub>	-40	85	°C	
Storage Temperature	T <sub>STG</sub>	-40	85	°C	3
Life Time (120 cd/m <sup>2</sup> )		10,000	-	hour	4
Life Time (80 cd/m <sup>2</sup> )		30,000	-	hour	4
Life Time (60 cd/m <sup>2</sup> )		50,000	-	hour	4

可视角度为所有

Viewing Angle			-	Free	-	degree
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## 直流电气特性

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V <sub>DD</sub>	-0.3	4	V	1, 2
Supply Voltage for Display	V <sub>CC</sub>	0	16.5	V	1, 2
Supply Voltage for DC/DC	V <sub>BAT</sub>	-0.3	4.5	V	1, 2
Operating Temperature	T <sub>OP</sub>	-40	85	°C	
Storage Temperature	T <sub>STG</sub>	-40	85	°C	3

<b>Characteristics</b>	<b>Symbol</b>	<b>Conditions</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
Supply Voltage for Logic	$V_{DD}$		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	$V_{CC}$	Note 5 (Internal DC/DC Disable)	8.5	9.0	9.5	V
<i>Supply Voltage for DC/DC</i>	$V_{BAT}$	<i>Internal DC/DC Enable</i>	3.5	-	4.2	V
<i>Supply Voltage for Display (Generated by Internal DC/DC)</i>	$V_{CC}$	<i>Note 6 (Internal DC/DC Enable)</i>	7.0	-	7.5	V
High Level Input	$V_{IH}$	$I_{OUT} = 100\mu A, 3.3MHz$	$0.8 \times V_{DD}$	-	$V_{DD}$	V
Low Level Input	$V_{IL}$	$I_{OUT} = 100\mu A, 3.3MHz$	0	-	$0.2 \times V_{DD}$	V
High Level Output	$V_{OH}$	$I_{OUT} = 100\mu A, 3.3MHz$	$0.9 \times V_{DD}$	-	$V_{DD}$	V
Low Level Output	$V_{OL}$	$I_{OUT} = 100\mu A, 3.3MHz$	0	-	$0.1 \times V_{DD}$	V
Operating Current for $V_{DD}$	$I_{DD}$		-	160	220	$\mu A$
Operating Current for $V_{CC}$ ( $V_{CC}$ Supplied Externally)	$I_{CC}$	Note 7	-	9	15	mA
<i>Operating Current for <math>V_{BAT}</math> (<math>V_{CC}</math> Generated by Internal DC/DC)</i>	$I_{BAT}$	<i>Note 8</i>	-	25.0	32.0	mA
Sleep Mode Current for $V_{DD}$	$I_{DD, SLEEP}$		-	-	10	$\mu A$
Sleep Mode Current for $V_{CC}$	$I_{CC, SLEEP}$		-	-	10	$\mu A$

时序和交流特性

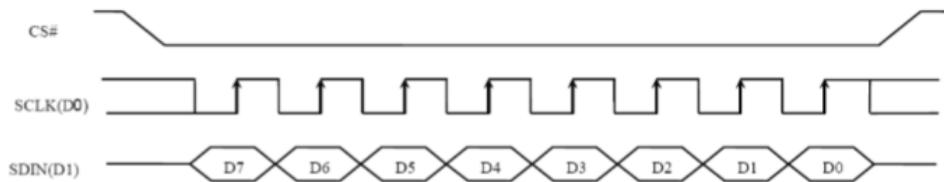
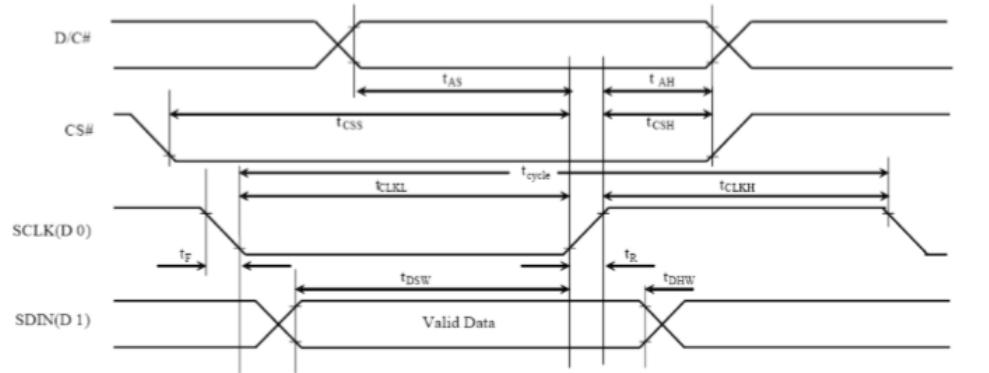
4线SPI

### 3.3 AC Characteristics

#### 3.3.1.1 Serial Interface Timing Characteristics: (4-wire SPI)

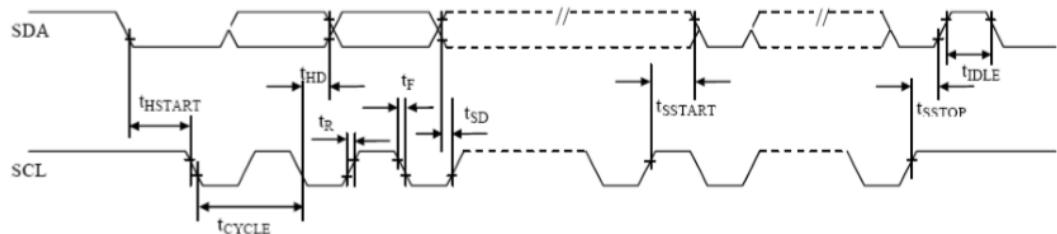
( $V_{DD} - V_{SS} = 1.65V\sim3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	100	-	-	ns
$t_{AS}$	Address Setup Time	15	-	-	ns
$t_{AH}$	Address Hold Time	15	-	-	ns
$t_{CSS}$	Chip Select Setup Time	20	-	-	ns
$t_{CSH}$	Chip Select Hold Time	20	-	-	ns
$t_{DSW}$	Write Data Setup Time	15	-	-	ns
$t_{DHW}$	Write Data Hold Time	25	-	-	ns
$t_{CLKL}$	Clock Low Time	30	-	-	ns
$t_{CLKH}$	Clock High Time	30	-	-	ns
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns



极性为低，相位第1沿(第一沿采样，第二沿输出)

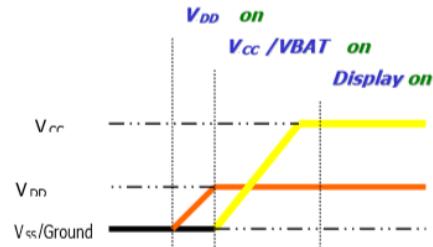
I2C



为了保护OLED面板寿命上下电要有顺序

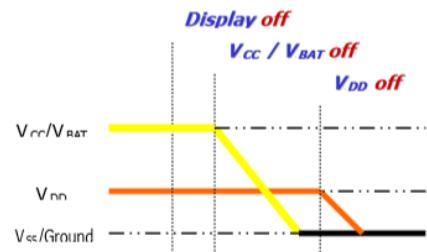
#### 4.2.1 Power up Sequence:

1. Power up  $V_{DD}$  /  $V_{BAT}$
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up  $V_{CC}$
6. Delay 100ms  
(When  $V_{CC}$  is stable)
7. Send Display on command



#### 4.2.2 Power down Sequence:

1. Send Display off command
2. Power down  $V_{CC}$  /  $V_{BAT}$
3. Delay 100ms  
(When  $V_{CC}$  /  $V_{BAT}$  is reach 0 and panel is completely discharged)
4. Power down  $V_{DD}$



$V_{CC}$ 是给面板供电的， $V_{DD}$ 是给芯片电路供电的。而且要后开启和先关闭 $V_{CC}$ 。

复位电路：

复位输入低时，初始化顺序如下：

1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

## 命令表

基础命令

注意D/C#的01，其中放在一个小格子中如第一个81下有A[7:0]表示先发1个81表示要设置什么，再紧跟1个A[7:0]表示设置的大小

**Table 9-1: Command Table**

(D/C#=0, R/W#(WR#)=0, E(RD#=1) unless specific setting is stated)

1. Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	81	1	0	0	0	0	0	0	1	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh )
0	A4/A5	1	0	1	0	0	1	0	X <sub>0</sub>	Entire Display ON	A4h, X <sub>0</sub> =0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X <sub>0</sub> =1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X <sub>0</sub>	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X <sub>0</sub>	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

81：设置对比度

A4/A5 设置全屏模式，是否忽略RAM内容

A6/A7 设置是否翻转显示颜色，RAM中的01表示意思相反

AE/AF:睡眠或显示模式

### 滚动命令表

0	26/27	0	0	1	0	0	1	1	X <sub>0</sub>	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte B[2:0] : Define start page address
0	A[7:0]	0	0	0	0	0	0	0	B <sub>2</sub>		000b - PAGE0 011b - PAGE3 110b - PAGE6
0	B[2:0]	*	*	*	*	*	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		001b - PAGE1 100b - PAGE4 111b - PAGE7
0	C[2:0]	*	*	*	*	*	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		010b - PAGE2 101b - PAGE5
0	D[2:0]	*	*	*	*	*	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		C[2:0] : Set time interval between each scroll step in terms of frame frequency
											000b - 5 frames 100b - 3 frames
											001b - 64 frames 101b - 4 frames
											010b - 128 frames 110b - 25 frame
											011b - 256 frames 111b - 2 frame
											D[2:0] : Define end page address
											000b - PAGE0 011b - PAGE3 110b - PAGE6
											001b - PAGE1 100b - PAGE4 111b - PAGE7
											010b - PAGE2 101b - PAGE5
											The value of D[2:0] must be larger or equal to B[2:0]

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description									
0	29/2A	0	0	1	0	1	0	X <sub>1</sub>	X <sub>0</sub>	Continuous	29h, X <sub>1</sub> X <sub>0</sub> =01b : Vertical and Right Horizontal Scroll									
0	A[2:0]	0	0	0	0	0	0		0	Vertical and	2Ah, X <sub>1</sub> X <sub>0</sub> =10b : Vertical and Left Horizontal Scroll									
0	B[2:0]	*	*	*	*	*	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	Horizontal Scroll	(Horizontal scroll by 1 column)									
0	C[2:0]	*	*	*	*	*	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	Setup	A[7:0] : Dummy byte									
0	D[2:0]	*	*	*	*	*	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		B[2:0] : Define start page address									
0	E[5:0]	*	*	E <sub>5</sub>	E <sub>4</sub>	E <sub>3</sub>	E <sub>2</sub>	E <sub>1</sub>	E <sub>0</sub>		<table border="1"> <tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr> <tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr> <tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr> </table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																		
001b – PAGE1	100b – PAGE4	111b – PAGE7																		
010b – PAGE2	101b – PAGE5																			
										C[2:0] : Set time interval between each scroll step in terms of frame frequency	<table border="1"> <tr><td>000b – 5 frames</td><td>100b – 3 frames</td></tr> <tr><td>001b – 64 frames</td><td>101b – 4 frames</td></tr> <tr><td>010b – 128 frames</td><td>110b – 25 frame</td></tr> <tr><td>011b – 256 frames</td><td>111b – 2 frame</td></tr> </table>	000b – 5 frames	100b – 3 frames	001b – 64 frames	101b – 4 frames	010b – 128 frames	110b – 25 frame	011b – 256 frames	111b – 2 frame	
000b – 5 frames	100b – 3 frames																			
001b – 64 frames	101b – 4 frames																			
010b – 128 frames	110b – 25 frame																			
011b – 256 frames	111b – 2 frame																			
										D[2:0] : Define end page address	<table border="1"> <tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr> <tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr> <tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr> </table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																		
001b – PAGE1	100b – PAGE4	111b – PAGE7																		
010b – PAGE2	101b – PAGE5																			
										The value of D[2:0] must be larger or equal to B[2:0]										
										E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0] =3Fh refer to offset =63 rows										
										<b>Note</b> <sup>(1)</sup> No continuous vertical scrolling is available.										
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah.  <b>Note</b> <sup>(1)</sup> After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.									
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:  Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh.  For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.									

0	A3 A[5:0] B[6:0]	1 * B <sub>6</sub>	0 * B <sub>5</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). [RESET = 0]  B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64]  <b>Note</b> (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line (X <sub>5</sub> X <sub>4</sub> X <sub>3</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub> of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls
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26/27: 控制左移还是右移

A: 无用

B: 定义起始页地址

C: 每次滚动的间隔帧数

地址设置命令表

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0	21 A[6:0] B[6:0]	0 * *	0 A <sub>6</sub> B <sub>6</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d)  B[6:0]: Column end address, range : 0-127d, (RESET =127d)
0	22 A[2:0] B[2:0]	0 * *	0 * *	1 *	0 *	0 *	0 A <sub>2</sub>	1 A <sub>1</sub>	0 A <sub>0</sub>	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)
0	B0~B7	1	0	1	1	0	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].

硬件设置表

0	40~7F	0	1	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Display Start Line	Set display RAM display start line register from 0~63 using X <sub>5</sub> X <sub>3</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub> . Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X <sub>0</sub>	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0	A8 A[5:0]	1 *	0 *	1 A <sub>5</sub>	0 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET=111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X <sub>3</sub>	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N-1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0	D3 A[5:0]	1 *	1 *	0 A <sub>5</sub>	1 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0	DA A[5:4]	1 0	1 0	0 A <sub>5</sub>	1 A <sub>4</sub>	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration  A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

## 时序设置命令

5. Timing & Driving Scheme Setting Command Table																							
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description												
0	D5 A[7:0]	1 A <sub>7</sub>	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	0 A <sub>3</sub>	1 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1)  A[7:4] : Set the Oscillator Frequency, F <sub>OSC</sub> . Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.												
0	D9 A[7:0]	1 A <sub>7</sub>	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)  A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h )												
0	DB A[6:4]	1 0	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	1 0	0 0	1 0	1 0	Set V <sub>COMH</sub> Deselect Level	<table border="1"> <tr> <th>A[6:4]</th> <th>Hex code</th> <th>V<sub>COMH</sub> deselect level</th> </tr> <tr> <td>000b</td> <td>00h</td> <td>~ 0.65 x V<sub>CC</sub></td> </tr> <tr> <td>010b</td> <td>20h</td> <td>~ 0.77 x V<sub>CC</sub> (RESET)</td> </tr> <tr> <td>011b</td> <td>30h</td> <td>~ 0.83 x V<sub>CC</sub></td> </tr> </table>	A[6:4]	Hex code	V <sub>COMH</sub> deselect level	000b	00h	~ 0.65 x V <sub>CC</sub>	010b	20h	~ 0.77 x V <sub>CC</sub> (RESET)	011b	30h	~ 0.83 x V <sub>CC</sub>
A[6:4]	Hex code	V <sub>COMH</sub> deselect level																					
000b	00h	~ 0.65 x V <sub>CC</sub>																					
010b	20h	~ 0.77 x V <sub>CC</sub> (RESET)																					
011b	30h	~ 0.83 x V <sub>CC</sub>																					
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation												

OLED有三种寻址模式page addressing mode, horizontal addressing mode and vertical addressing mode

Page addressing mode :

在页面寻址模式下，在读/写显示RAM后，列地址指针自动增加1。如果列地址指针到达列结束地址，则列地址指针将重置为列开始地址，页地址指针不会更改。为了访问下一页RAM内容，用户必须设置新的页和列地址。页寻址模式的页和列地址点移动顺序如图10-1所示

**Figure 10-1 : Address Pointer Movement of Page addressing mode**

	COL 0	COL 1	.....	COL 126	COL 127
PAGE0					→
PAGE1					→
:	:	:	:	:	:
PAGE6					→
PAGE7					→

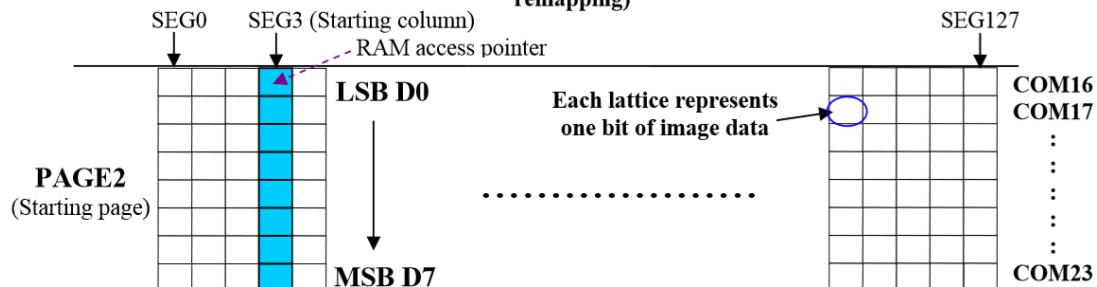
正常读写和页面寻址模式下需要设置以下步骤

In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to B7h.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the upper start column address of pointer by command 10h~1Fh.

For example, if the page address is set to B2h, lower column address is 03h and upper column address is 00h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 10-2. The input data byte will be written into RAM position of column 3.

**Figure 10-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)**



Horizontal addressing mode ( $A[1:0]=00b$ ) :

In horizontal addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 10-3. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-3.)

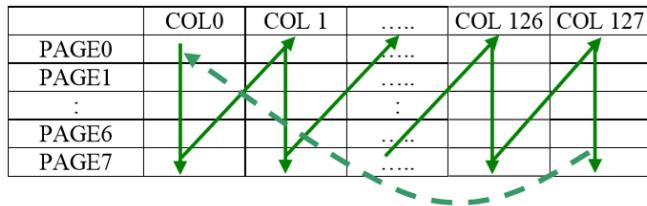
**Figure 10-3 : Address Pointer Movement of Horizontal addressing mode**

	COL 0	COL 1	.....	COL 126	COL 127
PAGE0					→
PAGE1	←				→
:	←	↓	↓	↓	↓
PAGE6	←				→
PAGE7	←				→

Vertical addressing mode: ( $A[1:0]=01b$ ) :

In vertical addressing mode, after the display RAM is read/written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 10-4. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-4.)

**Figure 10-4 : Address Pointer Movement of Vertical addressing mode**



In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

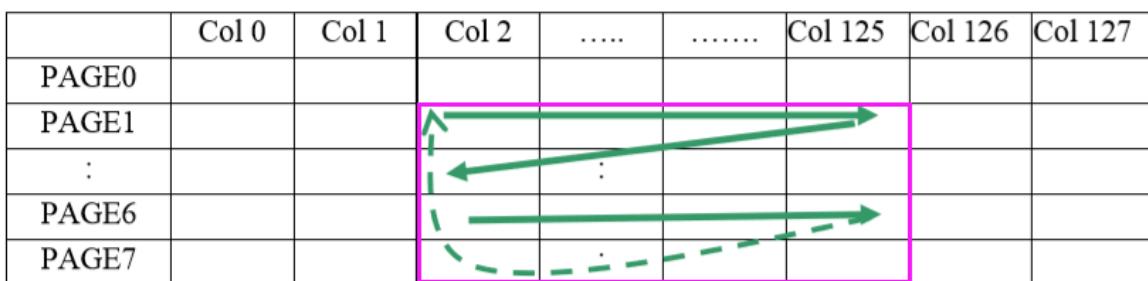
- Set the column start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

**设置列地址命令21：**此三字节命令指定显示数据RAM的列起始地址和结束地址。此命令还将列地址指针设置为列起始地址。此指针用于定义图形显示数据RAM中的当前读/写列地址。如果命令20h启用了水平地址增量模式，则在完成一列数据的读/写后，它将自动递增到下一列地址。每当列地址指针访问完结束列地址时，它将被重置回起始列地址，并且行地址将增加到下一行。

**设置页地址22：**这个三字节命令指定显示数据RAM的页面起始地址和结束地址。此命令还将页面地址指针设置为页面起始地址。该指针用于定义图形显示数据RAM中的当前读/写页面地址。如果通过命令20h启用垂直地址递增模式，则在完成读/写一页数据后，其自动递增到下一页地址。每当页地址指针完成对结束页地址的访问时，它被重置回起始页地址。

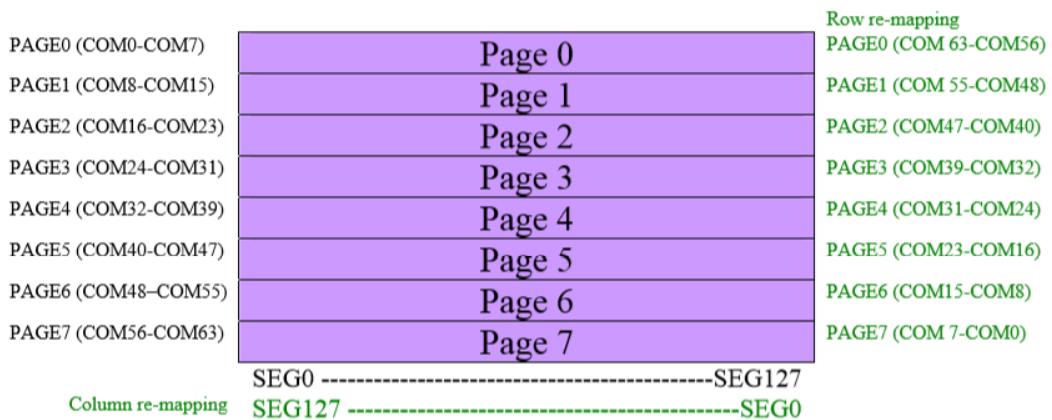
下图显示了通过示例的列和页地址指针移动的方式：列起始地址设置为2，列结束地址设置为125，页起始地址设置为1，页结束地址设置为6；水平地址增量模式通过命令20h启用。在这种情况下，图形显示数据RAM列可访问范围是从第2列到125列，并且仅从第1页到第6页。此外，列地址指针设置为2，页面地址指针设置为1。完成一个像素的数据读/写后，列地址自动增加1，以访问下一个RAM位置进行下一次读/写操作(图10-5中的实线)。每当列地址指针完成对结束列125的访问时，它被复位回列2，并且页地址自动增加1(图10-5中的虚线)。当访问结束页6和结束列125 RAM位置时，页地址重置回1，列地址重置回2(图10-5中的虚线)。图形

**Figure 10-5 : Example of Column and Row Address Pointer Movement**



设置显示起始行40-7f:

此命令通过选择0到63之间的值，设置显示起始线寄存器以确定显示RAM的起始地址。值等于0时，RAM行0映射到COM0。值等于1时，RAM行1映射到COM0，依此类推。亮暗和RAM对应起来。



设置对比度81：越大越亮，电流越大。

设置分割映射：This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 9-1.

Set Multiplex Ratio (A8h): 设置使用路数：即64路的话 整个屏幕都有用，32只有上一半COM可以用

Set COM Output Scan Direction (C0h/C8h)

设置设置偏置 (D3h):

设置startline 改变 COM0和RAM ROWn之间的对应关系

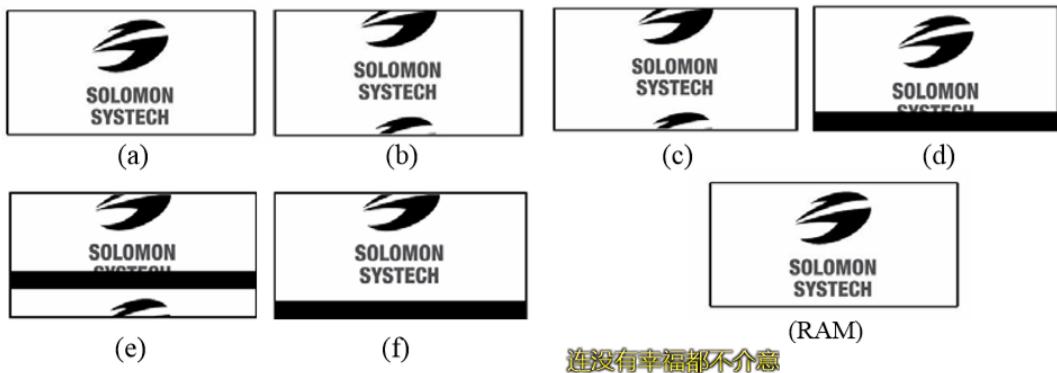
设置了remap后

Example of Set Display Offset and Display Start Line with no Remap

可以认为starline 是RAM和ROW之间的映射，而offset是COM和ROW之间的映射

Hardware pin name	Output						Set MUX ratio(A8h)	
	64 Normal		64 Normal		56 Normal		56 Normal	
	0	8	0	0	8	0	0	8
	0	0	8	0	0	8	0	8
COM0	Row0	RAM0	Row6	RAM8	Row0	RAM0	Row8	RAM8
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM1	Row9	RAM9
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM2	Row10	RAM10
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM3	Row11	RAM11
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM4	Row12	RAM12
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM5	Row13	RAM13
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM6	Row14	RAM14
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM7	Row15	RAM15
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM8	Row16	RAM16
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM9	Row17	RAM17
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM10	Row18	RAM18
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM11	Row19	RAM19

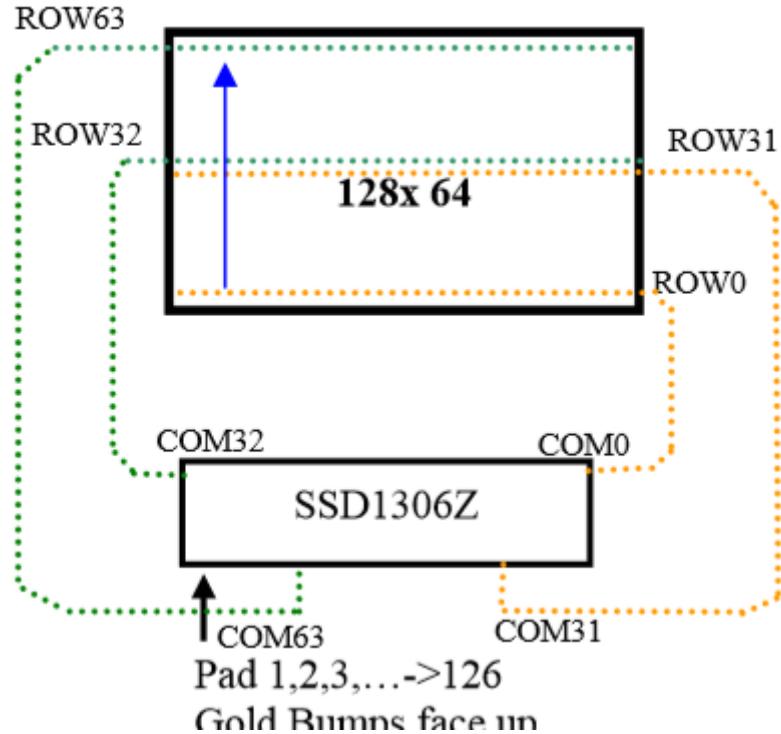
COM43	Row43	RAM43	Row51	RAM51	Row43	RAM43	Row51	RAM51	Row43	RAM51
COM44	Row44	RAM44	Row52	RAM52	Row44	RAM44	Row52	RAM52	Row44	RAM52
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row53	RAM53	Row45	RAM53
COM46	Row46	RAM46	Row54	RAM54	Row46	RAM46	Row54	RAM54	Row46	RAM54
COM47	Row47	RAM47	Row55	RAM55	Row47	RAM47	Row55	RAM55	Row47	RAM55
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM48	-	-	Row48	RAM56
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM49	-	-	Row49	RAM57
COM50	Row50	RAM50	Row58	RAM58	Row50	RAM50	-	-	Row50	RAM58
COM51	Row51	RAM51	Row59	RAM59	Row51	RAM59	-	-	Row51	RAM59
COM52	Row52	RAM52	Row60	RAM60	Row52	RAM60	-	-	Row52	RAM60
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	-	-	Row53	RAM61
COM54	Row54	RAM54	Row62	RAM62	Row54	RAM62	-	-	Row54	RAM62
COM55	Row55	RAM55	Row63	RAM63	Row55	RAM63	-	-	Row55	RAM63
COM56	Row56	RAM56	Row0	RAM0	Row56	RAM0	-	-	-	-
COM57	Row57	RAM57	Row1	RAM1	Row57	RAM1	-	-	-	-
COM58	Row58	RAM58	Row2	RAM2	Row58	RAM2	-	-	-	-
COM59	Row59	RAM59	Row3	RAM3	Row59	RAM3	-	-	-	-
COM60	Row60	RAM60	Row4	RAM4	Row60	RAM4	-	-	-	-
COM61	Row61	RAM61	Row5	RAM5	Row61	RAM5	-	-	-	-
COM62	Row62	RAM62	Row6	RAM6	Row62	RAM6	-	-	-	-
COM63	Row63	RAM63	Row7	RAM7	Row63	RAM7	-	-	-	-
Display examples	(a)	(b)	(c)	(d)	(e)	(f)				



连没有幸福都不介意

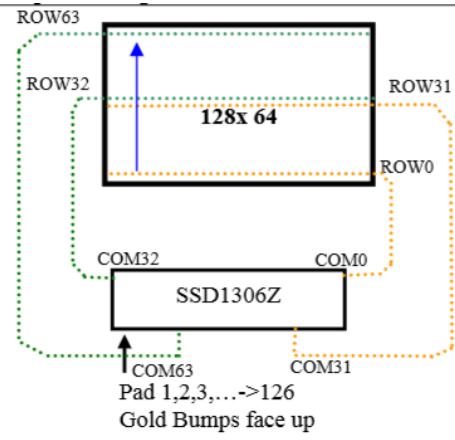
Set COM Pins Hardware Configuration (DAh)

COM和ROW的关系

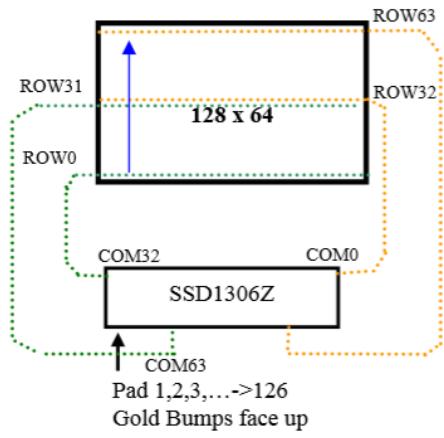


设置了DA A[5]=1发生如1->2的变化

- 1 Sequential COM pin configuration (DAh A[4] =0)  
 COM output Scan direction: from COM0 to COM63 (C0h)  
 Disable COM Left/Right remap (DAh A[5] =0)



- 2 Sequential COM pin configuration (DAh A[4] =0)  
 COM output Scan direction: from COM0 to COM63 (C0h)  
 Enable COM Left/Right remap (DAh A[5] =1)



图形加速命令：

水平滚动设置：

**Figure 10-7 : Horizontal scroll example: Scroll RIGHT by 1 column**

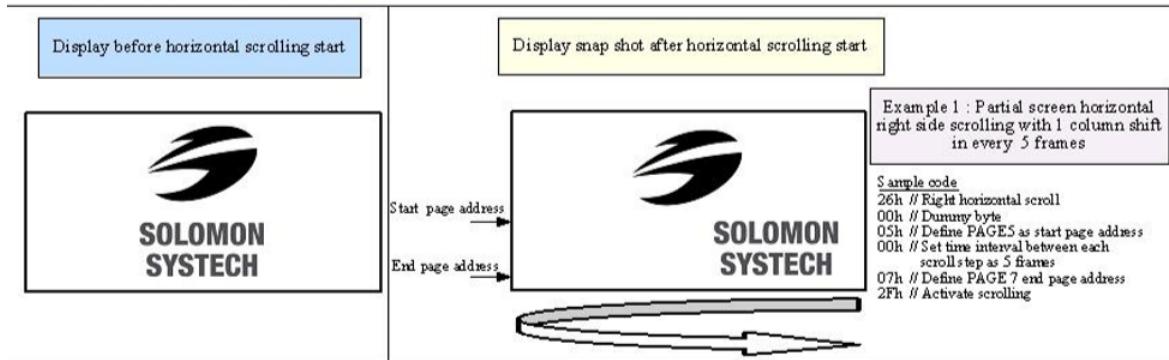
Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17
After one scroll step	SEG127	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16

**Figure 10-8 : Horizontal scroll example: Scroll LEFT by 1 column**

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17
After one scroll step	SEG127	SEG126	SEG125	SEG124	SEG123	SEG122	SEG121	SEG120	SEG119	SEG118	SEG117	SEG116	SEG115	SEG114	SEG113	SEG112	SEG111	SEG110

## 水平滚动设置例程

Figure 10-9 : Horizontal scrolling setup example



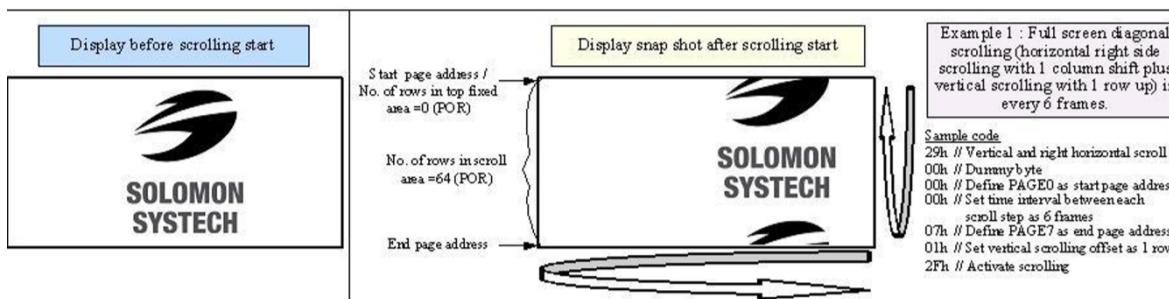
## 垂直和水平翻滚

此命令由6个连续字节组成，用于设置连续垂直滚动参数，并确定滚动起始页、结束页、滚动速度和垂直滚动偏移量。

命令29H/2Ah的字节B[2: 0]、C[2: 0]和D[2: 0]用于设置连续水平滚动。字节E[5: 0]用于设置连续垂直滚动偏移。所有这些字节一起用于设置连续对角线(水平+垂直)滚动。如果垂直滚动偏移字节E[5: 0]设置为零，则仅执行水平滚动(如命令26/27h)。

在发出此命令之前，必须停用卷轴(2EH)。否则，RAM内容可能会损坏。下图(图10-10)显示了使用连续垂直和水平滚动的示例：

Figure 10-10 : Continuous Vertical and Horizontal scrolling setup example



## 禁用滚动：Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

## 激活滚动：Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands :26h/27h/29h/2Ah . The setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

激活滚动后禁止以下操作1.RAM访问(数据写入或读取)2.更改水平滚动设置参数

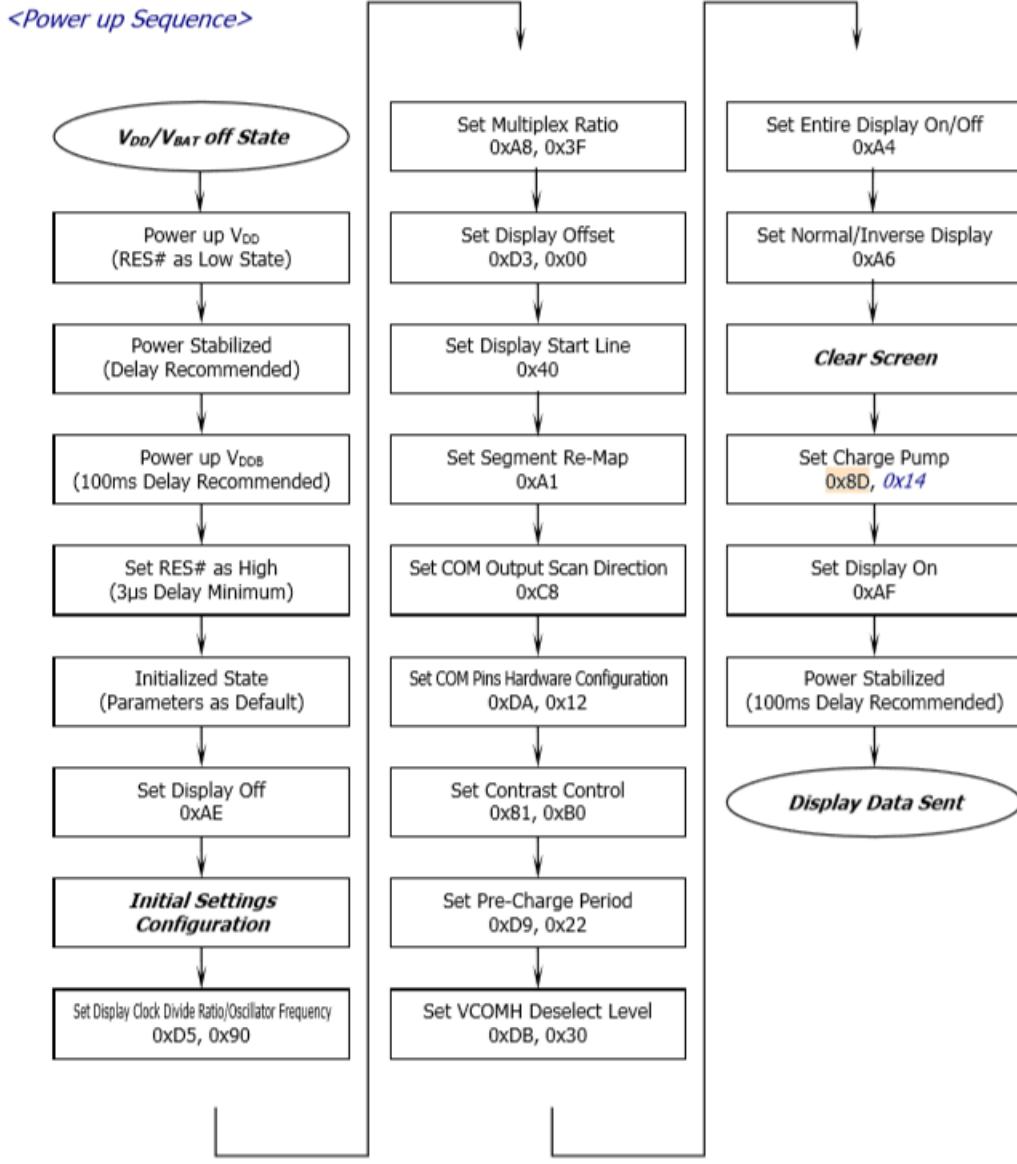
设置垂直滚动区域大小

this command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29/2Ah), the number of rows that in vertical scrolling can be set smaller or equal to the MUX ratio.

<https://blog.csdn.net/teavamc/article/details/73897397>

## 应用实例

### 4.4.2 V<sub>CC</sub> Generated by Internal DC/DC Circuit



引脚 总线接口	Data/Command 接口								控制信号				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW				NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#	
4-wire Spi	Tie LOW				NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#	
I2C	Tie LOW				SDAout	SDAin	SCI	Tie LOW			SAO	RES#	