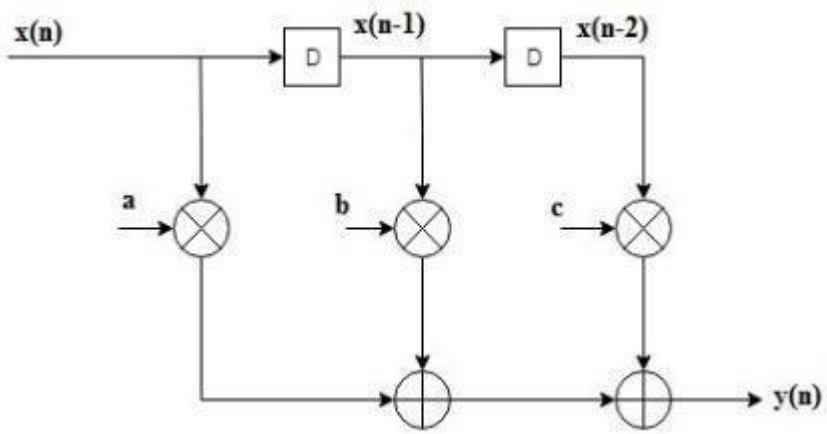
HITEC University, Taxila
Department of Computer Engineering

BS Computer Engineering Program

Course Title:	**EC-341: Digital System Design (3+1)**
Batch / Semester:	Batch 2020 / 6th Semester
Instructor:	Dr Imran Ashraf
Target CLOs:	CLO1, CLO2, CLO3

Complex Engineering Problem

Figure below shows 3-Tap FIR filter design. D in the figure show the pipeline register which add unit delay. The coefficients are a, b and c and you can assume the values to be 1, 0 and 1 respectively.



Part-I [CLO1]:

You increase the pipeline stages by adding more pipeline registers at various places in this circuit. Design a pipelined version of such a filter. Provide a clear diagram and briefly explain your pipelined design.

Part- II [CLO3]:

Analyze the advantage and disadvantage you get from your pipelined design and compare with the given design.

Part-III [CLO2]:

Apply coding styles in Verilog HDL to implement your design.

Deliverable

You need to submit the Report and working Source-code by uploading your deliverables on google classroom.

Following should at least be the contents of the deliverable to clearly communicate your analysis, design and implementation.

1. Report
    1. Not more than 5-page report.
    2. Top level block diagram showing input and output
    3. Detailed design
    4. Analysis of the design
    5. Other details, challenges, important things you encountered

2. Source code
    1. Properly formatted
    2. Properly documented