Hardware Design Guide

S5PV210

RISC Microprocessor

FEB 8, 2010

REV 1.0

SAMSUNG ELECTRONICS

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Revision History

Revision No	Description of Change	Refer to	Author(s)	Date
1.0	- First release version			Feb 08, 2010

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1. Overview

1.1. S5PV210 Pin Information

Definitions

Available Usage(AU)
- G/E/W : GPIO & EINT & Wake up source
- G/E : GPIO & EINT
- G : GPIO
- D : Dedicated signal
- I : Internally connected to MCP and ball out
- I(x) : Internally connected to MCP and No ball out

RET @ Power down

- No_Ret: this signal doesn't have a retention function in power down mode
- Ret_IO : this signal has a retention function in power down mode and released by setting Enable_GPIO bit (others[31])
- Ret_IO (sleep) : this signal has a retention function in only sleep mode and released by setting Enable_GPIO bit (others[31])
- Ret_CF : this signal has a retention function in power down mode and released by setting Enable_CF_IO bit (others[30])
- Ret_MMC : this signal has a retention function in power down mode and released by setting Enable_ MMC_IO bit (others[29])
- Ret_UART : this signal has a retention function in power down mode and released by setting Enable_GPIO_UART_IO bit (others[28]) => Only Uart2, 3
- Ret_Auto : this signal has a retention in power down mode and released automatically after wakeup.

note) Need to more attention when this kinds of signals are used for GPIO,.
Because these signals move to default signal level after wakeup until S/W set to the level.

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
VDD_EXT0	XuRXD[0]	GPA0[0]	GPI	PD	I(L)	UART_0_RXD				G/E	Ret_IO	NC	
	XuTXD[0]	GPA0[1]	GPI	PD	I(L)	UART_0_TXD				G/E	Ret_IO	NC	
	XuCTSn[0]	GPA0[2]	GPI	PD	I(L)	UART_0_CTSn				G/E	Ret_IO	NC	
	XuRTSn[0]	GPA0[3]	GPI	PD	I(L)	UART_0_RTSn				G/E	Ret_IO	NC	
	XuRXD[1]	GPA0[4]	GPI	PD	I(L)	UART_1_RXD				G/E	Ret_IO	NC	
	XuTXD[1]	GPA0[5]	GPI	PD	I(L)	UART_1_TXD				G/E	Ret_IO	NC	
	XuCTSn[1]	GPA0[6]	GPI	PD	I(L)	UART_1_CTSn				G/E	Ret_IO	NC	
	XuRTSn[1]	GPA0[7]	GPI	PD	I(L)	UART_1_RTSn				G/E	Ret_IO	NC	
VDD_EXT1	XuRXD[2]	GPA1[0]	GPI	PD	I(L)	UART_2_RXD		UART_AUDIO_RXD		G/E	Ret_UART	NC	for RP(Low Power Audio)debugging

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XuTXD[2]	GPA1[1]	GPI	PD	I(L)	UART_2_TXD		UART_AUDIO_TXD		G/E	Ret_UART	NC	for RP(Low Power Audio)debugging
	XuRXD[3]	GPA1[2]	GPI	PD	I(L)	UART_3_RXD	UART_2_CTSn			G/E	Ret_UART	NC	
	XuTXD[3]	GPA1[3]	GPI	PD	I(L)	UART_3_TXD	UART_2_RTSn			G/E	Ret_UART	NC	
VDD_EXT0	XspiCLK[0]	GPB[0]	GPI	PD	I(L)	SPI_0_CLK				G/E	Ret_IO	NC	
	XspiCSn[0]	GPB[1]	GPI	PD	I(L)	SPI_0_nSS				G/E	Ret_IO	NC	
	XspiMISO[0]	GPB[2]	GPI	PD	I(L)	SPI_0_MISO				G/E	Ret_IO	NC	
	XspiMOSI[0]	GPB[3]	GPI	PD	I(L)	SPI_0_MOSI				G/E	Ret_IO	NC	
VDD_EXT2	XspiCLK[1]	GPB[4]	GPI	PD	I(L)	SPI_1_CLK				G/E	Ret_IO	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XspiCSn[1]	GPB[5]	GPI	PD	I(L)	SPI_1_nSS				G/E	Ret_IO	NC	
	XspiMISO[1]	GPB[6]	GPI	PD	I(L)	SPI_1_MISO				G/E	Ret_IO	NC	
	XspiMOSI[1]	GPB[7]	GPI	PD	I(L)	SPI_1_MOSI				G/E	Ret_IO	NC	
VDD_AUD	Xi2s1SCLK	GPC0[0]	GPI	PD	I(L)	I2S_1_SCLK	PCM_1_SCLK	AC97BITCLK		G/E	Ret_IO	NC	
	Xi2s1CDCLK	GPC0[1]	GPI	PD	I(L)	I2S_1_CDCLK	PCM_1_EXTCLK	AC97RESETn		G/E	Ret_IO	NC	
	Xi2s1LRCK	GPC0[2]	GPI	PD	I(L)	I2S_1_LRCK	PCM_1_FSYNC	AC97SYNC		G/E	Ret_IO	NC	
	Xi2s1SDI	GPC0[3]	GPI	PD	I(L)	I2S_1_SDI	PCM_1_SIN	AC97SDI		G/E	Ret_IO	NC	
	Xi2s1SDO	GPC0[4]	GPI	PD	I(L)	I2S_1_SDO	PCM_1_SOUT	AC97SDO		G/E	Ret_IO	NC	
	Xpcm2SCLK	GPC1[0]	GPI	PD	I(L)	PCM_2_SCLK	SPDIF_0_OUT	I2S_2_SCLK		G/E	Ret_IO	NC	
	Xpcm2EXTCLK	GPC1[1]	GPI	PD	I(L)	PCM_2_EXTCLK	SPDIF_EXTCLK	I2S_2_CDCLK		G/E	Ret_IO	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xpcm2FSYNC	GPC1[2]	GPI	PD	I(L)	PCM_2_FSYNC	LCD_FRM	I2S_2_LRCK		G/E	Ret_IO	NC	
	Xpcm2SIN	GPC1[3]	GPI	PD	I(L)	PCM_2_SIN		I2S_2_SDI		G/E	Ret_IO	NC	
	Xpcm2SOUT	GPC1[4]	GPI	PD	I(L)	PCM_2_SOUT		I2S_2_SDO		G/E	Ret_IO	NC	
VDD_EXT0	XpwmTOUT[0]	GPD0[0]	GPI	PD	I(L)	TOUT_0				G/E	Ret_IO	NC	
	XpwmTOUT[1]	GPD0[1]	GPI	PD	I(L)	TOUT_1				G/E	Ret_IO	NC	
	XpwmTOUT[2]	GPD0[2]	GPI	PD	I(L)	TOUT_2				G/E	Ret_IO	NC	
	XpwmTOUT[3]	GPD0[3]	GPI	PD	I(L)	TOUT_3	PWM_MIE/PWM_MDNIE			G/E	Ret_IO	NC	MIE PWM control
	Xi2c0SDA	GPD1[0]	GPI	PD	I(L)	I2C0_SDA				G/E	Ret_IO	NC	
	Xi2c0SCL	GPD1[1]	GPI	PD	I(L)	I2C0_SCL				G/E	Ret_IO	NC	
VDD_EXT1	Xi2c1SDA	GPD1[2]	GPI	PD	I(L)	I2C1_SDA				G/E	Ret_IO	NC	For HDMI

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xi2c1SCL	GPD1[3]	GPI	PD	I(L)	I2C1_SCL				G/E	Ret_IO	NC	For HDMI
	Xi2c2SDA	GPD1[4]	GPI	PD	I(L)	I2C2_SDA	IEM_SCLK			G/E	Ret_IO	NC	
	Xi2c2SCL	GPD1[5]	GPI	PD	I(L)	I2C2_SCL	IEM_SPWI			G/E	Ret_IO	NC	
VDD_CAM	XciPCLK	GPE0[0]	GPI	PD	I(L)	CAM_A_PCLK				G/E	Ret_IO	NC	
	XciVSYNC	GPE0[1]	GPI	PD	I(L)	CAM_A_VSYNC				G/E	Ret_IO	NC	
	XciHREF	GPE0[2]	GPI	PD	I(L)	CAM_A_HREF				G/E	Ret_IO	NC	
	XciDATA[0]	GPE0[3]	GPI	PD	I(L)	CAM_A_DATA[0]				G/E	Ret_IO	NC	
	XciDATA[1]	GPE0[4]	GPI	PD	I(L)	CAM_A_DATA[1]				G/E	Ret_IO	NC	
	XciDATA[2]	GPE0[5]	GPI	PD	I(L)	CAM_A_DATA[2]				G/E	Ret_IO	NC	
	XciDATA[3]	GPE0[6]	GPI	PD	I(L)	CAM_A_DATA[3]				G/E	Ret_IO	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XciDATA[4]	GPE0[7]	GPI	PD	I(L)	CAM_A_DATA[4]				G/E	Ret_IO	NC	
	XciDATA[5]	GPE1[0]	GPI	PD	I(L)	CAM_A_DATA[5]				G/E	Ret_IO	NC	
	XciDATA[6]	GPE1[1]	GPI	PD	I(L)	CAM_A_DATA[6]				G/E	Ret_IO	NC	
	XciDATA[7]	GPE1[2]	GPI	PD	I(L)	CAM_A_DATA[7]				G/E	Ret_IO	NC	
	XciCLKenb	GPE1[3]	GPI	PD	I(L)	CAM_A_CLKOUT				G/E	Ret_IO	NC	
	XciFIELD	GPE1[4]	GPI	PD	I(L)	CAM_A_FIELD				G/E	Ret_IO	NC	
VDD_LCD	XvHSYNC	GPF0[0]	GPI	PD	I(L)	LCD_HSYNC	SYS_CS0	VEN_HSYNC		G/E	Ret_IO	NC	
	XvVSYNC	GPF0[1]	GPI	PD	I(L)	LCD_VSYNC	SYS_CS1	VEN_VSYNC		G/E	Ret_IO	NC	
	XvVDEN	GPF0[2]	GPI	PD	I(L)	LCD_VDEN	SYS_RS	VEN_HREF		G/E	Ret_IO	NC	
	XvVCLK	GPF0[3]	GPI	PD	I(L)	LCD_VCLK	SYS_WE	V601_CLK		G/E	Ret_IO	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XvVD[0]	GPF0[4]	GPI	PD	I(L)	LCD_VD[0]	SYS_VD[0]	VEN_DATA[0]		G/E	Ret_IO	NC	
	XvVD[1]	GPF0[5]	GPI	PD	I(L)	LCD_VD[1]	SYS_VD[1]	VEN_DATA[1]		G/E	Ret_IO	NC	
	XvVD[2]	GPF0[6]	GPI	PD	I(L)	LCD_VD[2]	SYS_VD[2]	VEN_DATA[2]		G/E	Ret_IO	NC	
	XvVD[3]	GPF0[7]	GPI	PD	I(L)	LCD_VD[3]	SYS_VD[3]	VEN_DATA[3]		G/E	Ret_IO	NC	
	XvVD[4]	GPF1[0]	GPI	PD	I(L)	LCD_VD[4]	SYS_VD[4]	VEN_DATA[4]		G/E	Ret_IO	NC	
	XvVD[5]	GPF1[1]	GPI	PD	I(L)	LCD_VD[5]	SYS_VD[5]	VEN_DATA[5]		G/E	Ret_IO	NC	
	XvVD[6]	GPF1[2]	GPI	PD	I(L)	LCD_VD[6]	SYS_VD[6]	VEN_DATA[6]		G/E	Ret_IO	NC	
	XvVD[7]	GPF1[3]	GPI	PD	I(L)	LCD_VD[7]	SYS_VD[7]	VEN_DATA[7]		G/E	Ret_IO	NC	
	XvVD[8]	GPF1[4]	GPI	PD	I(L)	LCD_VD[8]	SYS_VD[8]	V656_DATA[0]		G/E	Ret_IO	NC	
	XvVD[9]	GPF1[5]	GPI	PD	I(L)	LCD_VD[9]	SYS_VD[9]	V656_DATA[1]		G/E	Ret_IO	NC	
	XvVD[10]	GPF1[6]	GPI	PD	I(L)	LCD_VD[10]	SYS_VD[10]	V656_DATA[2]		G/E	Ret_IO	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XvVD[11]	GPF1[7]	GPI	PD	I(L)	LCD_VD[11]	SYS_VD[11]	V656_DATA[3]		G/E	Ret_IO	NC	
	XvVD[12]	GPF2[0]	GPI	PD	I(L)	LCD_VD[12]	SYS_VD[12]	V656_DATA[4]		G/E	Ret_IO	NC	
	XvVD[13]	GPF2[1]	GPI	PD	I(L)	LCD_VD[13]	SYS_VD[13]	V656_DATA[5]		G/E	Ret_IO	NC	
	XvVD[14]	GPF2[2]	GPI	PD	I(L)	LCD_VD[14]	SYS_VD[14]	V656_DATA[6]		G/E	Ret_IO	NC	
	XvVD[15]	GPF2[3]	GPI	PD	I(L)	LCD_VD[15]	SYS_VD[15]	V656_DATA[7]		G/E	Ret_IO	NC	
	XvVD[16]	GPF2[4]	GPI	PD	I(L)	LCD_VD[16]	SYS_VD[16]			G/E	Ret_IO	NC	
	XvVD[17]	GPF2[5]	GPI	PD	I(L)	LCD_VD[17]	SYS_VD[17]			G/E	Ret_IO	NC	
	XvVD[18]	GPF2[6]	GPI	PD	I(L)	LCD_VD[18]	SYS_VD[18]			G/E	Ret_IO	NC	
	XvVD[19]	GPF2[7]	GPI	PD	I(L)	LCD_VD[19]	SYS_VD[19]			G/E	Ret_IO	NC	
	XvVD[20]	GPF3[0]	GPI	PD	I(L)	LCD_VD[20]	SYS_VD[20]			G/E	Ret_IO	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XvVD[21]	GPF3[1]	GPI	PD	I(L)	LCD_VD[21]	SYS_VD[21]			G/E	Ret_IO	NC	
	XvVD[22]	GPF3[2]	GPI	PD	I(L)	LCD_VD[22]	SYS_VD[22]			G/E	Ret_IO	NC	
	XvVD[23]	GPF3[3]	GPI	PD	I(L)	LCD_VD[23]	SYS_VD[23]	V656_CLK		G/E	Ret_IO	NC	
	XvVSYNC_LDI	GPF3[4]	GPI	PD	I(L)	VSYNC_LDI	VSYNC_LDI	VSYNC_LDI		G/E	Ret_IO	NC	
	XvSYS_OE	GPF3[5]	GPI	PD	I(L)	SYS_OE	SYS_OE	VEN_FIELD		G/E	Ret_IO	NC	
VDD_EXT0	Xmmc0CLK	GPG0[0]	GPI	PD	I(L)	SD_0_CLK				G/E	Ret_MMC	NC	
	Xmmc0CMD	GPG0[1]	GPI	PD	I(L)	SD_0_CMD				G/E	Ret_MMC	NC	
	Xmmc0CDn	GPG0[2]	GPI	PD	I(L)	SD_0_CDn				G/E	Ret_MMC	NC	
	Xmmc0DATA[0]	GPG0[3]	GPI	PD	I(L)	SD_0_DATA[0]							
	Xmmc0DATA[1]	GPG0[4]	GPI	PD	I(L)	SD_0_DATA[1]				G/E	Ret_MMC	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xmmc0DATA [2]	GPG0[5]	GPI	PD	I(L)	SD_0_DATA[2]				G/E	Ret_MM C	NC	
	Xmmc0DATA [3]	GPG0[6]	GPI	PD	I(L)	SD_0_DATA[3]				G/E	Ret_MM C	NC	
	Xmmc1CLK	GPG1[0]	GPI	PD	I(L)	SD_1_CLK				G/E	Ret_MM C	NC	
	Xmmc1CMD	GPG1[1]	GPI	PD	I(L)	SD_1_CMD				G/E	Ret_MM C	NC	
	Xmmc1CDn	GPG1[2]	GPI	PD	I(L)	SD_1_CDn				G/E	Ret_MM C	NC	
	Xmmc1DATA [0]	GPG1[3]	GPI	PD	I(L)	SD_1_DATA[0]	SD_0_DATA[4]			G/E	Ret_MM C	NC	
	Xmmc1DATA [1]	GPG1[4]	GPI	PD	I(L)	SD_1_DATA[1]	SD_0_DATA[5]			G/E	Ret_MM C	NC	
	Xmmc1DATA [2]	GPG1[5]	GPI	PD	I(L)	SD_1_DATA[2]	SD_0_DATA[6]			G/E	Ret_MM C	NC	
	Xmmc1DATA	GPG1[6]	GPI	PD	I(L)	SD_1_DATA[3	SD_0_DATA[7]			G/E	Ret_MM	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	[3]					]					C		
VDD_EXT1	Xmmc2CLK	GPG2[0]	GPI	PD	I(L)	SD_2_CLK				G/E	Ret_MMC	NC	
	Xmmc2CMD	GPG2[1]	GPI	PD	I(L)	SD_2_CMD				G/E	Ret_MMC	NC	
	Xmmc2CDn	GPG2[2]	GPI	PD	I(L)	SD_2_CDn				G/E	Ret_MMC	NC	
	Xmmc2DATA[0]	GPG2[3]	GPI	PD	I(L)	SD_2_DATA[0]				G/E	Ret_MMC	NC	
	Xmmc2DATA[1]	GPG2[4]	GPI	PD	I(L)	SD_2_DATA[1]				G/E	Ret_MMC	NC	
	Xmmc2DATA[2]	GPG2[5]	GPI	PD	I(L)	SD_2_DATA[2]				G/E	Ret_MMC	NC	
	Xmmc2DATA[3]	GPG2[6]	GPI	PD	I(L)	SD_2_DATA[3]				G/E	Ret_MMC	NC	
VDD_EXT2	Xmmc3CLK	GPG3[0]	GPI	PD	I(L)	SD_3_CLK				G/E	Ret_MMC	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xmmc3CMD	GPG3[1]	GPI	PD	I(L)	SD_3_CMD				G/E	Ret_MMC	NC	
	Xmmc3CDn	GPG3[2]	GPI	PD	I(L)	SD_3_CDn				G/E	Ret_MMC	NC	
	Xmmc3DATA[0]	GPG3[3]	GPI	PD	I(L)	SD_3_DATA[0]	SD_2_DATA[4]			G/E	Ret_MMC	NC	
	Xmmc3DATA[1]	GPG3[4]	GPI	PD	I(L)	SD_3_DATA[1]	SD_2_DATA[5]			G/E	Ret_MMC	NC	
	Xmmc3DATA[2]	GPG3[5]	GPI	PD	I(L)	SD_3_DATA[2]	SD_2_DATA[6]			G/E	Ret_MMC	NC	
	Xmmc3DATA[3]	GPG3[6]	GPI	PD	I(L)	SD_3_DATA[3]	SD_2_DATA[7]			G/E	Ret_MMC	NC	
VDD_SYS0	XEINT[0]	GPH0[0]	GPI	PD	I(L)					G/E/W	No_Ret	NC	Can be used as a PS_HOLD pin Wakeup source
	XEINT[1]	GPH0[1]	GPI	PD	I(L)					G/E/	No_Ret	NC	wakeup source

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
										W			
	XEINT[2]	GPH0[2]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
	XEINT[3]	GPH0[3]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
	XEINT[4]	GPH0[4]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
	XEINT[5]	GPH0[5]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
	XEINT[6]	GPH0[6]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
	XEINT[7]	GPH0[7]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
VDD_SYS1	XEINT[8]	GPH1[0]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
	XEINT[9]	GPH1[1]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XEINT[10]	GPH1[2]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
	XEINT[11]	GPH1[3]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
	XEINT[12]	GPH1[4]	GPI	PD	I(L)			HDMI_CEC		G/E/ W	No_Ret	NC	wakeup source
	XEINT[13]	GPH1[5]	GPI	PD	I(L)			HDMI_HPD		G/E/ W	No_Ret	NC	wakeup source
	XEINT[14]	GPH1[6]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
	XEINT[15]	GPH1[7]	GPI	PD	I(L)					G/E/ W	No_Ret	NC	wakeup source
VDD_KEY	XEINT[16]	GPH2[0]	GPI	PD	I(L)		KP_COL[0]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[17]	GPH2[1]	GPI	PD	I(L)		KP_COL[1]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[18]	GPH2[2]	GPI	PD	I(L)		KP_COL[2]			G/E/	No_Ret	NC	wakeup source

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
										W			
	XEINT[19]	GPH2[3]	GPI	PD	I(L)		KP_COL[3]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[20]	GPH2[4]	GPI	PD	I(L)		KP_COL[4]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[21]	GPH2[5]	GPI	PD	I(L)		KP_COL[5]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[22]	GPH2[6]	GPI	PD	I(L)		KP_COL[6]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[23]	GPH2[7]	GPI	PD	I(L)		KP_COL[7]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[24]	GPH3[0]	GPI	PD	I(L)		KP_ROW[0]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[25]	GPH3[1]	GPI	PD	I(L)		KP_ROW[1]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[26]	GPH3[2]	GPI	PD	I(L)		KP_ROW[2]			G/E/ W	No_Ret	NC	wakeup source

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XEINT[27]	GPH3[3]	GPI	PD	I(L)		KP_ROW[3]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[28]	GPH3[4]	GPI	PD	I(L)		KP_ROW[4]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[29]	GPH3[5]	GPI	PD	I(L)		KP_ROW[5]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[30]	GPH3[6]	GPI	PD	I(L)		KP_ROW[6]			G/E/ W	No_Ret	NC	wakeup source
	XEINT[31]	GPH3[7]	GPI	PD	I(L)		KP_ROW[7]			G/E/ W	No_Ret	NC	wakeup source
VDD_AUD	Xi2s0SCLK	GPI[0]	Func 0	PD	O(L)	I2S_0_SCLK	PCM_0_SCLK			DS	Ret_IO (sleep)	NC	For low power audio
	Xi2s0CDCLK	GPI[1]	Func 0	PD	O(L)	I2S_0_CDCLK	PCM_0_EXTCLK			DS	Ret_IO (sleep)	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xi2s0LRCK	GPI[2]	Func 0	PD	O(L)	I2S_0_LRCK	PCM_0_FSYNC			DS	Ret_IO (sleep)	NC	Cannot be used as GPIO & EINT
	Xi2s0SDI	GPI[3]	Func 0	PD	I(L)	I2S_0_SDI	PCM_0_SIN			DS	Ret_IO (sleep)	NC	
	Xi2s0SDO[0]	GPI[4]	Func 0	PD	O(L)	I2S_0_SDO[0]	PCM_0_SOUT			DS	Ret_IO (sleep)	NC	
	Xi2s0SDO[1]	GPI[5]	Func 0	PD	O(L)	I2S_0_SDO[1]				DS	Ret_IO (sleep)	NC	
	Xi2s0SDO[2]	GPI[6]	Func 0	PD	O(L)	I2S_0_SDO[2]				DS	Ret_IO (sleep)	NC	
VDD_MODEM	XmsmADDR[0]	GPJ0[0]	GPI	PD	I(L)	MSM_ADDR[0]	CAM_B_DATA[0]	CF_ADDR[0]	MIPI_BYTE_CLK	G/E	Ret_CF	NC	
	XmsmADDR[	GPJ0[1]	GPI	PD	I(L)	MSM_ADDR[1]	CAM_B_DATA[	CF_ADDR[1]	MIPI_ESC_CL	G/E	Ret_CF	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	1]						1]		K				
	XmsmADDR[2]	GPJ0[2]	GPI	PD	I(L)	MSM_ADDR[2]	CAM_B_DATA[2]	CF_ADDR[2]	TS_CLK	G/E	Ret_CF	NC	
	XmsmADDR[3]	GPJ0[3]	GPI	PD	I(L)	MSM_ADDR[3]	CAM_B_DATA[3]	CF_IORDY	TS_SYNC	G/E	Ret_CF	NC	
	XmsmADDR[4]	GPJ0[4]	GPI	PD	I(L)	MSM_ADDR[4]	CAM_B_DATA[4]	CF_INTRQ	TS_VAL	G/E	Ret_CF	NC	
	XmsmADDR[5]	GPJ0[5]	GPI	PD	I(L)	MSM_ADDR[5]	CAM_B_DATA[5]	CF_DMARQ	TS_DATA	G/E	Ret_CF	NC	
	XmsmADDR[6]	GPJ0[6]	GPI	PD	I(L)	MSM_ADDR[6]	CAM_B_DATA[6]	CF_DRESETN	TS_ERROR	G/E	Ret_CF	NC	
	XmsmADDR[7]	GPJ0[7]	GPI	PD	I(L)	MSM_ADDR[7]	CAM_B_DATA[7]	CF_DMACKN	MHL_D0	G/E	Ret_CF	NC	
	XmsmADDR[8]	GPJ1[0]	GPI	PD	I(L)	MSM_ADDR[8]	CAM_B_PCLK	SROM_ADDR[16]	MHL_D1	G/E	Ret_CF	NC	
	XmsmADDR[9]	GPJ1[1]	GPI	PD	I(L)	MSM_ADDR[9]	CAM_B_VSYNC	SROM_ADDR[17]	MHL_D2	G/E	Ret_CF	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XmsmADDR[10]	GPJ1[2]	GPI	PD	I(L)	MSM_ADDR[10]	CAM_B_HREF	SROM_ADDR[18]	MHL_D3	G/E	Ret_CF	NC	
	XmsmADDR[11]	GPJ1[3]	GPI	PD	I(L)	MSM_ADDR[11]	CAM_B_FIELD	SROM_ADDR[19]	MHL_D4	G/E	Ret_CF	NC	
	XmsmADDR[12]	GPJ1[4]	GPI	PD	I(L)	MSM_ADDR[12]	CAM_B_CLKOUT	SROM_ADDR[20]	MHL_D5	G/E	Ret_CF	NC	
	XmsmADDR[13]	GPJ1[5]	GPI	PD	I(L)	MSM_ADDR[13]	KP_COL[0]	SROM_ADDR[21]	MHL_D6	G/E	Ret_CF	NC	
	XmsmDATA[0]	GPJ2[0]	GPI	PD	I(L)	MSM_DATA[0]	KP_COL[1]	CF_DATA[0]	MHL_D7	G/E	Ret_CF	NC	
	XmsmDATA[1]	GPJ2[1]	GPI	PD	I(L)	MSM_DATA[1]	KP_COL[2]	CF_DATA[1]	MHL_D8	G/E	Ret_CF	NC	
	XmsmDATA[2]	GPJ2[2]	GPI	PD	I(L)	MSM_DATA[2]	KP_COL[3]	CF_DATA[2]	MHL_D9	G/E	Ret_CF	NC	
	XmsmDATA[3]	GPJ2[3]	GPI	PD	I(L)	MSM_DATA[3]	KP_COL[4]	CF_DATA[3]	MHL_D10	G/E	Ret_CF	NC	
	XmsmDATA[	GPJ2[4]	GPI	PD	I(L)	MSM_DATA[4]	KP_COL[5]	CF_DATA[4]	MHL_D11	G/E	Ret_CF	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	4]												
	XmsmDATA[5]	GPJ2[5]	GPI	PD	I(L)	MSM_DATA[5]	KP_COL[6]	CF_DATA[5]	MHL_D12	G/E	Ret_CF	NC	
	XmsmDATA[6]	GPJ2[6]	GPI	PD	I(L)	MSM_DATA[6]	KP_COL[7]	CF_DATA[6]	MHL_D13	G/E	Ret_CF	NC	
	XmsmDATA[7]	GPJ2[7]	GPI	PD	I(L)	MSM_DATA[7]	KP_ROW[0]	CF_DATA[7]	MHL_D14	G/E	Ret_CF	NC	
	XmsmDATA[8]	GPJ3[0]	GPI	PD	I(L)	MSM_DATA[8]	KP_ROW[1]	CF_DATA[8]	MHL_D15	G/E	Ret_CF	NC	
	XmsmDATA[9]	GPJ3[1]	GPI	PD	I(L)	MSM_DATA[9]	KP_ROW[2]	CF_DATA[9]	MHL_D16	G/E	Ret_CF	NC	
	XmsmDATA[10]	GPJ3[2]	GPI	PD	I(L)	MSM_DATA[10]	KP_ROW[3]	CF_DATA[10]	MHL_D17	G/E	Ret_CF	NC	
	XmsmDATA[11]	GPJ3[3]	GPI	PD	I(L)	MSM_DATA[11]	KP_ROW[4]	CF_DATA[11]	MHL_D18	G/E	Ret_CF	NC	
	XmsmDATA[12]	GPJ3[4]	GPI	PD	I(L)	MSM_DATA[12]	KP_ROW[5]	CF_DATA[12]	MHL_D19	G/E	Ret_CF	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XmsmDATA[13]	GPJ3[5]	GPI	PD	I(L)	MSM_DATA[13]	KP_ROW[6]	CF_DATA[13]	MHL_D20	G/E	Ret_CF	NC	
	XmsmDATA[14]	GPJ3[6]	GPI	PD	I(L)	MSM_DATA[14]	KP_ROW[7]	CF_DATA[14]	MHL_D21	G/E	Ret_CF	NC	
	XmsmDATA[15]	GPJ3[7]	GPI	PD	I(L)	MSM_DATA[15]	KP_ROW[8]	CF_DATA[15]	MHL_D22	G/E	Ret_CF	NC	
	XmsmCSn	GPJ4[0]	GPI	PD	I(L)	MSM_CSn	KP_ROW[9]	CF_CSn[0]	MHL_D23	G/E	Ret_CF	NC	
	XmsmWEn	GPJ4[1]	GPI	PD	I(L)	MSM_WEn	KP_ROW[10]	CF_CSn[1]	MHL_HSYNC	G/E	Ret_CF	NC	
	XmsmRn	GPJ4[2]	GPI	PD	I(L)	MSM_Rn	KP_ROW[11]	CF_IORN	MHL_IDCK	G/E	Ret_CF	NC	
	XmsmIRQn	GPJ4[3]	GPI	PD	I(L)	MSM_IRQn	KP_ROW[12]	CF_IOWN	MHL_VSYNC	G/E	Ret_CF	NC	
	XmsmADVN	GPJ4[4]	GPI	PD	I(L)	MSM_ADVN	KP_ROW[13]	SROM_ADDR[22]	MHL_DE	G/E	Ret_CF	NC	
VDD_M0	Xm0CSn[0]	MP0_1[0]	Func 0	-	O(H)	SROM_CSn[0]				G	Ret_auto	NC	
	Xm0CSn[1]	MP0_1[1]	Func 0	-	O(H)	SROM_CSn[1]				G	Ret_auto	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm0CSn[2]	MP0_1[2]	Func 1	-	O(H)	SROM_CSn[2]	NFCSn[0]			G	Ret_auto	NC	
	Xm0CSn[3]	MP0_1[3]	Func 1	-	O(H)	SROM_CSn[3]	NFCSn[1]			G	Ret_auto	NC	
	Xm0CSn[4]	MP0_1[4]	Func 3	-	O(H)	SROM_CSn[4]	NFCSn[2]		ONANDXL_CSn[0]	I	Ret_auto	-	Should be connected to CE signal of OneNAND Externally
	Xm0CSn[5]	MP0_1[5]	Func 3	-	O(H)	SROM_CSn[5]	NFCSn[3]		ONANDXL_CSn[1]	G	Ret_auto	NC	
	Xm0OEn	MP0_1[6]	Func 0	-	O(H)	EBI_OEn				I	Ret_auto	-	Internally connected to OneNAND
	Xm0WEn	MP0_1[7]	Func 0	-	O(H)	EBI_WEn				I	Ret_auto	-	
	Xm0BEn[0]	MP0_2[0]	Func 0	-	O(H)	EBI_BEn[0]				G	Ret_auto	NC	
	Xm0BEn[1]	MP0_2[1]	Func 0	-	O(H)	EBI_BEn[1]				G	Ret_auto	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm0WAITn	MP0_2[2]	Func 0	-	I	SROM_WAITn				G	Ret_auto	NC	External pull up resistor is needed
	Xm0DATA_RDn	MP0_2[3]	Func 0	-	O(L)	EBI_DATA_RDn				G	Ret_auto	NC	
	Xm0FCLE	MP0_3[0]	Func 3	-	O(L)	NF_CLE			ONANDXL_ADDRVALID	I	Ret_auto	-	Internally connected to OneNAND
	Xm0FALE	MP0_3[1]	Func 3	-	O(L)	NF_ALE			ONANDXL_SMCLK	I	Ret_auto	-	
	Xm0FWEn	MP0_3[2]	Func 3	-	O(H)	NF_FWEn			ONANDXL_RPn	I	Ret_auto	-	
	Xm0FREn	MP0_3[3]	Func 0	-	O(H)	NF_FREn				G	Ret_auto	NC	
	Xm0FRnB[0]	MP0_3[4]	Func 3	-	I	NF_RnB[0]			ONANDXL_INT[0]	I	Ret_auto	-	Internally connected to OneNAND
	Xm0FRnB[1]	MP0_3[5]	Func 3	-	I	NF_RnB[1]			ONANDXL_INT[1]	G	Ret_auto	NC	
	Xm0FRnB[2	MP0_3[6]	Func	-	I	NF_RnB[2]				G	Ret_aut	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	]		0								o		
	Xm0FRnB[3]	MP0_3[7]	Func 0	-	I	NF_RnB[3]				G	Ret_auto	NC	
	Xm0ADDR[0]	MP0_4[0]	Func 0	-	O(L)	EBI_ADDR[0]				G	Ret_auto	NC	
	Xm0ADDR[1]	MP0_4[1]	Func 0	-	O(L)	EBI_ADDR[1]				G	Ret_auto	NC	
	Xm0ADDR[2]	MP0_4[2]	Func 0	-	O(L)	EBI_ADDR[2]				G	Ret_auto	NC	
	Xm0ADDR[3]	MP0_4[3]	Func 0	-	O(L)	EBI_ADDR[3]				G	Ret_auto	NC	
	Xm0ADDR[4]	MP0_4[4]	Func 0	-	O(L)	EBI_ADDR[4]				G	Ret_auto	NC	
	Xm0ADDR[5]	MP0_4[5]	Func 0	-	O(L)	EBI_ADDR[5]				G	Ret_auto	NC	
	Xm0ADDR[6]	MP0_4[6]	Func 0	-	O(L)	EBI_ADDR[6]				G	Ret_auto	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm0ADDR[7]	MP0_4[7]	Func 0	-	O(L)	EBI_ADDR[7]				G	Ret_auto	NC	
	Xm0ADDR[8]	MP0_5[0]	Func 0	-	O(L)	EBI_ADDR[8]				G	Ret_auto	NC	
	Xm0ADDR[9]	MP0_5[1]	Func 0	-	O(L)	EBI_ADDR[9]				G	Ret_auto	NC	
	Xm0ADDR[10]	MP0_5[2]	Func 0	-	O(L)	EBI_ADDR[10]				G	Ret_auto	NC	
	Xm0ADDR[11]	MP0_5[3]	Func 0	-	O(L)	EBI_ADDR[11]				G	Ret_auto	NC	
	Xm0ADDR[12]	MP0_5[4]	Func 0	-	O(L)	EBI_ADDR[12]				G	Ret_auto	NC	
	Xm0ADDR[13]	MP0_5[5]	Func 0	-	O(L)	EBI_ADDR[13]				G	Ret_auto	NC	
	Xm0ADDR[14]	MP0_5[6]	Func 0	-	O(L)	EBI_ADDR[14]				G	Ret_auto	NC	
	Xm0ADDR[1	MP0_5[7]	Func	-	O(L)	EBI_ADDR[15				G	Ret_aut	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	5]		0			]					o		
	Xm0DATA[0]	MP0_6[0]	Func 0	-	O(L)	EBI_DATA[0]				I	Ret_auto	-	Internally connected to OneNAND
	Xm0DATA[1]	MP0_6[1]	Func 0	-	O(L)	EBI_DATA[1]				I	Ret_auto	-	
	Xm0DATA[2]	MP0_6[2]	Func 0	-	O(L)	EBI_DATA[2]				I	Ret_auto	-	
	Xm0DATA[3]	MP0_6[3]	Func 0	-	O(L)	EBI_DATA[3]				I	Ret_auto	-	
	Xm0DATA[4]	MP0_6[4]	Func 0	-	O(L)	EBI_DATA[4]				I	Ret_auto	-	
	Xm0DATA[5]	MP0_6[5]	Func 0	-	O(L)	EBI_DATA[5]				I	Ret_auto	-	
	Xm0DATA[6]	MP0_6[6]	Func 0	-	O(L)	EBI_DATA[6]				I	Ret_auto	-	
	Xm0DATA[7]	MP0_6[7]	Func 0	-	O(L)	EBI_DATA[7]				I	Ret_auto	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm0DATA[8]	MP0_7[0]	Func 0	-	O(L)	EBI_DATA[8]				I	Ret_auto	-	
	Xm0DATA[9]	MP0_7[1]	Func 0	-	O(L)	EBI_DATA[9]				I	Ret_auto	-	
	Xm0DATA[10]	MP0_7[2]	Func 0	-	O(L)	EBI_DATA[10]				I	Ret_auto	-	
	Xm0DATA[11]	MP0_7[3]	Func 0	-	O(L)	EBI_DATA[11]				I	Ret_auto	-	
	Xm0DATA[12]	MP0_7[4]	Func 0	-	O(L)	EBI_DATA[12]				I	Ret_auto	-	
	Xm0DATA[13]	MP0_7[5]	Func 0	-	O(L)	EBI_DATA[13]				I	Ret_auto	-	
	Xm0DATA[14]	MP0_7[6]	Func 0	-	O(L)	EBI_DATA[14]				I	Ret_auto	-	
	Xm0DATA[15]	MP0_7[7]	Func 0	-	O(L)	EBI_DATA[15]				I	Ret_auto	-	
VDD_M1	Xm1ADDR[0	MP1_0[0]	Func	-	O(L)	LD0_ADDR[0]				I(X)	Ret_aut	-	Internally connnected to

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	]		0								o		OneDRAM
	Xm1ADDR[1]	MP1_0[1]	Func 0	-	O(L)	LD0_ADDR[1]				I(X)	Ret_auto	-	
	Xm1ADDR[2]	MP1_0[2]	Func 0	-	O(L)	LD0_ADDR[2]				I(X)	Ret_auto	-	
	Xm1ADDR[3]	MP1_0[3]	Func 0	-	O(L)	LD0_ADDR[3]				I(X)	Ret_auto	-	
	Xm1ADDR[4]	MP1_0[4]	Func 0	-	O(L)	LD0_ADDR[4]				I(X)	Ret_auto	-	
	Xm1ADDR[5]	MP1_0[5]	Func 0	-	O(L)	LD0_ADDR[5]				I(X)	Ret_auto	-	
	Xm1ADDR[6]	MP1_0[6]	Func 0	-	O(L)	LD0_ADDR[6]				I(X)	Ret_auto	-	
	Xm1ADDR[7]	MP1_0[7]	Func 0	-	O(L)	LD0_ADDR[7]				I(X)	Ret_auto	-	
	Xm1ADDR[8]	MP1_1[0]	Func 0	-	O(L)	LD0_ADDR[8]				I(X)	Ret_auto	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm1ADDR[9]	MP1_1[1]	Func0	-	O(L)	LD0_ADDR[9]				I(X)	Ret_auto	-	
	Xm1ADDR[10]	MP1_1[2]	Func0	-	O(L)	LD0_ADDR[10]				I(X)	Ret_auto	-	
	Xm1ADDR[11]	MP1_1[3]	Func0	-	O(L)	LD0_ADDR[11]				I(X)	Ret_auto	-	
	Xm1ADDR[12]	MP1_1[4]	Func0	-	O(L)	LD0_ADDR[12]				I(X)	Ret_auto	-	
	Xm1ADDR[13]	MP1_1[5]	Func0	-	O(L)	LD0_ADDR[13]				I(X)	Ret_auto	-	
	Xm1ADDR[14]	MP1_1[6]	Func0	-	O(L)	LD0_ADDR[14]				I(X)	Ret_auto	-	
	Xm1ADDR[15]	MP1_1[7]	Func0	-	O(L)	LD0_ADDR[15]				I(X)	Ret_auto	-	
	Xm1DATA[0]	MP1_2[0]	Func0	-	I	LD0_DATA[0]				I(X)	Ret_auto	-	
	Xm1DATA[1	MP1_2[1]	Func	-	I	LD0_DATA[1]				I(X)	Ret_aut	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	]		0								o		
	Xm1DATA[2]	MP1_2[2]	Func 0	-	I	LD0_DATA[2]				I(X)	Ret_auto	-	
	Xm1DATA[3]	MP1_2[3]	Func 0	-	I	LD0_DATA[3]				I(X)	Ret_auto	-	
	Xm1DATA[4]	MP1_2[4]	Func 0	-	I	LD0_DATA[4]				I(X)	Ret_auto	-	
	Xm1DATA[5]	MP1_2[5]	Func 0	-	I	LD0_DATA[5]				I(X)	Ret_auto	-	
	Xm1DATA[6]	MP1_2[6]	Func 0	-	I	LD0_DATA[6]				I(X)	Ret_auto	-	
	Xm1DATA[7]	MP1_2[7]	Func 0	-	I	LD0_DATA[7]				I(X)	Ret_auto	-	
	Xm1DATA[8]	MP1_3[0]	Func 0	-	I	LD0_DATA[8]				I(X)	Ret_auto	-	
	Xm1DATA[9]	MP1_3[1]	Func 0	-	I	LD0_DATA[9]				I(X)	Ret_auto	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm1DATA[10]	MP1_3[2]	Func0	-	I	LD0_DATA[10]				I(X)	Ret_auto	-	
	Xm1DATA[11]	MP1_3[3]	Func0	-	I	LD0_DATA[11]				I(X)	Ret_auto	-	
	Xm1DATA[12]	MP1_3[4]	Func0	-	I	LD0_DATA[12]				I(X)	Ret_auto	-	
	Xm1DATA[13]	MP1_3[5]	Func0	-	I	LD0_DATA[13]				I(X)	Ret_auto	-	
	Xm1DATA[14]	MP1_3[6]	Func0	-	I	LD0_DATA[14]				I(X)	Ret_auto	-	
	Xm1DATA[15]	MP1_3[7]	Func0	-	I	LD0_DATA[15]				I(X)	Ret_auto	-	
	Xm1DATA[16]	MP1_4[0]	Func0	-	I	LD0_DATA[16]				I(X)	Ret_auto	-	
	Xm1DATA[17]	MP1_4[1]	Func0	-	I	LD0_DATA[17]				I(X)	Ret_auto	-	
	Xm1DATA[1	MP1_4[2]	Func	-	I	LD0_DATA[18				I(X)	Ret_aut	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	8]		0			]					o		
	Xm1DATA[19]	MP1_4[3]	Func 0	-	I	LD0_DATA[19]				I(X)	Ret_auto	-	
	Xm1DATA[20]	MP1_4[4]	Func 0	-	I	LD0_DATA[20]				I(X)	Ret_auto	-	
	Xm1DATA[21]	MP1_4[5]	Func 0	-	I	LD0_DATA[21]				I(X)	Ret_auto	-	
	Xm1DATA[22]	MP1_4[6]	Func 0	-	I	LD0_DATA[22]				I(X)	Ret_auto	-	
	Xm1DATA[23]	MP1_4[7]	Func 0	-	I	LD0_DATA[23]				I(X)	Ret_auto	-	
	Xm1DATA[24]	MP1_5[0]	Func 0	-	I	LD0_DATA[24]				I(X)	Ret_auto	-	
	Xm1DATA[25]	MP1_5[1]	Func 0	-	I	LD0_DATA[25]				I(X)	Ret_auto	-	
	Xm1DATA[26]	MP1_5[2]	Func 0	-	I	LD0_DATA[26]				I(X)	Ret_auto	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm1DATA[27]	MP1_5[3]	Func0	-	I	LD0_DATA[27]				I(X)	Ret_auto	-	
	Xm1DATA[28]	MP1_5[4]	Func0	-	I	LD0_DATA[28]				I(X)	Ret_auto	-	
	Xm1DATA[29]	MP1_5[5]	Func0	-	I	LD0_DATA[29]				I(X)	Ret_auto	-	
	Xm1DATA[30]	MP1_5[6]	Func0	-	I	LD0_DATA[30]				I(X)	Ret_auto	-	
	Xm1DATA[31]	MP1_5[7]	Func0	-	I	LD0_DATA[31]				I(X)	Ret_auto	-	
	Xm1DQS[0]	MP1_6[0]	Func0	-	I	LD0_DQS[0]				I(X)	Ret_auto	-	
	Xm1DQS[1]	MP1_6[1]	Func0	-	I	LD0_DQS[1]				I(X)	Ret_auto	-	
	Xm1DQS[2]	MP1_6[2]	Func0	-	I	LD0_DQS[2]				I(X)	Ret_auto	-	
	Xm1DQS[3]	MP1_6[3]	Func	-	I	LD0_DQS[3]				I(X)	Ret_aut	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
			0								o		
	Xm1DQSn[0]	MP1_6[4]	Func 0	-	I	LD0_DQSn[0]				I(X)	Ret_auto	-	
	Xm1DQSn[1]	MP1_6[5]	Func 0	-	I	LD0_DQSn[1]				I(X)	Ret_auto	-	
	Xm1DQSn[2]	MP1_6[6]	Func 0	-	I	LD0_DQSn[2]				I(X)	Ret_auto	-	
	Xm1DQSn[3]	MP1_6[7]	Func 0	-	I	LD0_DQSn[3]				I(X)	Ret_auto	-	
	Xm1DQM[0]	MP1_7[0]	Func 0	-	O(L)	LD0_DQM[0]				I(X)	Ret_auto	-	
	Xm1DQM[1]	MP1_7[1]	Func 0	-	O(L)	LD0_DQM[1]				I(X)	Ret_auto	-	
	Xm1DQM[2]	MP1_7[2]	Func 0	-	O(L)	LD0_DQM[2]				I(X)	Ret_auto	-	
	Xm1DQM[3]	MP1_7[3]	Func 0	-	O(L)	LD0_DQM[3]				I(X)	Ret_auto	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm1CKE[0]	MP1_7[4]	Func 0	-	O(L)	LD0_CKE[0]				I(X)	Ret_auto	-	
	Xm1CKE[1]	MP1_7[5]	Func 0	-	O(L)	LD0_CKE[1]				I(X)	Ret_auto	-	
	Xm1SCLK	MP1_7[6]	Func 0	-	O(L)	LD0_SCLK				I(X)	Ret_auto	-	
	Xm1nSCLK	MP1_7[7]	Func 0	-	O(H)	LD0_nSCLK				I(X)	Ret_auto	-	
	Xm1CSn[0]	MP1_8[0]	Func 0	-	O(H)	LD0_CSn_0				I(X)	Ret_auto	-	
	Xm1CSn[1]	MP1_8[1]	Func 0	-	O(H)	LD0_CSn_1				I(X)	Ret_auto	-	
	Xm1RASn	MP1_8[2]	Func 0	-	O(H)	LD0_RASn				I(X)	Ret_auto	-	
	Xm1CASn	MP1_8[3]	Func 0	-	O(H)	LD0_CASn				I(X)	Ret_auto	-	
	Xm1WEn	MP1_8[4]	Func	-	O(H)	LD0_WEn				I(X)	Ret_aut	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
			0								o		
VDD_M2	Xm2ADDR[0]	MP2_0[0]	Func 0	-	O(L)	LD1_ADDR[0]				I(X)	Ret_auto	-	Internally connnected to mDDR
	Xm2ADDR[1]	MP2_0[1]	Func 0	-	O(L)	LD1_ADDR[1]				I(X)	Ret_auto	-	
	Xm2ADDR[2]	MP2_0[2]	Func 0	-	O(L)	LD1_ADDR[2]				I(X)	Ret_auto	-	
	Xm2ADDR[3]	MP2_0[3]	Func 0	-	O(L)	LD1_ADDR[3]				I(X)	Ret_auto	-	
	Xm2ADDR[4]	MP2_0[4]	Func 0	-	O(L)	LD1_ADDR[4]				I(X)	Ret_auto	-	
	Xm2ADDR[5]	MP2_0[5]	Func 0	-	O(L)	LD1_ADDR[5]				I(X)	Ret_auto	-	
	Xm2ADDR[6]	MP2_0[6]	Func 0	-	O(L)	LD1_ADDR[6]				I(X)	Ret_auto	-	
	Xm2ADDR[7]	MP2_0[7]	Func 0	-	O(L)	LD1_ADDR[7]				I(X)	Ret_auto	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm2ADDR[8]	MP2_1[0]	Func0	-	O(L)	LD1_ADDR[8]				I(X)	Ret_auto	-	
	Xm2ADDR[9]	MP2_1[1]	Func0	-	O(L)	LD1_ADDR[9]				I(X)	Ret_auto	-	
	Xm2ADDR[10]	MP2_1[2]	Func0	-	O(L)	LD1_ADDR[10]				I(X)	Ret_auto	-	
	Xm2ADDR[11]	MP2_1[3]	Func0	-	O(L)	LD1_ADDR[11]				I(X)	Ret_auto	-	
	Xm2ADDR[12]	MP2_1[4]	Func0	-	O(L)	LD1_ADDR[12]				I(X)	Ret_auto	-	
	Xm2ADDR[13]	MP2_1[5]	Func0	-	O(L)	LD1_ADDR[13]				I(X)	Ret_auto	-	
	Xm2ADDR[14]	MP2_1[6]	Func0	-	O(L)	LD1_ADDR[14]				I(X)	Ret_auto	-	
	Xm2ADDR[15]	MP2_1[7]	Func0	-	O(L)	LD1_ADDR[15]				I(X)	Ret_auto	-	
	Xm2DATA[0	MP2_2[0]	Func	-	I	LD1_DATA[0]				I(X)	Ret_aut	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	]		0								o		
	Xm2DATA[1]	MP2_2[1]	Func 0	-	I	LD1_DATA[1]				I(X)	Ret_auto	-	
	Xm2DATA[2]	MP2_2[2]	Func 0	-	I	LD1_DATA[2]				I(X)	Ret_auto	-	
	Xm2DATA[3]	MP2_2[3]	Func 0	-	I	LD1_DATA[3]				I(X)	Ret_auto	-	
	Xm2DATA[4]	MP2_2[4]	Func 0	-	I	LD1_DATA[4]				I(X)	Ret_auto	-	
	Xm2DATA[5]	MP2_2[5]	Func 0	-	I	LD1_DATA[5]				I(X)	Ret_auto	-	
	Xm2DATA[6]	MP2_2[6]	Func 0	-	I	LD1_DATA[6]				I(X)	Ret_auto	-	
	Xm2DATA[7]	MP2_2[7]	Func 0	-	I	LD1_DATA[7]				I(X)	Ret_auto	-	
	Xm2DATA[8]	MP2_3[0]	Func 0	-	I	LD1_DATA[8]				I(X)	Ret_auto	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm2DATA[9]	MP2_3[1]	Func0	-	I	LD1_DATA[9]				I(X)	Ret_auto	-	
	Xm2DATA[10]	MP2_3[2]	Func0	-	I	LD1_DATA[10]				I(X)	Ret_auto	-	
	Xm2DATA[11]	MP2_3[3]	Func0	-	I	LD1_DATA[11]				I(X)	Ret_auto	-	
	Xm2DATA[12]	MP2_3[4]	Func0	-	I	LD1_DATA[12]				I(X)	Ret_auto	-	
	Xm2DATA[13]	MP2_3[5]	Func0	-	I	LD1_DATA[13]				I(X)	Ret_auto	-	
	Xm2DATA[14]	MP2_3[6]	Func0	-	I	LD1_DATA[14]				I(X)	Ret_auto	-	
	Xm2DATA[15]	MP2_3[7]	Func0	-	I	LD1_DATA[15]				I(X)	Ret_auto	-	
	Xm2DATA[16]	MP2_4[0]	Func0	-	I	LD1_DATA[16]				I(X)	Ret_auto	-	
	Xm2DATA[1	MP2_4[1]	Func	-	I	LD1_DATA[17				I(X)	Ret_aut	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	7]		0			]					o		
	Xm2DATA[18]	MP2_4[2]	Func 0	-	I	LD1_DATA[18]				I(X)	Ret_auto	-	
	Xm2DATA[19]	MP2_4[3]	Func 0	-	I	LD1_DATA[19]				I(X)	Ret_auto	-	
	Xm2DATA[20]	MP2_4[4]	Func 0	-	I	LD1_DATA[20]				I(X)	Ret_auto	-	
	Xm2DATA[21]	MP2_4[5]	Func 0	-	I	LD1_DATA[21]				I(X)	Ret_auto	-	
	Xm2DATA[22]	MP2_4[6]	Func 0	-	I	LD1_DATA[22]				I(X)	Ret_auto	-	
	Xm2DATA[23]	MP2_4[7]	Func 0	-	I	LD1_DATA[23]				I(X)	Ret_auto	-	
	Xm2DATA[24]	MP2_5[0]	Func 0	-	I	LD1_DATA[24]				I(X)	Ret_auto	-	
	Xm2DATA[25]	MP2_5[1]	Func 0	-	I	LD1_DATA[25]				I(X)	Ret_auto	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm2DATA[26]	MP2_5[2]	Func0	-	I	LD1_DATA[26]				I(X)	Ret_auto	-	
	Xm2DATA[27]	MP2_5[3]	Func0	-	I	LD1_DATA[27]				I(X)	Ret_auto	-	
	Xm2DATA[28]	MP2_5[4]	Func0	-	I	LD1_DATA[28]				I(X)	Ret_auto	-	
	Xm2DATA[29]	MP2_5[5]	Func0	-	I	LD1_DATA[29]				I(X)	Ret_auto	-	
	Xm2DATA[30]	MP2_5[6]	Func0	-	I	LD1_DATA[30]				I(X)	Ret_auto	-	
	Xm2DATA[31]	MP2_5[7]	Func0	-	I	LD1_DATA[31]				I(X)	Ret_auto	-	
	Xm2DQS[0]	MP2_6[0]	Func0	-	I	LD1_DQS[0]				I(X)	Ret_auto	-	
	Xm2DQS[1]	MP2_6[1]	Func0	-	I	LD1_DQS[1]				I(X)	Ret_auto	-	
	Xm2DQS[2]	MP2_6[2]	Func	-	I	LD1_DQS[2]				I(X)	Ret_aut	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
			0								o		
	Xm2DQS[3]	MP2_6[3]	Func 0	-	I	LD1_DQS[3]				I(X)	Ret_auto	-	
	Xm2DQSn[0]	MP2_6[4]	Func 0	-	I	LD1_DQSn[0]				I(X)	Ret_auto	-	
	Xm2DQSn[1]	MP2_6[5]	Func 0	-	I	LD1_DQSn[1]				I(X)	Ret_auto	-	
	Xm2DQSn[2]	MP2_6[6]	Func 0	-	I	LD1_DQSn[2]				I(X)	Ret_auto	-	
	Xm2DQSn[3]	MP2_6[7]	Func 0	-	I	LD1_DQSn[3]				I(X)	Ret_auto	-	
	Xm2DQM[0]	MP2_7[0]	Func 0	-	O(L)	LD1_DQM[0]				I(X)	Ret_auto	-	
	Xm2DQM[1]	MP2_7[1]	Func 0	-	O(L)	LD1_DQM[1]				I(X)	Ret_auto	-	
	Xm2DQM[2]	MP2_7[2]	Func 0	-	O(L)	LD1_DQM[2]				I(X)	Ret_auto	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	Xm2DQM[3]	MP2_7[3]	Func 0	-	O(L)	LD1_DQM[3]				I(X)	Ret_auto	-	
	Xm2CKE[0]	MP2_7[4]	Func 0	-	O(L)	LD1_CKE[0]				I(X)	Ret_auto	-	
	Xm2CKE[1]	MP2_7[5]	Func 0	-	O(L)	LD1_CKE[1]				I(X)	Ret_auto	-	
	Xm2SCLK	MP2_7[6]	Func 0	-	O(L)	LD1_SCLK				I(X)	Ret_auto	-	
	Xm2nSCLK	MP2_7[7]	Func 0	-	O(H)	LD1_nSCLK				I(X)	Ret_auto	-	
	Xm2CSn[0]	MP2_8[0]	Func 0	-	O(H)	LD1_CSn_0				I(X)	Ret_auto	-	
	Xm2CSn[1]	MP2_8[1]	Func 0	-	O(H)	LD1_CSn_1				I(X)	Ret_auto	-	
	Xm2RASn	MP2_8[2]	Func 0	-	O(H)	LD1_RASn				I(X)	Ret_auto	-	
	Xm2CASn	MP2_8[3]	Func	-	O(H)	LD1_CASn				I(X)	Ret_aut	-	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
			0								o		
	Xm2WEn	MP2_8[4]	Func 0	-	O(H)	LD1_WEn				I(X)	Ret_auto	-	
VDD_SYS0	XjTRSTn	ETC0[0]	-	PD	I(L)	XjTRSTn				DS	Ret_auto	NC	Internally connected to Pd resistor
	XjTMS	ETC0[1]	-	PU	I(H)	XjTMS				DS	Ret_auto	NC	Internally connected to Pu resistor
	XjTCK	ETC0[2]	-	PD	I(L)	XjTCK				DS	Ret_auto	NC	Internally connected to Pd resistor
	XjTDI	ETC0[3]	-	PU	I(H)	XjTDI				DS	Ret_auto	NC	Internally connected to Pu resistor
	XjTDO	ETC0[4]	-	-	O(L)	XjTDO				DS	Ret_auto	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XjDBGSEL	ETC0[5]	-	-	I	XjDBGSEL				DS	Ret_auto	PD	Externally should be connected to pull down resistor or GND
	XOM[0]	ETC1[0]	-	-	I	XOM[0]				DS	No_Ret	PU/ PD	Booting option
	XOM[1]	ETC1[1]	-	-	I	XOM[1]				DS	No_Ret	PU/ PD	OneNAND case: OM[5:0]=2b'001001'
	XOM[2]	ETC1[2]	-	-	I	XOM[2]				DS	No_Ret	PU/ PD	
	XOM[3]	ETC1[3]	-	-	I	XOM[3]				DS	No_Ret	PU/ PD	
	XOM[4]	ETC1[4]	-	-	I	XOM[4]				DS	No_Ret	PU/ PD	
	XOM[5]	ETC1[5]	-	-	I	XOM[5]				DS	No_Ret	PU/ PD	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XDDR2SEL	ETC1[6]	-	-	I	XDDR2_SEL				DS	Ret_IO	PD	mDDR: 'Low', DDR2 & LPDDR2 : 'High'. Should connect to pull down or GND
	XPWRRGTON	ETC1[7]	-	-	O(L)	XPWRRGTON				DS	No_Ret	NC	
	XnRESET	ETC2[0]	-	-	I	XnRESET				DS	No_Ret	PU	
VDD_AUD	XCLKOUT	ETC2[1]	-	-	O(L)	CLKOUT				DS	No_Ret	NC	
VDD_SYS0	XnRSTOUT	ETC2[2]	-	-	O(L)	XnRSTOUT				DS	No_Ret	NC	
	XnWRESET	ETC2[3]		PU	I(H)	XnWRESET				DS	No_Ret	NC	Internally connected to Pu resistor
VDD_CKO	XRTCCLKO	ETC2[4]	-	-	O(L)	RTC_CLKOUT				DS	No_Ret	NC	
VDD_SYS0	XuotgDRVVBUS	ETC2[5]	-	-	O(L)	XuotgDRVVBUS				DS	Ret_IO	NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XuhostPWREN	ETC2[6]	-	-	O(L)	XuhostPWREN				DS	Ret_IO	NC	Charge pump enable signal
	XuhostOVERCUR	ETC2[7]		-	I	XuhostOVERCUR				DS	Ret_IO	PD	
VDD_RTC	XrtcXTI	ETC4[0]	-	-	I	XrtcXTI				DS	No_Ret	PD	-14pF external cap(each pad) -10Mohm feedback register(between pad)
	XrtcXTO	ETC4[1]	-	-	O(L)	XrtcXTO				DS	No_Ret	NC	
VDD_SYS0	XXTI	ETC4[2]	-	-	I	XXTI				DS	No_Ret	PD	-14pF external cap(each pad) -5Mohm feedback register(between pad)
	XXTO	ETC4[3]	-	-	O(L)	XXTO				DS	No_Ret	NC	
VDD_SYS0	XusbXTI	ETC4[4]	-	-	I	XusbXTI				DS	No_Ret	PD	-14pF external cap(each pad) -5Mohm feedback register(between pad)
	XusbXTO	ETC4[5]	-	-	O(L)	XusbXTO				DS	No_Ret	NC	
VDD_ADC	XadcAIN[0]	ANALOG[0]				AIN[0]				DS		NC	
	XadcAIN[1	ANALOG[1				AIN[1]				DS		NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	]	]											
	XadcAIN[2]	ANALOG[2]				AIN[2]				DS		NC	
	XadcAIN[3]	ANALOG[3]				AIN[3]				DS		NC	
	XadcAIN[4]	ANALOG[4]				AIN[4]				DS		NC	
	XadcAIN[5]	ANALOG[5]				AIN[5]				DS		NC	
	XadcAIN[6]	ANALOG[6]				AIN[6]				DS		NC	
	XadcAIN[7]	ANALOG[7]				AIN[7]				DS		NC	
	XadcAIN[8]	ANALOG[8]				AIN[8]				DS		NC	
	XadcAIN[9]	ANALOG[9]				AIN[9]				DS		NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
VDD_DAC	XdacOUT	ANALOG[11]				XdacOUT				DS		NC	75ohm pull-down
	XdacIREF	ANALOG[14]				XdacIREF				DS		NC	1.2Kohm/1% pull-down
	XdacVREF	ANALOG[15]				XdacVREF				DS		GND	100nF GND tie
	XdacCOMP	ANALOG[16]				XdacCOMP				DS		NC	100nF VDD_DAC tie
VDD_HDMI	XhdmiTX0P	ANALOG[17]				HDMI_TX0P				DS		NC	
	XhdmiTX0N	ANALOG[18]				HDMI_TX0N				DS		NC	
	XhdmiTX1P	ANALOG[19]				HDMI_TX1P				DS		NC	
	XhdmiTX1N	ANALOG[20]				HDMI_TX1N				DS		NC	
	XhdmiTX2P	ANALOG[2				HDMI_TX2P				DS		NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
		1]											
	XhdmiTX2N	ANALOG[22]				HDMI_TX2N				DS		NC	
	XhdmiTXCP	ANALOG[23]				HDMI_TXCP				DS		NC	
	XhdmiTXCN	ANALOG[24]				HDMI_TXCN				DS		NC	
	XhdmiREXT	ANALOG[25]				HDMI_REXT				DS		PD	4.6Kohm 1% pull-down
VDD_HDMI_OSC	XhdmiXTI	ANALOG[26]				HDMI_XI				DS		PD	-14pF external cap(each pad) -5Mohm feedback register(between pad)
	XhdmiXTO	ANALOG[27]				HDMI_XO				DS		NC	
VDD_MIPI_A	XmipiMDP0	ANALOG[28]				MIPI_MDP_0				DS		NC	
	XmipiMDP1	ANALOG[29]				MIPI_MDP_1				DS		NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XmipiMDP2	ANALOG[30]				MIPI_MDP_2				DS		NC	
	XmipiMDP3	ANALOG[31]				MIPI_MDP_3				DS		NC	
	XmipiMDN0	ANALOG[32]				MIPI_MDN_0				DS		NC	
	XmipiMDN1	ANALOG[33]				MIPI_MDN_1				DS		NC	
	XmipiMDN2	ANALOG[34]				MIPI_MDN_2				DS		NC	
	XmipiMDN3	ANALOG[35]				MIPI_MDN_3				DS		NC	
	XmipiSDP0	ANALOG[36]				MIPI_SDP_0				DS		NC	
	XmipiSDP1	ANALOG[37]				MIPI_SDP_1				DS		NC	
	XmipiSDP2	ANALOG[3				MIPI_SDP_2				DS		NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
		8]											
	XmipiSDP3	ANALOG[39]				MIPI_SDP_3				DS		NC	
	XmipiSDN0	ANALOG[40]				MIPI_SDN_0				DS		NC	
	XmipiSDN1	ANALOG[41]				MIPI_SDN_1				DS		NC	
	XmipiSDN2	ANALOG[42]				MIPI_SDN_2				DS		NC	
	XmipiSDN3	ANALOG[43]				MIPI_SDN_3				DS		NC	
	XmipiMDPCLK	ANALOG[44]				MIPI_CLK_TX_P				DS		NC	
	XmipiMDNCLK	ANALOG[45]				MIPI_CLK_TX_N				DS		NC	
	XmipiSDPCLK	ANALOG[46]				MIPI_CLK_RX_P				DS		NC	

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XmipiSDNCLK	ANALOG[47]				MIPI_CLK_RX_N				DS		NC	
	XmipiVREG_0P4V	ANALOG[48]				MIPI_Reg_cap				DS		NC	2nF GND tie
VDD_UOTG_A	XuotgDP	ANALOG[49]				XuotgDP				DS		NC	
	XuotgREXT	ANALOG[50]				XuotgREXT				DS		NC	44.2ohm/1% pull-down
	XuotgDM	ANALOG[51]				XuotgDM				DS		NC	
	XefFSOURCE_0	ANALOG[53]				efrom_fsource_0				DS		GND	Should be tied to GND. Not pull-down
VDD_UHOST_A	XuhostDP	ANALOG[59]				XuhostDP				DS		NC	
	XuhostREXT	ANALOG[60]				XuhostREXT				DS		NC	44.2ohm/1% pull-down

IO Power Domain	Ball Name	Port	GPIO Reset value		Reset status	Func-0	Func-1	Func-2	Func-3	AU	RET @ Power down	Not Used	Circuit guide
			In/ Out	Pu/ Pd									
	XuhostDM	ANALOG[61]				XuhostDM				DS		NC	
VDD_UOTG_A	XuotgID	ANALOG[63]				XuotgID				DS		NC	
	XuotgVBUS	ANALOG[64]				XuotgVBUS				DS		NC	
	Xepllfilter												1.8nF cap

2. Ball number assignment

Table 2.1-1 S5PV210 584 Pin Assignment – Pin Number Order (1/8)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
A1	VSS	AA16	VSS_UHOST_AC	AC6	XVVD_22	AD21	XUOTGDP
A2	XMSMDATA_15	AA17	XCIDATA_7	AC7	XVVD_13	AD22	XI2C1SCL
A3	XMSMIRQN	AA18	XCICLKENB	AC8	XVVD_11	AD23	XUHOSTPWREN
A4	XMSMADVN	AA19	XCIDATA_3	AC9	XVVD_7	AD24	XEINT_28
A5	XMMC0DATA_1	AA20	XEINT_29	AC10	XADCAIN_3	AD25	XEINT_26
A6	XMMC1DATA_2	AA21	XEINT_20	AC11	XADCAIN_0	AE1	VSS
A7	XURTSN_0	AA22	XEINT_4	AC12	XADCAIN_1	AE2	XI2S0SDI
A8	XPWMTOUT_2	AA23	XEINT_21	AC13	XURXD_3	AE3	XI2S0LRCK
A9	XMMC3CLK	AA24	XEINT_12	AC14	XUTXD_2	AE4	XVSYS_OE
A10	XMMC3DATA_3	AA25	XEINT_7	AC15	XMIPIVREG_0P4V	AE5	XVVD_15
A11	XSPIMOSI_1	AB1	XPCM0FSYNC	AC16	XI2C2SDA	AE6	XVVD_10
A12	XM1DATA_31	AB2	XPCM0SIN	AC17	XUHOSTREXT	AE7	XVVD_6
A13	XM1DATA_29	AB3	XI2S1CDCLK	AC18	XUOTGVBUS	AE8	XMIPISDN3
A14	XM1DATA_26	AB4	XI2S1SDO	AC19	XUOTGDRVVBUS	AE9	XMIPISDN2
A15	XM1DQS_2	AB5	XVVD_20	AC20	XURXD_2	AE10	XMIPISDNCLK
A16	XM1SCLK	AB6	XVVD_5	AC21	XCIPCLK	AE11	XMIPISDN1
A17	XM1DATA_13	AB7	XVVD_3	AC22	XUHOSTOVERCUR	AE12	XMIPISDN0
A18	XM1DQSN_1	AB8	XVVD_2	AC23	XEINT_13	AE13	XMIPIMDP3
A19	XM1DATA_11	AB9	XVVD_1	AC24	XEINT_24	AE14	XMIPIMDP2
A20	XM1DATA_10	AB10	XVVDEN	AC25	XEINT_22	AE15	XMIPIMDPCLK

Table 2.0-1 S5PV210 584 Pin Assignment – Pin Number Order (2/8)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
A21	XM1DATA_5	AB11	XADCAIN_2	AD1	XI2S1SCLK	AE16	XMIPIMDP1
A22	XM1DQSN_0	AB12	XADCAIN_9	AD2	XI2S0SCLK	AE17	XMIPIMDP0
A23	XM1DATA_3	AB13	XUTXD_3	AD3	XI2S0SDO_0	AE18	XUOTGREXT
A24	XM1DATA_0	AB14	XCIHREF	AD4	XEFFSOURCE_0	AE19	XUHOSTDP
A25	VSS	AB15	XCIDATA_0	AD5	XVVD_18	AE20	XUSBXTO
AA1	XPCM0EXTCLK	AB16	XCIDATA_1	AD6	XVVD_14	AE21	XUOTGDM
AA2	XPCM0SCLK	AB17	XCIDATA_6	AD7	XVVD_16	AE22	XI2C2SCL
AA3	XI2S0SDO_2	AB18	XDDR2SEL	AD8	XMIPISDP3	AE23	XI2C1SDA
AA4	XMMC2CDN	AB19	XCIFIELD	AD9	XMIPISDP2	AE24	XCLKOUT
AA5	XI2S1SDI	AB20	XCIDATA_2	AD10	XMIPISDPCLK	AE25	VSS
AA6	XVVD_19	AB21	XCIDATA_4	AD11	XMIPISDP1	B1	XMSMDATA_10
AA7	XVVD_17	AB22	XEINT_25	AD12	XMIPISDP0	B2	XMSMDATA_13
AA8	XVVD_8	AB23	XEINT_31	AD13	XMIPIMDN3	B3	XMSMDATA_14
AA9	XVVD_0	AB24	XEINT_19	AD14	XMIPIMDN2	B4	XMSMWEN
AA10	XVVCLK	AB25	XEINT_14	AD15	XMIPIMDNCLK	B5	XMMC0CLK
AA11	XADCAIN_8	AC1	XPCM0SOUT	AD16	XMIPIMDN1	B6	XMMC1CLK
AA12	XADCAIN_7	AC2	XI2S1LRCK	AD17	XMIPIMDN0	B7	XSPICLK_0
AA13	XVHSYNC	AC3	XI2S0SDO_1	AD18	XUOTGID	B8	XUCTSN_1
AA14	XCIVSYNC	AC4	XI2S0CDCLK	AD19	XUHOSTDM	B9	XPWMTOUT_1
AA15	VSS_UHOST_A	AC5	XVVD_21	AD20	XUSBXTI	B10	XMMC3DATA_0

Table 2.0-2 S5PV210 584 Pin Assignment – Pin Number Order (3/8)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
B11	XSPICSN_1	D1	XMSMDATA_4	E16	XM1ADDR_14	G6	XMSMADDR_1
B12	XM1DATA_30	D2	XMSMDATA_6	E17	XM1ADDR_2	G7	VSS
B13	XM1DATA_28	D3	XMSMDATA_3	E18	XM1ADDR_8	G8	XMSMCSN
B14	XM1DATA_25	D4	XMSMDATA_9	E19	XM1ADDR_12	G9	XMSMRN
B15	XM1DQSN_2	D5	XMSMADDR_7	E20	XM1ADDR_1	G10	XURXD_1
B16	XM1NSCLK	D6	XMMC0DATA_2	E21	XM1ADDR_0	G11	VDD_EXT2
B17	XM1DATA_14	D7	XMMC1DATA_0	E22	XM2DQM_3	G12	XSPICLK_1
B18	XM1DQS_1	D8	XUTXD_0	E23	XM2DATA_23	G13	XSPIMISO_1
B19	XM1DATA_8	D9	XUCTSN_0	E24	XM2DATA_22	G14	XM1CSN_1
B20	XM1DATA_9	D10	XMMC3CMD	E25	XM2DATA_21	G15	XM1CKE_0
B21	XM1DATA_4	D11	XMMC3DATA_2	F1	XMSMADDR_10	G16	XM1CKE_1
B22	XM1DQS_0	D12	XM1DQS_3	F2	XMSMADDR_13	G17	XM1WEN
B23	XM1DATA_2	D13	XM1DATA_24	F3	XMSMDATA_0	G18	XM1CSN_0
B24	XM2DATA_31	D14	XM1DQM_2	F4	XM0ADDR_14	G19	VSS
B25	XM2DATA_29	D15	XM1DATA_18	F5	XMSMADDR_6	G20	XM2ADDR_8
C1	XMSMDATA_7	D16	XM1DATA_16	F6	XMSMADDR_8	G21	XM2CKE_1
C2	XMSMDATA_8	D17	XM1DQM_1	F7	XMMC0CDN	G22	XM2DATA_19
C3	XMSMDATA_11	D18	XM1ADDR_4	F8	XMMC1CMD	G23	XM2DATA_18
C4	XMSMDATA_12	D19	XM1ADDR_6	F9	XMMC1DATA_3	G24	XM2SCLK
C5	XMMC0DATA_0	D20	XM1ADDR_7	F10	XUTXD_1	G25	XM2NSCLK

Table 2.0-3 S5PV210 584 Pin Assignment – Pin Number Order (4/8)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
C6	XMMC0DATA_3	D21	XM1ADDR_15	F11	XI2C0SDA	H1	XMSMADDR_0
C7	XMMC1CDN	D22	XM2DATA_28	F12	XPWMTOUT_3	H2	XMSMADDR_5
C8	XURXD_0	D23	XM2DATA_26	F13	XM1DATA_22	H3	XM0ADDR_15
C9	XI2C0SCL	D24	XM2DATA_25	F14	XM1ADDR_11	H4	XM0ADDR_8
C10	XMMC3DATA_1	D25	XM2DATA_24	F15	XM1ADDR_5	H5	XM0ADDR_3
C11	XM1DQM_3	E1	XMSMDATA_2	F16	XM1ADDR_9	H6	XM0ADDR_12
C12	XM1DQSN_3	E2	XMSMDATA_1	F17	XM1CASN	H7	XMSMADDR_3
C13	XM1DATA_27	E3	XMSMDATA_5	F18	XM1ADDR_13	H19	XM2ADDR_9
C14	XM1DATA_23	E4	XMSMADDR_2	F19	XM1ADDR_10	H20	XM2ADDR_13
C15	XM1DATA_19	E5	XMSMADDR_12	F20	XM2ADDR_5	H21	XM2DQM_2
C16	XM1DATA_17	E6	XMMC0CMD	F21	XM2ADDR_4	H22	XM2ADDR_6
C17	XM1DATA_15	E7	XMMC1DATA_1	F22	XM2DATA_27	H23	XM2ADDR_11
C18	XM1DATA_12	E8	XPWMTOUT_0	F23	XM2DATA_20	H24	XM2DATA_17
C19	XM1DATA_7	E9	XSPICSN_0	F24	XM2DQS_2	H25	XM2DATA_16
C20	XM1DATA_6	E10	XURTSN_1	F25	XM2DQSN_2	J1	XM0CSN_2
C21	XM1DQM_0	E11	XMMC3CDN	G1	XMSMADDR_4	J2	XM0FWEN
C22	XM1DATA_1	E12	XM1RASN	G2	XMSMADDR_9	J3	XM0ADDR_10
C23	XM2DATA_30	E13	XM1DATA_20	G3	XMSMADDR_11	J4	XM0ADDR_2
C24	XM2DQS_3	E14	XM1DATA_21	G4	XM0ADDR_9	J5	XM0ADDR_7
C25	XM2DQSN_3	E15	XM1ADDR_3	G5	XM0ADDR_13	J6	XM0ADDR_4

Table 2.0-5 S5PV210 584 Pin Assignment – Pin Number Order (5/8)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
J7	VDD_MODEM	L1	XM0DATA_8	M20	VDD_APLL	P14	VDD_ARM
J9	XSPIMISO_0	L2	XM0DATA_9	M21	XM2DATA_8	P15	VDD_ARM
J10	VDD_EXT0	L3	XM0DATA_1	M22	XM2DATA_5	P16	VSS
J11	XSPIMOSI_0	L4	XM0DATA_10	M23	XM2DATA_7	P17	VDD_CKO
J12	VSS	L5	XM0DATA_2	M24	XM2DATA_9	P19	VSS_VPLL
J13	VDD_M1	L6	XM0FRNB_3	M25	XM2DATA_11	P20	VDD_VPLL
J14	VDD_M1	L7	XM0ADDR_1	N1	XM0DATA_4	P21	VDD_RTC
J15	VDD_M1	L9	VSS	N2	XM0DATA_5	P22	XM2WEN
J16	VDD_M1	L10	VDD_INT	N3	XM0CSN_4	P23	XM2DATA_0
J17	VDD_M2	L11	VDD_INT	N4	XM0DATA_7	P24	XM2DATA_3
J19	XM2ADDR_7	L12	VSS	N5	XM0DATA_14	P25	XM2DQM_0
J20	XM2ADDR_14	L13	VDD_ARM	N6	XM0BEN_1	R1	XHDMITXCN
J21	XM2RASN	L14	VDD_ARM	N7	XM0CSN_5	R2	XHDMITXCP
J22	XM2ADDR_12	L15	VDD_ARM	N9	XM0CSN_3	R3	XM0FRNB_0
J23	XM2CASN	L16	VSS	N10	VDD_INT	R4	XM0OEN
J24	XM2CKE_0	L17	VDD_M2	N11	VDD_INT	R5	XJTMS
J25	XM2DATA_14	L19	XM2ADDR_1	N12	VSS	R6	VDD_HDMI_PLL
K1	XM0FCLE	L20	XM2ADDR_0	N14	VDD_ARM	R7	VSS_HDMI
K2	XM0FALE	L21	XM2ADDR_2	N15	VDD_ARM	R9	VSS
K3	XM0DATA_0	L22	XM2DQM_1	N16	VDD_ARM	R10	VSS

Table 2.0-6 S5PV210 584 Pin Assignment – Pin Number Order (6/8)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
K4	XM0ADDR_5	L23	XM2DATA_10	N17	VSS	R11	VDD_INT
K5	XM0ADDR_0	L24	XM2DQS_1	N19	VSS_MPLL	R12	VDD_INT
K6	XM0ADDR_6	L25	XM2DQSN_1	N20	VDD_MPLL	R13	VDD_INT
K7	XM0ADDR_11	M1	XM0DATA_11	N21	XM2CSN_0	R14	VSS
K9	VDD_M0	M2	XM0FREN	N22	XM2DATA_6	R15	VSS
K10	VSS	M3	XM0DATA_12	N23	XM2DATA_4	R16	VSS
K11	VSS	M4	XM0DATA_3	N24	XM2DQS_0	R17	VDD_ALIVE
K12	VSS	M5	XM0DATA_13	N25	XM2DQSN_0	R19	VSS_EPLL
K13	VDD_INT	M6	XM0FRNB_1	P1	XM0DATA_6	R20	VDD_EPLL
K14	VDD_INT	M7	XM0DATA_RDN	P2	XM0DATA_15	R21	XEPLLFILTER
K15	VDD_INT	M9	VDD_M0	P3	XJDBGSEL	R22	XRTCCLKO
K16	VSS	M10	VSS	P4	XM0WEN	R23	XM2ADDR_3
K17	VDD_M2	M11	VDD_INT	P5	XJTRSTN	R24	XM2DATA_1
K19	VSS	M12	VSS	P6	VDD_HDMI	R25	XM2DATA_2
K20	XM2ADDR_15	M13	VDD_ARM	P7	VSS_HDMI_PLL	T1	XHDMITX0N
K21	XM2CSN_1	M14	VDD_ARM	P9	VDD_SYS0	T2	XHDMITX0P
K22	XM2ADDR_10	M15	VDD_ARM	P10	VSS	T3	XM0BEN_0
K23	XM2DATA_13	M16	VSS	P11	VDD_INT	T4	XM0CSN_1
K24	XM2DATA_15	M17	VDD_M2	P12	VSS	T5	XJTDI
K25	XM2DATA_12	M19	VSS_APLL	P13	VSS	T6	VSS_HDMI_OSC

Table 2.0-7 S5PV210 584 Pin Assignment – Pin Number Order (7/8)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
T7	VDD_HDMI_OSC	V1	XHDMITX2N	Y2	XHDMIXTI		
T9	VDD_EXT1	V2	XHDMITX2P	Y3	XMMC2DATA_2		
T10	VSS	V3	XM0FRNB_2	Y4	XMMC2DATA_0		
T11	VDD_INT	V4	XDACCOMP	Y5	XMMC2DATA_1		
T12	VSS	V5	XDACVREF	Y6	XMMC2CLK		
T13	VSS	V6	VSS_DAC	Y7	XVVD_23		
T14	VSS	V7	VDD_DAC	Y8	XVVD_12		
T15	VSS	V19	VDD_CAM	Y9	XVVD_4		
T16	VSS	V20	XEINT_8	Y10	XVVSYNC		
T17	VDD_KEY	V21	XEINT_18	Y11	XADCAIN_4		
T19	VDD_SYS1	V22	XEINT_9	Y12	XADCAIN_6		
T20	XNRSTOUT	V23	XOM_2	Y13	VDD_MIPI_A		
T21	XNWRESET	V24	XOM_5	Y14	VSS_UHOST_D		
T22	XOM_1	V25	XOM_4	Y15	VSS_UOTG_AC		
T23	XOM_0	W1	XHDMIREXT	Y16	VDD_UHOST_A		
T24	XRTCXTI	W2	XM0WAITN	Y17	VSS_UOTG_A		
T25	XRTCXTO	W3	XJTDO	Y18	XCIDATA_5		
U1	XHDMITX1N	W4	XMMC2DATA_3	Y19	XEINT_30		
U2	XHDMITX1P	W5	XDACIREF	Y20	XEINT_23		
U3	XM0CSN_0	W6	XMMC2CMD	Y21	XEINT_0		

Table 2.0-8 S5PV210 584 Pin Assignment – Pin Number Order (8/8)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
U4	XJTCK	W7	VSS	Y22	XEINT_27		
U5	XDACOUT	W8	XVVSYNC_LDI	Y23	XEINT_17		
U6	VSS_DAC_A	W9	XVVD_9	Y24	XEINT_10		
U7	VDD_DAC_A	W10	VDD_ADC	Y25	XEINT_3		
U9	VDD_AUD	W11	VSS_ADC				
U10	VDD_LCD	W12	XADCAIN_5				
U11	VSS_MIPI	W13	VDD_UHOST_D				
U12	VDD_MIPI_D	W14	VDD_MIPI_PLL				
U13	VDD_MIPI_D	W15	VDD_ALIVE				
U14	VSS_MIPI	W16	VDD_UOTG_A				
U15	VDD_UOTG_D	W17	VSS_UOTG_D				
U16	VDD_SYS0	W18	VDD_EXT1				
U17	VDD_SYS0	W19	VSS				
U19	VDD_AUD	W20	XEINT_15				
U20	XEINT_16	W21	XEINT_6				
U21	XOM_3	W22	XEINT_11				
U22	XPWRRGTON	W23	XEINT_2				
U23	XNRESET	W24	XEINT_5				
U24	XXTI	W25	XEINT_1				
U25	XXTO	Y1	XHDMIXTO				

3. Power

3.1. Pin Power Domain

Group	Power Ball Name	Signal Ball Name
DIGITAL IO POWER	VDD_M2	XM2ADDR[13:0],XM2BA[1:0],XM2CASN,XM2RASN, XM2WEN,XM2CKE0,XM2CKE1/ADDR14,XM2CSN[1:0], XM2DQS[3:0],XM2DQSN[3:0],XM2DM[3:0],XM2SCLK, XM2SCLKN,XM2DATA[31:0]
	VDD_M1	XM1ADDR[13:0],XM1BA[1:0],XM1CASN,XM1RASN, XM1WEN,XM1CKE0,XM1CKE1/ADDR14,XM1CSN[1:0], XM1DQS[3:0],XM1DQSN[3:0],XM1DM[3:0],XM1SCLK, XM1SCLKN,XM1DATA[31:0]
	VDD_M0	XM0ADDR_[15:0],XM0BEN_[1:0],XM0CSN_[5:0], XM0DATA_[15:0],XM0DATA_RDN,XM0FALE,XM0FCLE, XM0FREN,XM0FRNB_[3:0],XM0FWEN,XM0OEN,XM0WAITN, XM0WEN, XEFFSOURCE_0
	VDD_LCD	XVHSYNC,XVSYS_OE,XVVCLK,XVVD_[23:0],XVVDEN, XVVSYNC,XVVSYNC_LDI
	VDD_CAM	XCICLKENB,XCIDATA_[7:0],XCIFIELD,XCIHREF,XCIPCLK, XCIVSYNC
	VDD_AUD	XI2S0CDCLK,XI2S0LRCK,XI2S0SCLK,XI2S0SDI, XI2S0SDO_[2:0],XI2S1CDCLK,XI2S1LRCK,XI2S1SCLK, XI2S1SDI,XI2S1SDO,XPCM2EXTCLK,XPCM2FSYNC, XPCM2SCLK,XPCM2SIN,XPCM2SOUT,XCLKOUT
	VDD_MODEM	XMSMADDR_[13:0],XMSMADVN,XMSMCSN, XMSMDATA_[15:0],XMSMIRQN,XMSMRN,XMSMWEN
	VDD_KEY	XEINT_[31:16]
	VDD_SYS0	XXTI,XXTO,XOM_[5:0],XPWRRGTON,XNRESET,XNRSTOUT,XN WRESET,XEINT_[7:0],XUOTGDRVVBUS,XUHOSTPWREN,XUH OSTOVERCUR,XDDR2SEL,XUSBXTI,XUSBXTO,XJTRSTN,XJTM S,XJTCK,XJTDI,XJTDO,XJDBGSEL
	VDD_SYS1	XEINT_[15:8]
	VDD_EXT0	XMMC0CDN,XMMC0CLK,XMMC0CMD,XMMC0DATA_[3:0], XMMC1CDN,XMMC1CLK,XMMC1CMD,XMMC1DATA_[3:0], XSPICLK_0,XSPICSN_0,XSPIMISO_0,XSPIMOSI_0,XURXD_0, XUTXD_0,XUCTSN_0,XURTSN_0,XURXD_1,XUTXD_1, XUCTSN_1,XURTSN_1,XI2C0SDA,XI2C0SCL, XPWMTOUT_[3:0]
	VDD_EXT1	XMMC2CDN,XMMC2CLK,XMMC2CMD,XMMC2DATA_[3:0], XI2C1SCL,XI2C1SDA,XI2C2SCL,XI2C2SDA,XURXD_2,

Group	Power Ball Name	Signal Ball Name
		XUTXD_2,XURXD_3,XUTXD_3
	VDD_EXT2	XMMC3CDN,XMMC3CLK,XMMC3CMD,XMMC3DATA_[3:0], XSPICLK_1,XSPICSN_1,XSPIMISO_1,XSPIMOSI_1
	VDD_CKO	XRTCCLKO
	VDD_RTC	XRTCXTI,XRTCXTO
ANALOG POWER - should be OFF in Sleep mode	VDD_DAC	XDACCOMP,XDACIREF,XDACOUT_0,XDACVREF
	VDD_HDMI	XHDMIREXT,XHDMITX0N,XHDMITX0P,XHDMITX1N, XHDMITX1P,XHDMITX2N,XHDMITX2P,XHDMITXCN, XHDMITXCP
	VDDOSC_HDMI	XHDMIXTI,XHDMIXTO
	VDD_MIPI_D	XMIPIMDNCLK, XMIPIMDPCLK, XMIPISDNCLK, XMIPISDPCLK, XMIPIVREG_0P4V
	VDD_MIPI_A	XMIPIMDN[3:0], XMIPIMDP[3:0], XMIPISDN[3:0], XMIPISDP[3:0],
	VDD_UOTG_A	XUOTGDM,XUOTGDP,XUOTGID,XUOTGREXT,XUOTGVBUS
	VDD_UHOST_A	XUHOSTDM,XUHOSTDP,XUHOSTREXT
	VDD_ADC	XADCAIN_[9:0]

3.2. Recommend Operating Conditions

Symbol		On/Off @ Reset	On/Off @ Sleep	Min	Typ	Max	Unit
VDDALIVE		On	On	1.05	1.1	1.35	V
VDDAPLL VDDMPLL VDDEPLL VDDVPLL		On	Off	1.0	1.1	1.2	
VDDINT	800MHz	On	Off	1.15	1.2	1.35	
	1GHz			1.15	1.3	1.35	
VDDARM	800MHz	On	Off	1.15	1.2	1.35	
	1GHz			1.15	1.3	1.35	
VDD_M0		On	On	1.7	1.8/2.5/3.3	3.6	
VDD_M1		On	On	1.15	1.2/1.8	1.9	
VDD_M2		On	On	1.15	1.2/1.8	1.9	
VDD_SYS0		On	On	1.7	1.8/2.5/3.0	3.6	
VDD_SYS1		On	On	1.7	1.8/2.5/3.0	3.6	
VDD_EXT0		On	On	1.7	1.8/2.5/3.0	3.6	
VDD_EXT1		On	On	1.7	1.8/2.5/3.0	3.6	
VDD_EXT2		On	On	1.7	1.8/2.5/3.0	3.6	
VDD_CKO		On	On	1.7	2.5/3.0	3.6	
VDD_RTC		On	On	1.7	2.5/3.0	3.6	
VDD_LCD		On	On	1.7	2.5/3.0	3.6	
VDD_CAM		On	On	1.7	2.5/3.0	3.6	
VDD_AUD		On	On	1.7	2.5/3.0	3.6	
VDD_MODEM		On	On	1.7	2.5/3.0	3.6	
VDD_KEY		On	On	1.7	2.5/3.0	3.6	
VDD_ADC		On	On/Off	3.0	3.3	3.6	
VDD_DAC_A		On/Off	Off	3.0	3.3	3.6	
VDD_DAC		On/Off	Off	3.0	3.3	3.6	
VDD_HDMI		On/Off	Off	1.05	1.1	1.15	
VDD_HDMI_PLL		On/Off	Off	1.05	1.1	1.15	
VDD_HDMI_OSC		On/Off	Off	3.0	3.3	3.6	

Symbol	On/Off @ Reset	On/Off @ Sleep	Min	Typ	Max	Unit
VDD_MIPI_A	On/Off	Off	1.7	1.8	1.9	
VDD_MIPI_D	On/Off	Off	1.05	1.1	1.15	
VDD_MIPI_PLL	On/Off	Off	1.05	1.1	1.15	
VDD_UOTG_A	On/Off	Off	3.0	3.3	3.6	
VDDI_UOTG_D	On/Off	Off	1.05	1.1	1.15	
VDD_UHOST_A	On/Off	Off	3.0	3.3	3.6	
VDDI_UHOST_D	On/Off	Off	1.05	1.1	1.15	
Operating Temperature TA			Industrial	-40 to 85		°C
Operating Temperature TA			Extended	-20 to 70		°C

On: Must be On the power
Off: Must be Off the power in the sleep mode
On/Off: On/Off can be selected

Note 1) VDD_M1/M2 power depends on MCP voltage..

3.3. Circuit design without level shifter

Power / IP	VDD_EXT0	VDD_EXT1	VDD_EXT2
SD/MMC	MMC0, MMC1	MMC2	MMC3
SPI	SPI0	SPI1	SPI1
Uart	UART0, UART1	UART2, UART3	
I2C	I2C0	I2C1, I2C2	

MMC 4channel, SPI 2channel, Uart 4channel and I2C 3channel has different Power domains

Ex) 2 MMC channel , 2Uart channel ¸1 SPI channel, 1 I2C channel : 1.8V,

2MMC channel, 2Uart channel, 1 SPI channel, 2 I2C channel : 3.0V

=> VDD_EXT0: 1.8V MMC0,1(2channel), SPI0(1channel), Uart0.1(2channel), I2C0 (1channel)

VDD_EXT1: 3.0V MMC2(1channel), Uart2,3 (2channel), I2C1, 2(2channel)

VDD_EXT2: 3.0V MMC3(1channel), SPI1(1channel)

Ex) 4 MMC channel , 4Uart channel ¸2 SPI channel, 3 I2C channel : 3.0V,

=> VDD_EXT0, VDD_EXT1, VDD_EXT2 : 3.0V

3.4. Power On/Off Sequence

Power On sequence

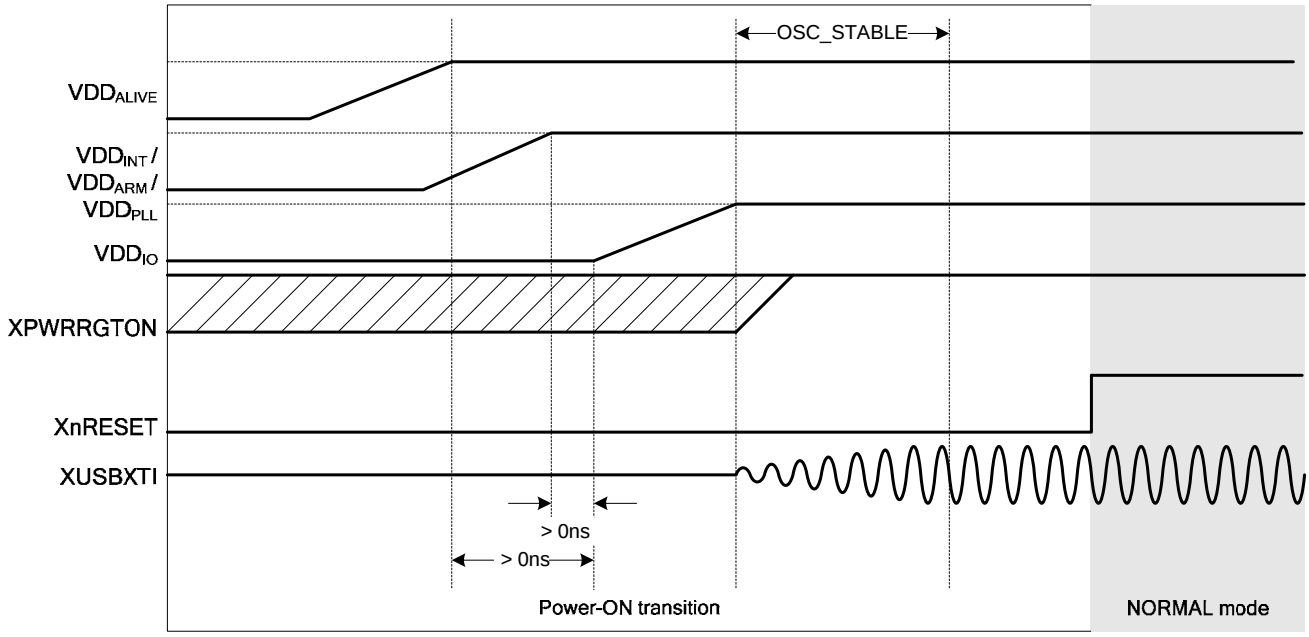


Figure 3-1) Power on sequence

Note) 1. OSC's frequency should be meet the specification which is 24Mhz

Power Off Sequence

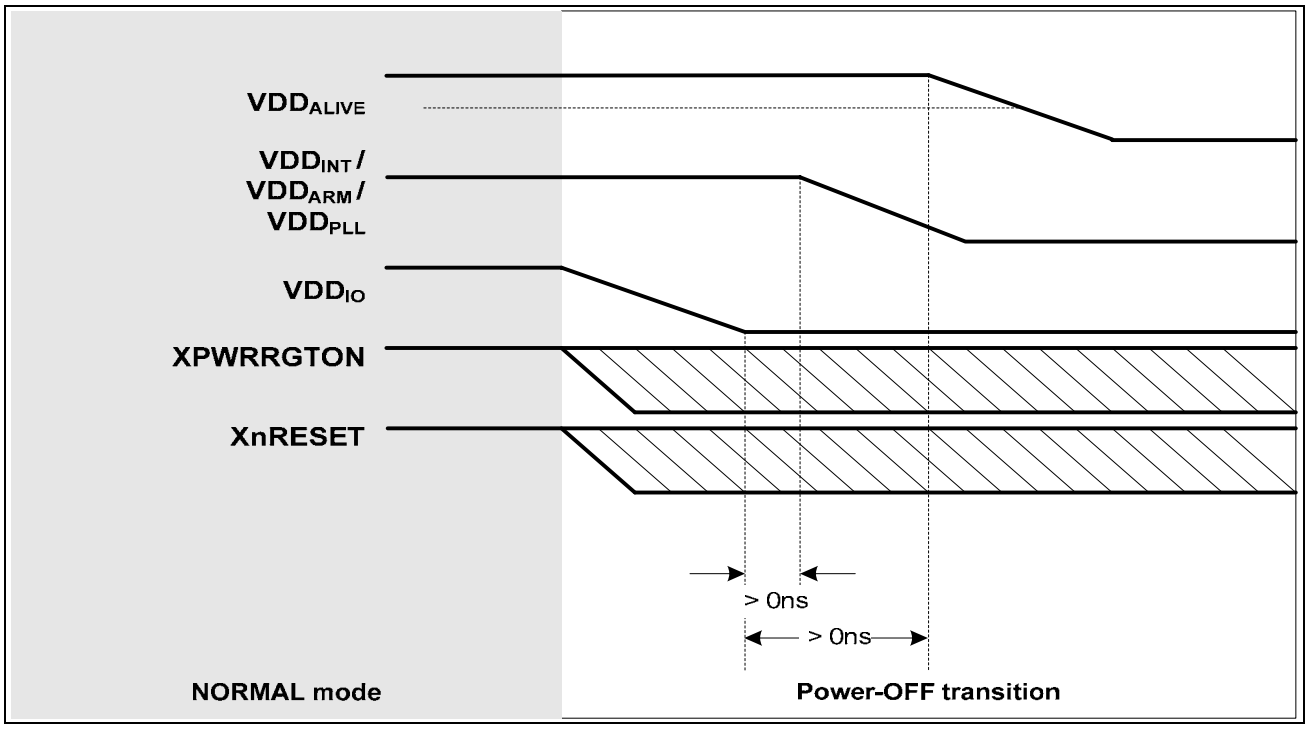


Figure 3-2) Power off sequence

3.5. Pin configuration guide in Sleep mode

Pin Condition			Configuration
No connected pin			Input with internal Pull-up/down resistor Enable
GPIO	**Input Pin**	If External Device doesn't drive 'High' or 'Low' level	Input with internal Pull-up/down Enable resistor or Output Low
		If External Device drive 'High' or 'Low' level	Input with internal Pull-up/down resistor Disable
	Output pin	If External Device's Power is Off	Output Low
		If External Device's Power is On	High or Low (It depends on External device's status)
Memory I/O (DRAM)	**I/O pin**	XMDATA, XM(n)DQS	Input pull-down or Output low controlled by LPCON
	Output pin	XMNCS, XMRAS, XMCAS, XMWE, XMCKE, XM(n)SCLK, XMADDR, XMDQM	Previous state

Retention IO

S5PV210 has a lot of retention I/O that is remaining data during the Power down mode
(deep-stop(top off), deep-idle(top off), sleep mode)
Alive block GPIO (GPH0, GPH1,GPH 2, GPH3) is not retention I/O
After wake up from power down mode, you should first set GPIO configuration as the same ones before those power down mode and then you should set ENABLE_GPIO, ENABLE_MMC_IO, and ENABLE_UART_IO bits to '1' so that normal I/O pad can be used
When wakeup from power down mode, the status of GPIO is kept. but M0 port status can be changed to reset value.
Before design circuits, you should check that the external device can be affected by changing status when wakeup.

For example)
You use Xm0ADDR[15] as output signal and connect to reset of external device(reset is active low).
When wakeup from power down mode, this pin can be changed 'high' to 'low' because the reset status of use Xm0ADDR[15] is output low

CAUTION)
- M0 Port can be changed to reset value when wakeup from power down mode
- In case of MMC booting mode, MMC signals can be changed to reset value when wakeup from power down mode .

4. SYSCON

4.1. Signal Description

- JTAG (Dedicated signal)

Ball Name	I/O	Description
XJTRSTN	I	XjTRSTn (TAP Controller Reset) resets the TAP controller at start.
XJTMS	I	XjTMS (TAP Controller Mode Select) controls the sequence of the TAP controller's states.
XJTCK	I	XjTCK (TAP Controller Clock) provides the clock input for the JTAG logic.
XJTDI	I	XjTDI (TAP Controller Data Input) is the serial input for test instructions and data.
XJTDO	O	XjTDO (TAP Controller Data Output) is the serial output for test instructions and data.
XJDBGSEL	I	JTAG selection. 0: Cortex A8 Core JTAG, 1: Peripherals JTAG

Note) JTAG signals don't need external pull-up/down registers. Because C110 has internal pull-up/down registers for JTAG signal.

- RESET / ETC (Dedicated signal)

Ball Name	I/O	Description
XOM_0 ~ XOM_5	I	Operating Mode control signals (6bit)
XDDR2SEL	I	Selection DDR type (LPDDR1/2 or DDR2)
XPWRRGTON	O	Power Regulator enable
XNRESET	I	System Reset
XCLKOUT	O	Clock out signal
XNRSTOUT	O	For External device reset control
XNWRESET	I	System Warm Reset.
XRTCCLKO	O	RTC Clock out
Xepllfilter		1.8nF capacitance for EPLL Filter

- **Clock (Dedicated signal)**

Ball Name	I/O	Description
XRTCXTI	I	32.768 KHz crystal input for RTC
XRTCXTO	O	32.768 KHz crystal output for RTC
XXTI	I	Crystal Input for internal osc circuit
XXTO	O	Crystal output for internal osc circuit.
XUSBXTI	I	Crystal Input for internal USB circuit
XUSBXTO	O	Crystal output for internal USB circuit
XHDMIXTI	I	Crystal Input for internal HDMI circuit
XHDMIXTO	O	Crystal output for internal HDMI circuit

- **E-fuse (Dedicated signal)**

Ball Name	I/O	Description
XEFFSOURCE_0	I	Power PAD for efuse ROM's FSOURCE. Should be tied to GND

4.2. Booting Option

OM[5:0] pin should be tied with VDDSYS or GND, directly. It is aimed for minimize leakage current when entering the sleep mode. But if you have to get an option, you should add a pull-up and pull-down resistor with 100K ohms over.

OM[5]	OM[4]	OM[3]	OM[2]	OM[1]	OM[0]	OM[5]	OM[4]	OM[3] OM[2] OM[1]	OM[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	Boot Mode	I-ROM	eSSD	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			Nand 2KB, 5cycle (Nand 8bit ECC)	X-TAL
					1'b1				X-TAL(USB)
			1'b1	1'b0	1'b0			Nand 4KB, 5cycle (Nand 8bit ECC)	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			Nand 4KB, 5cycle (Nand 16bit ECC)	X-TAL
					1'b1				X-TAL(USB)
		1'b1	1'b0	1'b0	1'b0			OnenandMux	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			OnenandDemux	X-TAL
					1'b1				X-TAL(USB)
			1'b1	1'b0	1'b0			SD/MMC	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			eMMC(4-bit)	X-TAL
					1'b1				X-TAL(USB)
	1'b1	1'b0	1'b0	1'b1	1'b0			Reserved	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			Nand 2KB, 4cycle (Nand 8bit ECC)	X-TAL
					1'b1				X-TAL(USB)
			1'b1	1'b0	1'b0			iROM NOR boot	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			eMMC(8-bit)	X-TAL
					1'b1				X-TAL(USB)
1'b1	1'b0	1'b0	1'b0	1'b0	1'b0		I-ROM **First boot UART ->USB**	eSSD	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			Nand 2KB, 5cycle	X-TAL
					1'b1				X-TAL(USB)
			1'b1	1'b0	1'b0			Nand 4KB, 5cycle	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			Nand 16bit ECC (Nand 4KB, 5cycle)	X-TAL
					1'b1				X-TAL(USB)
		1'b1	1'b0	1'b0	1'b0			OnenandMux(Audi)	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			OnenandDemux(Audi)	X-TAL
					1'b1				X-TAL(USB)
			1'b1	1'b0	1'b0			SD/MMC	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			eMMC(4-bit)	X-TAL
					1'b1				X-TAL(USB)

Note) If OM[5] is set to 1, It is used for debug mode that UART boot is first and USB boot is second. UART boot has some kind of error case. In case of UART error, the iROM boot sequence moves to second USB boot. USB boot also has some kind of error case like UART. If USB boot is fail, boot sequence move to main memory boot.
Please refer to iROM application note which is more detail about error case.

4.3. Feature of the IROM Boot mode

- Overview

C110 iROM boot has two step boot mode. First is a normal memory boot and second is SDMMC CH2 boot. (OneNand, Nand, SDMMC_CH0 these kinds of memories are used for first boot.)
If first boot is failed, boot sequence moves to SDMMC CH2. The first boot fail cases are checksum Error and SDMMC init error etc, Refer to iROM application note.

1. OneNAND :

- Xm0CSn4/NFCSn2/ONANDXL_CSn0 signal should be used for boot

2. NAND :

- Using S/W 8bit ECC at boot page

- S5PV210 supports 16bit ECC in case of 4KB, 5cycle Nand type,.

- Xm0CSn2/NFCSn0 signal should be used for boot

3. SD/MMC and eMMC :

- SDMMC CH0 is used for first 4bit boot.

- SDMMC CH2 is used for second boot

4. eMMC boot :

- SD/MMC CH0 is used for eMMC boot(4/8 bit). Bus width is controlled by OM setting

5. UART boot :

- UART CH2 is used for UART boot and Debug message

Note) OM[4:0] signal don't need a pull-up/down register. But OM[5] signal needs a pull-down register. This register intends to change a boot mode between Normal storage and UART/USB boot.

4.4. Clock

4.4.1. Input Clock

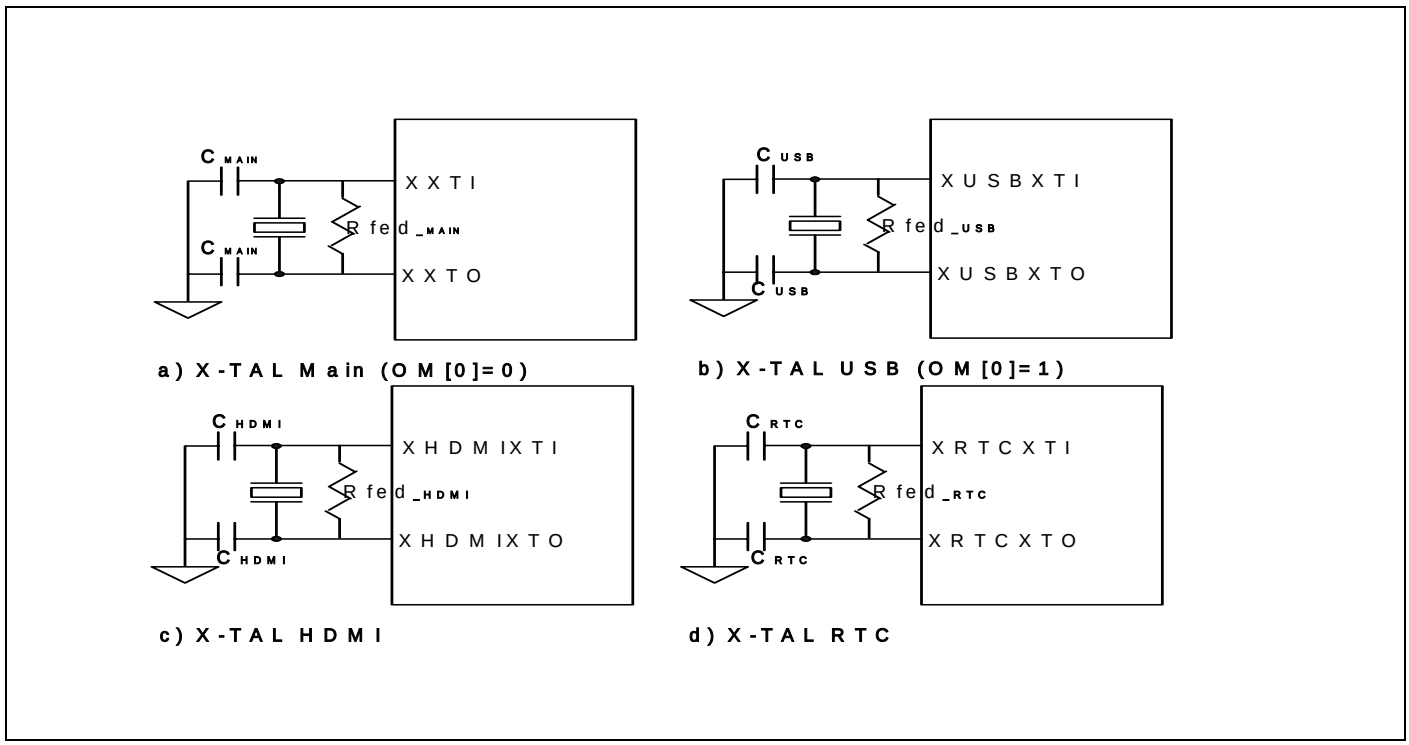
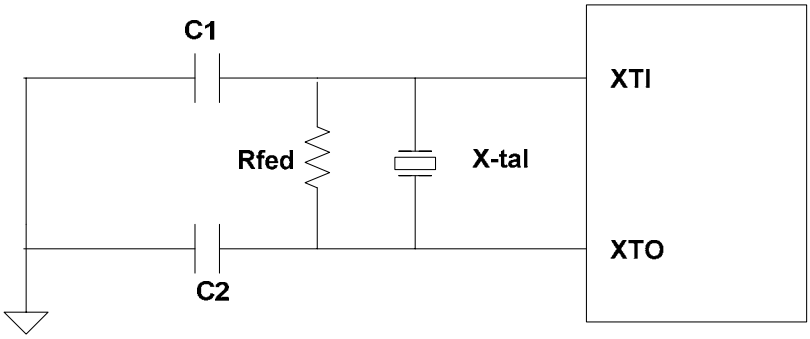


Figure 4-1) Input Clock Example

External capacitance used for X-tal	C_{MAIN}	Depends on Crystal's load capacitance(CL)
	C_{USB}	Depends on Crystal's load capacitance(CL)
	C_{HDMI}	Depends on Crystal's load capacitance(CL)
	C_{RTC}	Depends on Crystal's load capacitance(CL)
Feedback resistor between XTI with XTO	Rfed $_{MAIN}$	5M Ohm
	Rfed $_{USB}$	5M Ohm
	Rfed $_{HDMI}$	5M Ohm
	Rfed $_{RTC}$	10M Ohm
Crystal requirement for X-tal main,usb,hdmi		ESR: 60ohm max.
		Shunt capacitance: 7pF max.
		Frequence Torelance: ±50ppm
		Aging: ±5.0ppm/year max.
Crystal requirement for X-tal rtc		ESR: 80Kohm max.
		Shunt capacitance: 2pF max.
		Frequence Torelance: ±20ppm

		Aging: ±3.0ppm/year max.

Note) External capacitance calculation



External capacitor C1,2 can be calculated by following equation.

CL { (C1 + C_{IC_IN}) (C2 + C_{IC_OUT}) / (C_{IC_IN} + C1 + C2 + C_{IC_OUT}) } + pcb strays (assumed to **1~3pF)**

i) Load capacitance (CL) is specified when ordering crystal.

ii) Pin capacitance

Pin capacitance for X-tal main,usb,hdmi	C_{IC_IN}	1.8 pF
	C_{IC_OUT}	2.5 pF
Pin capacitance for X-tal rtc	C_{IC_IN}	1.2 pF
	C_{IC_OUT}	2.5 pF

EX) If Crystal has CL=14pF , then C1,C2 are around 22pF.

5. MEMORY SUBSYSTEM

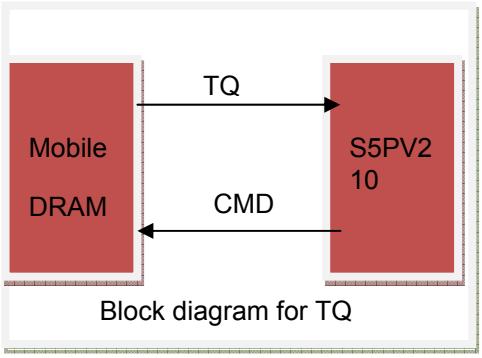
5.1. Signal Description

Signal	I/O	Description
XDDR2SEL	I	Memory Type Selection (0; LPDDR1, 1: DDR2, LPDDR2)
Xm1SCLK, Xm2SCLK	O	Memory Clock
Xm1nSCLK, Xm2nSCLK	O	Memory Negative Clock
Xm1RASn, Xm2RASn	O	Row Address Selection
Xm1CASn, Xm2CASn	O	Column Address Selection
Xm1WEn, Xm2WEn	O	Write Enable
Xm1DATA[31:0], Xm2DATA[31:0]	I/O	Memory Data Bus
Xm1DQM[3:0], Xm2DQM[3:0]	O	Write Masking Per Byte
Xm1DQS[3:0], Xm2DQS[3:0]	I/O	Data Strobe Signal Per Byte
Xm1DQSn[3:0], Xm2DQSn[3:0]	I/O	Data Strobe Negative Signal Per Byte
ADCT[18:0](Address & Control), CKE	O	Memory Address, Bank Address, CS, CKE signals

5.2. TQ : Temperature Indicator

Samsung mDDR includes the enhanced feature, Temperature Indicator (TQ), which informs MDRAM's internal temperature of controller, in order to notice that DRAM inside temperature become higher than 85'C which is the highest temperature guaranteed normally in the specification. In over 85'C, DRAM refresh cycle is derated according as the temperature goes up, controllers need to adjust auto-refresh cycle based on MDRAM temperature. Generally, it is well known that the auto-refresh cycle of DRAM tends to be half every 10'C up over 85'C. The guidance for auto-refresh cycle over 85'C is provided by specification.

Temp	Auto-Refresh cycle
-25 ~ 85C	7.8us
85 ~ 95 C	3.9us



Block diagram for TQ

5.3. PCB LAYOUT GUIDELINES FOR MEMORY

Power and ground design guide

General design rule is applied on this case.

I. Ground layer has to be placed adjacent to signal layer for current return path.

II. Ground plane has not to be split.

III. Connection of ground pins

a) Connect to ground plane through ground via as short as possible.

b) Connect ground pad of bypass capacitor to ground plane through ground via as short as possible.

c) Join together ground pins adjacent each other for making lower impedance.

IV. Connection of power pin

a) Place bypass capacitor near power pin as short as possible.

b) Connect power pad of bypass capacitor to power plane through power via as short as possible.

c) Pay attention whether power via makes ground plane split or not.

The value of bypass capacitor is determined by considering impedance profile of power plane and operating frequency. And the number of capacitors is as large as possible considering of PCB space.

Trace routing guide

I. DQ, DQM, DQS signal

Signals in same group have pattern length matched within 1.5mm for equalizing timing skew. If signals in same group have to be routed on different layer, impedance of the layer must be considered.

Data Group	Mask Signal	Clock
DQ [7:0]	DQM0	DQS0
DQ [15:8]	DQM1	DQS1
DQ[23:16]	DQM2	DQS2
DQ[31:24]	DQM3	DQS3

a) DQS0 & DATA[7:0], DQM0 Skew: -/+ 50ps (Target length: -/+ 5.0mm)

b) DQS1 & DATA[15:8], DQM0 Skew: -/+ 50ps (Target length: -/+ 5.0mm)

c) DQS2 & DATA[23:16], DQM0 Skew: -/+ 50ps (Target length: -/+ 5.0mm)

d) DQS3 & DATA[31:24], DQM0 Skew: -/+ 50ps (Target length: -/+ 5.0mm)

II. CSn, CKE, ADDR[13:0], BA[1:0], RASn, CASn, WEn, AP signal

a) SCLK(n) & ADDR[15:0], CASn, RASn, CKE[1:0], WEn Skew: -/+ 100ps (Target length: -/+ 10mm).

b) T-branch topology is recommended for Command, Address and Control net.(CKE[1:0], CSn[1:0], ADDR[15:0], RASn, CASn, WEn)

c) Do not route near high speed signals (SCLK, SCLKn, DQS(n)[3:0] and DATA net) or have enough spacing over 3*WIDTH.

d) Direct connect GATEI (pin B10) to GATEO (pin C10).

III. SCLK, SCLKn signal

a) Star topology is recommenced.

b) Recommended differential impedance is 100 ohm.

c)SCLK & SCLKn Skew: -/+ 10ps (Target length: -/+ 1.0mm).

d) SCLK(n) & DQS[3:0] Skew: -/+ 100ps (Target length: -/+ 10mm).IV. Others

6. SROM Controller

6.1. Signal Description

Signal	I/O	Description
SROM_CSn[5:0]	O	SROM Chip select Note) Bank0 supports only 16bit data bus width.
EBI_OEn	O	Memory Port 0 SROM / OneNAND Output Enable
EBI_WEn	O	Memory Port 0 SROM / OneNAND Write Enable
EBI_BEn[1:0]	O	Memory Port 0 SROM Byte Enable
SROM_WAITn	I	Memory Port 0 SROM nWait
EBI_DATA_RDn	O	Memory Port 0 SROM/OneNAND/CF If data is output, this signal goes to High. If data is input, this signal goes to Low.
EBI_ADDR[15:0]	O	Memory port 0 Address bus
EBI_DATA[15:0]	IO	Memory port 0 Data bus

			SRAM/ROM	S5PV210
Addr. connection	8bit data bus		A0	**Xm0ADDR0**
	16bit data bus	Half-word base(AddrMode =0)(default)	A0	**Xm0ADDR0**
		Byte base(AddrMode =1)	A0	**Xm0ADDR1**

Note. 1) SROM_BW [AddrMode] : Register for Address base of each memory bank
2) Bank0 supports only 16bit data bus width.

6.2. SRAM/ROM Interface Examples

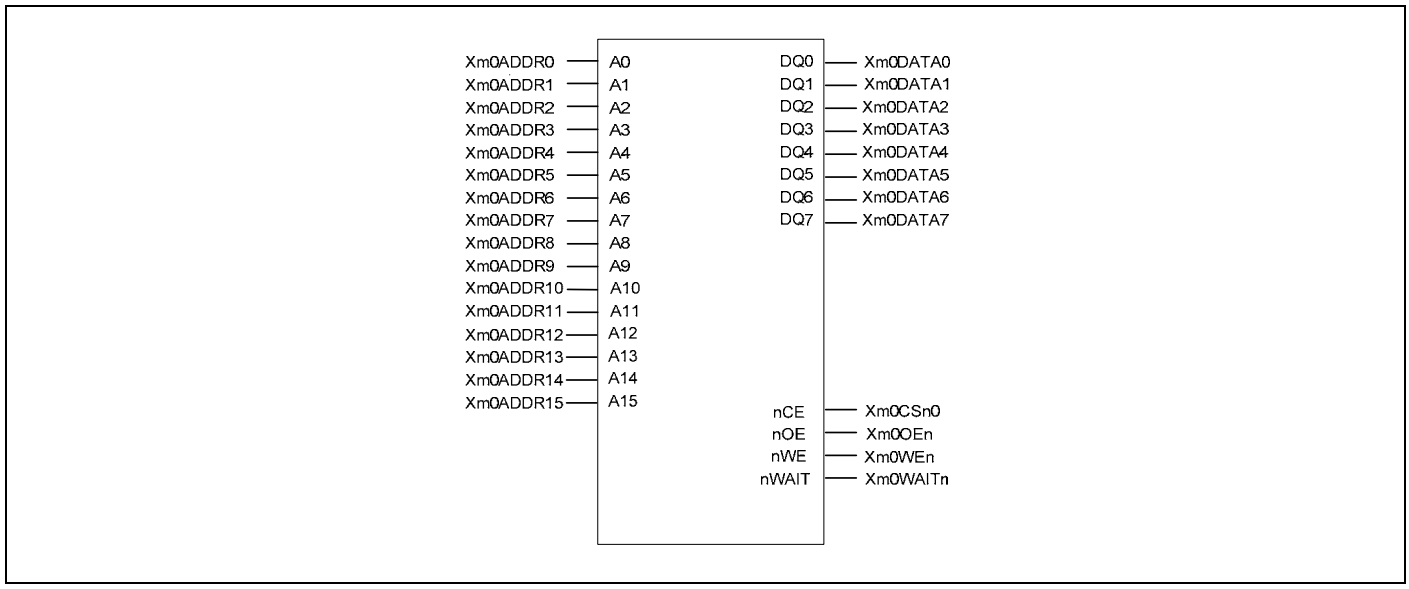


Figure 6-1) Memory Interface with 8-bit SRAM

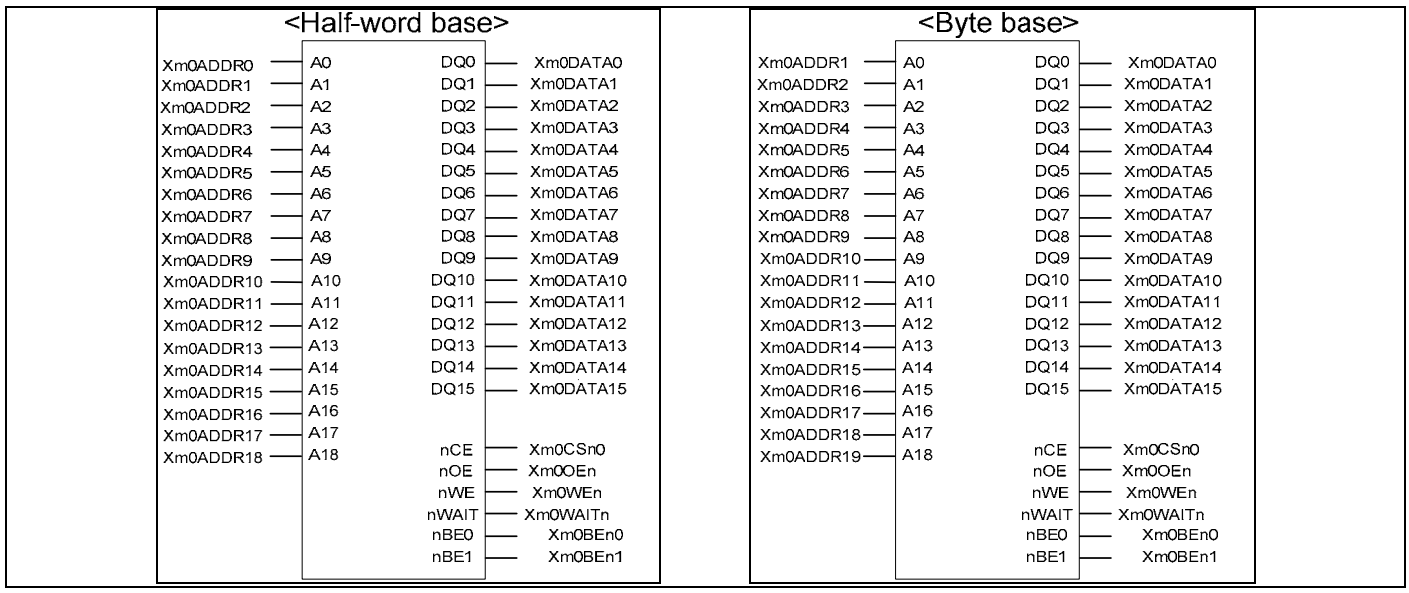


Figure 6-2) Memory Interface with 16-bit SRAM

Note. 1) Xm0ADDR[16:22] are muxed with other functions. And Xm0ADDR[16:22] are not released retention automatically like Xm0ADDR[0:15].
2) Address space : Up to 16MB per Bank

7. OneNAND Controller

Overview

S5PV210 supports external 16-bit bus for OneNAND and Flex-OneNAND memory devices. The OneNAND controller supports asynchronous and synchronous read/write bus operations. It also integrates its own dedicated DMA engine and microsequencer to accelerate the OneNAND memory device operation.

7.1. Signal Description

Signal	I/O	Description	Comment
Xm0ADDR[15:0]	IO	Xm0ADDR[15:0] (ADDR Bus) outputs address during memory read/write address phase, inputs data during memory read data phase and outputs data during memory write data phase.	
Xm0DATA[15:0]	IO	Xm0DATA[15:0] (Data Bus) outputs address during memory read/write address phase, inputs data during memory read data phase and outputs data during memory write data phase.	
ONANDXL_CSn[1:0]	O	ONANDXL_CSn[0:1] (Chip Select) are activated when the address of a memory is within the address region of each bank. ONANDXL_CSn[0:1] can be assigned to either SROMC or OneNAND controller by System Controller SFR setting. Active LOW.	ONANDXL_CSn[0] should be connected to OneNand device externally.
Xm0WEn	O	Xm0WEn (Write Enable) indicates that the current bus cycle is a write cycle. Active LOW.	
Xm0OEn	O	Xm0OEn (Output Enable) indicates that the current bus cycle is a read cycle. Active LOW.	
ONDXL_INT[0:1]	I	Interrupt inputs from OneNAND memory Bank 0, 1.	- ONDXL_INT[0] is connected to OneNand device internally. - 4.7Kohm external pull-up
ONDXL_AVD	O	Address valid output. Active LOW.	
ONDXL_RPn	O	System reset output for OneNAND memory. Active LOW.	
ONDXL_SMCLK	O	Static memory clock for synchronous static memory devices. Must be less than 83MHz.	
PmOndCEB	I	OneNand memory signal. Should be connected to c110 chip select signal externally.	

7.2. Circuit Diagram Example

S5PV210 has an external OneNAND control ports.

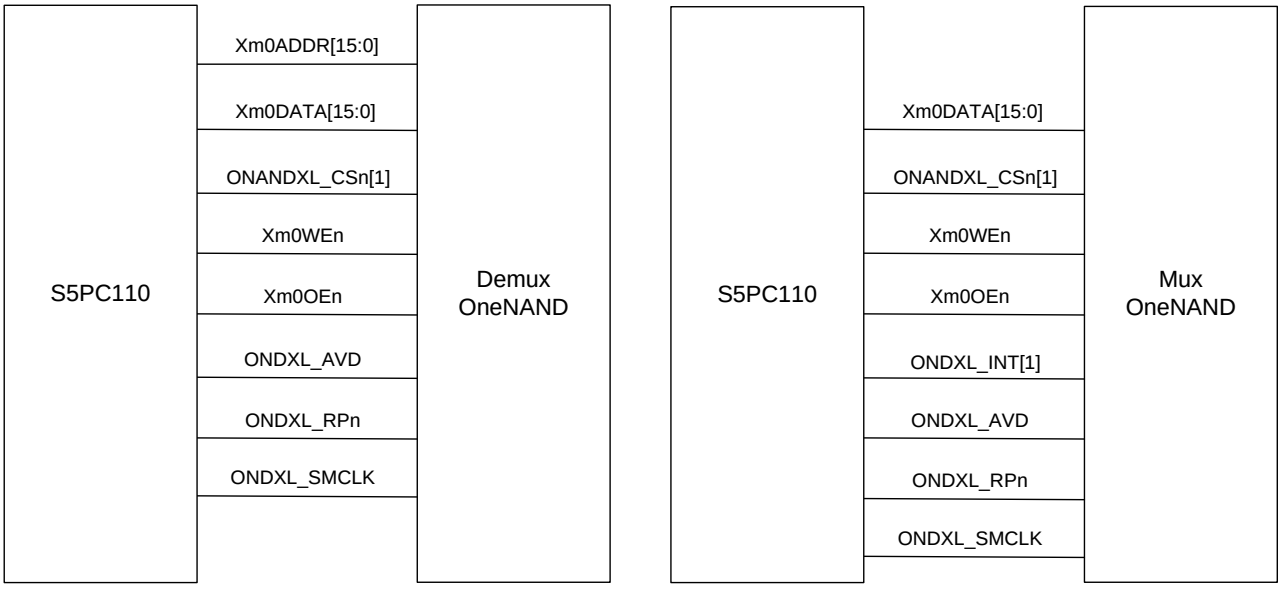


Figure 7-1) Mux & Demux OneNand connection block diagram

Note) In case of internal OneNand(POP), ONANDXL_CSn[0] and ONDXL_INT[0] signals are used for internal OneNand. If you want to use a external OneNand additionally, Only ONANDXL_CSn[1] and ONDXL_INT[1] should be used for it

Caution

- The INT pin of each OneNAND device must be pulled up by an 4.7KOhm external pull-up resistor.
- If you want to boot by OneNAND, you should use ONANDXL_CSn0, ONDXL_INT 0 .
- OneNand signal power domain belongs to VDD_M0

8. NAND Flash Controller

8.1. Signal Description

Signal	I/O	Description	Comment
NF_CLE	O	Memory Port 0 NAND Command Latch Enable	
NF_ALE	O	Memory Port 0 NAND Address Latch Enable	
NF_FWEn	O	Memory Port 0 NAND Flash Write Enable	
NF_FREn	O	Memory Port 0 NAND Flash Read Enalbe	
NF_RnB[3:0]	I	Memory Port 0 NAND Flash Ready/Busy	- NF_RnB[0] signal used for iROM boot - 4.7Kohm external pull-up
XM0DATA[15:0]	IO	Memory port 0 Data bus	
Xm0nCS[2] / NFCSn[0]	O	Memory Port 0 NAND Chip Select0	- Used for iROM boot
Xm0nCS[3] / NFCSn[1]	O	Memory Port 0 NAND Chip Select1	
Xm0nCS[4] / NFCSn[2]	O	Memory Port 0 NAND Chip Select2	
Xm0nCS[5] / NFCSn[3]	O	Memory Port 0 NAND Chip Select3	

Xm0nCS2, Xm0nCS3, Xm0nCS4, Xm0nCS5 can be used for NAND device. Some large capacity NAND flash have two or more nCE signal.

Figure 8-1) 1-CE case and 2-CE case connection

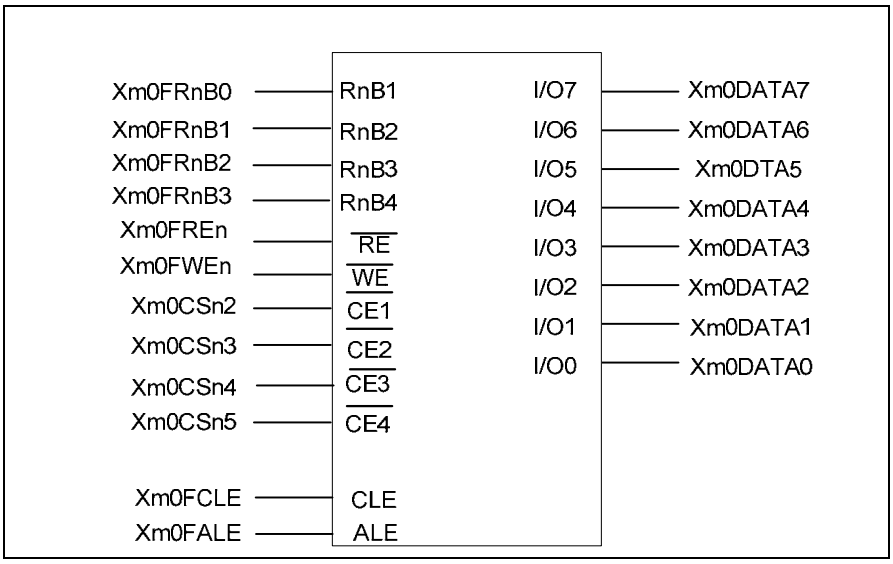


Figure 8-2) 4-CE case connection

(1) Nand signal power domain belongs to VDD_M0. Confirm the voltage level of another SRAM interface.

(2) External 4.7K pull-up resistor need to be added to RnB signal.

(3) When NAND is selected for iROM booting storage, Xm0CSn2(NFCSn0),Xm0FRnB0 should be used for NAND chip select & RnB.

9. CF Controller

9.1. CFCON feature

CF Controller support only True-IDE mode.(don't support PC card mode.) This is compatible with ATA/ATAPI-6 standard.

Cautions

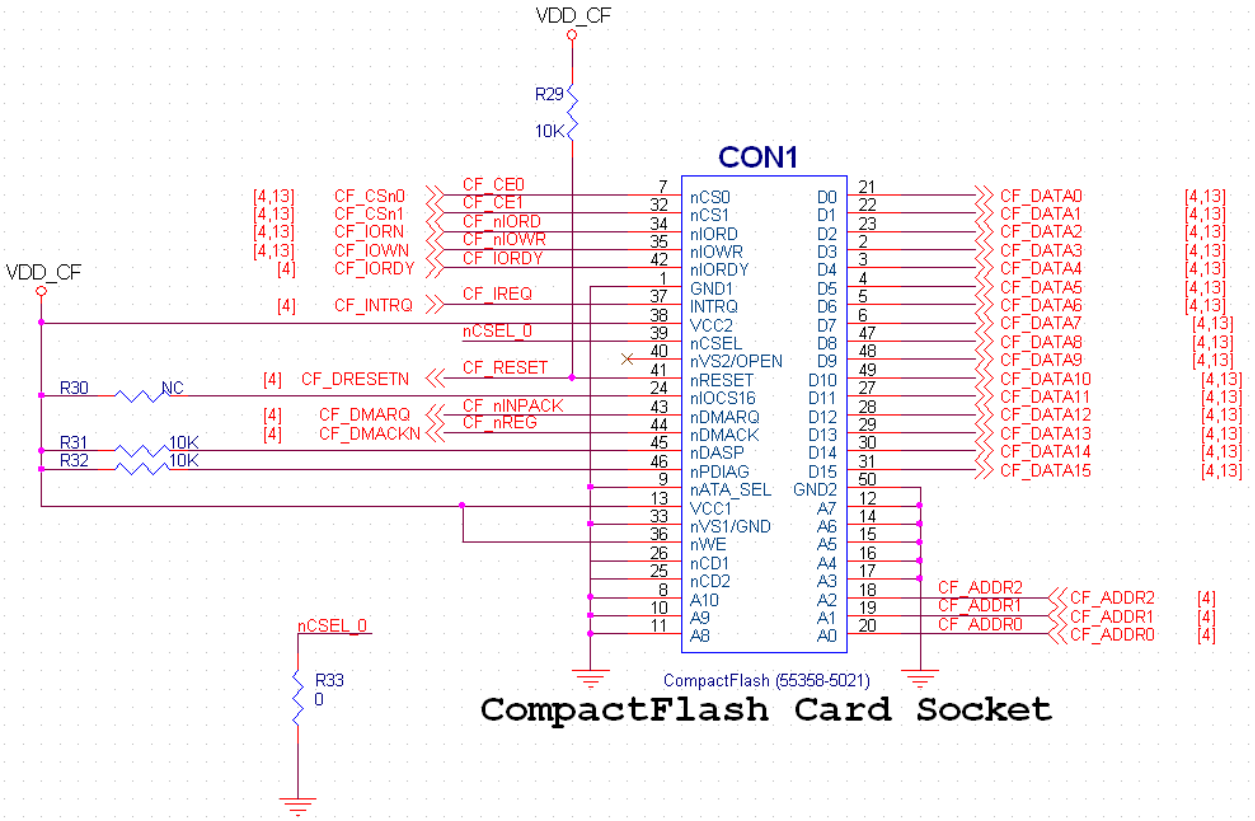
(1) Check voltage domain of CF address and data, because addr/data shared MSM interface.

(2) CF Card Vdd is controlled by GPIO. Because CF Controller don't support Hot-plug function. So if your B'd turn-on state and CF card inserted after, CF controller don't recognize. So you have to control the Vdd by GPIO (turn-off and a few time after turn-on)

9.2. Signal Description

Signal	I/O	Description
CF_ADDR[2:0]	O	CF CARD address for ATAPI
CF_IORDY	I	CF Wait signal from CF card
CF_INTRQ	I	CF Interrupt from CF card
CF_DMARQ	I	CF DMA Request
CF_DRESETN	O	CF DMA Reset
CF_DMACKN	O	CF DMA Acknowledge
CF_DATA[15:0]	IO	CF card DATA
CF_CSn[0]	O	CF chip select bank 0
CF_CSn[1]	O	CF chip select bank 1
CF_IORN	O	CF Read strobe for I/O mode
CF_IOWN	O	CF Write strobe for I/O mode

9.3. CF 1-slot operation guide



9.4. CF 2-slot operation guide

(1) S5PV210 CF Controller can use CF card and HDD together by using 2slot operation (master and slave)

(2) Follow Figure 10_2) using 2 slot Schematic

(master socket is selected by nCSEL_n pin state. Master : low-level, Slave : NC)

(ex) CON1 : Master, CON2 : Slave => nCSEL_0 = low-level, nCSEL_1 = NC

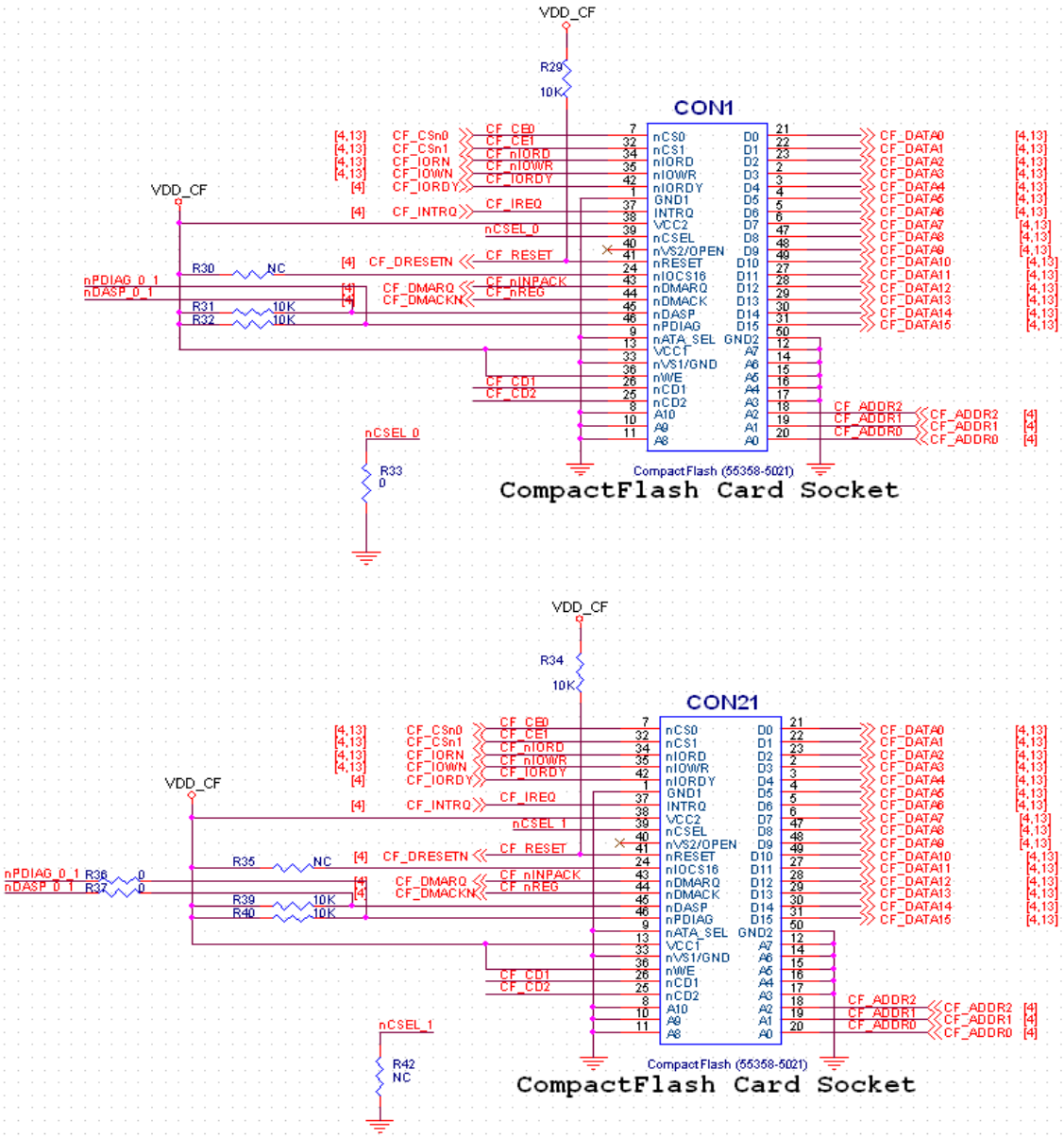


Figure 9-2) 2 Slot Operation Schematic example

10. PWM TIMER

10.1. Overview

The S5PV210 has five 32-bit timers. These timers generate internal interrupts to the ARM subsystem. In addition, Timers 0, 1, 2 and 3 include a Pulse Width Modulation (PWM) function which drives an external I/O signal. The PWM for timer 0 has an optional dead-zone generator capability to support a large current device. Timer 4 are internal timers without output pins.

10.2. Signal Description

Signal	I/O	Description
TOUT_0/1/2/3	O	PWM Timer Output
PWM_MIE	O	PWM output from MIE

PWM Usage

You can use PWM Usage at below functions.

- LCD back light control
- Vibrate motor control

11. UART

11.1. Signal descriptoin

Signal	I/O	Description	Comment
UART0/1/2/3_RXD	I	UART receives data input	CH0 FIFO Depth : 256byte CH1 FIFO Depth : 64byte CH2 FIFO Depth : 16byte CH3 FIFO Depth : 16byte - CH2 is for Low Power Audio(RP) - UART2_CTSn and UART2_RTSn signals are muxed with UART3_RXD and UART3_TXD respectively.
UART0/1/2/3_TXD	O	UART transmits data output	
UART0/1/2_CTSn	I	UART clear to send input signal	
UART0/1/2_RTSn	O	UART request to send output signal	

Note)1.Channel #0,1,2 support Auto Flow Control with RTS & CTS signal.

2. UART Ch 0, 1, 2 and 3 supports IrDA 1.0

3. UART Ch 2 is used for iROM booting message and iROM UART booting.

So, it is better to use UART ch 2 for debugging message.

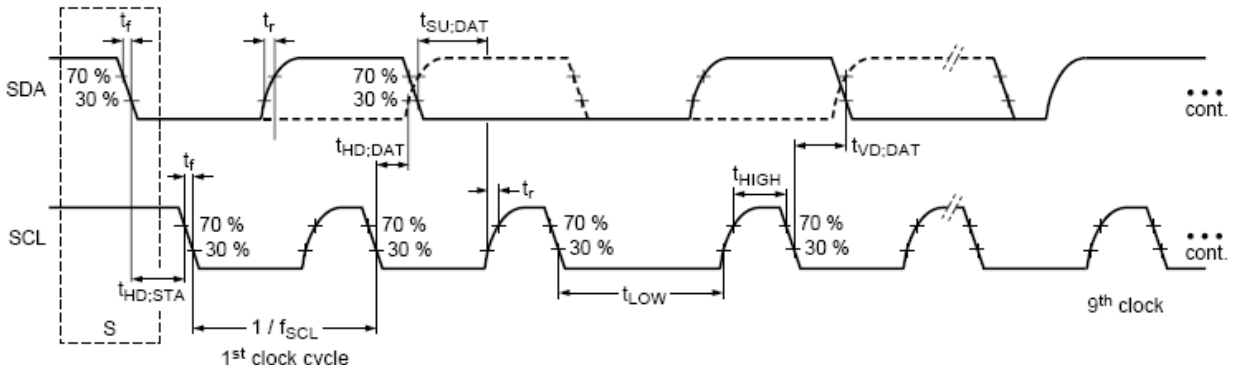
12. IIC-BUS INTERFACE

IIC Bus interface has 2 signals out which are Xi2cSCL and Xi2cSDA. Generally, Each signal need to be pulled up by 1Kohm resistor to VDD_EXT0(Xi2cSCL0, Xi2cSDA0) or VDD_EXT1(Xi2cSCL1/2, Xi2cSDA1/2) . But this resistor value should be changed by signal bus loading capacitance. S5PV210 has 3 IIC control block, Channel 1 can use internally for HDMI DDC control. Channel 0 and 2 can be used general IIC port. But When you use HDM DDC, You should not use Channel 1 in general IIC,

12.1. Pin Description

Signal	I/O	Description	Comment
Xi2cSCL0/1/2	IO	Bus clock	- 1Kohm external pull-up - Xi2C CH1 is used for HDMI
Xi2cSDA0/1/2	IO	Bus data	

12.2. Equation of the pull-up resistor value



V_{IL} = 0.3 V_{DD} V_{IH} = 0.7 V_{DD}

Figure 12-1) Definition of timing for High-Speed mode devices on the IIC –bus

1) tr (Rising time) which depends on Pull- up resistance and bus capacitance affects SCL frequency change (Higher tr makes slower SCL), especially when it is High-Speed mode (400kHz)
2) tr (Rising time) maximum is 300 ns , minimum is 20 + 0.1 Cb (bus capacitance)
3) When tr (Rising time) is 300ns, SCL might be maximum 13% slower than original setting value
4) To make real SCL within 1% variation of setting value(400kHz) , tr (Rising time) should be less than 80nsec
5) User can use this formula to determine Rp , Cb and tr
   Rp(Pull-up resistance) Max is a function of the rise time minimum (tr) and the estimated bus capacitance(Cb)

V(t1)=0.3x V_{dd}=V_{dd} (1 – e^(-t1/RC)); then t1=0.3566749xRC)

V(t2)=0.7x V_{dd}=V_{dd} (1 – e^(-t2/RC)); then t2=1.2039729xRC)

T = t2 – t1 = 0.8473 x RC

$R_{p(max)}$ = t_r / (0.8473 x C_b)

13. SPI

13.1. Signal Description

Signal	I/O	Description
SPI0/1_CLK	IO	SPI clock
SPI0/1_nSS	IO	SPI chip select
SPI0/1_MISO	IO	SPI master input / slave output line
SPI0/1_MOSI	IO	SPI master output / slave input line

13.2. EXTERNAL Loading Capacitance

S5PV210 has three SPI controllers. Both controllers should follow the external loading capacitance below.

Output capacitance must be lower than 30pF at the channel 0/1.

13.3. SPI Maximum Speed

The maximum frequency Master Tx/Master Rx/Slave Rx/Slave Tx(CPHA=0) is up to 50MHz.

The maximum frequency Slave Tx is up to 20MHz(CPHA=1).

14. USB Host

14.1. Singnal Description

Ball Name	I/O	Description
XUHOSTPWREN	O	USB HOST charge pump enable
XUHOSTOVERCUR	I	USB HOST over current flag
XUHOSTDP	IO	USB HOST Data pin DATA(+)
XUHOSTREXT	IO	USB HOST External 44.2ohm (+/- 1%) pull-down
XUHOSTDM	IO	USB HOST Data pin DATA(-)

14.2. Power Domain

VDD_UHOST_A is for USB Host Phy analog power supplied with 3.3V, and VDD_UHOST_D is for USB Host Phy digital power supplied with 1.1V.

Caution! VDD_UHOST_D must be brought up first, followed by VDD_UHOST_A, in order to limit power consumption and prevent voltage stress on the device.

14.3. Circuit Diagram Example

To minimize power consumption in USB Host block, SEC recommends that user should control powers for VDD_UHOST_A and VDD_UHOST_D.

(1) use Charge Pump Circuit or connect B'd 5V power to VBUS in order to supply VBUS to a bus-powered USB device.

(2) connect regulator's nOC in to XuhOVERCUR in order to detect over-current condition.

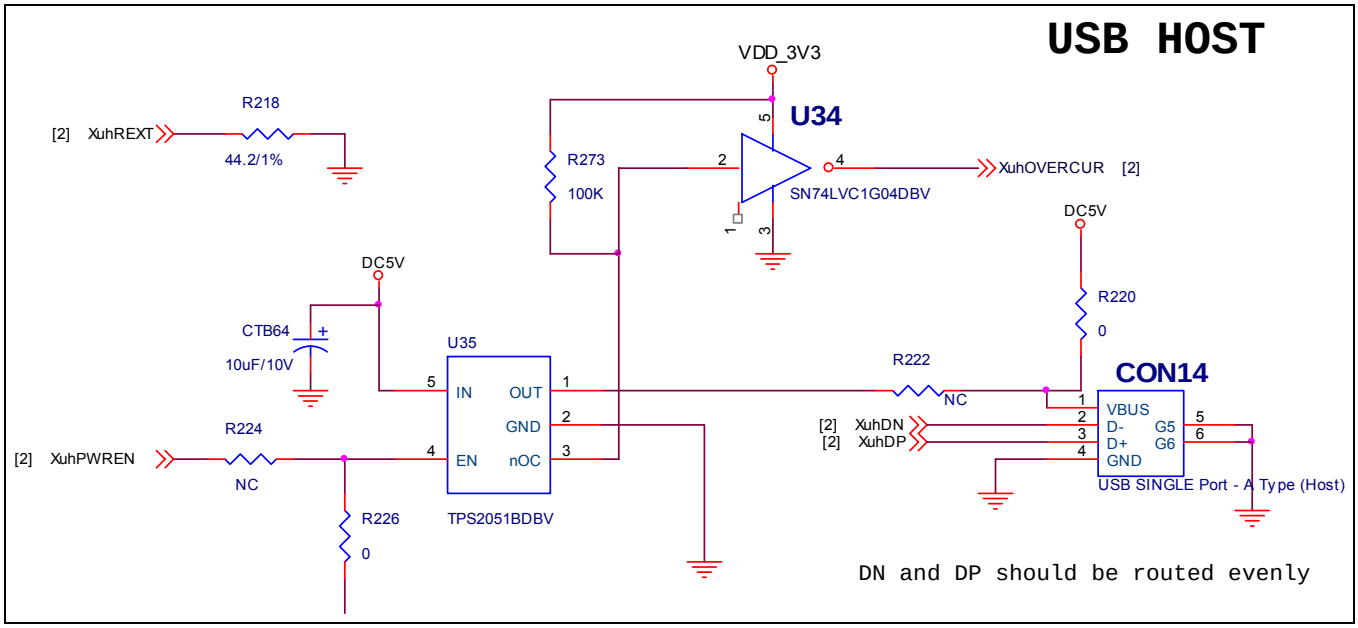


Figure 14-1) USB Host circuit example

14.4. USB SIGNAL ROUTING

Introduction

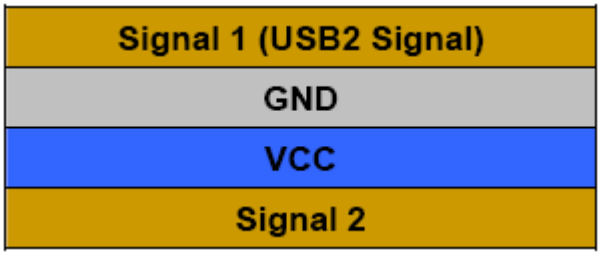
This document conducts a guide to integrate a discrete high speed usb device onto a four layer PCB. The board design guidelines handle trace separation, termination placement requirements and overall trace length guidelines

PCB layout guidelines

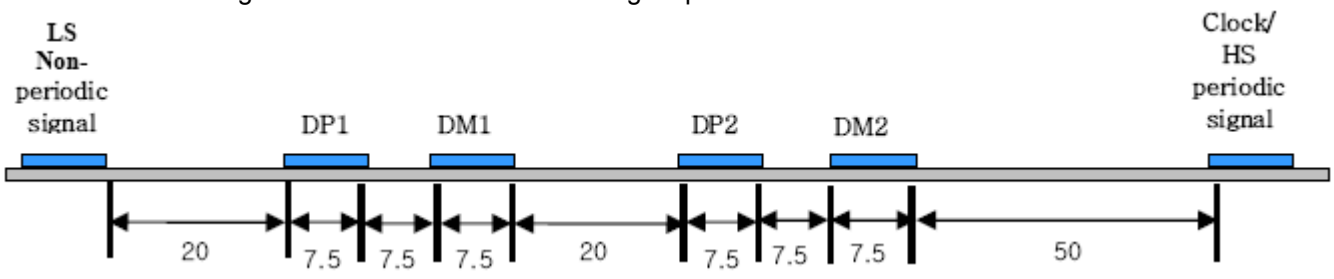
Routing and placement

When an engineer lays out a new design, the excellent signal quality and minimized EMI problem must be required. That is based on four layer board. The first layer is for signal layer. The second layer is for ground. The third layer is for power and the fourth layer is for signal layer again. We should basically consider the following instruction.

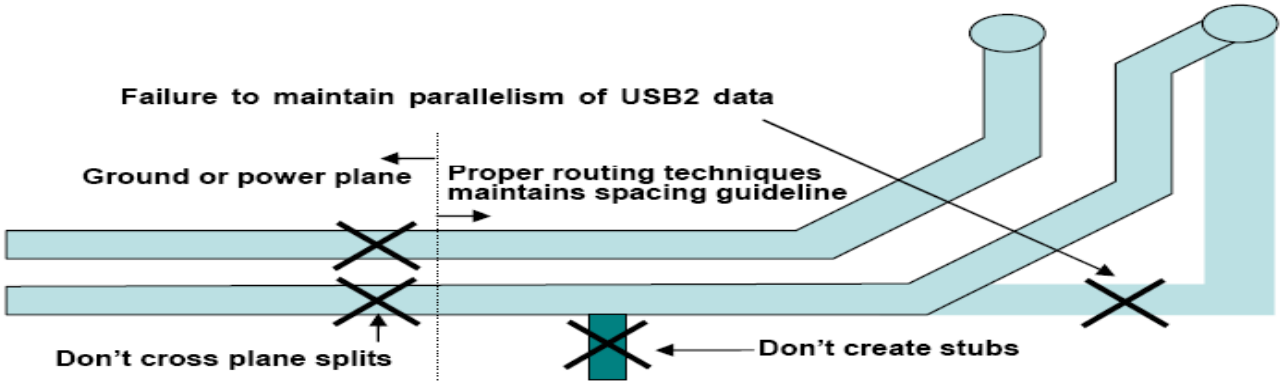
I. HS signals should be placed on top shown in the below figure



II. HS clock and HS USB different pairs should be first routed with minimum trace length.
III. Route high-speed USB signals not using vias and stubs with using two 45 degree turns or an arc instead of making a single 90 degree trun. This reduces signal reflections and impedance changes that affect signal quality.
IV. Do not route usb traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
V. Route all traces over continuous planes(VCC and GND), with no interruptions. Avoid crossing over anti-etch if at all possible.
VI. Ther parallelism between USB differential signals with the trace spacing should be maintained. The deviation should be minimized.
VII. The minimized length of high speed clock and periodic signal traces is highly recommended. The suggested spacing to clock signal is 50mils (1mils = 0.0254mm)
VIII. To prevent crosstalk, you should 20-mil minimum spacing between HS usb signal pairs. For example,
IX. Max trace length mismatch between HS usb signal pairs such as DM and DP should be under 150mils.



X. Poor routing mistake



15. USB 2.0 HS OTG

15.1. Signal Descriptoin

Ball Name	I/O	Description	Comment
XUOTGDRVVUBS	O	USB OTG charge pump enable	
XUOTGDP	IO	USB OTG Data pin DATA(+)	
XUOTGREXT	IO	USB OTG External 44.2ohm (+/- 1%) resistor connection	
XUOTGDM	IO	USB OTG Data pin DATA(-)	
XUOTGID	IO	USB OTG Mini-Receptacle Identifier	
XUOTGVBUS	IO	USB OTG Mini-Receptacle Vbus	- Available volatage level :4.0V~6.0V

15.2. Power Domain

VDD_UOTG_A_AP is for USB OTG Phy analog power supplied with 3.3V, and VDD_UOTG_D_AP is for USB OTG Phy digital power supplied with 1.1V.

Caution! VDD_UOTG_D_AP must be brought up first, followed by VDD_UOTG_A_AP, in order to limit power consumption and prevent voltage stress on the device.

Circuit Diagram Example

To minimize power consumption in USB OTG block, SEC recommends that user should control powers for VDD_UOTG_A_AP and VDD_UOTG_D_AP.

(1) use Charge Pump in order to supply VBUS to a bus-powered USB device.

To use Only Device mode but OTG mode.

(1) XusbID : leave as a no connect(Device mode)

(2) XusbDRVVBUS : leave as a no connect (The charge pump circuit should be removed)

(3) Refer to following circuit diagram about other signals.

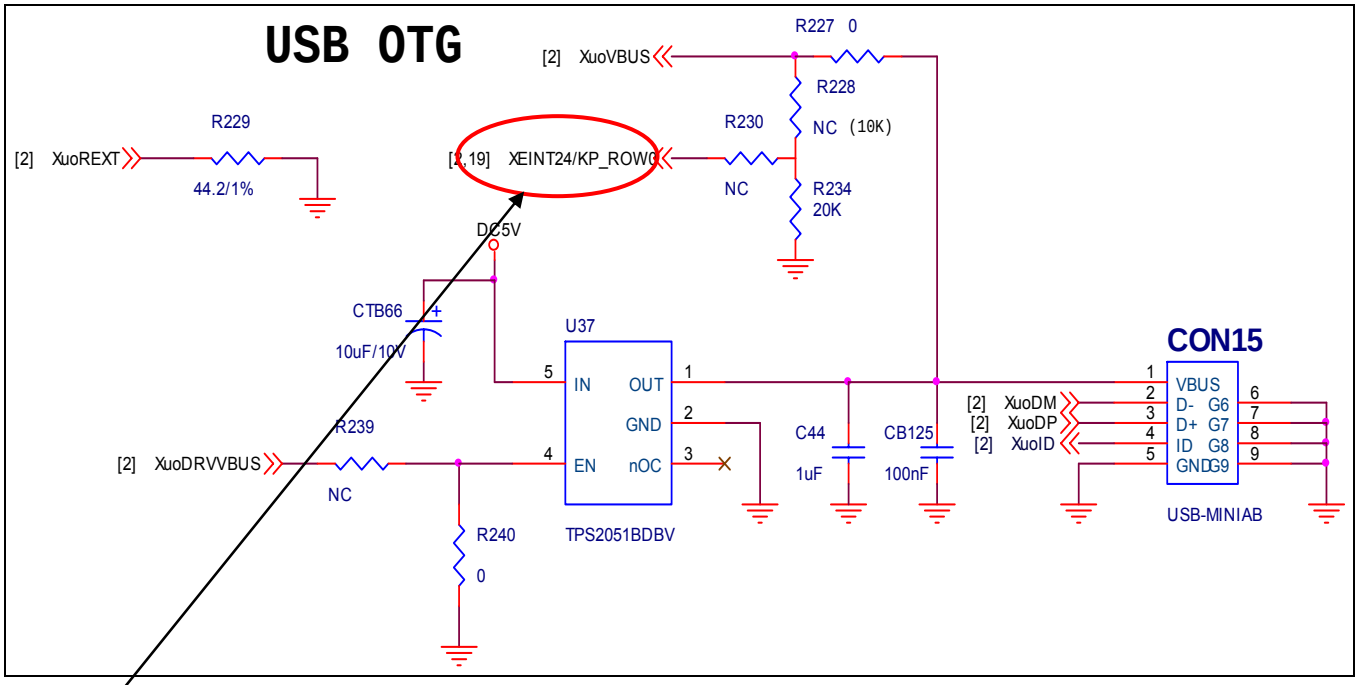


Figure 15-1) USB OTG Circuit Example

Note) In this case VBUS signal can be used for wakeup source. XEINT[31:0] signals are available.

16. MODEM INTERFACE

This specification defines the interface between the Base-band Modem and the Application Processor for the data-exchange of these two devices. For the data-exchange, the AP (Application Processor, S5PV210) has a DPSRAM(Dual Port SRAM, 16KB) buffer (on-chip) and the Modem chip can access that DPSRAM buffer using a typical asynchronous-SRAM interface.

16.1. Signal Description

Signal	I/O	Description
XmsmADDR[13:0]	I	MODEM (MSM) IF Address
XmsmDATA[15:0]	IO	MODEM (MSM) IF Data
XmsmCSn	I	MODEM (MSM) IF Chip Select
XmsmWEn	I	MODEM (MSM) IF Write enable
XmsmREn	I	MODEM (MSM) IF Read enable
XmsmIRQn	O	MODEM (MSM) IF Interrupt to MODEM
XmsmADVn	I	MODEM (MSM) IF Address Valid from MODEM Chip

16.2. Pin Connection Example

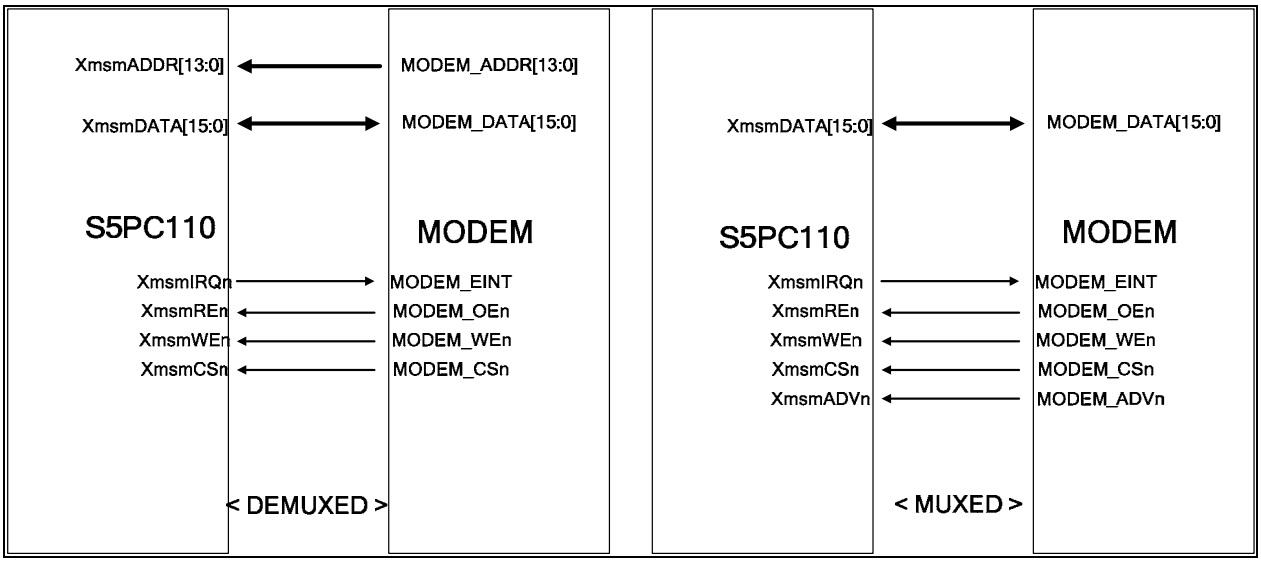


Figure 16-1) Modem I/F Pin connection example

Caution

(1) Voltage level is same between MODEM(memory bus and EXINT) and AP(MODEM I/F). Confirm the datasheet what you want to use.

(2) There is only one interrupt request pin from AP to MODEM(XmsmIRQn). Any other extra interrupt request pin doesn't needs between AP and modem because interrupt requests from modem to AP are delivered through XmsmADDR[12:0] and XmsmDATA[15:0] by writing some value to INT2AP register of DPSRAM in AP.

(3) Refer the datasheet's timing specification.

(4) Address connection between MODEM and AP follows the memory controlling policy of MODEM.

17. SD/MMC HOST CONTROLLER

S5PV210 has three slots for supporting high speed SD/MMC interface. SDMMC0 as 4-bit/8-bit MMC interface, SDMMC1 support 4-bit MMC interfaces. Every MMC controller belongs to VDD_EXT0/1/2 power.

17.1. Signal Description

Signal	I/O	Description
SD0/1/2/3_CLK	O	CLOCK (SD/SDIO/MMC card interface channel 0)
SD0/1/2/3_CMD	IO	COMMAND/RESPONSE (SD/SDIO/MMC card interface channel 0)
SD0/1/2/3_CDn	I	CARD DETECT (SD/SDIO/MMC card interface channel 0)
SD0/1/2/3_DATA[3:0]	IO	DATA[3:0] (SD/SDIO/MMC card interface channel 0)

17.2. Muxed Signal usage

	Case 1 (4 Channel Usage)	Case 2 (2 Channel Usage)
Channel 0	4-bit mode	8-bit mode
Channel 1	4-bit mode	Not available
Channel 2*	4-bit mode	8-bit mode
Channel 3*	4-bit mode	Not available

Every controller has up to 52MHz speed. So clock and data line should have same routing path.

(1) Voltage level should be the same between device and SD/MMC IO(VDD_EXT0/1/2).

Ch 0,1 belongs VDD_EXT0 power domain. Ch2 belongs VDD_EXT1. Ch3 belongs VDD_EXT2

(2) Add a 10K-external pull-up resistor to CMD line needs. And add 51K-external pull-up resistors to Data line.

(3) MMC channel 0 shares data lines with MMC channel 1 and MMC channel 2 shares data lines with MMC channel 3. So it is impossible that CH0(or CH2) 8bit and CH1(or CH3) are used at the same time.

(4) DAT[3] card detection method didn't recommend by following issues.

i) Difficult to detect when card is removed during operation.

ii) Pull-down resistor of dat3 cause different impedance between data lines.

iii) Some cards don't have enough internal pull-up resistors.

(5) SDMMC CH2 can be used for iROM second booting. So SD card slot is better to connect to CH2 for debugging.

18. TSI

18.1. Signal Description

Signal	I/O	Description
TS_CLK	I	TSI system clock
TS_SYNC	I	TSI synchronization control signal
TS_VAL	I	TSI valid signal
TS_DATA	I	TSI input data
TS_ERROR	I	TSI error indicate signal

18.2. Connection Example

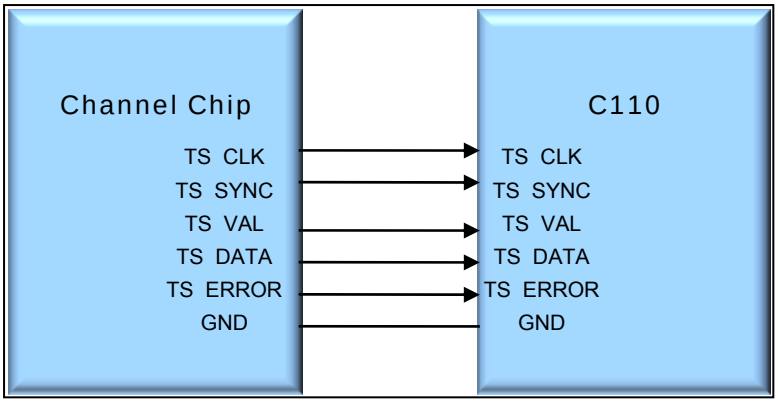


Figure 18-1) TSI Connection Example

19. DISPLAY CONTROLLER

19.1. Signal Description

Signal	I/O	Description	LCD type
LCD_HSYNC	O	Horizontal Sync Signal for RGB interfacel	RGB I/F
LCD_VSYNC	O	Vertical Sync Signal for RGB interface	
LCD_VDEN	O	Data Enable for RGB interface	
LCD_VCLK	O	Video Clock for RGB interface	
LCD_VD[23:0]	O	LCD pixel data output for RGB interface	
SYS_OE	O	Output Enable for RGB interface	
VSYNC_LDI	O	LCD i80 VSYNC Interface	CPU I/F
SYS_CS0	O	Chip select LCD0 for LCD Indirect i80 System interface	
SYS_CS1	O	Chip select LCD1 for LCD Indirect i80 System interface	
SYS_RS	O	Register/State Select Signal for LCD Indirect i80 System interface	
SYS_WE	O	Write Enable for LCD Indirect i80 System interface	
SYS_VD[23:0]	IO	Video data input/output for LCD Indirect i80 System interface	
SYS_OE	O	Output Enable for LCD Indirect i80 System interface	
VEN_HSYNC	O	Horizontal Sync Signal for 601 interface	ITU 601/656 I/F
VEN_VSYNC	O	Vertical Sync Signal for 601 interface	
VEN_HREF	O	Data Enable for 601 interface	
V601_CLK	O	Data Clock for 601 interface	
VEN_DATA[7:0]	O	YUV422 format data output for 601 interface	
V656_DATA[7:0]	O	YUV422 format data output for 656 interface	
V656_CLK	O	Data Clock for 656 interface	
VEN_FIELD	O	Field Signal for 601 interface	

19.2. VD signal connection

Ball Name	Func0		Func1		Func2	
		IO		IO		IO
XVHSYNC	LCD_HSYNC	O	SYS_CS0	O	VEN_HSYNC	O
XVVSYNC	LCD_VSYNC	O	SYS_CS1	O	VEN_VSYNC	O
XVVDEN	LCD_VDEN	O	SYS_RS	O	VEN_HREF	O
XVVCLK	LCD_VCLK	O	SYS_WE	O	V601_CLK	O
XVVD_0	LCD_VD[0]	O	SYS_VD[0]	IO	VEN_DATA[0]	O
XVVD_1	LCD_VD[1]	O	SYS_VD[1]	IO	VEN_DATA[1]	O
XVVD_2	LCD_VD[2]	O	SYS_VD[2]	IO	VEN_DATA[2]	O
XVVD_3	LCD_VD[3]	O	SYS_VD[3]	IO	VEN_DATA[3]	O
XVVD_4	LCD_VD[4]	O	SYS_VD[4]	IO	VEN_DATA[4]	O
XVVD_5	LCD_VD[5]	O	SYS_VD[5]	IO	VEN_DATA[5]	O
XVVD_6	LCD_VD[6]	O	SYS_VD[6]	IO	VEN_DATA[6]	O
XVVD_7	LCD_VD[7]	O	SYS_VD[7]	IO	VEN_DATA[7]	O
XVVD_8	LCD_VD[8]	O	SYS_VD[8]	IO	V656_DATA[0]	O
XVVD_9	LCD_VD[9]	O	SYS_VD[9]	IO	V656_DATA[1]	O
XVVD_10	LCD_VD[10]	O	SYS_VD[10]	IO	V656_DATA[2]	O
XVVD_11	LCD_VD[11]	O	SYS_VD[11]	IO	V656_DATA[3]	O
XVVD_12	LCD_VD[12]	O	SYS_VD[12]	IO	V656_DATA[4]	O
XVVD_13	LCD_VD[13]	O	SYS_VD[13]	IO	V656_DATA[5]	O
XVVD_14	LCD_VD[14]	O	SYS_VD[14]	IO	V656_DATA[6]	O
XVVD_15	LCD_VD[15]	O	SYS_VD[15]	IO	V656_DATA[7]	O
XVVD_16	LCD_VD[16]	O	SYS_VD[16]	IO		
XVVD_17	LCD_VD[17]	O	SYS_VD[17]	IO		
XVVD_18	LCD_VD[18]	O	SYS_VD[18]	IO		
XVVD_19	LCD_VD[19]	O	SYS_VD[19]	IO		
XVVD_20	LCD_VD[20]	O	SYS_VD[20]	IO		
XVVD_21	LCD_VD[21]	O	SYS_VD[21]	IO		
XVVD_22	LCD_VD[22]	O	SYS_VD[22]	IO		
XVVD_23	LCD_VD[23]	O	SYS_VD[23]	IO	V656_CLK	O
XVVSYNC_LDI	LCD_VCLK_B	O	VSYNC_LDI	O	VSYNC_LDI	O
XVSYS_OE	SYS_OE	O	SYS_OE	O	VEN_FIELD	O

19.3. VD signal connection at each bpp mode.

	Parallel RGB			Serial RGB		601
	24BPP (888)	18BPP (666)	16BPP (565)	24BPP (888)	18BPP (666)	
XVVD_23	R[7]	R[5]	R[4]	D[7]	D[5]	
XVVD_22	R[6]	R[4]	R[3]	D[6]	D[4]	
XVVD_21	R[5]	R[3]	R[2]	D[5]	D[3]	
XVVD_20	R[4]	R[2]	R[1]	D[4]	D[2]	
XVVD_19	R[3]	R[1]	R[0]	D[3]	D[1]	
XVVD_18	R[2]	R[0]	-	D[2]	D[0]	
XVVD_17	R[1]	-	-	D[1]	-	
XVVD_16	R[0]	-	-	D[0]	-	
XVVD_15	G[7]	G[5]	G[5]	-	-	
XVVD_14	G[6]	G[4]	G[4]	-	-	
XVVD_13	G[5]	G[3]	G[3]	-	-	
XVVD_12	G[4]	G[2]	G[2]	-	-	
XVVD_11	G[3]	G[1]	G[1]	-	-	
XVVD_10	G[2]	G[0]	G[0]	-	-	
XVVD_9	G[1]	-	-	-	-	
XVVD_8	G[0]	-	-	-	-	
XVVD_7	B[7]	B[5]	B[4]	-	-	VEN_DATA[7]
XVVD_6	B[6]	B[4]	B[3]	-	-	VEN_DATA[6]
XVVD_5	B[5]	B[3]	B[2]	-	-	VEN_DATA[5]
XVVD_4	B[4]	B[2]	B[1]	-	-	VEN_DATA[4]
XVVD_3	B[3]	B[1]	B[0]	-	-	VEN_DATA[3]
XVVD_2	B[2]	B[0]	-	-	-	VEN_DATA[2]
XVVD_1	B[1]	-	-	-		VEN_DATA[1]
XVVD_0	B[0]	-	-	-	-	VEN_DATA[0]

	I80 CPU I/F (Parallel)									
	16BPP(565)	18BPP(666)		18BPP(666)		24BPP (888)		18BPP(666)	16BPP(565)	
Lx_DATA16	000	001		010		011		100	101	
		1st	2nd	1st	2nd	1st	2nd		1st	2nd
XVVD_23	-	-	-	-	-	-	-	-	-	-
XVVD_22	-	-	-	-	-	-	-	-	-	-
XVVD_21	-	-	-	-	-	-	-	-	-	-
XVVD_20	-	-	-	-	-	-	-	-	-	-
XVVD_19	-	-	-	-	-	-	-	-	-	-
XVVD_18	-	-	-	-	-	-	-	-	-	-
XVVD_17	-	-	-	-	-	-	-	R[5]	-	-
XVVD_16	-	-	-	-	-	-	-	R[4]	-	-
XVVD_15	R[4]	R[5]	-	-	-	R[7]	B[7]	R[3]	-	-
XVVD_14	R[3]	R[4]	-	-	-	R[6]	B[6]	R[2]	-	-
XVVD_13	R[2]	R[3]	-	-	-	R[5]	B[5]	R[1]	-	-
XVVD_12	R[1]	R[2]	-	-	-	R[4]	B[4]	R[0]	-	-
XVVD_11	R[0]	R[1]	-	-	-	R[3]	B[3]	G[5]	-	-
XVVD_10	G[5]	R[0]	-	-	-	R[2]	B[2]	G[4]	-	-
XVVD_9	G[4]	G[5]	-	-	-	R[1]	B[1]	G[3]	-	-
XVVD_8	G[3]	G[4]	-	R[5]	G[2]	R[0]	B[0]	G[2]	-	-
XVVD_7	G[2]	G[3]	-	R[4]	G[1]	G[7]	-	G[1]	R[4]	G[2]
XVVD_6	G[1]	G[2]	-	R[3]	G[0]	G[6]	-	G[0]	R[3]	G[1]
XVVD_5	G[0]	G[1]	-	R[2]	B[5]	G[5]	-	B[5]	R[2]	G[0]
XVVD_4	B[4]	G[0]	-	R[1]	B[4]	G[4]	-	B[4]	R[1]	B[4]
XVVD_3	B[3]	B[5]	-	R[0]	B[3]	G[3]	-	B[3]	R[0]	B[3]
XVVD_2	B[2]	B[4]	-	G[5]	B[2]	G[2]	-	B[2]	G[5]	B[2]
XVVD_1	B[1]	B[3]	B[1]	G[4]	B[1]	G[1]	-	B[1]	G[4]	B[1]
XVVD_0	B[0]	B[2]	B[0]	G[3]	B[0]	G[0]	-	B[0]	G[3]	B[0]

20. Camera Interface

20.1. Signal Description

Signal	I/O	Description
CAM_A/B_PCLK	I	Pixel Clock, driven by the Camera processor A
CAM_A/B_VSYNC	I	Vertical Sync, driven by the Camera processor A
CAM_A/B_HREF	I	Horizontal Sync, driven by the Camera processor A
CAM_A/B_DATA[7:0]	I	Pixel Data for YCbCr in 8-bit mode or for Y in 16-bit mode, driven by the Camera processor A
CAM_A/B_CLKOUT	O	Master Clock to the Camera processor A
CAM_A/B_FIELD	I	Software Reset or Power Down for the external Camera processor A

Note) 1.C110 don't have a dedicated CAM RESET signal. So, GPIO should be allocated for it.
2. C100 has two camera port A, B

20.2. Camera INPUT

Camera Interface can support the next video standards,

(1) ITU-R BT 601 YCbCr 8-bit mode

(2) ITU-R BT 656 YCbCr 8-bit mode

*** Maximum. 8192 x 8192 pixels Camera input support**

Camera Interface max. Horizontal size

	Item	Max size		
		CAMIF 0	CAMIF 1	CAMIF 2
Scaler	Scaler input Hsize	4224	4224	1920
	Scaler bypass mode	8192	8192	8192
Output Rotator	TargetHsize(without output rotation)	4224	4224	1920
	TargetHsize(with output rotation)	1920	1920	1280
Input Rotator	REAL_WIDTH(without input rotation)	8192	8192	8192
	REAL_HEIGHT(with input rotation)	1920	1920	1280

20.3. Restriction

HREF is valid after VSYNC pulse at capture start

Max Clock Speed is 100MHz

21. MIPI DSI & CSI

21.1. Signal Description

Ball Name	I/O	Description	Comment
XMIPIMDP0	IO	Master DATA LANE0 DP for MIPI-DPHY	
XMIPIMDP1	IO	Master DATA LANE1 DP for MIPI-DPHY	
XMIPIMDP2	IO	Master DATA LANE2 DP for MIPI-DPHY	
XMIPIMDP3	IO	Master DATA LANE3 DP for MIPI-DPHY	
XMIPIMDN0	IO	Master DATA LANE0 DN for MIPI-DPHY	
XMIPIMDN1	IO	Master DATA LANE1 DN for MIPI-DPHY	
XMIPIMDN2	IO	Master DATA LANE2 DN for MIPI-DPHY	
XMIPIMDN3	IO	Master DATA LANE3 DN for MIPI-DPHY	
XMIPIMDPCLK	IO	Master CLK Lane DP for MIPI-DPHY	
XMIPIMDNCLK	IO	Master CLK Lane DN for MIPI-DPHY	
XMIPISDP0	IO	Slave DATA LANE0 DP for MIPI-DPHY	
XMIPISDP1	IO	Slave DATA LANE1 DP for MIPI-DPHY	
XMIPISDP2	IO	Slave DATA LANE2 DP for MIPI-DPHY	
XMIPISDP3	IO	Slave DATA LANE3 DP for MIPI-DPHY	
XMIPISDN0	IO	Slave DATA LANE0 DN for MIPI-DPHY	
XMIPISDN1	IO	Slave DATA LANE1 DN for MIPI-DPHY	
XMIPISDN2	IO	Slave DATA LANE2 DN for MIPI-DPHY	
XMIPISDN3	IO	Slave DATA LANE3 DN for MIPI-DPHY	
XMIPISDPCLK	IO	Slave CLK Lane DP for MIPI-DPHY	
XMIPISDNCLK	IO	Slave CLK Lane DN for MIPI-DPHY	
XMIPIVREG_0P4V	IO	Regulator capacitor for MIPI-DPHY	Connect 2nF Cap. To GND

21.2. Design Guide

- It is NOT attached passive device on Dp, Dn Cable Interface.
- Routing Length of Dp and Dn have same length between Master and Slave.(An aberration of them is under 3mm)
- Maximum Loading capacitance of Cable interface is 70pF.
- Differential Cable Interface impedance is 100 Ω .
- It is connected to 2nF Capacitance on XMIPIVREG_0P4V Pin

22. TV ENCODER

22.1. Signal Description

Ball Name	I/O	Description	Comment
XdacCOMP	IO	External capacitor connection	Connect 0.1uF ceramic capacitor to VDDDAC
XdacVREF	IO	Reference voltage input	Connect 0.1uF ceramic capacitor to GND
XdacIREF	IO	External resistor connection	Connect 1.2KΩ to GND for full scale output (1.3V)(Tolerance +- 1%)
XdacOUT	IO	Analog output of DAC	Connect 75Ω to GND. (Tolerance +- 1%) Full scale output current of the DAC is 26.7mA.

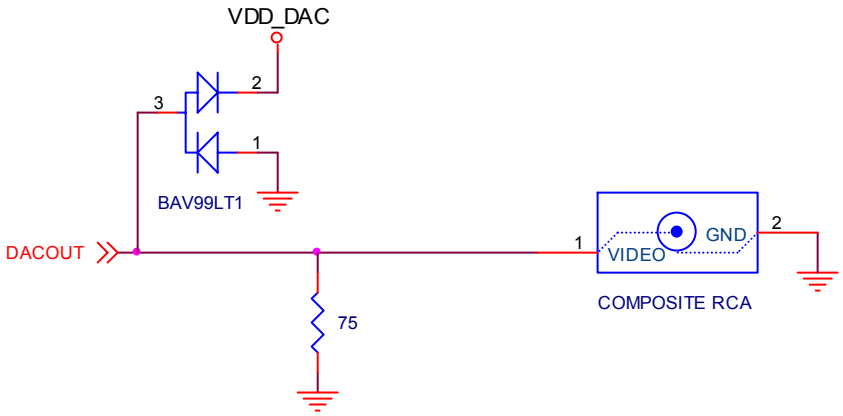


Figure 22-1) TV Encoder connection example

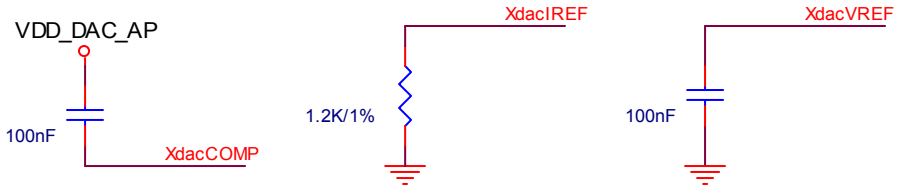


Figure 22-2) DAC Reference pin connection

23. HDMI

23.1. Overview

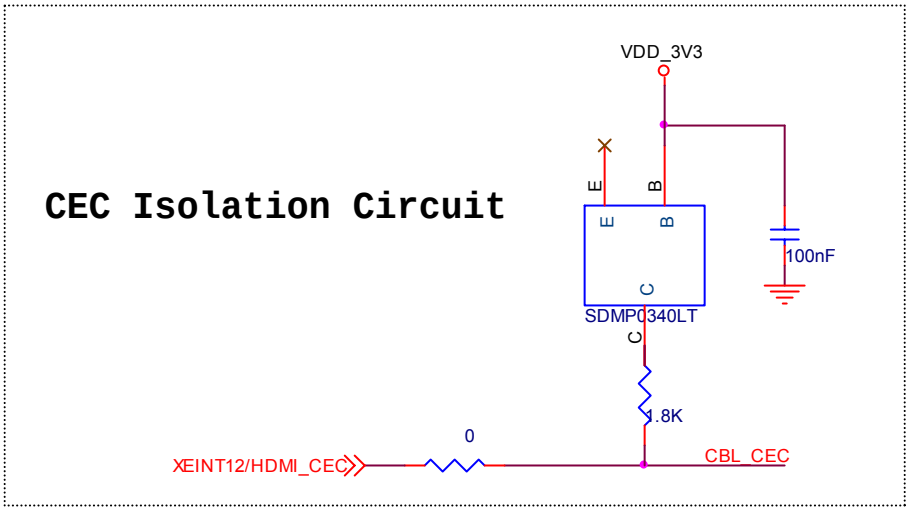
HDMI 1.3 Tx Subsystem V1.0 is comprised of an HDMI Tx Core with I2S/SPDIF input interface, CEC block and HDCP Key Block

23.2. Signal Description

- ADC/ DAC / HDMI/ MIPI (Dedicated)

Ball Name	I/O	Description	Comment
XHDMITX0P	O	HDMI Phy TX0 P	TMDS output data pairs.
XHDMITX0N	O	HDMI Phy TX0 N	
XHDMITX1P	O	HDMI Phy TX1 P	
XHDMITX1N	O	HDMI Phy TX1 N	
XHDMITX2P	O	HDMI Phy TX2 P	
XHDMITX2N	O	HDMI Phy TX2 N	
XHDMITXCP	O	HDMI Phy TX Clock P	TMDS output clock pair.
XHDMITXCN	O	HDMI Phy TX Clock N	
XHDMIREXT	I	HDMI Phy Registance	External Reference Resistor. 4.6K, A 1% resistor is connected to ground
HDMI_CEC	I/O		Signal of CEC channel (muxed with XEINT12)
HDMI_HPD	I		HDMI Hot Plug Detection Signal (muxed with XEINT13)
XHDMIXTI	I	HDMI crystal input	
XHDMIXTO	O	HDMI crystal output	

23.3. Circuit Diagram Example



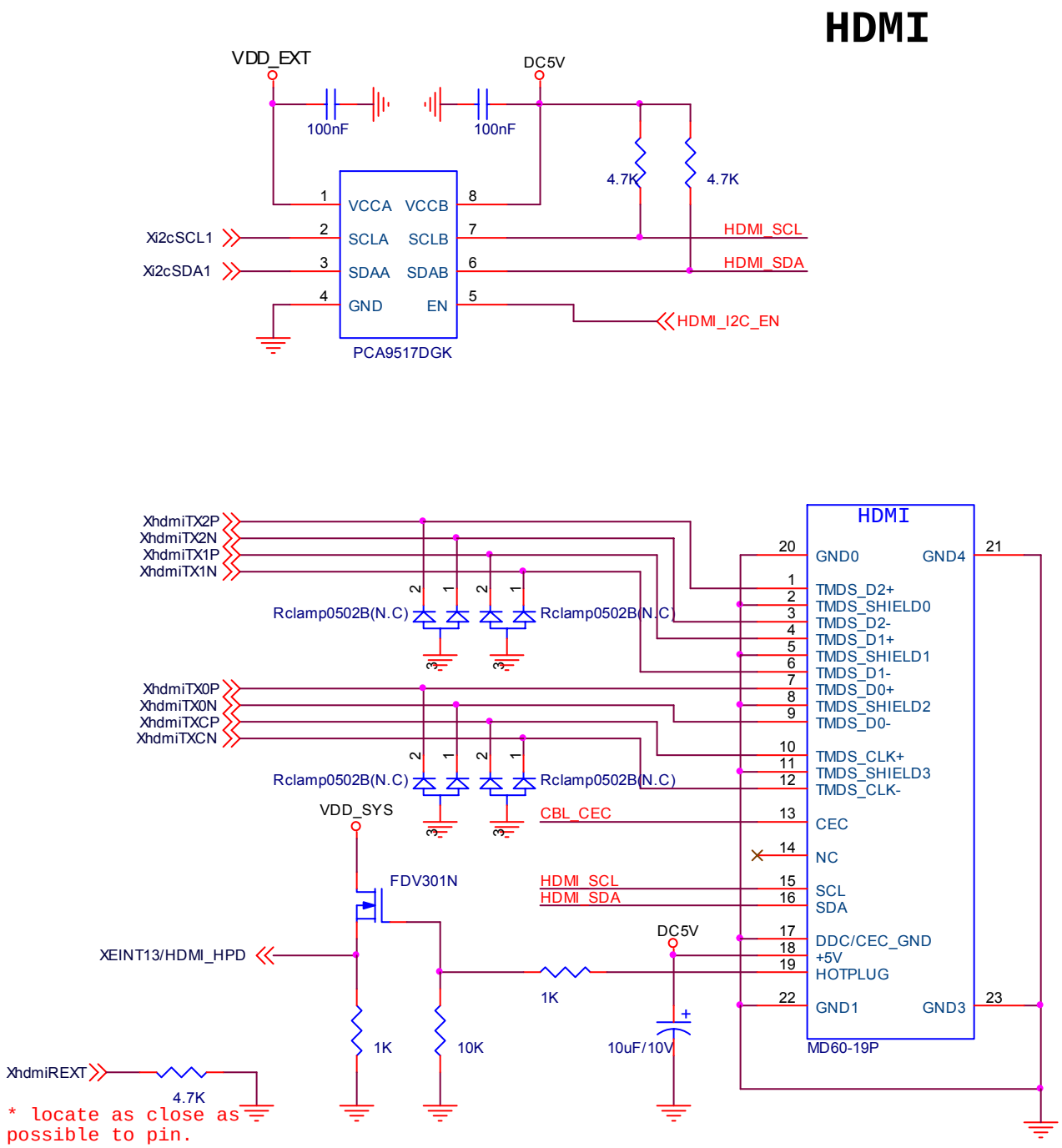
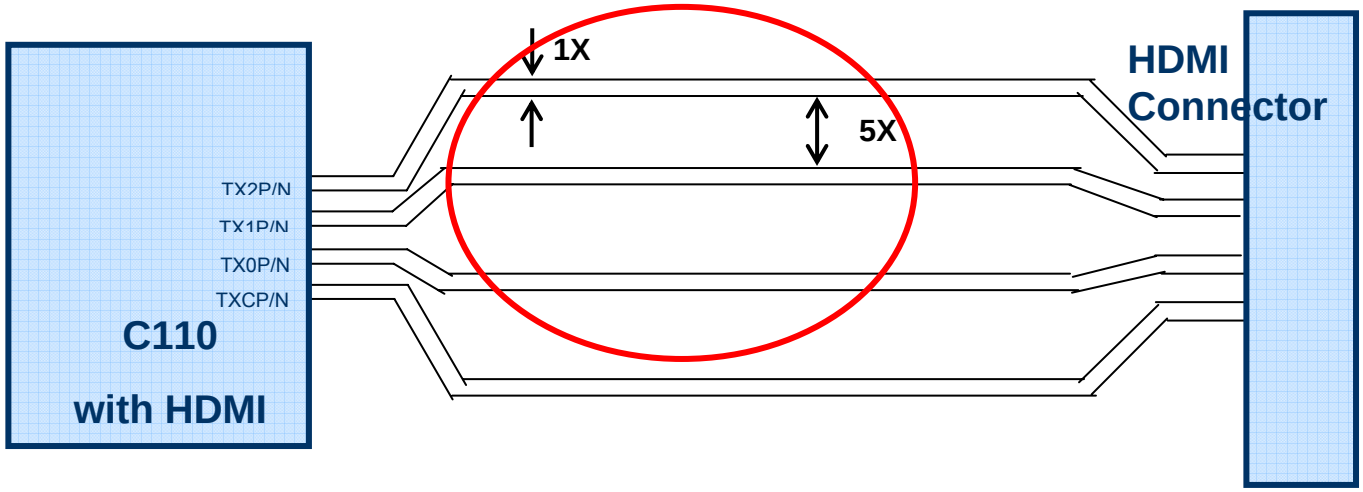


Figure 23-1) HDMI Circuit Diagram example

23.4. PCB Artwork Guide

A) Transmission Line Design of Differential pairs

- For high-frequency signal transmission along the traces of the differential signals, the trace structure must be a transmission line structure. The strip line structure and the microstrip line structure are the most recommended structures.
- For the traces of the differential pairs, the grounded plane should be a continuous plane. The ground plane of the microstrip line and the strip line should be continuous. Any discontinuity or slot in the ground plane causes signal reflections.
- The differential line on the top layer of the PCB with the microstrip line structure is most recommended.
- The number of via on the differential line should be minimized.
- pre-determined differential line impedance of the differential pairs is 100[Ohm].
  And recommended range of the differential line impedance of the trace is between 95[Ohm] to 105[Ohm].



B) Decoupling Capacitor

- Small size MLCC's are used. In all these cases, the capacitors should be placed as close as possible to the package. When choosing these components, the smallest components should be chosen since they have the least parasitic inductance.
- Ferrite Bead is used for high frequency noise rejection. But ferrite bead can induce IR voltage drop due to DC resistance. We recommend to use ferrite bead with small DC resistance considering max current.

C) More general guidelines

- Route the length of parallel signal lines is kept to same if possible.

- Limit your trace length. Longer trace display more resistance and inductance and introduce more delays. It also limits the bandwidth which varies inversely with the square of trace length.

- Do not use any clock signal loops. Keep clock lines straight when possible.

- Do not route signals close to the edge of the PCB board.

- Route clock signals on the top layer and make sure that there is no via's. Via's change the impedance and introduce more skew and reflections.

24. IIS MULTI AUDIO INTERFACE (v5.1)

24.1. Signal Description

Signal	I/O	Description
I2S_0_SCLK	IO	IIS-bus serial clock for channel 0 (Lower Power Audio)
I2S_0_CDCLK	IO	IIS CODEC system clock for channel 0 (Lower Power Audio)
I2S_0_LRCK	IO	IIS-bus channel select clock for channel 0 (Lower Power Audio)
I2S_0_SDI	I	IIS-bus serial data input for channel 0 (Lower Power Audio)
I2S_0_SDO[2:0]	O	IIS-bus serial data output for channel 0 (Lower Power Audio)

24.2. Audio Port

There are three IIS Interface Controllers in S5PV210. IIS channel 1,2 are for normal 2 channel IIS. You can use 5.1 channel IIS with channel 0.

External Clock Source

S5PV210 provides a master clock to the codec through the I2S_CDCLK line. This configuration has an advantage that it is not necessary to configure oscillator circuit. For the making Master Clock, S5PV210 uses and divided EPLL, MPLL or PCLK (refer to the User's Manual). Among these clock sources, divided EPLL is used for Lower Power Audio especially.

If an oscillator circuit is configured for a precise clock for the Sampling Frequency without PLLs or Internal clocks, there is a way to accept to this frequency as a source of master clock through the I2S_CDCLK line.

S5PV210 can supply 24MHz clock to Codec chip via xCLKOUT line.(refer to the User's Manual). Even at Power down mode, this signal keep supplying to Codec chip. When Codec chip need 24MHz, external oscillator circuit can be reduced by using this configuration.

Connection Example

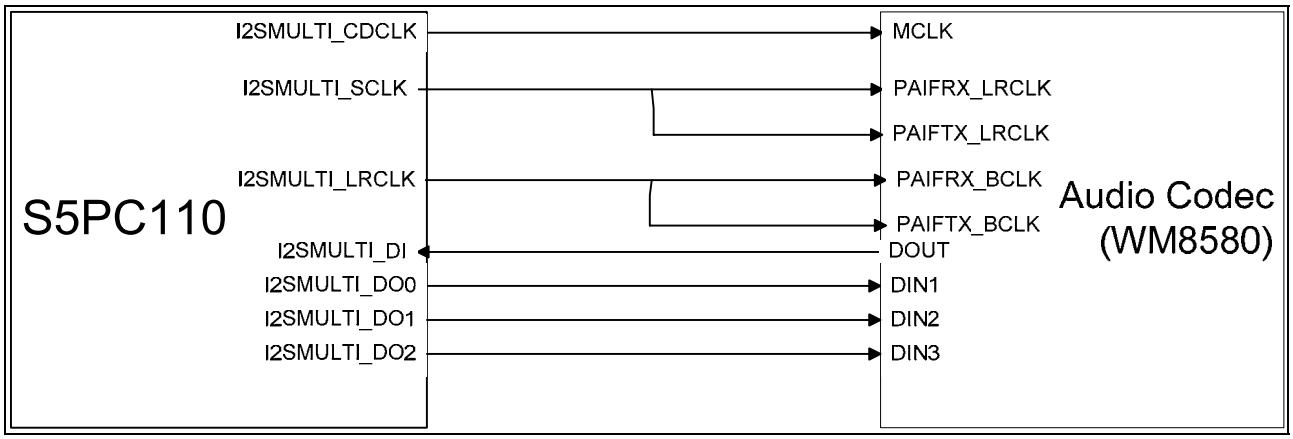


Figure 24-1) IIS Connection Example with WM8580 (Master Mode)

25. IIS BUS CONTROLLER

25.1. Signal Description

Signal	I/O	Description
I2S_1_SCLK	IO	IIS-bus serial clock for channel 1
I2S_1_CDCLK	IO	IIS CODEC system clock for channel 1
I2S_1_LRCK	IO	IIS-bus channel select clock for channel 1
I2S_1_SDI	I	IIS-bus serial data input for channel 1
I2S_1_SDO	O	IIS-bus serial data output for channel 1
I2S_2_SCLK	IO	IIS-bus serial clock for channel 2
I2S_2_CDCLK	IO	IIS CODEC system clock for channel 2
I2S_2_LRCK	IO	IIS-bus channel select clock for channel 2
I2S_2_SDI	I	IIS-bus serial data input for channel 2
I2S_2_SDO	O	IIS-bus serial data output for channel 2

25.2. External Clock Source

S5PV210 provides a master clock to the codec through the Xi2sCDCLK line. This configuration has an advantage that it is not necessary to configure oscillator circuit. For the making Master Clock, S5PV210 uses and divides EPLL, MPLL or PCLK (refer to the User's Manual). If an oscillator circuit is configured for a precise clock for the Sampling Frequency without PLLs or Internal clocks, there is a way to accept to this frequency as a source of master clock through the Xi2sCDCLK line.

S5PV210 can supply 24MHz clock to Codec chip via CLKOUT line.(refer to the User's Manual). Even at Power down mode, this signal keep supplying to Codec chip. When Codec chip need 24MHz, external oscillator circuit can be reduced by using this configuration.

25.3. Connection Example

This example shows I2S connection using WM8580 Secondary interface.

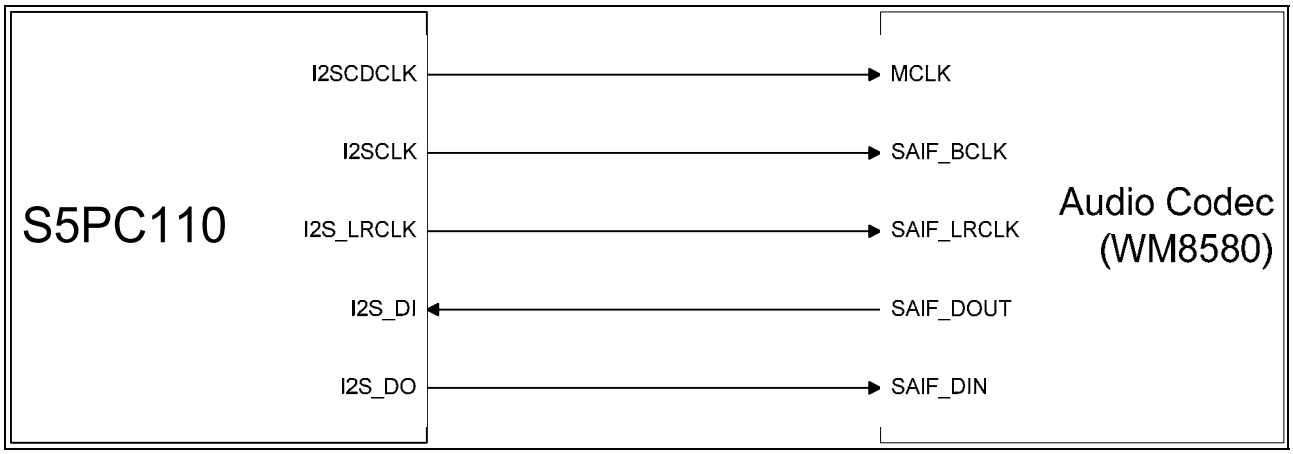


Figure 25-1) IIS Connection Example with WM8580 (Master Mode)

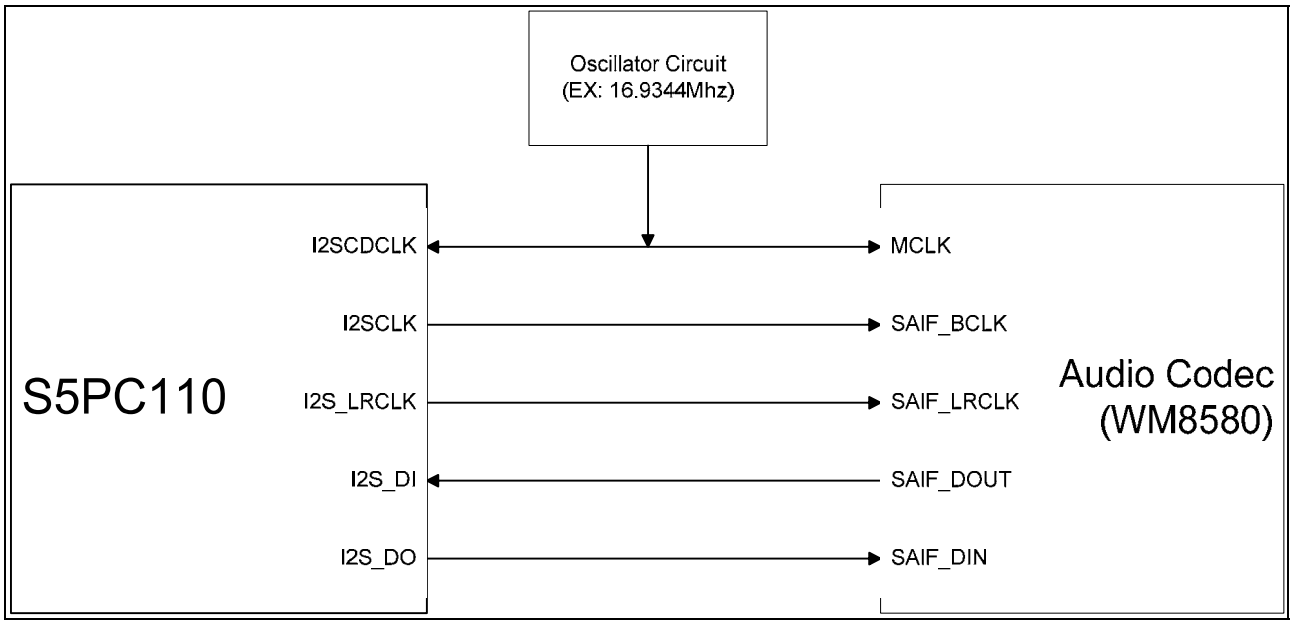


Figure 25-2) External OSC Circuit for IISCDCLK (with WM8580)

26. AC97 CONTROLLER

26.1. AC97 Signal Description

Signal	I/O	Description
AC97BITCLK	I	12.288MHz BITCLK from AC97 CODEC
AC97RESETn	O	nReset for CODEC
AC97SYNC	O	48KHz Frame SYNC
AC97SDI	I	Serial Data In From AC97 CODEC
AC97SDO	O	Serial Data OUT to AC97 CODEC

26.2. Audio Ports

In S5PV210, There is one AC97 Controller. AC97 PORT is shared with I2S channel 1 and PCM channel 1.functions.

26.3. Connection Example

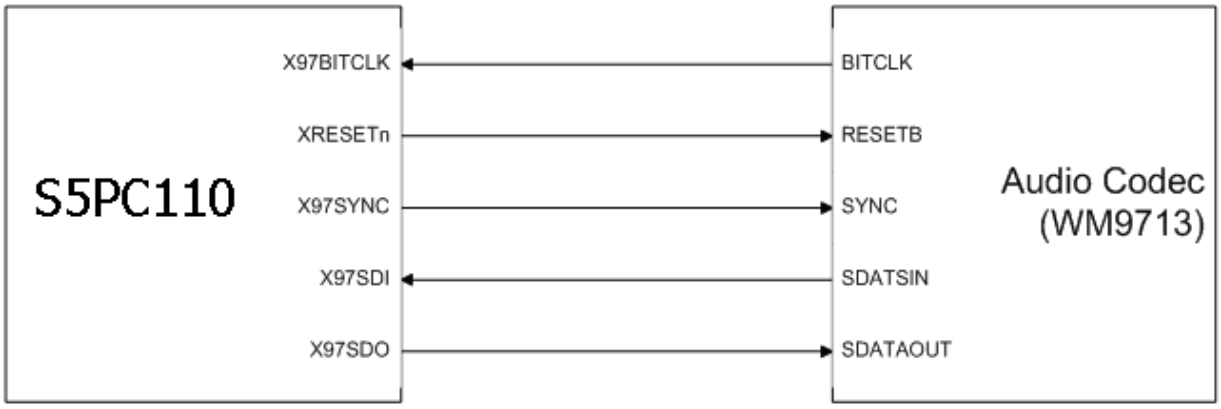


Figure 26-1) AC97 connection example

27. PCM BUS CONTROLLER

27.1. Signal Description

Signal	I/O	Description
PCM_0_SCLK	O	PCM Serial Shift Clock for channel 0
PCM_0_EXTCLK	I	Optional reference clock for channel 0
PCM_0_FSYNC	O	PCM Sync indicating start of word for channel 0
PCM_0_SIN	I	PCM Serial Data Input for channel 0
PCM_0_SOUT	O	PCM Serial Shift Clock for channel 0
PCM_1_SCLK	O	PCM Serial Shift Clock for channel 1
PCM_1_EXTCLK	I	Optional reference clock for channel 1
PCM_1_FSYNC	O	PCM Sync indicating start of word for channel 1
PCM_1_SIN	I	PCM Serial Data Input for channel 1
PCM_1_SOUT	O	PCM Serial Shift Clock for channel 1
PCM_2_SCLK	O	PCM Serial Shift Clock for channel 2
PCM_2_EXTCLK	I	Optional reference clock for channel 2
PCM_2_FSYNC	O	PCM Sync indicating start of word for channel 2
PCM_2_SIN	I	PCM Serial Data Input for channel 2
PCM_2_SOUT	O	PCM Serial Shift Clock for channel 2

27.2. External Clock Source

To make PCM Serial clock and PCM Frame Sync, PCM interface controller divides EPLL, MPLL or PCLK When these clocks are divided, its advantage is that it is not necessary to configure oscillator circuit(for feeding auxiliary clock(256fs/384fs) to Codec chip (MCLK), please refer to SEC).

If an oscillator circuit is configured for a precise clock for the Sampling Frequency without PLLs or Internal clocks, there is a way to accept to this frequency as source of PCM Serial clock and PCM Frame Sync through the XpcmEXTCLK line.

27.3. Connection Example

This example shows PCM connection using WM8580 Secondary interface. For Primary interface refer I2S multi audio interface.

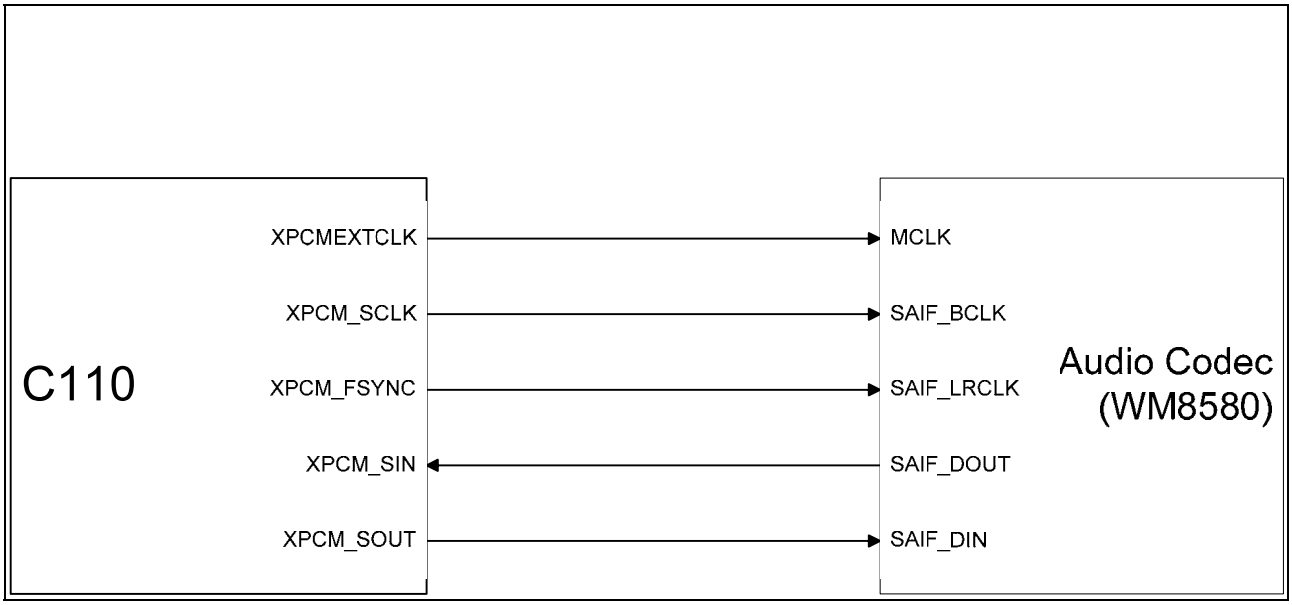


Figure 27-1) Internal clocks(ex:EPLL) for PCM master clock (with WM8580)

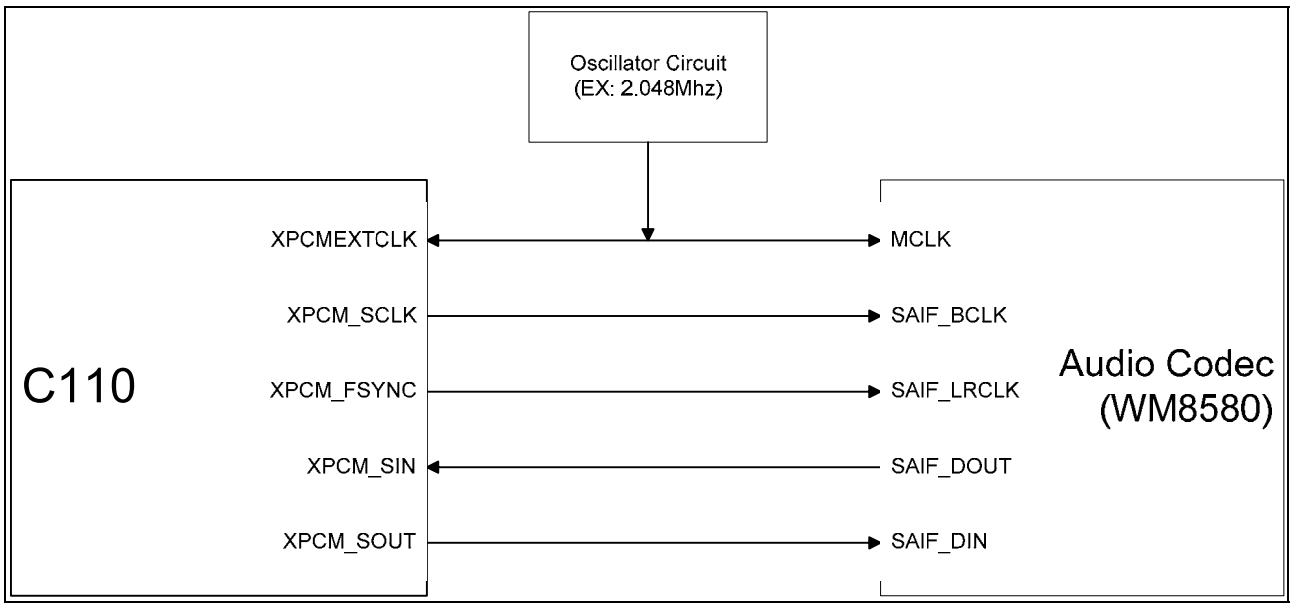


Figure 27-2) External clocks(ex:2.048MHz) for PCM master clock (with WM8580)

28. SPDIF

28.1. Signal Description

Signal	I/O	Description
SPDIF_EXTCLK	I	Global audio main clock(External MCLK)
SPDIF_0_OUT	O	SPDIFOUT data output(Tx only)

Connection Example

This example shows using TOSLINK.

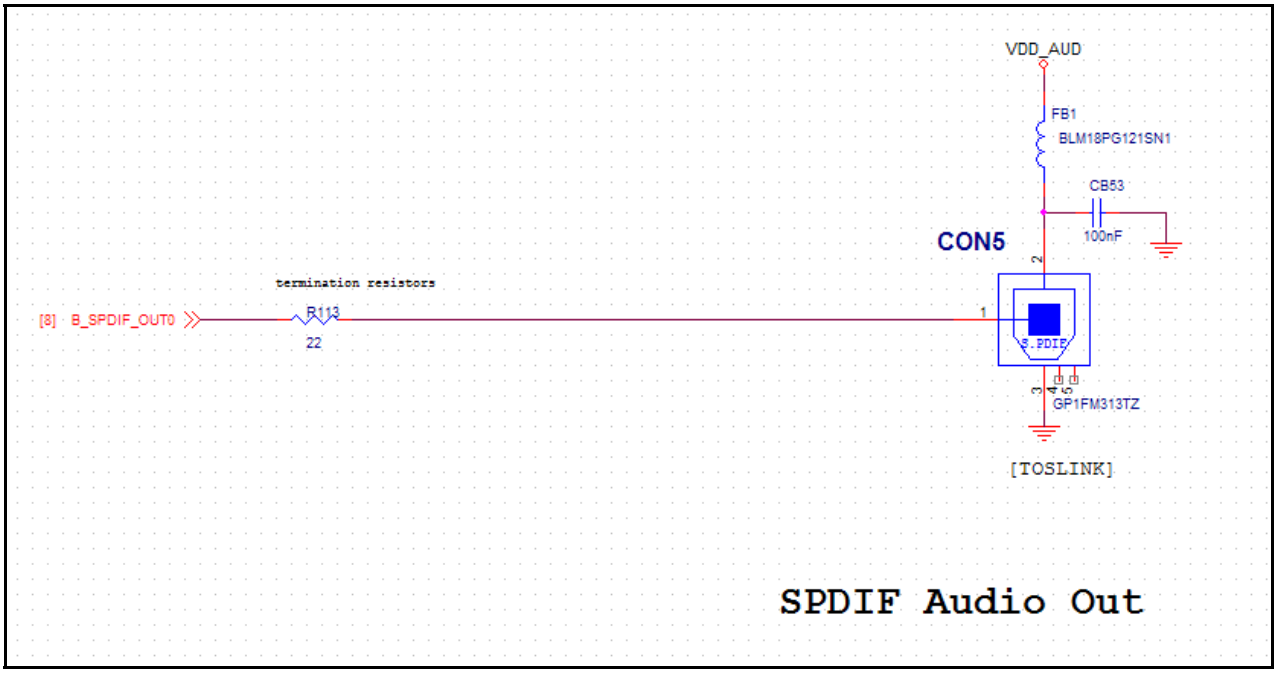


Figure 28-1) SPDIF Connection Example

29. ADC&TOUCH SCREEN INTERFACE

The 10/12bit CMOS ADC is a recycling type device with 10-channel analog inputs. It's maximum conversion rate of 1Msps with 5MHz A/D converter clock. Touch screen interface can control/select pads (XP,XM,YP,YM) of the touch screen for X,Y position. In S5PV210, There are available two Touch screen interface. A mapped with touch signal like bellows.

-AIN[9] = XP1,

-AIN[8] = XM1

-AIN[7] = YP1,

-AIN[6] = YM1,

-AIN[5] = XP0,

-AIN[4] = XM0

-AIN[3] = YP0,

-AIN[2] = YM0,

Note) When Touch Screen device is not used, XM, XP, YM or YP can be connected to Analog Input Signal for Normal ADC conversion .

30. KEYPAD INTERFACE

In S5PV210, The Key Pad ports multiplexed with GPIO ports provide up to 14 row and 8 columns.

Keypad signals(Key_pad_ROW and Key_pad_COL) are multiplexed Host I/F and EINT. Therefore it is requisite to set GPIO ports as keypad function.

Refer to GPH2,GPH3,GPJ4 registers.

Signal	I/O	Description
KP_COL[7:0]	O	KeyIF_Column_data[7:0]
KP_ROW[13:0]	I	KeyIF_Row_data[13:0]

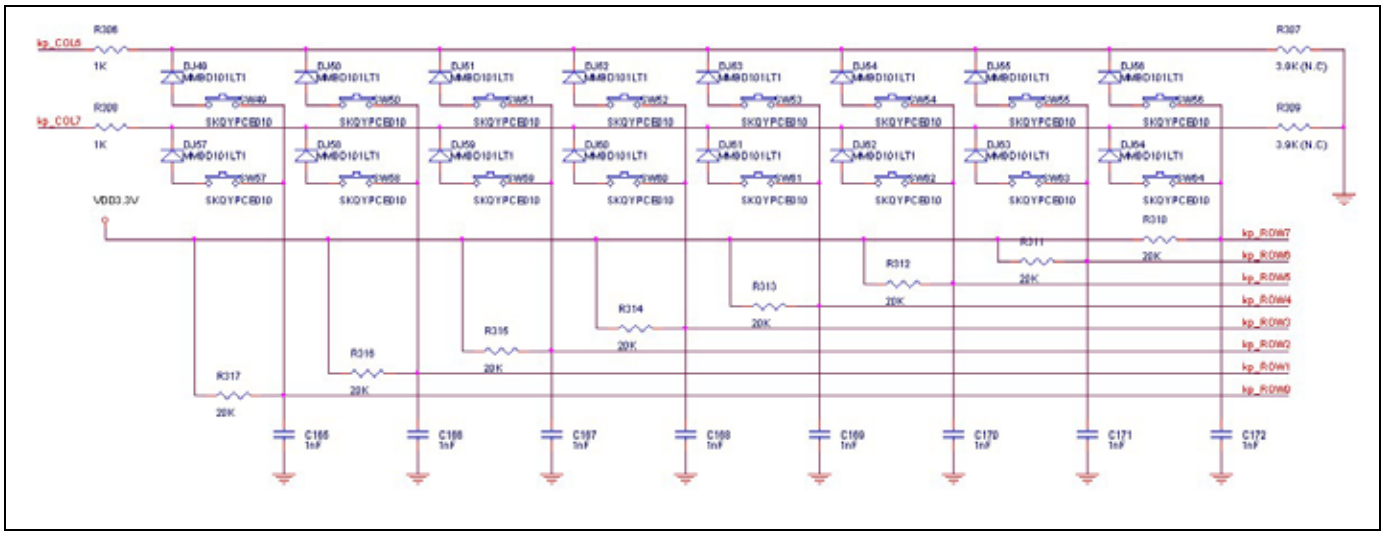


Figure 30-1) Multi-key input keypad example