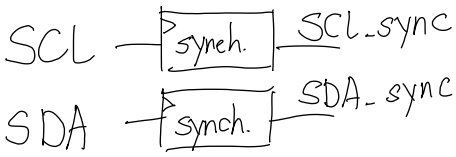
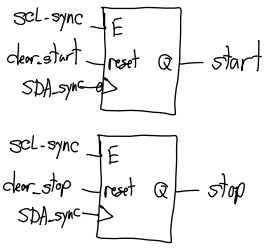
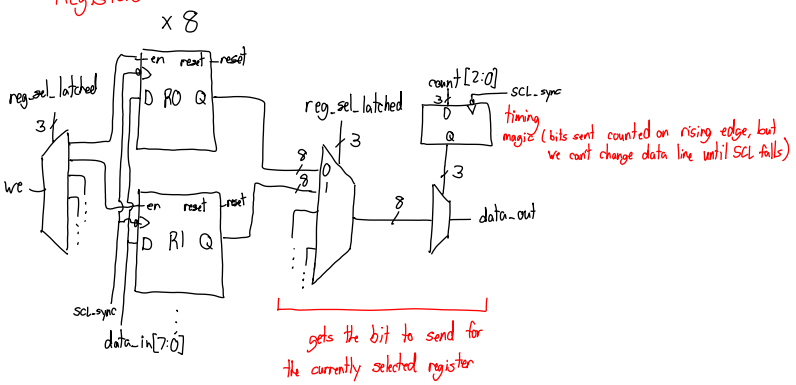
Input Synchronization



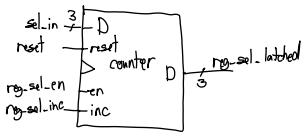
Start/Stop Detect



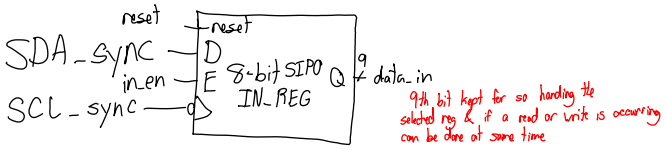
Registers



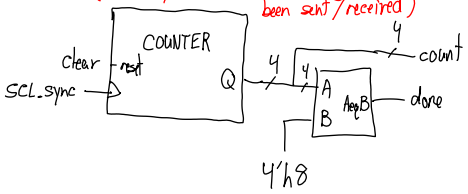
Latch the selected address so it can be accessed later



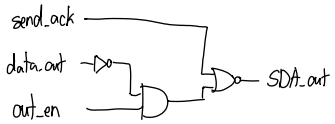
Data Input



(a handy counter for knowing when 8 bits have been sent/received)

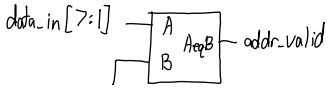


Output Generation



SDA pulled low if sending ack or if data_out is low and the output is enabled

Address Check



7'h20
currently hard-coded but could come from a register

⟶ = all clock edges

⟶ = only clock edges when SCL is falling

~~A~~All states besides RESET transition to INIT when stop is asserted
All states transition to WAIT when start is asserted