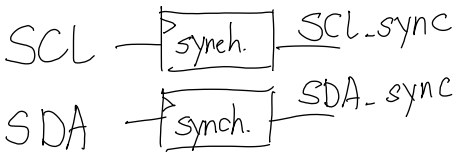
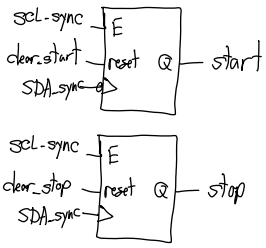
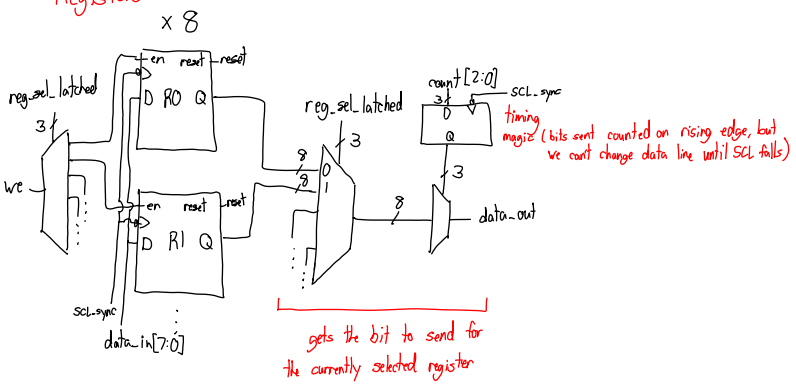
Input Synchronization



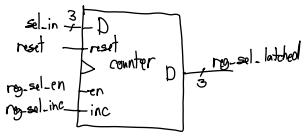
Start/Stop Detect



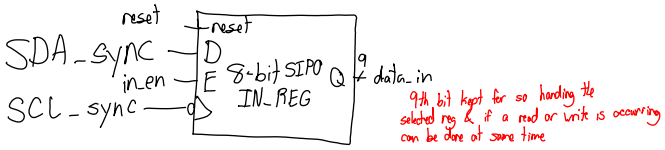
Registers



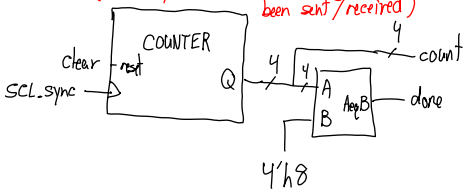
Latch the selected address so it can be accessed later



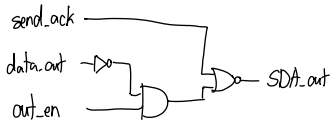
Data Input



(a handy counter for knowing when 8 bits have been sent/received)

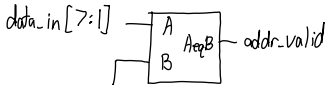


Output Generation



SDA pulled low if sending ack or if data_out is low and the output is enabled

Address Check

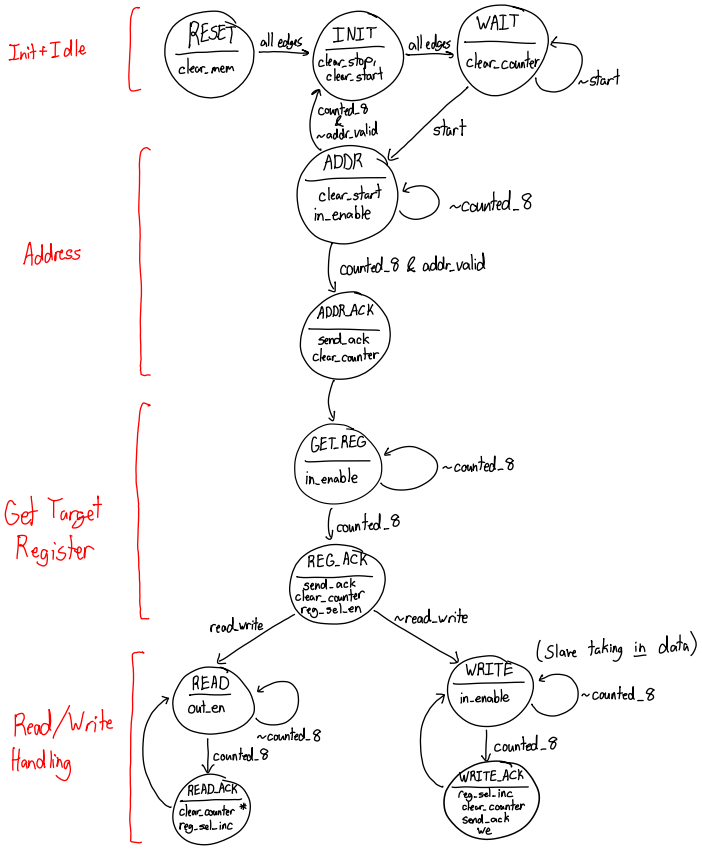


7'h20
currently hard-coded but could come from a register

*Note: All state transitions happen when a falling edge of SCL is detected, but both Reset and Init can transition on any edge

for simplicity:

*All states besides RESET transition to INIT when stop is asserted



* Need to double check but I believe the master sends the ACK. I don't think I need to do anything though, because immediately after a NACK will be a stop signal