ASSIGNMENT REPORT

MULTI-STAGE OPERATIONAL AMPLIFIER

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Submission Date : 31st March 2025

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1. Introduction

Operational amplifiers, or op-amps, are regarded as one of the building blocks for modern analogue integrated-circuit design. From their origins in the vacuum tube era, followed by their evolution into integrated circuits via discrete transistors, op-amps have become an indispensable part of signal processing systems, instruments and communications equipment everywhere.

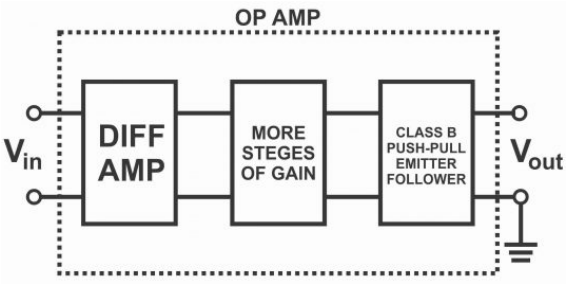


Figure 1: Block Diagram of an OP amp

Multi-stage operational amplifiers represent a way to break through the limitations of single-stage designs. Such an approach as remarked upon by (Gray, Hurst, Lewis, & Meyer, 2009), lets designers distribute the requirements for gain and bandwidth over several amplification stages, thereby optimizing performance parameters which might otherwise be in conflict with each other in single-stage designs. This architecture also allows trade-offs between gain, bandwidth, power consumption, and noise performance to be overcome.

The development of CMOS technology has revolutionized the design of op-amps. According to (Razavi, 2017), the migration to submicron CMOS processes has brought both challenges and opportunities for analogue designers, particularly in managing short-channel effects taking advantage of higher integration densities achieved through silicon oxynitride processes. Today's wide bandwidth multi-stage amplifiers, built in TSMC's 0.18um process, must juggle various performance goals while also addressing worries about reduced supply voltages and variabilities of devices.

Multi-stage amplifiers typically consist of differential input stages, followed by gain and then output stages. In this his characterization, (Johns & Martin, 2008) explain that every stage serves a specific purpose. The input stage has a very high input impedance and common-mode rejection capability, intermediate stages provide voltage gain, while output stages deliver current drive capability. This strategic partitioning enables the designer to optimize each stage for its function yet still maintain a high overall level of system performance.

The design of multi-stage op-amps for specific loading conditions, e.g. capacitance and resistance in parallel, demands a carefully thought-out approach to frequency compensation techniques. (Allen & Holberg, 2012) emphasize that proper proper frequency compensation is essential if oscillator started instabilities are to be avoided, retaining acceptable phase margin throughout the amplifier's operating range. This assumes particular importance when creating open-loop configurations, where no feedback stability is inherently provided.

2. Aim and Objectives

The aim of this assignment is to design a multi-stage operational amplifier in open-loop configuration capable of driving a 5 pF and 50 Ω load in parallel based on appropriate TSMC 0.18 µm CMOS process. The amplifier must achieve the following specifications:

- Supply voltage, VDD=1.8 V
- Total DC power consumption, PDC≤20 mW
- Input Voltage, Vin=2 mVp
- Open Loop Gain, AV=35 dB−38 dB
- Open Loop Bandwidth, $f3dB$≥200 kHz
- The biasing circuit must be designed using current mirror.

Tasks:

Students are required to complete the following tasks:

1. **Identify** suitable topology of the multi-stage CMOS amplifiers based on the above specifications and perform necessary calculations based on the designed amplifier.
2. **Evaluate** the designed circuit using SPICE simulator. Perform relevant simulations such as DC analysis, transient response and AC analysis.
3. **Investigate** a more advanced circuit architecture (i.e. employing appropriate feedback topology) with insightful explanation, calculations and simulation results.
4. **Conclude** on the overall work carried out in this assignment with relevant analysis, along with detailed applications and discussion

3. Design and Calculation

Overview

The multi-stage operational amplifier is a three-stage design combined to achieve the desired gain characteristics performances. The first stage includes a differential amplifier utilized with active and passive current mirrors giving high input impedance and good common mode rejection ratio (CMRR). The second stage has a common source amplifier configuration when it adds very much to the total voltage gain of the circuit. The last stage is a buffer (and thereby impedance matching and loading related) manufactured specifically as a common drain or source follower.

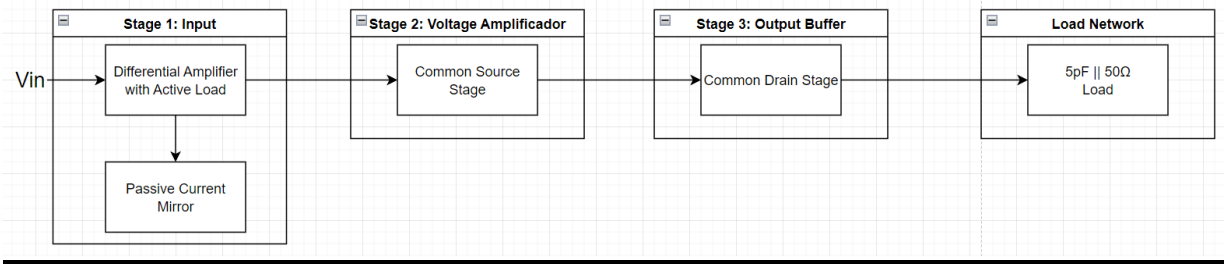


Figure 2: Block diagram of the full multistage amplifier

First Stage

The input stage includes a differential amplifier with an active load which is the primary part of operational amplifier. This initial, mission critical stage makes differential inputs available in single-ended output while making very good common-mode rejection ratio (CMRR). It employs transistors M1 and M2 as the differential pair, each with a 25µm width, chosen to minimize production variability to ensure a balanced operation and optimal trans conductance. Transistors M5 and M6 of 6µm are the active loads for amplification with high output resistance. The stage is working in a DC bias point of 0.6V of common mode setting necessary working conditions for transistors. Coupled with the differential amplifier is a passive current mirror consisting of M3, M4, and provides a biasing current of approximately 0.5mA for the differential pair stable. With this above current mirror configuration M3 is biased in linear region and M4 biased in saturation, so that M3 is operated in current is supplied consistently within minor changes of the supply voltage, so that it provides a reliable reference for the whole circuit.

Table 3.1: Operating region table

Transistor	Type	Region	Given condition
M1	nMOS	Saturation	$V_{DS} \geq V_{GS} - V_{TH}$
M2	nMOS	Saturation	$V_{DS} \geq V_{GS} - V_{TH}$
M3	nMOS	Linear	$V_{DS} < V_{GS} - V_{TH}$
M4	nMOS	Saturation	$V_{DS} \geq V_{GS} - V_{TH}$
M5	pMOS	Saturation	$\lvert V_{DS}\rvert \geq \lvert V_{SG}\rvert - \lvert V_{TH}\rvert$
M6	pMOS	Saturation	$\lvert V_{DS}\rvert \geq \lvert V_{SG}\rvert - \lvert V_{TH}\rvert$

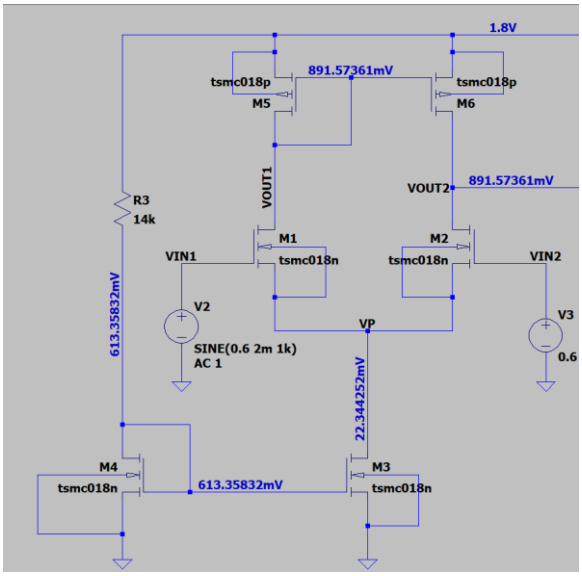


Figure 3: First Stage of the Multistage

DC Analysis of Passive Current Mirror (First stage)

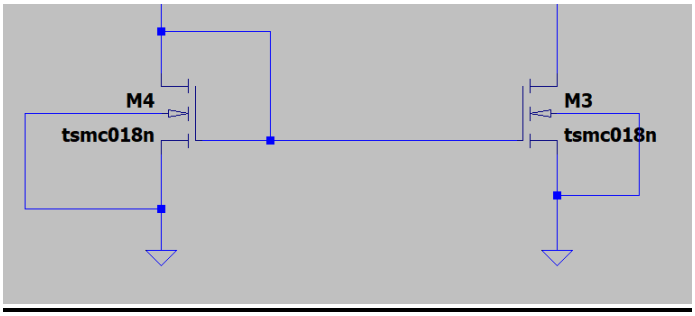


Figure 4: Passive current mirror (First stage)

To obtain the current of the passive current mirror we should look at their transistors:

The current in transistor M4 is set to be at 8.48x10^{-5} A. Hence:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$\mu_n C_{ox} = \frac{2I_D}{\frac{W}{L}(V_{GS} - V_{TH})^2} = \frac{2 \cdot 8.48 \cdot 10^{-5}}{\frac{5 \cdot 10^{-6}}{0.18 \cdot 10^{-6}}(0.613 - 0.494)^2}$$

$$\mu_n C_{ox} = 4.31 \cdot 10^{-4}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 = \frac{1}{2}4.31 \cdot 10^{-4} \cdot \frac{5 \cdot 10^{-6}}{0.18 \cdot 10^{-6}}(0.613 - 0.494)^2$$

$$I_D = 8.47 \cdot 10^{-5} A$$

The final value obtained for the current from the transistor 4 which is operating in saturation mode is $I_D = 8.47 \cdot 10^{-5} A$.

Differential Amplifier Stage (AC and DC Analysis in first stage):

Basically, for the differential amplifier the intention is to filter out unwanted noise within the input signal. Now, to generate a noiseless signal, the parameters such as length and width of the transistors M1, M2, M5, and M6 are going to be able to load properly and tuned. Moreover, transistors like M1 and M2 have a width of 25µ while M5 and M6 have a width of 6µ:

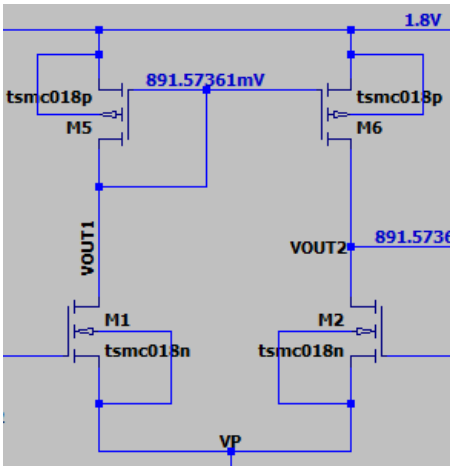


Figure 5: Differential amplifier with active current mirror (First stage)

The equations for the gain, resistance in differential amplifier is as follow:

$$G = G_m \cdot R_{out}$$

$$i_{out} = g_{m1}\frac{V_{in}}{2} - \left(-g_{m2}\frac{V_{in}}{2}\right) = g_{m1,2} \cdot V_{in}$$

$$G_m = \frac{i_{out}}{V_{in}} = g_{m1,2}$$

$$R_{out} = r_{02}//r_{04}$$

$$G = g_{m1,2}(r_{02}//r_{04})$$

After that we have the Id formulas for both linear and saturation of the transistors:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$I_D = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}$$

The small signal for the differential amplifier is defined as follow:

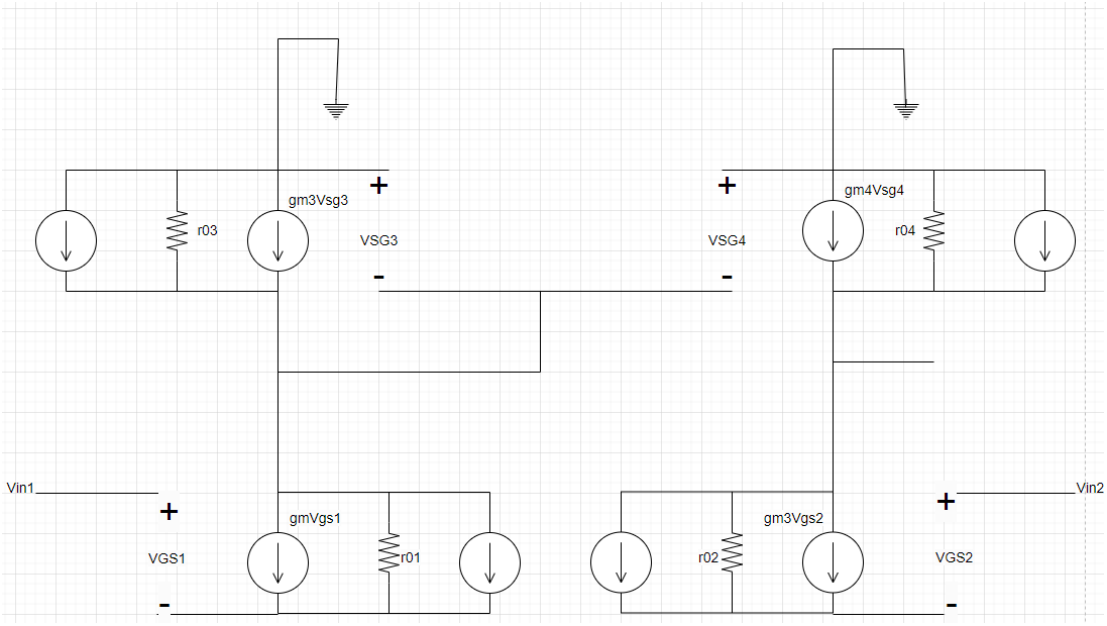


Figure 6: Small signal of differential amplifier (first stage)

In the next table the values obtained for Id in each transistor for the first stage is going to be reflected:

Table 3.2: Current Id for all the transistors

Transistor	I_D (A)
M1	0.000259
M2	0.000259
M3	0.000517
M4	0.0000848
M5	-0.000259
M6	-0.000259

By proving those values for Id obtained from the simulation results and using the formula for saturation, the next method can be applied.

Second Stage

The second stage is of common source type which gives high voltage gain as inverting wave. The current stage contains the 44µm-wid transistor M7 digested to get enough trans conductance to remain the following stage. The load resistor R1 (210Ω) has the function to make the voltage gain characteristic while defining the proper current biasing conditions. This stage mainly contributes the most part of the total gain of the amplifier of 35.08 dB; hence, it is very significant to the circuit performance. Running at around 5.04mA of current, the common source stage must consume a lot of power to achieve the high gain affiliates the circuit is asked to accomplish and make it with wide bandwidth. M7 transistor works reliably in saturated region, therefore highest gain and directivity during an amplification. This stage is the main gain stage, connecting high-impedance differential input circuit portion to low-impedance output requirements.

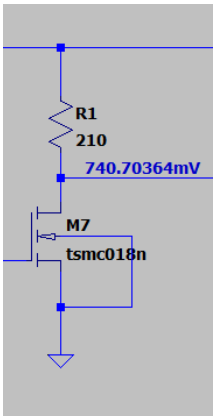


Figure: Second Stage of the Multistage

Common source DC and AC analysis

Since we have a nMOS transistor across the transistor M8, the current Id formula is:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

The small signal of the common source amplifier will be:

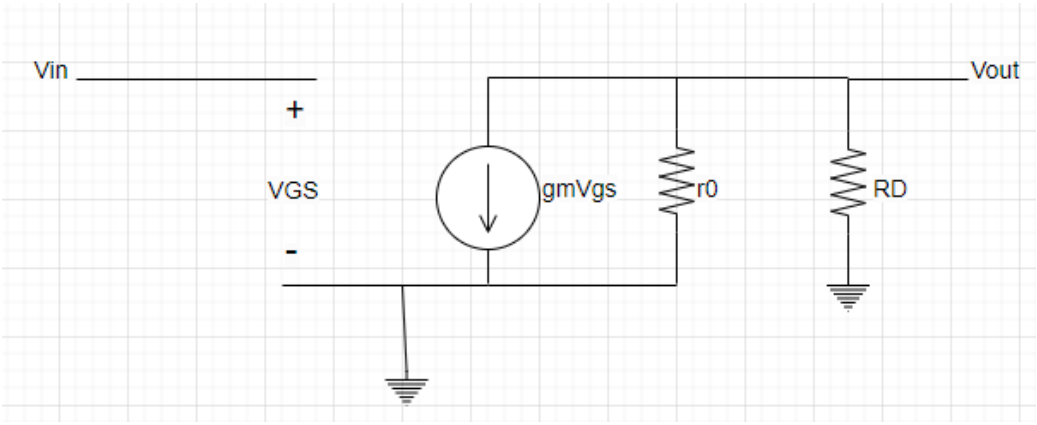


Figure 7: Small signal of common source stage (second stage)

Following the small signal model for the common source stage, let us apply the Kirchoff's voltage rule at the output, the gain would be obtained by the following equation:

$$A_v = -gm(r_0 - R_D)$$

Third Stage

The third stage incorporates a common drain amplifier, a source follower to which is essential impedance matching and driver for loads off-chip. Transistor M8, with its significant increase in width of 180µm is designed to handle larger current requirements and drive the required load conditions. In paralleling with R2 (8kΩ), gives a current capability of nearly 2.99mA. The common drain configuration has almost unity voltage gain but full current gain with very low output impedance, which is required to keep the signal integrity with any capacitive or low resistance loading. Running in its saturation mode M8 assures linear behaviour across full range of expected signal. This buffer stage effectively decouples the high-gain second stage from load intolerance, so any load effect does not impair the amplifier's performance properties.

Load Network

The load network is a 5pF capacitor in parallel with a 50Ω resistor, which mimic the conditions stated for external load of the operational amplifier. This combination in parallel of R2 gives rise to both resistive and capacitive loading difficulties, that the output stage needs to counter. The capacity element also generates frequency-dependent loading affects that would potentially limit bandwidth or even trigger instability if unmanaged. On the other hand, the relatively low 50Ω impedance requires considerable drive current from the output stage to be delivered. This load configuration is a common scenario for signal processing or transmission line driving, or analogue front-end type of circuits. The successful operation of this load, at the same time adhering to the performance specifications shows the reliability of the amplifier design.

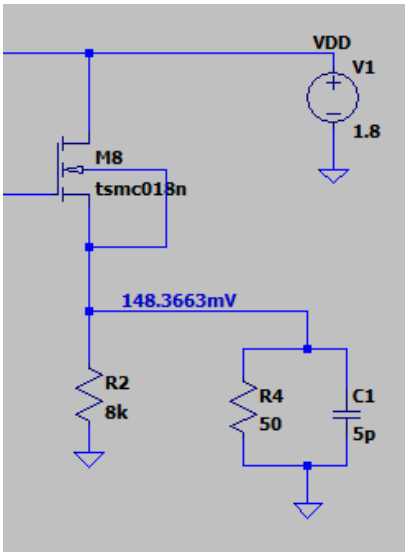


Figure 8: Buffer stage (third stage)

The current formula in this nMOS transistor is determine by:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Completed multistage amplifier:

The first stage is formed by a differential amplifier with an active current mirror and a passive current mirror starting from the first transistor M1 until transistor M6.

The second stage starts from transistor M7 which is a common source amplifier topology that is connecting to the next amplifier topology or transistor.

The third stage is transistor M8 which is a common-drain amplifier topology, or a source follower connected to the resistor R2.

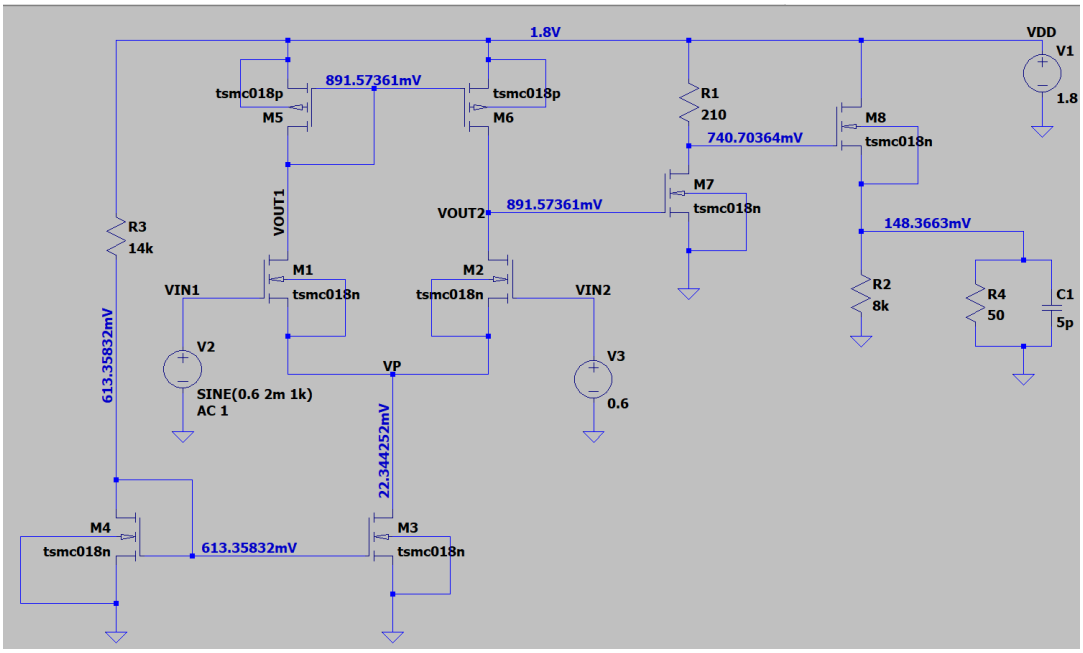


Figure 9: Full circuit

If we have to calculate the total current across all the capacitors as well as the gain, then we could follow up the next equation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

4. Simulation Results

The whole design of the multistage was designed in LTSpice. The multistage is formed by three different stages as mentioned before. In this section, screenshots are going to be taken and used to explain the multistage amplifier as well as the simulation results obtained. The multistage is formed by both nMOS and pMOS transistors based on a model called TSMC 0.18µ that can be found into LTSpice.

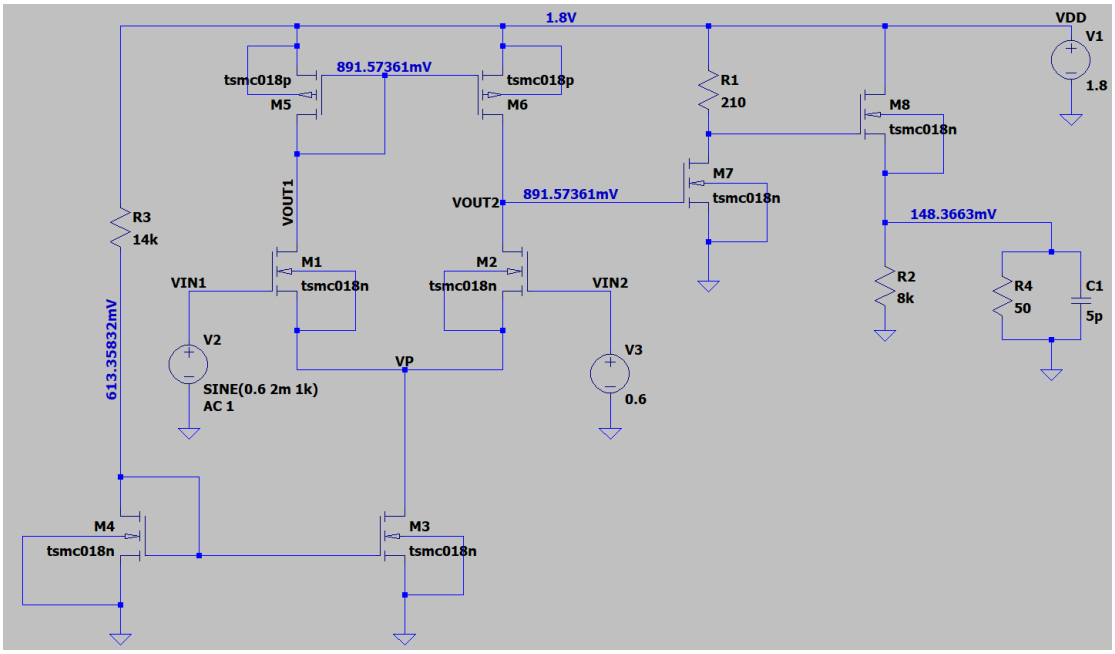


Figure 10: Full circuit design in LTSpice

As it can be observed from the circuit above, the multistage amplifier comprises of three different stages:

Stage 1:

In this stage we have around 6 transistors that are divided into three parameters: Differential amplifier with Active current Mirror and Passive Current Mirror.

Stage 1:

From stage two there is a visible common source stage with a resistive load.

Stage 3:

At the end, there is an output buffer stage around stage 3.

In this section, there will be an experiment analysis that will be divided into:

- DC operating point of the transistor: this is to determine the state of the voltages and currents in a transistor or amplifier when there is not any signal that is applied.
- DC sweep analysis: will determine the reaction or how the circuit behave or respond when changes are applied to any parameter such as power supply voltage or temperature. DC sweep is an important parameter that will help us to understand about the sensitivity of the circuit based on the changes applied to it.
- AC analysis: The ac analysis informs us about how the circuit handles signals of different frequencies. It has to do with gain, phase shifts, and frequency response.
- Transient Response: it will show how the circuit is going to react over time when the signals are changed suddenly.

There are some essentials parameters that was implemented while designing the multistage amplifier:

DC Operating point analysis

In the next table, the conditions for the operating point analysis are stated to determine whether one transistor is in saturation, triode, or cut off:

Table 4.1: DC Operating analysis

Transistor	Type	Region	Given condition
M1	nMOS	Saturation	$V_{DS} \geq V_{GS} - V_{TH}$
M2	nMOS	Saturation	$V_{DS} \geq V_{GS} - V_{TH}$
M3	nMOS	Linear	$V_{DS} < V_{GS} - V_{TH}$
M4	nMOS	Saturation	$V_{DS} \geq V_{GS} - V_{TH}$
M5	pMOS	Saturation	$\|V_{DS}\| \geq \|V_{SG}\| - \|V_{TH}\|$
M6	pMOS	Saturation	$\|V_{DS}\| \geq \|V_{SG}\| - \|V_{TH}\|$

In the first place, all the transistors into the circuit are not in a cut-off state which means that all the transistors are in an "ON" state. However, to go further analysis and examining the behaviour of each transistor we would look at the conditions from the table, so that, the operating point can be observed.

According to transistor M1 and M2 that have the same width at 25µ, the operating point from where they both operate is in saturation mode based on the next condition:

$$V_{DS} \geq V_{GS} - V_{TH}$$

$$0.869 \geq 0.578 - 0.498$$

$$0.869 \geq 0.08$$

- Like transistor M2 which is operating in saturation mode as well.

--- Operating Point ---

V(vin1):	0.6	voltage
V(vout2):	0.891574	voltage
V(vin2):	0.6	voltage
V(n003):	0.613358	voltage
V(vout1):	0.891574	voltage
V(vp):	0.0223443	voltage
V(vdd):	1.8	voltage
V(n002):	0.740704	voltage
V(n001):	0.148366	voltage
Id(M1):	0.000258592	device_current
Ig(M1):	0	device_current
Is(M1):	-0.000258592	device_current
Ib(M1):	-8.79229e-13	device_current
I(V1):	-0.00863209	device_current
I(R3):	8.47601e-05	device_current
Id(M7):	0.00504427	device_current
Ig(M7):	0	device_current
Is(M7):	-0.00504427	device_current
Ib(M7):	-7.50704e-13	device_current
I(R2):	1.85458e-05	device_current
I(V3):	0	device_current
Id(M3):	0.000517185	device_current
Ig(M3):	0	device_current
Is(M3):	-0.000517185	device_current
Ib(M3):	-2.81291e-14	device_current
Id(M8):	0.00298587	device_current
Ig(M8):	0	device_current
Is(M8):	-0.00298587	device_current
Ib(M8):	-1.66163e-12	device_current
I(C1):	7.41832e-25	device_current
Id(M4):	8.47601e-05	device_current
Ig(M4):	0	device_current
Is(M4):	-8.47601e-05	device_current
Ib(M4):	-6.23358e-13	device_current
Id(M5):	-0.000258592	device_current
Ig(M5):	-0	device_current
Is(M5):	0.000258592	device_current
Ib(M5):	9.18426e-13	device_current
Id(M6):	-0.000258592	device_current
Ig(M6):	-0	device_current
Is(M6):	0.000258592	device_current
Ib(M6):	9.18426e-13	device_current
I(R4):	0.00296733	device_current
Id(M2):	0.000258592	device_current
Ig(M2):	0	device_current
Is(M2):	-0.000258592	device_current
Ib(M2):	-8.79229e-13	device_current
I(V2):	0	device_current
I(R1):	0.00504427	device_current

Figure 11: DC Operating point simulation results

All the simulation results can be observed from figure 10 above regarding the operating.

Total Power Consumption

The total current from each transistor is:

$$I_d(M1) + I_d(M2) + I_d(M3) + I_d(M4) + I_d(M5) + I_d(M6) + I_d(M7) + I_d(M8)$$

$$Sum = 0.000258592 + 0.000258592 + 0.000517185 + 0.0000847601 + (-0.000258592) + (-0.00863209) + 0.00504427 + 0.00298587$$

$$Sum = 0.008631835A$$

The total current flowing through all transistors is approximately 8.63mA which is close to the current drawn from the power supply I(V1) which is -0.00863209 A, and it is correct because the power supply provides the current for the entire circuit.

Power consumption

$$P = V_{DD} \cdot I_D = 1.8V \cdot 8.63mA$$

$$Power\ consumption = 15.534mW$$

Spice Error Log

There is another section where we can get further details or information about the circuit:

Semiconductor Device Operating Points:

--- BSIM3 MOSFETS ---

Name:	M1	M2	M3	M4	M7
Model:	tsmc018n	tsmc018n	tsmc018n	tsmc018n	tsmc018n
Id:	2.59e-04	2.59e-04	5.17e-04	8.48e-05	5.04e-03
Vgs:	5.78e-01	5.78e-01	6.13e-01	6.13e-01	8.92e-01
Vds:	8.69e-01	8.69e-01	2.23e-02	6.13e-01	7.41e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	4.98e-01	4.98e-01	5.05e-01	4.94e-01	4.99e-01
Vdsat:	7.82e-02	7.82e-02	9.04e-02	9.52e-02	1.83e-01
Gm:	4.08e-03	4.08e-03	5.40e-03	1.11e-03	1.81e-02
Gds:	1.06e-04	1.06e-04	2.03e-02	3.44e-05	9.45e-04
Gmb	9.76e-04	9.76e-04	1.33e-03	2.67e-04	4.31e-03

Name:	M8	M5	M6
Model:	tsmc018n	tsmc018p	tsmc018p
Id:	2.99e-03	-2.59e-04	-2.59e-04
Vgs:	5.92e-01	-9.08e-01	-9.08e-01
Vds:	1.65e+00	-9.08e-01	-9.08e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00
Vth:	4.94e-01	-4.83e-01	-4.83e-01
Vdsat:	8.61e-02	-3.19e-01	-3.19e-01
Gm:	4.05e-02	1.00e-03	1.00e-03
Gds:	9.15e-04	3.02e-05	3.02e-05

Figure 12: Spice error log

DC Sweep analysis

As it can be observed from the figure below, V2 is the source, and the type of sweep is linear as you can see other characteristics:

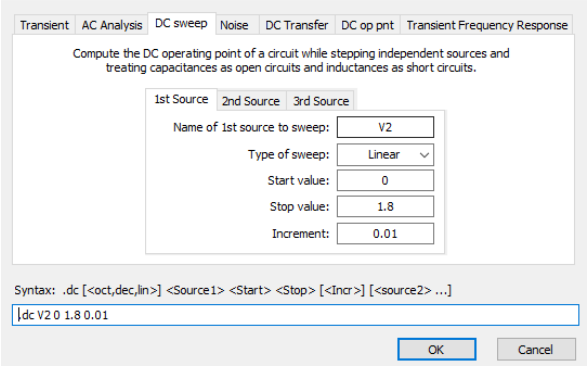


Figure 13: DC Sweep

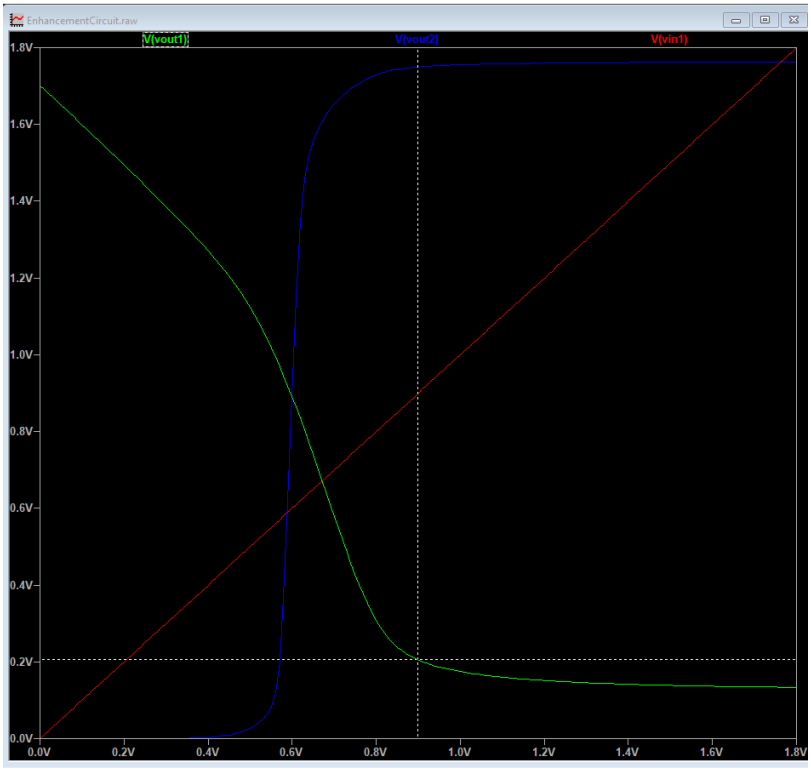


Figure 14: DC sweep analysis

The graph is showing a DC sweep where VIN1 (red line) oscillate from 0V to 1.8V, and at the same time monitoring the responses of VOUT1 (green), and VOUT (blue).

There is a comparison clearly for the input voltage (VIN1) against the voltage (VIN2=0.6V) which is producing a higher and suitable output.

Transient Analysis:

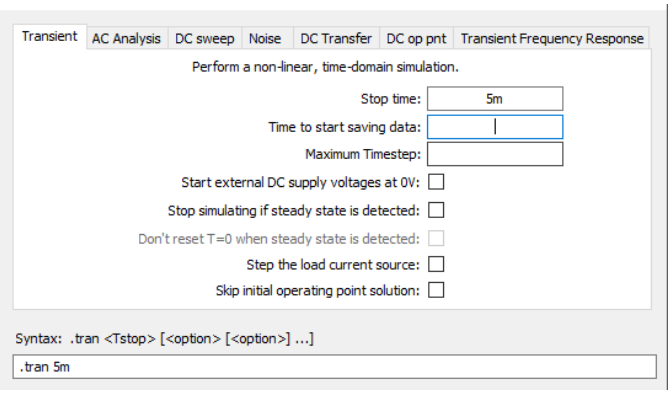


Figure 15: Transient Analysis

Transient Response:

The graph that was obtained in the simulation is:

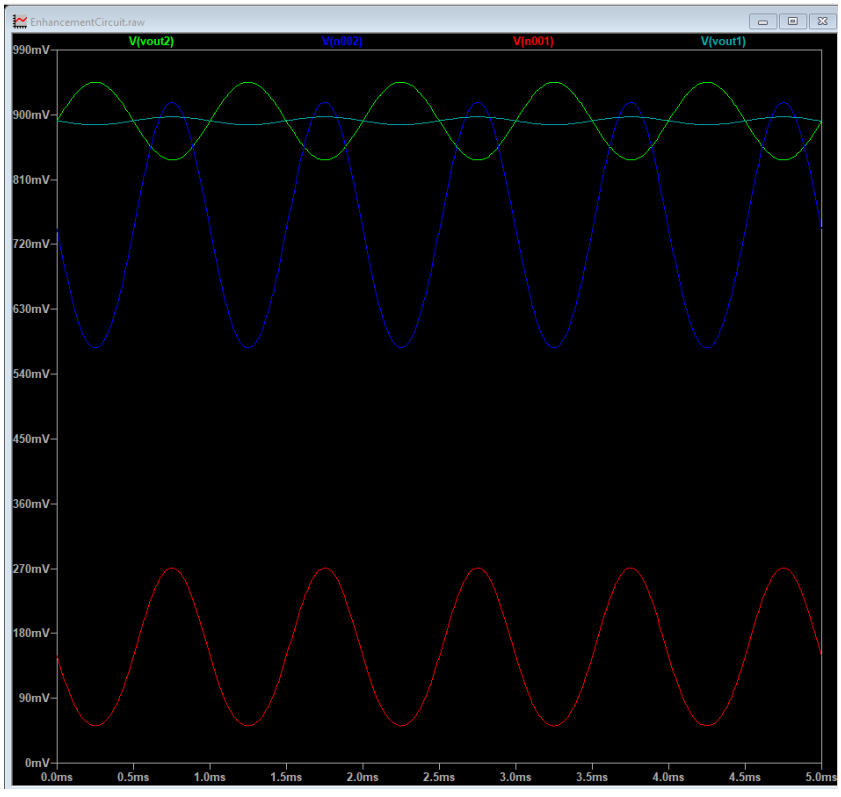


Figure 16: Transient results from LTSpice

Table 4.2: Three stages of the Amplifier

Stage	Type	Components	Function	Input/Output
First Stage	Differential amplifier with active + passive current mirrors	M1-M4, M5-M6, R3 (14k)	Signal amplification with high gain and good CMRR	Input: VIN1, VIN2 Output: VOUT1
Second Stage	Common source amplifier	M7, R1 (210Ω)	Voltage gain amplification	Input: VOUT1 Output: VOUT2
Third Stage	Common drain (source follower)	M8, R2 (8k), R4 (50Ω), C1 (5pF)	Buffer (impedance matching)	Input: VOUT2 Output: Final output

The circuit is performing differential amplification. Take the difference between the sinusoidal input (VIN1) and the triangular wave (VIN2). The difference is amplified and pushed out to produce a final output. The 180° phase reversal is characteristic of the common source amplifier stage.

The operating points evident from the schematic (fig 15) are:

- VOUT2 is biased at about 891.58mV
- The output stage has a DC level of approximately 148.37mV

AC Analysis

In the figure 16 below we have the AC Analysis configuration. The analysis will compute the small-signal AC behaviour of the circuit around its DC operating point and help determine characteristics like gain and phase at different frequencies within that range (description extracted from online material).

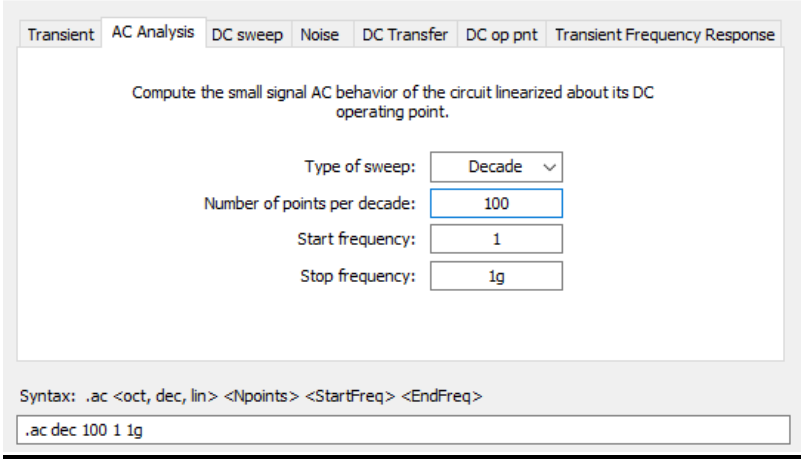


Figure 17: AC Analysis simulation

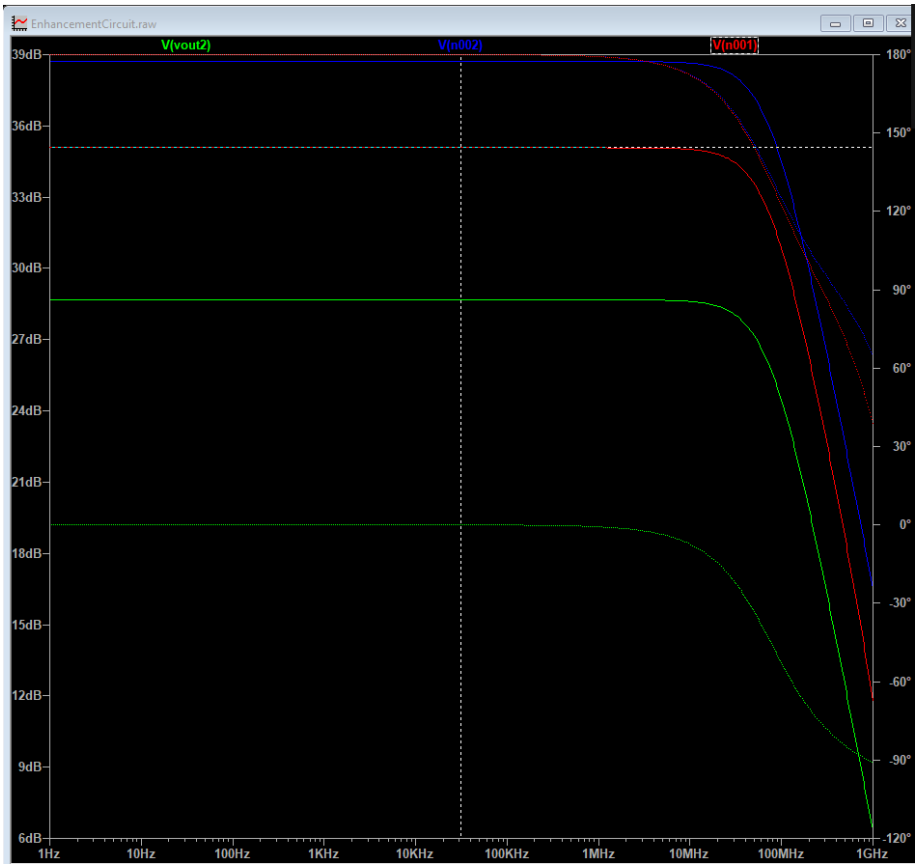
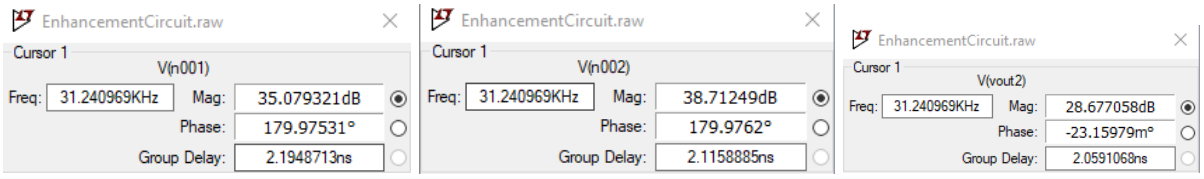


Figure 18: AC Analysis as Gain (dB) and Phase

In the graph above we could observed the frequency response of the multistage amplifier and it is divided based on the three stages which are represented by:

- First stage is represented by Vout2-green.
- Second stage is represented by V(n002)-blue

- Third stage is represented by V(n001)-red



Flat Response Region (1Hz-100kHz): All three stages show flat gain and minimal phase shift characteristics in the mid-band region, demonstrating good mid-band response.

Roll-off Region (v>100MHz): All signals roll-off at high-frequency, with V(vout2) rolling off first, which indicates bandwidth limitations.

Phase Response: At mid frequencies, the differential amplifier outputs (V(n001) and V(n002)) have approximately 180° phase shift with respect to the input signal as expected for the inverting operation, whereas V(vout2) has slight phase shift until high frequencies.

The first stage (differential amplifier) has moderate gain with low phase shift but rolls off sooner than the next stage. The gain is highest in the second stage (common source) along with 180° phase inversion. The third stage (the buffer), therefore, lowers overall gain versus the second stage a little but keeps bandwidth, and serves its purpose of impedance matching without much loss in performance.

Table 4.3: Gain and Phase of the three stages

Stage	Signal	Gain	Phase
First Stage (Differential Amplifier)	V(vout2) (green)	28.68 dB	-0.023°
Second Stage (Common Source)	V(n002) (blue)	38.71 dB	179.98°
Third Stage (Output Buffer)	V(n001) (red)	35.08 dB	179.98°

5. Literature Review

Two-Stage CMOS Op-Amp with Miller Compensation

The (Goyal, S., Sachdeva, N., & Sachdeva, T., 2015) explains the complete analysis and design procedure of a two-stage CMOS operational amplifier based on TSMC 180nm technology. The study focuses on addressing analogue integrated circuit design difficulties brought by continued supply voltage reduction and transistor channel length scaling because high-performance op-amp design regains paramount importance. Operational amplifiers function as essential components which drive analogue along with mixed-signal systems. Multiple applications demand additional stages beyond a single design stage because single-stage gain remains inadequate according to the authors. Additional design stages result in additional phase shift that may cause operational issues in feedback control systems. The paper investigates frequency compensation methods by concentrating on Miller compensation as a solution to this problem.

explain two versions of Miller compensation that include Single Capacitor Miller Compensation (SCMC) followed by SCMC with a nulling resistor. Adding a capacitor between the output and input of the second stage in traditional SCMC implementation shifts the dominant pole to frequencies at the lower end. Predictable right-half plane zero formation occurs because of this technique, whereas it negatively affects phase margin values. The integration of a nulling resistor with the compensation capacitor eliminates or shifts the RHP zero to the LHP, which enhances overall stability performance. Two stages of operational amplifiers operate from a 2.5 V supply voltage while featuring a differential input stage with an active load (first stage) and a common source amplifier (second stage). The first part of this stage uses differential pairs to achieve excellent input impedance and common-mode rejection capabilities, and the next section expands output swing and gain potential. All transistors receive stable operating points through the biasing circuit that depends on current mirrors.

Simulation tests conducted with Tanner EDA tools proved the effectiveness of each compensation technique. The execution of SCMC design results in 57.18dB gain coupled with 56-degree phase margin and 10MHz unity gain bandwidth and 115kHz 3dB bandwidth. The design of SCMC with nulling resistor achieves 48.27dB gain along with 11.21MHz unity gain bandwidth and 205kHz 3dB bandwidth and shows a remarkable phase margin of 86.48 degrees. Transient analysis reveals the SCMC design features a positive slew rate of 13.5V/μs plus negative slew rate

of 10.84V/μs however the SCMC with nulling resistor design shows slightly decreased positive slew rate (12.34V/μs yet it delivers enhanced negative slew rate (11.21V/μs. Inputting a 0.8mV signal into the op-amp yields a 1.1V output that verifies its excellent gain capability. The comparison shows that both approaches sacrifice different design characteristics. Using the SCMC with nulling resistor design results in 15.6% reduction of gain but achieves a 54% increase in phase margin and 78% improvement in bandwidth. Multiple performance aspects of multi-stage amplifiers remain unaffected when adding nulling resistors resolves stability problems. The authors find that designers must apply scaling according to requirements or product specifications because a universal best scaling method does not exist for all applications. The paper brings new analytical perspectives to low-voltage two-stage CMOS operational amplifiers in sub-micron technologies for compensation approach development.

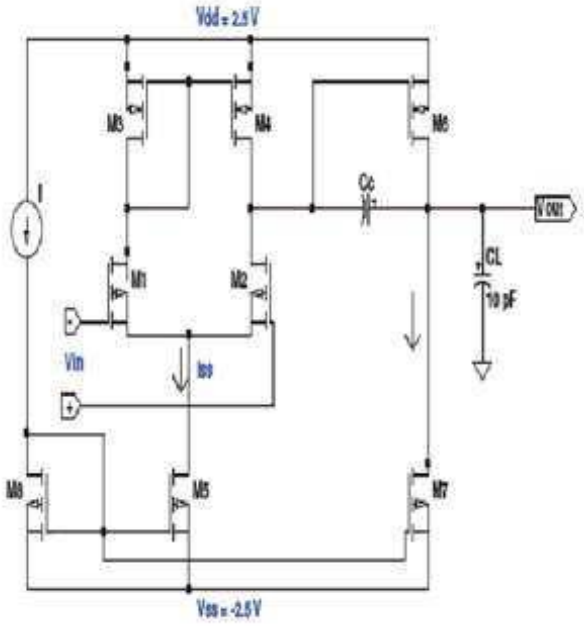


Figure 19: Topology Used for Two Stage CMOS op-amp

In figure 19 we have an operational amplifier circuit contains eight transistors that include five NMOS along with three PMOS devices arranged through a two-stage structure

6. Discussion

Technology advances have introduced multiple issues and opportunities which require optimization when designing operational amplifiers in integrated circuits. The presented study compares its discussed three-stage operational amplifier solution against the two-stage CMOS

operational amplifier with Miller compensation approach described by (Goyal, S., Sachdeva, N., & Sachdeva, T., 2015). The evaluation shows important information about design choices and presents possible ways to enhance performance.

Architecture and Topology Comparison

The primary architectural difference lies in the number of stages used in each design. The present circuit architecture consists of three stages which include a differential amplifier with active and passive mirror current components (first stage) and a common source amplifier (second stage) and a common drain buffer (third stage). The mentioned paper utilizes two stages in its design by using a differential input stage with an active load and following it with a common source amplifier and Miller compensation methods implemented. This design difference between the two structures creates a major influence on operational characteristics. The third stage addition in the design strengthens the circuit's ability to drive loads by using the common drain buffer specifically suited for 5 pF capacitive and 50 Ω resistive parallel load conditions. A third stage in the circuit design enhances the load driving ability yet it introduces stability concerns because phase shifts from multiple stages increase circuit complexity.

Gain Performance Analysis

The main distinction between these designs emerges from their different open loop gain levels. The open-loop gain reached 35.08 dB in the three-stage design because it fulfilled the design specifications for 35-38 dB gain. The two-stage design described in the reference document utilizes a nulling resistor and SCMC to achieve 48.27 dB of gain, which exceeds the measured 35.08 dB of the present design by approximately 13 dB. The significant gain difference between these designs reaches a total of 13 dB.

The right-half plane zero issue becomes resolvable through the usage of Miller compensation combined with a nulling resistor to sustain high gain performance. The Miller compensation technique applies the Miller effect to achieve lower frequency dominant poles by multiplying the second stage gain against effective capacitance. The stability benefits of their method is coupled with higher gain capability through this technique.

The design’s present configuration might have limited its gain distribution between three stages because it required enhanced stability techniques. The common drain buffer installed in the third stage operates as an impedance match while improving load driving ability yet provides little voltage gain that leads to the reduced overall gain values when compared with the original work.

Bandwidth and Frequency Response

The test of bandwidth showcases significant distinctive characteristics between the two circuit designs. The present design (the proposed) has achieved a bandwidth at 78.94 MHz beyond the required minimum of 200 kHz. The design presented in the reference paper or research paper operates at a limited bandwidth of 205 kHz because it uses the SCMC coupled with nulling resistors. The significant difference in bandwidth can be evaluated through various analytical approaches. The present design achieves its increased bandwidth because of:

- A fundamental requirement of this stage consists of using a common drain buffer to produce exceptional high-frequency reaction.
- The design compromise of amplifier bandwidth against total gain exists widely in amplifier engineering principles.
- Smaller compensation capacitance values lead to increased pole frequencies in the system.

The design employs Miller compensation to improve stability, yet it reduces bandwidth because it automatically creates a dominant low-frequency pole. The enhanced phase margin to 86.48 degrees in the referenced design provides stable performance during feedback variations but reduces bandwidth capabilities.

Power Consumption and Supply Voltage Considerations

The current design functions at a power supply of 1.8 V because modern CMOS manufacturing requires lower operating voltages. At 1.8 V supply operation the current prototype uses 15.53 mW power while adhering to a maximum threshold of 20 mW.

Due to missing power consumption data from the referenced design the direct comparison between power efficiency becomes impossible. The current design achieves an important power-saving benefit for portable electronic systems because it operates at lower supply voltages.

Stability and Phase Margin Considerations

The main shortcoming of the three-stage amplifier is the lack of phase margin measurements for the multi-stage operational amplifier design. Operational amplifiers in feedback configurations need phase margin data to determine their stability performance because it represents a fundamental stability evaluation parameter. The implementation with SCMC and nulling resistor produces exceptional phase margin results of 86.48° to ensure stability in different operating situations. More stability problems may happen as the number of amplifier stages increases because of extra phase shifts. The three-stage design demands additional advanced compensation

strategies when compared to two-stage designs for ensuring equivalent stability results. There is limited ability to conduct definitive stability performance assessments because current design phase margin data exists only through empirical measurements.

Enhancements Opportunities

The conducted comparative analysis reveals different potential improvements that can enhance the existing three-stage design:

1. To enhance the phase margin, we can apply the SCMC with the nulling resistor implementation technique found in a referenced design, which would maintain usable bandwidth. Adding a compensation capacitor between the second stage output and input and connecting the nulling resistor serves to reduce the right-half plane zero effect.
2. Enhancing gain involves optimizing Stage 2, which may succeed by enlarging M7 width and modifying R1 resistance to boost transconductance under power usage constraints.
3. A frequency compensation approach should be developed exclusively for the three-stage amplifier system by utilizing nested Miller compensation or multipath nested Miller compensation because these methods excel in amplifiers with three or more stages.
4. A refined design of the current mirror biasing circuit should be implemented because it needs additional improvements to resist temperature and process variation effects using bandgap references to ensure stable performance.

Table 6.1: Key Metrics Comparison

Parameter	Three-Stage Amplifier	Referenced Paper (SCMC + RZ)
Open-Loop Gain (AV)	35.08 dB	48.27 dB
Bandwidth	78.94 MHz	205 kHz
Phase Margin (PM)	Not Analyzed[1]	86.48°
Supply Voltage	1.8 V	2.5 V
Power Consumption	15.53 mW	Not Specified

7. Conclusion

Operational amplifier design involves trade-offs, as evidenced by the comparison between the three-stage amplifier model and the CMOS two-stage option with Miller compression features. The current design delivers high bandwidth performance together with reduced supply voltage, but the referenced design reaches higher gain and phase margins through its implementation of Miller compensation.

Different performance specifications reveal that designers need to optimize amplifiers according to application needs. The three-stage design becomes preferable for applications needing improved bandwidth performance together with reduced supply voltage requirements. Applications requiring high gain and stability benefit most when using the two-stage design with the Miller compensation technique.

A primary area of research should combine the advantages of the two designs through enhancing the three-stage architecture with advanced compensation techniques like nulling resistors which can boost gain while maintaining its existing excellent bandwidth capabilities.

8. References

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