

**ASIA PACIFIC UNIVERSITY**

**TECHNOLOGY & INNOVATION**

EE057-4-2 VLSI DESIGN

GUIDED LAB REPORT

|  |  |
| --- | --- |
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**TABLES:**

Table 1: Multiplexer

Table 2: Demultiplexer

Table 3: Full Adder

Table 4: Full Subtractor

Table 5: JK Flip Flop

Table 6: SR Flip Flop

Table 7: 4-bit Binary to Gray

**INTRODUCTION**

The world nowadays is becoming more digitalize in such a way that the binary digits, 0s and 1s is getting so interesting because many operations can be achieved through the manipulations of those binary digits. Therefore, in this digital world we can analyse certain Hardware Description Languages such as VHDL which is the one that I implemented in this assignment. VHDL language is a very powerful language which is related to circuits and systems and through it we can simulate or perform many tasks for example logic operations, data processing, etc. Besides that, I had the opportunity to use the VHDL language to perform tasks such as Multiplexer, Demultiplexers, 1-bit Full Adders, Subtractors, JK and SR Flip Flops, and 4-bit Binary to Gray converters.

To explore this lab report assignment, it is important to have a solid understanding and a theoretical background foundation. Multiplexers and demultiplexers are important components in digital circuits. Multiplexers allow us to choose from multiple inputs and take it toward a single output signal while in demultiplexers we have a single input that is directed toward multiple output signals.

Full adders and subtractors are involved in arithmetic operations. We can perform some operations such as addition and subtraction using binary numbers.

JK and SR flip-flops are related to memory and sequential logic because they both can store and control the states in digital systems. Besides that, they both have the capacity for storage and synchronization.

Finally, the 4-bit Binary to Gray code converter where we simply convert binary numbers to Gray which is important in digital communication.

# **OBJECTIVES**

1. Demonstrate the HDL codes for an 8X1 Multiplexer and 1X8 Demultiplexer and verify its functionality.
2. Demonstrate the HDL code to describe the functions of a full Adder and subtractor.
3. Demonstrate the HDL codes for SR and JK flip flops and verify their functionality.
4. Demonstrate the HDL code for the 4-bit Binary to Gray code converter.

# **MODULE CODES**

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Figure 1: Multiplexer and Demultiplexer

Module: Multiplexer 8-to-1

My VHDL entity name is MUX\_8\_to\_1.

* Eight input signals have been defined (F0 to F7).
* Three select signals are defined in the code (S from 0 to 2).
* One output signal named Y.
* I added a conditional assignment to direct the selected input to the output based on the value of S.
* I finally implemented a suitable testbench file where I used various combinations of input signals and select lines to prove that the output is working smoothly.

Module: Demultiplexer 1-to-8

My VHDL entity name is DEMUX\_8\_to\_1.

* One input signal has been defined (I).
* Three select signals are defined in the code (S from 0 to 2).
* Eight-bit output signal named F.
* I created a suitable signal assignment that distributes the input signal to the correct output line based on S.

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Figure 2: Full Adder Dataflow Modelling and Full Subtractor

Module: Full Adder

My VHDL entity name is Full Adder.

* Three inputs have been implemented in the module file which are A, B, Cin(Carry-in).
* Two outputs have been used which are Sum and Cout(Carry-out).
* XOR logic has been used for sum.
* AND-OR has been used for carry-out.

Module: Full Subtractor

My VHDL entity name is Full Subtractor.

* Three inputs have been implemented in the module file which are A, Bin (borrow-in).
* Two outputs have been used which are Diff and Bout (borrow-out).
* XOR logic has been used for difference and borrow out.

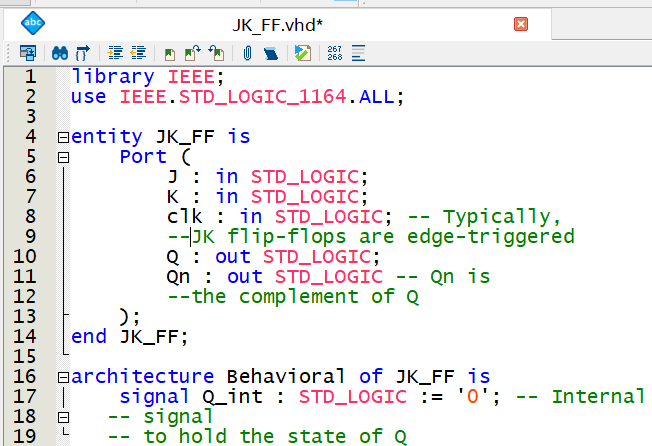
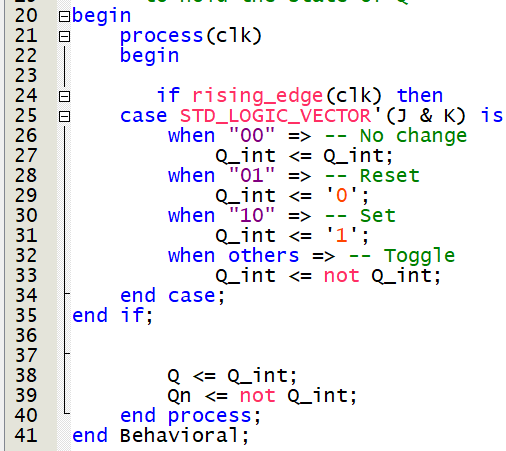
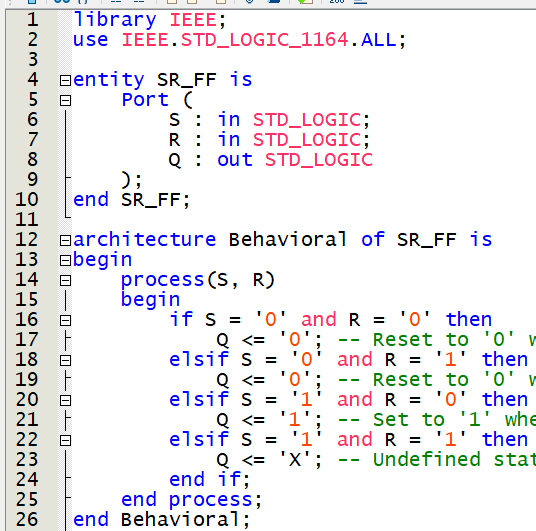
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Figure 3: SR and JK Flip Flops

Module: SR Flip Flop

My VHDL entity name is SR\_FF.

* Two inputs have been implemented in the module file which are S(set), R(reset).
* One output has been used which is Q.

Module: JK Flip Flop

My VHDL entity name is JK\_FF.

* Three inputs have been implemented in the module file which are J, K, clk (clock).
* I developed a process block where I set the clk (clock) as rising edge and I defined the conditions or behavior of Q and Qn(Complement of Q) based on the inputs such as J and K.

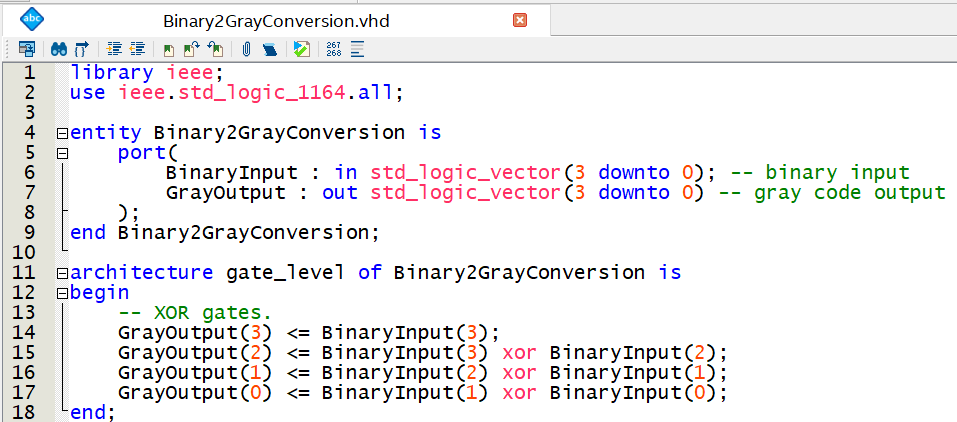
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Figure 4: Binary2GrayConversion

Module: Binary2GrayConversion

My VHDL entity name is Binary2GrayConversion.

* One input has been implemented in the module file which is the 4-bit input (BinaryInput).
* One output has been used which is the 4-bit gray output (GrayOutput).
* A screenshot of a computer code

  Description automatically generatedXOR gates has been used to convert from each digit or bit of the binary to the correspondent gray code.

Figure 5: Full Adder with Process Statement

Module Code: Full Adder with process

My VHDL entity name is FullAdder.

* Three inputs have been implemented in the module file which are A, B, and Cin.
* Two outputs have been used which ae Sum (represents the sum bit of the addition) and Cout (represents the carry-out bits).
* The process statement into the behavioral architecture is sensitive to changes to any input (A, B, Cin).
* We calculate the Sum inside the process through an XOR operation whereas for Cout we use a combination of OR and AND.

# **TESTBENCH FILES**A screenshot of a computer program Description automatically generated

Figure 6: Testbenches: Multiplexer and Demultiplexer

**Testbench: 1\_to\_8 Demultiplexer.**

* I used a single input which is “I” and 3-bit selected signal which is “S”;
* The output is an 8-bit vector which is “F”.
* My testbench for the demultiplexer goes through different selected values, S, to test the input, “I”, across the 8-bit output.

**Testbench: Multiplexer 1\_to\_8.**

* Eight inputs have been implemented from F0 to F7, and 3-bit selected signal which is “S”;
* There is only one single output, “Y”.
* My testbench tests various input combinations and it goes through different selected signals.

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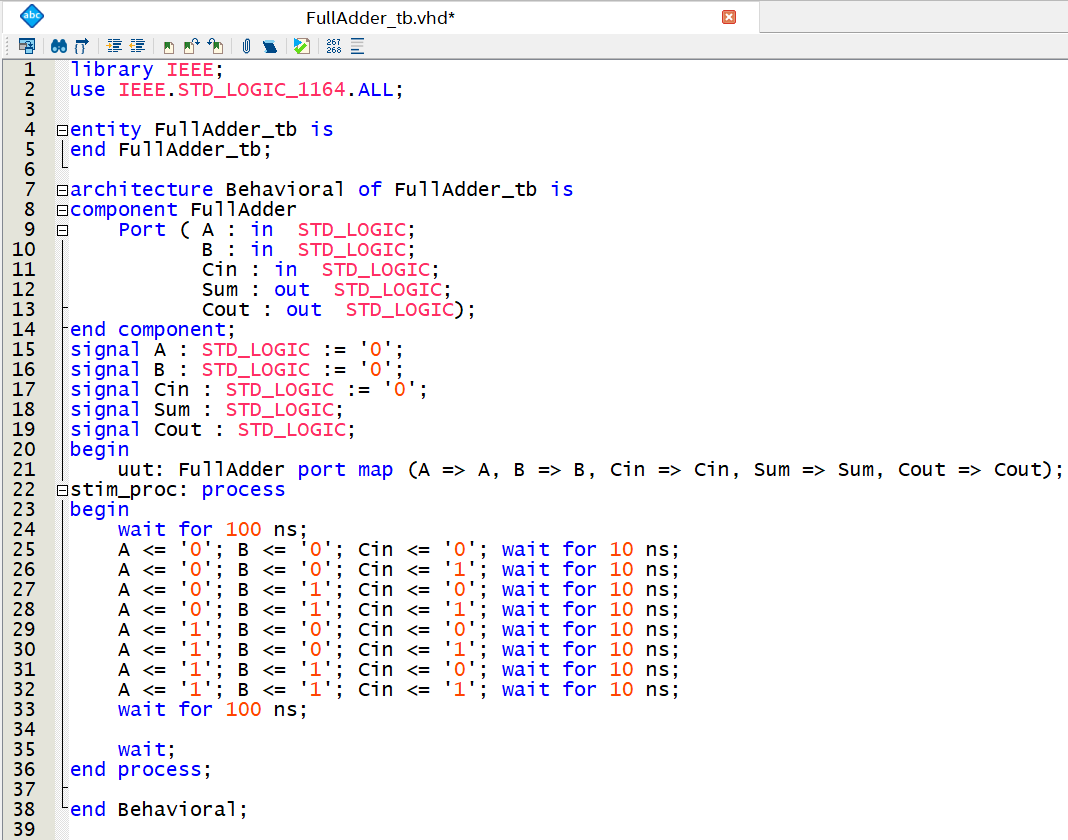
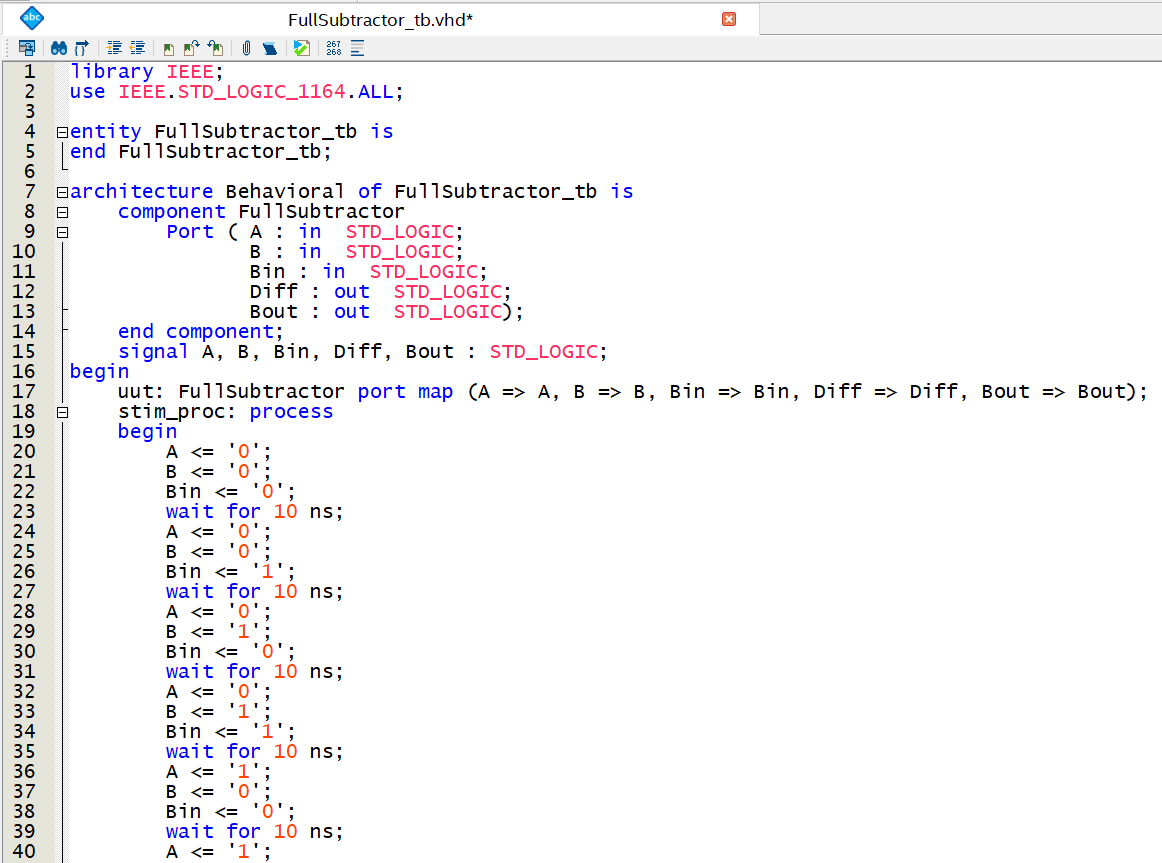
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Figure 7: Testbenches: Full Adder Dataflow Modelling and Full Subtractor

**Testbench: Full Adder**

* Three inputs which are A, B, and Cin (carry-in).
* Two outputs that are Sum and Cout (carry-out).
* In the testbench we have all the possible combinations of the inputs to test the full adder functionality.

**Testbench: Full Subtractor**

* Three inputs which are A, B, and Bin (borrow-in).
* Two outputs which are Diff (difference) and Bout (borrow-out).
* My testbench tests all the possible combinations of inputs to test the full subtractor functionality.

A screenshot of a computer program

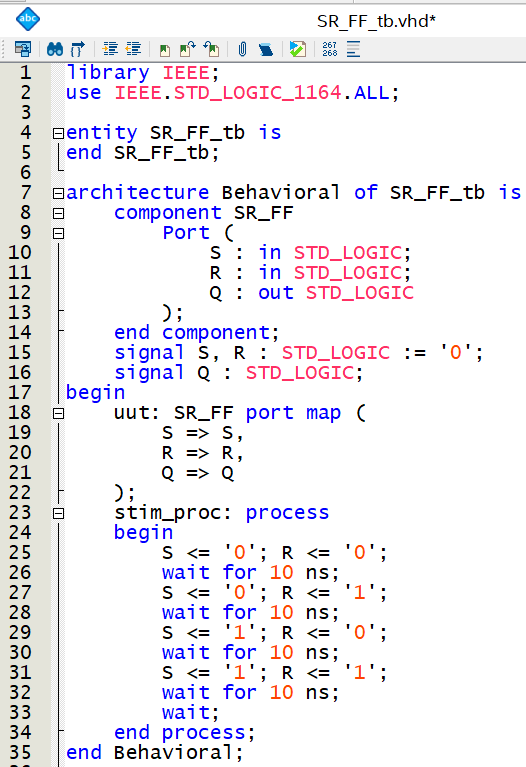
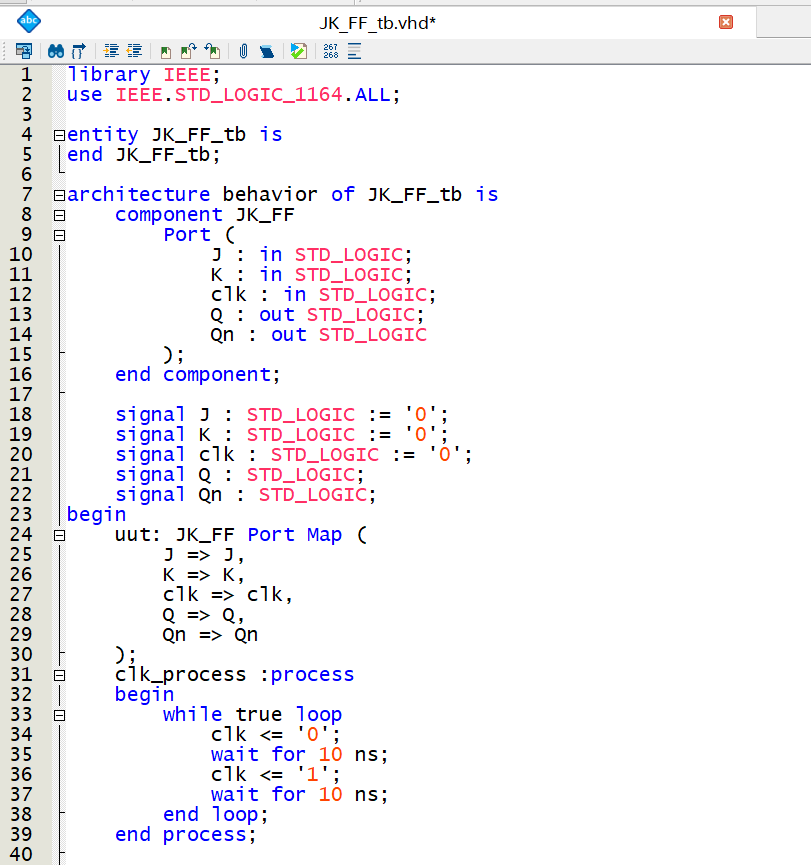
Description automatically generatedFigure 8: Testbench for Full Adder Behavioral Model

**Testbench: Full Adder**

* Three inputs which are A, B, and Cin (carry-in).
* Two outputs that are Sum and Cout (carry-out).
* In the testbench we have all the possible combinations of the inputs to test the full adder functionality.
* The input signals are all initiated from zero (input signal).

Figure 9: Testbenches: SR and JK Flip Flop

A screen shot of a computer program

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**Testbench: SR Flip Flop**

* Two inputs which are S and R.
* Only one output, which is Q.
* My testbench test all the condition of Set and Reset inputs to visualize the changes in the flip flop.

**Testbench: JK Flip Flop**

* Three inputs which are J, R, and clk (clock signal).
* Two outputs, which are Q, and Qn(a complement of Q).
* My testbench test all the condition of J and RK inputs to visualize the changes in the flip flop which can be Set, Reset, No change, and Toggle.

A screenshot of a computer code

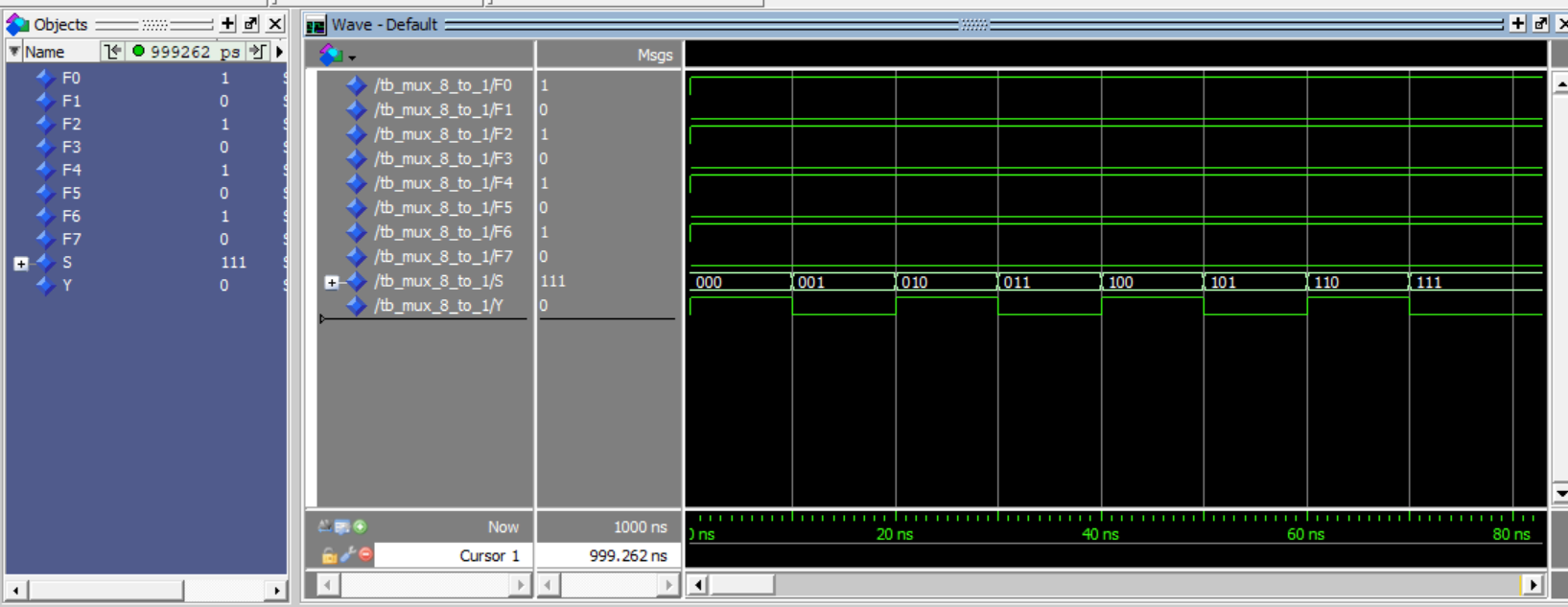
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Figure 10: Testbench for Binary to Gray Converter

**Testbench: 4-bit Binary to Gray converter**

* A single input which is 4-bit Binary Input.
* A single output which is 4-bit Gray code.
* My testbench tests the possible 4-bit binary values that correspond to each 4-bit Gray code.

# **RESULTS**

Table 2: Multiplexer

|  |  |  |
| --- | --- | --- |
| Inputs, F | Select, S | Output, Y |
| 1 | 000 | F0 |
| 0 | 001 | F1 |
| 1 | 010 | F2 |
| 0 | 011 | F3 |
| 1 | 100 | F4 |
| 0 | 101 | F5 |
| 1 | 110 | F6 |
| 0 | 111 | F7 |

Figure 11: Waveform for Multiplexer

Table 2: Demultiplexer

Figure 12: Waveform for Demultiplexer

|  |  |  |
| --- | --- | --- |
| I (input) | S (select) | F (output) |
| 1 | 000 | 00000001 |
| 1 | 001 | 00000010 |
| 1 | 010 | 00000100 |
| 1 | 011 | 00001000 |
| 1 | 100 | 00010000 |
| 1 | 101 | 00100000 |
| 1 | 110 | 01000000 |
| 1 | 111 | 10000000 |

A screen shot of a computer

Description automatically generatedTable 3: Full Adder (Same for both styles)

Figure 13: Waveform for Full Adder Dataflow Model

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Cin | Sum | Cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

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Figure 14: Waveform for Full Adder Behavioural Model

Table 4: Full Subtractor

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Bin | Diff | Bout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

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Figure 15: Waveform for Full Subtractor

A screenshot of a computer

Description automatically generatedTable 5: JK Flip Flop

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| J | K | clk | Q | Qn |
| 0 | 0 | High | 0 | 1 |
| 0 | 1 | High | 0 | 1 |
| 1 | 0 | High | 1 | 0 |
| 1 | 1 | High | 1 | 0 |

Figure 16: Waveform for JK FF

Table 6: SR Flip Flop

|  |  |  |
| --- | --- | --- |
| S | R | Q |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | X |

A screen shot of a computer

Description automatically generated

Figure 17: Waveform for SR FF

Table 7: 4-bit Binary to Gray

|  |  |
| --- | --- |
| Binary | Gray |
| 0000 | 0000 |
| 0001 | 0001 |
| 0010 | 0011 |
| 0011 | 0010 |
| 0100 | 0110 |
| 0101 | 0111 |
| 0110 | 0101 |
| 0111 | 0100 |
| 1000 | 1100 |
| 1001 | 1101 |
| 1010 | 1111 |
| 1011 | 1110 |
| 1100 | 1010 |
| 1101 | 1011 |
| 1110 | 1001 |
| 1111 | 1000 |

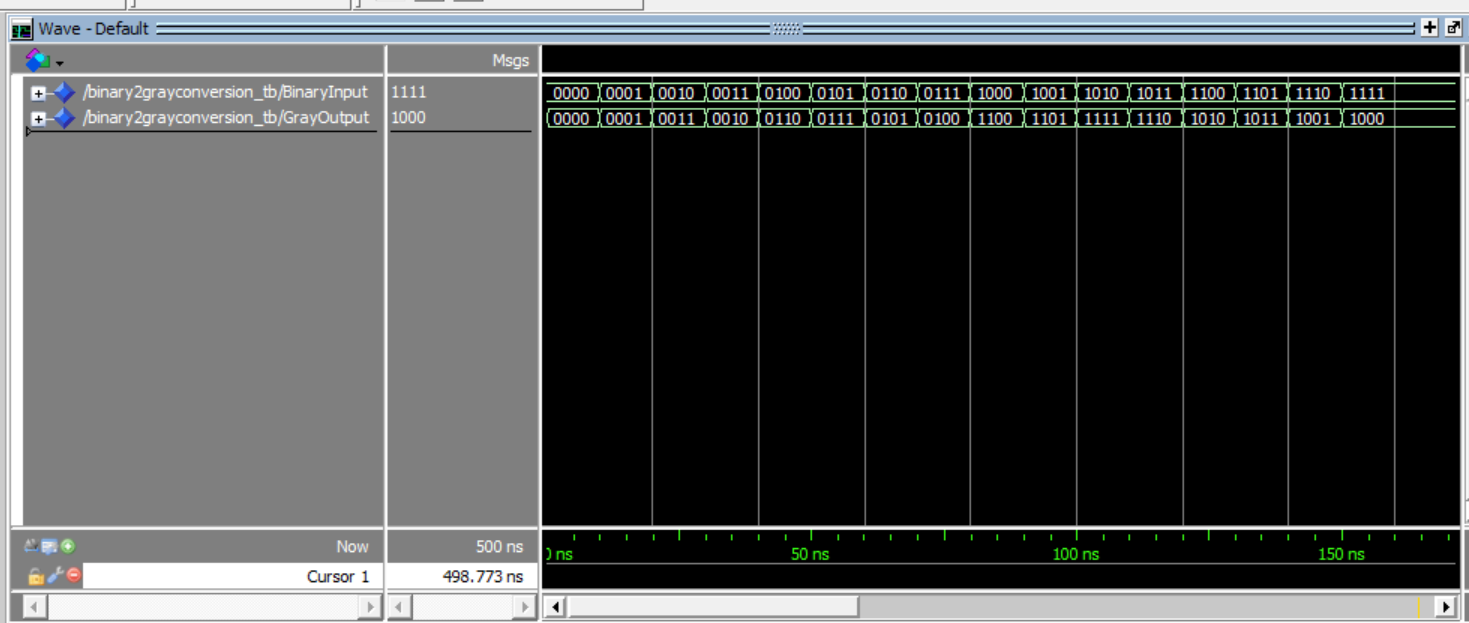


Figure 18: Waveform for 4-bit Binary to Gray

# **DISCUSSION**

I am going to conduct a discussion separately from each component based on the output obtained from the truth table and their respective waveforms:

**MULTIPLEXER 8x1**

In the waveform for the multiplexer from waveform 1, we can appreciate an alignment on what a multiplexer should look like. Besides that, that waveform indicates a proper selection of the inputs which means that it shows the selection of the input starting from the first one until the last one (F0 to F7) in which each one is assigned to a value that is going to direct the output. The select line S is the one that controls the input that is going to be connected to the output Y. Moreover, the observer behaviour in the waveform effectively matches the truth table where each combination of the select lines is linked to the input that is going to direct or take the output Y. As an example, when the select, S is assigned to 001, then the input F1 which is 0 is going to go to the output Y which is going to be zero as well. In the waveform, you can observe how the set of inputs is reflected from the active to low signal as we go through each select line.

**DEMULTIPLEXER 1x8**

The behaviour of the demultiplexer is the exact opposite of the multiplexer because, in a demultiplexer as the one that is illustrated in Waveform 2, we consider or take only a single input that is going to be distributed to the output based on the selected line, S. In my project, I set the input as one which is being taken as an input and it is going to be directed towards the corresponding output based on the select value. The waveform validates the behaviour of the truth table where the more we get different select lines in binary, it will affect the location of the input which is going to be changing its position. As an example, if the input I, which is 1 decides to target the select line 000, we will get 00000001 which means that we will have the LSB set as 1 while the other will remain zero as stated in the module code for demultiplexer in figure 1.

**FULL ADDER**

In waveform 3, we can observe that it is an implementation of the binary values such as A, B, and Cin which represent the addition of the three variables A, B, and Cin. In the waveform, we can track the value of the variable inputs which are all set to zero according to the waveform’s figure 3 since it is the beginning of the stage where all of them are zero. Let us analyze a case where we have the values of A=0, B=1, Cin=0. Basically, in this situation, to get the Sum and the Cout we must follow the next requirements:

0+1 is equal to 1, now when we make an addition of that 1 plus 0, we will get 1 in the sum while we won't have any carry out which is going to give us 0, so basically that example summarizes the behaviour of the full adder as it also matches with the truth values in the table which correspond to the waveform displayed accordingly. Every possible combination of the variable inputs corresponds to the sum and carry out. On the other hand, there is another style of full adder where I included a process statement that contains the flow on how the changes will be made according to the addition.

**FULL SUBTRACTOR**

For waveform 4, we can see an illustration of what a full subtractor looks like where I implemented three variables such as A, B, and Bin. The waveform for the full subtractor starts from zero, and so all the variables. If we move the point in such a place where A and B are equal to zero while the Bin is set to 1. The Diff (difference), and the Bout (borrow out) will be 1 as well. This is because if we subtract zero (A) minus zero (0) is going to be zero, so if we have zero (B) minus 1 we will need to have a borrow value from Bout which is one and the difference is going to be 1.

We can observe that the truth table for full subtractor matches with the waveform 4 where we initially set all the variables as zero, and that can be proved and shown in the truth table. The waveform represents accurately the binary subtraction process indicating whether a borrow is required for each one of the inputs as I explained in the example mentioned earlier.

**JK FLIP FLOP**

In JK flip-flop flop there are multiple conditions, but one of the most important ones is the toggle behaviour which can be reflected in the waveform provided n waveform Figure 5. Starting with the toggle behaviour when J and K are high, then we will get the present state, Q as low while the next state is going to be high when the clock is low. In another case, using the same condition when the clock is high as well as J and K the Q value is going to be high whereas the Qn will be low. This behaviour of the JK flip flop can be observed in the waveform which matches with the truth table of the JK flip flop.

**SR FLIP FLOP**

We can identify the waveform for SR Flip Flop in waveform 6 which demonstrates the set and reset behaviour provided in the truth table for SR. I implemented only three conditions in the waveform as we have in the truth table. As an example, we can observe in the table the condition where the S is high and the R is low, the final value of Q is going to be set to high when the clock is not rising. On the other hand, when the S is low and the R is high, then the Q will be low when the clock is rising. Basically, you can see how the truth table is fulfilled based on the waveform defined for SR Flip Flop.

**BINARY TO GRAY**

In the waveform for Binary to Gray, we can appreciate a direct conversion from Binary to Gray output. The behaviour behind that conversion is that, as the input from any binary is changing, we can observe how the output of Gray values is being adjusted or aligned based on the binary input which is due to the implementation of the XOR gate that has been used in the process of conversion from binary to Gray. In the waveform, we have a proper validation of the correct implementation of 4-bit binary input to its corresponding Gray equivalent output.

# **CONCLUSION**

I successfully demonstrated the application of all components such as full adder, full subtractor, JK, and SR flip flop, as well as the 4-bit binary to Gray conversion by using VHDL code simulation. Besides that, I was able to get suitable waveforms for each of them. So, I explored and analyzed the validation and accuracy of those waveforms, being able to compare them with the truth table for every component. The truth tables and the waveforms are matched which is an achievement of completing the application of this lab assignment.

Finally, I was able to fully understand the process behind all the components as well as gain some knowledge in the use of the software Quartus Prime where I implemented the lab project. The VHDL language is a powerful tool that helped me in designing the components. I gained a lot of understanding of the techniques of using VHDL coding and I am looking forward to involving myself in future projects or labs where I can use VHD and be able to explore a lot more about designing and testing the logic of digital circuits.

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