Computer Architecture
CS 325 - 001
Department of Physics and Computer Science
Medgar Evers College
Exam 1 - Part A

Instructions:

- **The exam requires completing a set of tasks within 90 minutes.**
- **Write your solutions to tasks 1 through 5 in the text file 'answers.txt'.**
- **Instructions for task 6 will be provided once part A is submitted.**
- **Use the IAS instruction set when necessary:**
- **Notes are not allowed.**
- **Cheating of any kind is prohibited and will not be tolerated.**
- **Violating and/or failing to follow any of the rules will result in an automatic zero (0) for the exam.**

TO ACKNOWLEDGE THAT YOU HAVE READ AND UNDERSTOOD THE INSTRUCTIONS ABOVE, PRINT YOUR NAME AND THE DATE ON YOUR SUBMISSIONS

Grading

Section	Maximum Points	Points Earned
1	3	
2	3	
3	3	
4	3	
5	4	
6	4	
Total	20	

1. **Provide the full name and purpose of all the registers of the IAS computer.**

2. **Convert each of the following numbers to the requested base. You must show work to receive full credit.**

   a. $E6A9B_{16}$ **to binary**

   b. 101101_2 **to decimal**

   c. 10011110101110_2 **to hexadecimal**

   d. 87_{10} **to binary**

3. **Find the twos-complement of each binary number. You must show work to receive full credit.**

   a. 001000011000 **b. 110001001000** **c. 011101001001** **d. 101001010000**

4. **Write an IAS program, in hexadecimal, of the statement below, given L, M, and N are the addresses C3, 44, and 2D, respectively**

$$\mathbf{L} = \frac{\mathbf{N}(2\mathbf{N}+3)}{\mathbf{M}}$$

5. **Using the list of instruction commands below, trace the following code, starting from address 000, by listing sequential changes to the registers and memory.**

Memory:

000: 0100505006	**001: 0C00721005**	**002: 090050B007**	**003: 0A00014000**
004: 2100500000	**005: 0000000042**	**006: 000000001E**	**007: 0000000004**

- **IAS Instruction Set**

Mnemonic	Opcode	Description
LMA	0A	Transfer contents from MQ to AC
LDM	09	Transfer M(X) to MQ
STA	21	Transfer contents from AC to memory location X
LDA	01	Transfer M(X) to AC
LDN	02	Transfer -M(X) to AC
ALD	03	Transfer |M(X)| to AC
ALN	04	Transfer -|M(X)| to AC
BRL	0D	Takes next instruction from left half of M(X)
BRR	0E	Takes next instruction from right half of M(X)
BPL	0F	If AC >= 0, takes next instruction from the left half of M(X)
BPR	10	If AC >= 0, takes next instruction from the right half of M(X)
ADD	05	Add M(X) to AC; put result in AC
AAD	07	Add |M(X)| to AC; put result in AC
SUB	06	Subtract M(X) from AC; put result in AC
ASB	08	Subtract |M(X)| from AC; put result in AC
MUL	0B	Multiply M(X) by MQ; put most significant bits of result in AC; least significant in MQ
DIV	0C	Divide AC by M(X); put quotient in MQ and remainder in AC
LSH	14	Multiply AC by 2
RSH	15	Divide AC by 2
STL	12	Transfer AC[28:39] to M(X)[8:19]
STR	13	Transfer AC[28:39] to M(X)[28:39]
HLT	00	Halts