CS203 - Lab 5/Course project

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Project Proposal:

1. Title: **Wallace Tree Multiplier**
   Objective:
   Implement Wallace Tree Multiplier for two 8-bit numbers using Verilog.
   Implementation:
   Implementing a dataflow model in Verilog for Wallace Tree Multiplier using Half Adder and Full Adder. Execute stage wise to simplify and obtain the final result.
   - For unsigned numbers, we will obtain a 16-bit answer.
   - For signed numbers, we will check the MSB, create cases and multiply accordingly.

   Functionality:
   We want to create a multiplier in which we can multiply any number with 8 bits.
   Note: Further scope of our project can be passing the output as input for successive multiplication (sequential design).

2. Title: **Smart Car Parking System**
   Objective:
   Design a car parking system with various functionality for efficient control and systematic organisation.
   Implementation:
   Based on weight, we can allot vehicles on different floors. Heavier the vehicle i.e. higher the value of the number, lower the floor assigned and vice versa.
   To avoid congestion, we can only allot a vehicle based on the positive edge of the clock.
   By using a comparator, we can allot the floor.
   By using a counter we can check whether or not a floor can allot more vehicles.

3. Title: **Fibonacci number generator**
   Objective:
   Finding the Nth Fibonacci number using sequential design.
   Implementation: Using Verilog, we will generate fibonacci numbers using adders sequentially and will feedback the output as input for further iterations. Overflow limit will be 16-bits.
   Functionality:
   Finding Fibonacci numbers for various different values of N in the testbench.