EEL 4768: Computer Architecture
Project #2 Virtual Memory Simulator

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In this project, you will write a code that simulates the operation of the virtual memory. The code simulates the Page Table, the TLB and the Frame Table. To keep the project simple, we'll assume there is only one process running and, therefore, there's one page table in the simulation. Below are the parameters of the virtual memory system we're considering.

- Virtual address space — 1 MB = 2^20 Bytes = 1,048,576 Bytes
- Virtual address — 20-bit
- Physical address space — 256 KB = 2^18 Bytes = 262,144 Bytes
- Physical address — 18-bit
- Page size — 1 KB = 2^10 bytes = 1024 Bytes
- Number of virtual pages — 2^20 / 2^10 = 2^10 = 1024 virtual pages
- Number of physical pages — 2^18 / 2^10 = 2^8 = 256 physical pages (frames)

In the simulation, we're using all the design criteria we've studied. Pages are placed in a fully associative way in the memory. We use the write-back scheme with the dirty-bit optimization. The replacement scheme is the Least Recently Used (LRU) approximation using the reference bit.

Below are the criteria of the TLB that caches the recently used translations.

- Size — 8 translations
- Fully associative — Any translation can go anywhere in the TLB
- Block size — 1 translation (copy one translation at a time to/from the page table)
- Write policy — write-back (update D,R bits in the TLB only; update the page table upon eviction of the translation)

The three data structures shown below represent the main data of the simulation.

```
#define VPAGES          1024        // number of virtual pages
#define TLB_SIZE        8           // TLB size
#define FRAMES          256         // number of frames

unsigned int PageTable[VPAGES][4];
unsigned int TLB [TLB_SIZE][5];
unsigned int FrameTable[FRAMES];
```

Main Data Structures of the Simulation

This is the format of the main data structures of the simulation. The simulation keeps track of 8 translation entries in the TLB, 1024 virtual pages in the Page Table and 256 frames in the Frame Table. A frame is a page in the RAM. The frame table keeps track of our RAM space and indicates whether each frame is currently allocated or available.

Format of the TLB

Entry	Valid bit	Dirty bit	Reference bit	Tag (full virtual page number)	Frame number (physical page number)
0					
…					
7					

Format of the Page Table

Page #	Valid bit	Dirty bit	Reference bit	Frame number (physical page number)
0				
…				
1023				

Format of the Frame Table

Frame #	0	1	2	3	…	255
Allocated (y/n)	1	0	1	1	…	0

Measurements

These are the main results reported by the simulation.

TLB hit	The requested translation is found in the TLB
TLB miss	The requested translation is not in the TLB
TLB hit rate	TLB hit / (TLB hit + TLB miss)
Page table hit	Following a TLB miss, the requested page is found in the RAM
Page fault	Following a TLB miss, the requested page is found on the hard disk
Page table hit rate	Page table hit / (Page table hit + Page fault)
TLB shootdown	A translation is evicted from the TLB to make room for a new translation
Page eviction	A page is evicted from the RAM (frames) to make room for a new page
Hard disk read	A page is brought from the hard disk to the RAM
Hard disk write	A page evicted from the RAM is modified (dirty), so it's written to the hard disk

Guidelines

- Work in groups of two people (each member writes half of the requested functions; the members then review each other's codes before integrating the whole code).
- The code can be written in any language.
- The attached functions layout can be modified to suit your preference. If you plan to use a completely different functions setup, please discuss your approach with the instructor.

Deliverables

- Submit all the source files (with instructions for compilation, if needed).
- Submit a report that contains (1) a reproduction of the case studies below, (2) the answers to the requested interpretations of the case studies and, (3) a new case study that you design (e.g. investigate the frequency of clearing the reference bits; e.g. investigate a new locality pattern such as accessing pages 0, 1, 2, 1, 2, 3, 2, 3, 4, etc; or any other idea you come up with).
- Include screenshots of your results in the report
- Tabulate the results in the same format shown below
- Only one group member uploads the materials! The other group member upload a text file mentioning the group member in charge of doing the upload.

Grading Criteria (5 points)

- All the functions are written (code style and readability are graded). (2 pts)
- All the case studies listed below are reproduced and the interpretations are answered. (2 pts)
- A new case study is designed and evaluated. (1 pt)

Case Study #1 Access 5 addresses from the same page

Five random addresses from the same virtual page number (VPN=0) are accessed. In the results below, T indicates the time, which is a counter that increments by one at every access.

```
----------------------------------------
        VIRTUAL MEMORY SIMULATION
----------------------------------------
T:      1     Address: w      51          VPN: 0
T:      2     Address: r     374          VPN: 0
T:      3     Address: w     846          VPN: 0
T:      4     Address: w     219          VPN: 0
T:      5     Address: w     433          VPN: 0

--------------------------------------------------------------------------------
                           SIMULATION RESULTS
--------------------------------------------------------------------------------
TLB hits: 4             TLB misses: 1           TLB hit rate: 80.00%
TLB Shootdowns: 0       TLB Writes: 1

Pg Table accesses: 1
Pg Table hits: 0        Pg faults: 1            Pg Table hit rate: 0.00%
Pg evictions: 0         Pg Table writes: 1

Hard disk reads: 1      Hard disk writes: 0
--------------------------------------------------------------------------------
```

Interpret the results above that are marked in red. (explain why these results were obtained)

Case Study #2 Access 5 addresses from different pages

Five random addresses are accessed. They belong to five different pages.

```
----------------------------------------
        VIRTUAL MEMORY SIMULATION
----------------------------------------
T:      1     Address: w  178406          VPN: 174
T:      2     Address: r  442630          VPN: 432
T:      3     Address: w  507896          VPN: 495
T:      4     Address: r  212346          VPN: 207
T:      5     Address: r  439947          VPN: 429

--------------------------------------------------------------------------------
                            SIMULATION RESULTS
--------------------------------------------------------------------------------
TLB hits: 0             TLB misses: 5           TLB hit rate: 0.00%
TLB Shootdowns: 0       TLB Writes: 5

Pg Table accesses: 5
Pg Table hits: 0        Pg faults: 5            Pg Table hit rate: 0.00%
Pg evictions: 0         Pg Table writes: 5

Hard disk reads: 5      Hard disk writes: 0
--------------------------------------------------------------------------------
```

Interpret the results above that are marked in red.

Case Study #3 Access 20 addresses from different pages

Twenty random addresses from different pages are accessed. We selected the pages sequentially.

```
----------------------------------------
        VIRTUAL MEMORY SIMULATION
----------------------------------------
T:      1     Address: r     845          VPN: 0
T:      2     Address: w    1857          VPN: 1
T:      3     Address: w    2103          VPN: 2
T:      4     Address: w    4081          VPN: 3
T:      5     Address: w    5068          VPN: 4
T:      6     Address: w    5535          VPN: 5
T:      7     Address: w    6345          VPN: 6
T:      8     Address: r    7304          VPN: 7
T:      9     Address: w    8704          VPN: 8
T:     10     Address: w    9315          VPN: 9
T:     11     Address: r   10374          VPN: 10
T:     12     Address: r   12160          VPN: 11
T:     13     Address: w   12961          VPN: 12
T:     14     Address: r   13553          VPN: 13
T:     15     Address: w   14405          VPN: 14
T:     16     Address: r   15578          VPN: 15
T:     17     Address: w   16960          VPN: 16
T:     18     Address: r   18067          VPN: 17
T:     19     Address: w   18734          VPN: 18
T:     20     Address: r   20470          VPN: 19

------------------------------------------------------------------------------
                          SIMULATION RESULTS
------------------------------------------------------------------------------
TLB hits: 0             TLB misses: 20          TLB hit rate: 0.00%
TLB Shootdowns: 12      TLB Writes: 20

Pg Table accesses: 20
Pg Table hits: 0        Pg faults: 20           Pg Table hit rate: 0.00%
Pg evictions: 0         Pg Table writes: 20

Hard disk reads: 20     Hard disk writes: 0
------------------------------------------------------------------------------
```

Interpret the results above that are marked in red.

Case Study #4 Access 500 random addresses

500 random addresses are accessed. Read/write with the same probability of 50%.

```
-------------------------------------------------------------------------
                            SIMULATION RESULTS
-------------------------------------------------------------------------
TLB hits: 4             TLB misses: 496         TLB hit rate: 0.80%
TLB Shootdowns: 488     TLB Writes: 496

Pg Table accesses: 496
Pg Table hits: 99       Pg faults: 397          Pg Table hit rate: 19.96%
Pg evictions: 141       Pg Table writes: 397

Hard disk reads: 397    Hard disk writes: 0
-------------------------------------------------------------------------
```

Interpret the results above that are marked in red.

Case Study #5 Access 500 random addresses, all accesses are writes

500 random addresses are accessed with write operations.

```
-------------------------------------------------------------------------
                            SIMULATION RESULTS
-------------------------------------------------------------------------
TLB hits: 4             TLB misses: 496         TLB hit rate: 0.80%
TLB Shootdowns: 488     TLB Writes: 496

Pg Table accesses: 496
Pg Table hits: 83       Pg faults: 413          Pg Table hit rate: 16.73%
Pg evictions: 157       Pg Table writes: 413

Hard disk reads: 413    Hard disk writes: 157
-------------------------------------------------------------------------
```

Interpret the results above that are marked in red.

Case Study #6 1000 memory accesses; each 40 consecutive addresses from the same page

We accessed 40 random addresses from page 0, then 40 random addresses from page 1, then 40 random addresses from page 2, etc. In total, 25 pages are accessed. Each access is either read or write with 50% probability.

```
--------------------------------------------------------------------------------
                              SIMULATION RESULTS
--------------------------------------------------------------------------------
TLB hits: 975           TLB misses: 25          TLB hit rate: 97.50%
TLB Shootdowns: 17      TLB Writes: 25

Pg Table accesses: 25
Pg Table hits: 0        Pg faults: 25           Pg Table hit rate: 0.00%
Pg evictions: 0         Pg Table writes: 25

Hard disk reads: 25     Hard disk writes: 0
--------------------------------------------------------------------------------
```

Interpret the results above that are marked in red.

Show how the reported hit rate can be computed by hand.

Case Study #7 3000 memory accesses; each 10 consecutive addresses from the same page

We access 10 random addresses from page 0, then 10 random addresses from page 1, etc. In total, 300 pages are accessed. Each access is either read or write with 50% probability.

```
--------------------------------------------------------------------------------
                              SIMULATION RESULTS
--------------------------------------------------------------------------------
TLB hits: 2700          TLB misses: 300         TLB hit rate: 90.00%
TLB Shootdowns: 292     TLB Writes: 300

Pg Table accesses: 300
Pg Table hits: 0        Pg faults: 300          Pg Table hit rate: 0.00%
Pg evictions: 44        Pg Table writes: 300

Hard disk reads: 300    Hard disk writes: 44
--------------------------------------------------------------------------------
```

Interpret the results above that are marked in red.

Show how the reported hit rate can be computed by hand.

Show how the reported page evictions can be computed by hand.

Make sure you explain why all evicted pages were dirty and ended up being written to the hard disk.