**port list** :

{A B C Sum Carry Clock Scan\_clk Scan\_en cg\_en gen\_clk\_mux}

**cell list** :

{mux1 gate CLK\_B1 reg1 reg2 reg3 G1 G2 G3 G4 G5 G7 G6 reg4 reg5 B1 B2}

**pin list** :

{mux1/I0 mux1/I1 mux1/S mux1/Z mux1/VDD mux1/VSS gate/A1 gate/A2 gate/Z gate/VDD gate/VSS CLK\_B1/I CLK\_B1/Z CLK\_B1/VDD CLK\_B1/VSS reg1/D reg1/SI reg1/SE reg1/CP reg1/Q reg1/VDD reg1/VSS reg2/D reg2/SI reg2/SE reg2/CP reg2/Q reg2/VDD reg2/VSS reg3/D reg3/SI reg3/SE reg3/CP reg3/Q reg3/VDD reg3/VSS G1/A1 G1/A2 G1/Z G1/VDD G1/VSS G2/A1 G2/A2 G2/Z G2/VDD G2/VSS G3/A1 G3/A2 G3/Z G3/VDD G3/VSS G4/A1 G4/A2 G4/Z G4/VDD G4/VSS G5/A1 G5/A2 G5/Z G5/VDD G5/VSS G7/A1 G7/A2 G7/Z G7/VDD G7/VSS G6/A1 G6/A2 G6/Z G6/VDD G6/VSS reg4/D reg4/SI reg4/SE reg4/CP reg4/Q reg4/VDD reg4/VSS reg5/D reg5/SI reg5/SE reg5/CP reg5/Q reg5/VDD reg5/VSS B1/I B1/Z B1/VDD B1/VSS B2/I B2/Z B2/VDD B2/VSS}

**net list** :

{\*Logic0\* A B C Sum Carry Clock Scan\_clk Scan\_en cg\_en gen\_clk\_mux n4 n5 n6 n7 n8 n9 n10 n11 n12 n13 n14 n15 CLK mux\_clock gated\_clock}

**Netlist** :

module fulladdder (A,B,C,Sum,Carry,Clock, Scan\_clk,Scan\_en,cg\_en, gen\_clk\_mux );

input A,B,C,Clock,Scan\_clk,Scan\_en,cg\_en, gen\_clk\_mux;

output Sum,Carry;

//wire n1, n2, n3, n4, n5, n6, n7, n8, n9, n10, n11, n12, n13;

wire  n4, n5, n6, n7, n8, n9, n10, n11, n12, n13, n14, n15, CLK, mux\_clock,gated\_clock;

//clock Path - Clock - > CLK

CKMUX2SGD1BWP30P140 mux1(.I0(Clock), .I1(Scan\_clk), .S(Scan\_en), .Z(mux\_clock));

AN2SGD0BWP30P140 gate(.A1(mux\_clock), .A2(cg\_en), .Z(gated\_clock));

//LATQ\_X1M\_A9G33 icg\_latch(.G(Clock), .D(gated), .Q(gated\_clock));

//Generated clock

BUFFSGD3BWP30P140HVT CLK\_B1 (.I(gated\_clock), .Z(CLK) );

SDFQOPPSBSGD1BWP30P140HVT reg1(.D(A), .CP(CLK), .Q(n4), .SI(1'b0), .SE(1'b0));

SDFQOPPSBSGD1BWP30P140HVT reg2(.D(B), .CP(CLK), .Q(n5), .SI(1'b0), .SE(1'b0));

SDFQOPPSBSGD1BWP30P140HVT reg3(.D(C), .CP(CLK), .Q(n6), .SI(1'b0), .SE(1'b0));

XOR2SGD0BWP30P140 G1(.A1(n4), .A2(n5), .Z(n7));

XOR2SGD0BWP30P140 G2(.A1(n7), .A2(n6), .Z(n8));

//BC

AN2SGD0BWP30P140 G3(.A1(n5), .A2(n6), .Z(n9));

//AB

AN2SGD0BWP30P140 G4(.A1(n4), .A2(n5), .Z(n10));

//AC

AN2SGD0BWP30P140 G5(.A1(n4), .A2(n6), .Z(n11));

OR2SGD1BWP30P140 G7(.A1(n9), .A2(n10), .Z(n12));

OR2SGD1BWP30P140 G6(.A1(n12), .A2(n11), .Z(n13));

SDFQOPPSBSGD1BWP30P140HVT reg4(.D(n13), .CP(CLK), .Q(n14), .SI(1'b0), .SE(1'b0));

SDFQOPPSBSGD1BWP30P140HVT reg5(.D(n8), .CP(CLK), .Q(n15), .SI(1'b0), .SE(1'b0));

BUFFSGD3BWP30P140HVT B1 (.I(n14), .Z(Carry) );

BUFFSGD3BWP30P140HVT B2 (.I(n15), .Z(Sum) );

//get\_lib\_cells \*/\*BUF\*

//get\_lib\_pins tcbn22ullbwp30p140sgssg0p72vm40c\_ccs/BUFFSGD3BWP30P140HVT/\*

endmodule

**SDC** :

###############################################################################

set sdc\_version 2.1

set\_units -time ns -capacitance pF -current mA -voltage V -resistance kOhm

###############################################################################

#

# Units

# capacitive\_load\_unit           : 1 pF

# current\_unit                   : 0.001 A

# resistance\_unit                : 1 kOhm

# time\_unit                      : 1 ns

# voltage\_unit                   : 1 V

###############################################################################

set\_operating\_conditions -analysis\_type on\_chip\_variation  -library [get\_libs \

{tcbn22ullbwp30p140sgssg0p72vm40c\_hm\_lvf\_p\_ccs.db:tcbn22ullbwp30p140sgssg0p72vm40c\_ccs}]

###############################################################################

# Clock Related Information

###############################################################################

create\_clock -name sys\_clk -period 0.5 -waveform { 0 0.25 } [get\_ports {Clock}]

set\_clock\_uncertainty  0.1 [get\_clocks {sys\_clk}]

set\_clock\_transition -rise -max  0.1 [get\_clocks {sys\_clk}]

set\_clock\_transition -fall -max  0.1 [get\_clocks {sys\_clk}]

set\_clock\_transition -rise -min  0.1 [get\_clocks {sys\_clk}]

set\_clock\_transition -fall -min  0.1 [get\_clocks {sys\_clk}]

create\_clock -name test\_clk -period 2 -waveform { 0 1 } [get\_ports {Scan\_clk}]

set\_clock\_uncertainty -setup  0.54 [get\_clocks {test\_clk}]

set\_clock\_transition -rise -max  0.1 [get\_clocks {test\_clk}]

set\_clock\_transition -fall -max  0.1 [get\_clocks {test\_clk}]

set\_clock\_transition -rise -min  0.1 [get\_clocks {test\_clk}]

set\_clock\_transition -fall -min  0.1 [get\_clocks {test\_clk}]

set\_clock\_groups -asynchronous -name G1 -group [get\_clocks {sys\_clk}] -group \

[get\_clocks {test\_clk}]

###############################################################################

# Point to Point exceptions

###############################################################################

###############################################################################

# External Delay Information

###############################################################################

set\_input\_delay  0.25 [get\_ports {A}]

set\_input\_delay  0.25 [get\_ports {B}]

set\_input\_delay  0.25 [get\_ports {C}]

set\_input\_delay  0.25 [get\_ports {Scan\_en}]

set\_input\_delay  0.25 [get\_ports {cg\_en}]

set\_input\_delay  0.25 [get\_ports {gen\_clk\_mux}]

set\_output\_delay  0.25 [get\_ports {Sum}]

set\_output\_delay  0.25 [get\_ports {Carry}]

set\_load -pin\_load  0.5 [get\_ports {Sum}]

set\_load -pin\_load  0.5 [get\_ports {Carry}]

set\_input\_transition -rise -min  0.1 [get\_ports {A}]

set\_input\_transition -fall -min  0.1 [get\_ports {A}]

set\_input\_transition -rise -max  0.1 [get\_ports {A}]

set\_input\_transition -fall -max  0.1 [get\_ports {A}]

set\_input\_transition -rise -min  0.1 [get\_ports {B}]

set\_input\_transition -fall -min  0.1 [get\_ports {B}]

set\_input\_transition -rise -max  0.1 [get\_ports {B}]

set\_input\_transition -fall -max  0.1 [get\_ports {B}]

set\_input\_transition -rise -min  0.1 [get\_ports {C}]

set\_input\_transition -fall -min  0.1 [get\_ports {C}]

set\_input\_transition -rise -max  0.1 [get\_ports {C}]

set\_input\_transition -fall -max  0.1 [get\_ports {C}]

set\_input\_transition -rise -min  0.1 [get\_ports {Clock}]

set\_input\_transition -fall -min  0.1 [get\_ports {Clock}]

set\_input\_transition -rise -max  0.1 [get\_ports {Clock}]

set\_input\_transition -fall -max  0.1 [get\_ports {Clock}]

set\_input\_transition -rise -min  0.1 [get\_ports {Scan\_clk}]

set\_input\_transition -fall -min  0.1 [get\_ports {Scan\_clk}]

set\_input\_transition -rise -max  0.1 [get\_ports {Scan\_clk}]

set\_input\_transition -fall -max  0.1 [get\_ports {Scan\_clk}]

set\_input\_transition -rise -min  0.1 [get\_ports {Scan\_en}]

set\_input\_transition -fall -min  0.1 [get\_ports {Scan\_en}]

set\_input\_transition -rise -max  0.1 [get\_ports {Scan\_en}]

set\_input\_transition -fall -max  0.1 [get\_ports {Scan\_en}]

set\_input\_transition -rise -min  0.1 [get\_ports {cg\_en}]

set\_input\_transition -fall -min  0.1 [get\_ports {cg\_en}]

set\_input\_transition -rise -max  0.1 [get\_ports {cg\_en}]

set\_input\_transition -fall -max  0.1 [get\_ports {cg\_en}]

set\_input\_transition -rise -min  0.1 [get\_ports {gen\_clk\_mux}]

set\_input\_transition -fall -min  0.1 [get\_ports {gen\_clk\_mux}]

set\_input\_transition -rise -max  0.1 [get\_ports {gen\_clk\_mux}]

set\_input\_transition -fall -max  0.1 [get\_ports {gen\_clk\_mux}]

###############################################################################

# POCV Information

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