Computer Architecture

HW2 Report

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```
Inferred memory devices in process
        in routine ALU line 236 in file
                '/home/raid7_2/userb09/b9502158/HW2/01_RTL/HW2.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      done_reg       | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|   shifted_reg_reg   | Flip-flop |  64   |  Y  | N  | Y  | N  | N  | N  | N  |
|      state_reg      | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|    operand_a_reg    | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|    operand_b_reg    | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
|     counter_reg     | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb09/b9502158/HW2/01_RTL/ALU.db:ALU'
Loaded 1 design.
Current design is 'ALU'.
ALU
design_vision>
```