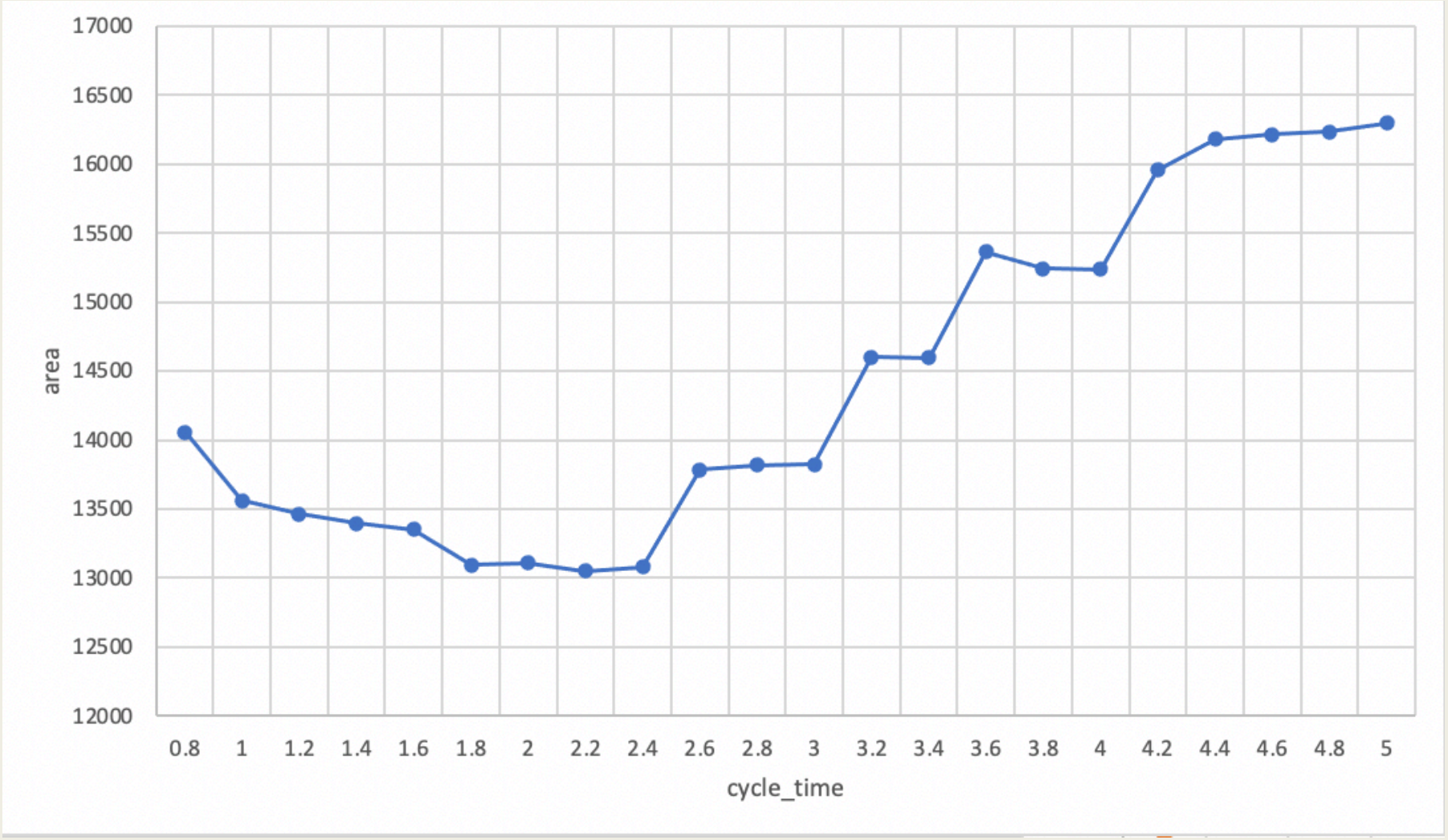
4/13 MEETING

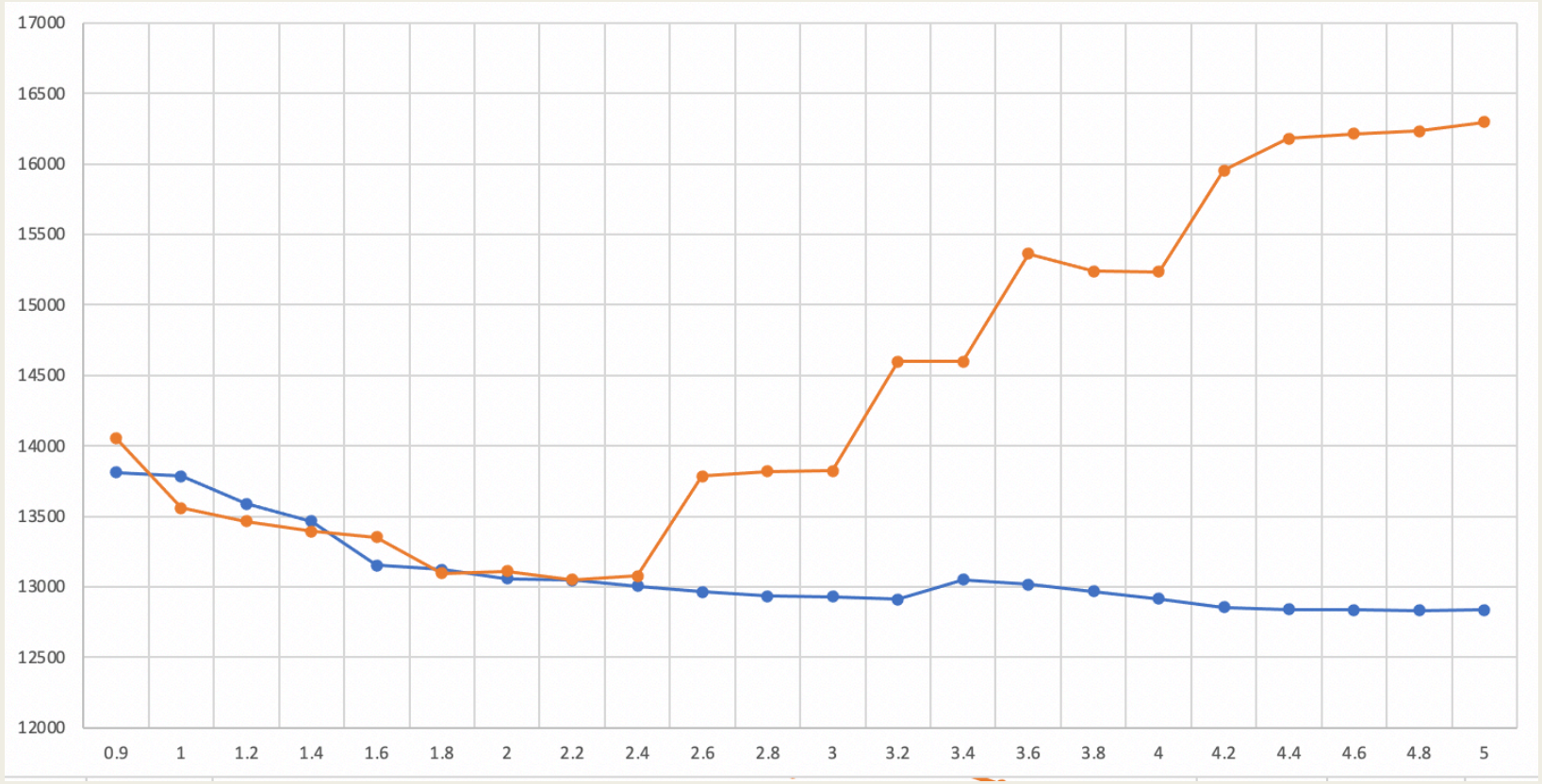
Problem : CT越高 Area越高



Solved!

更改 syn_rule.tcl

set_clock_uncertainty
set_input_transition
set_clock_transition
都設為常數
(blue : after)
(orange : before)



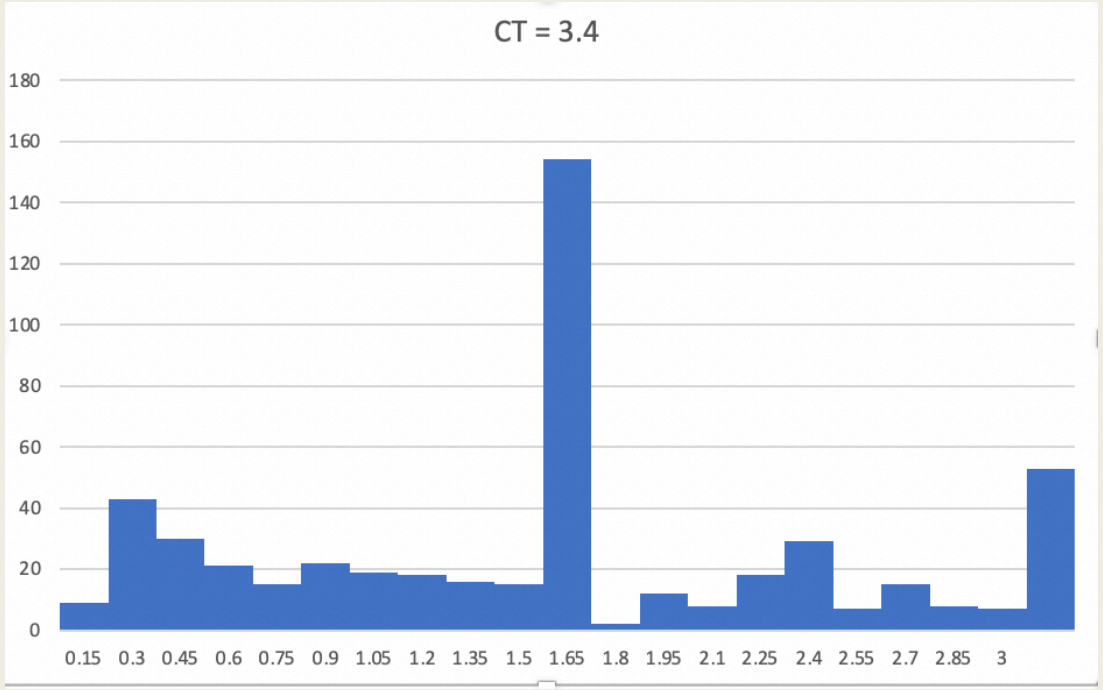
Problem：加入EDFF合成失敗

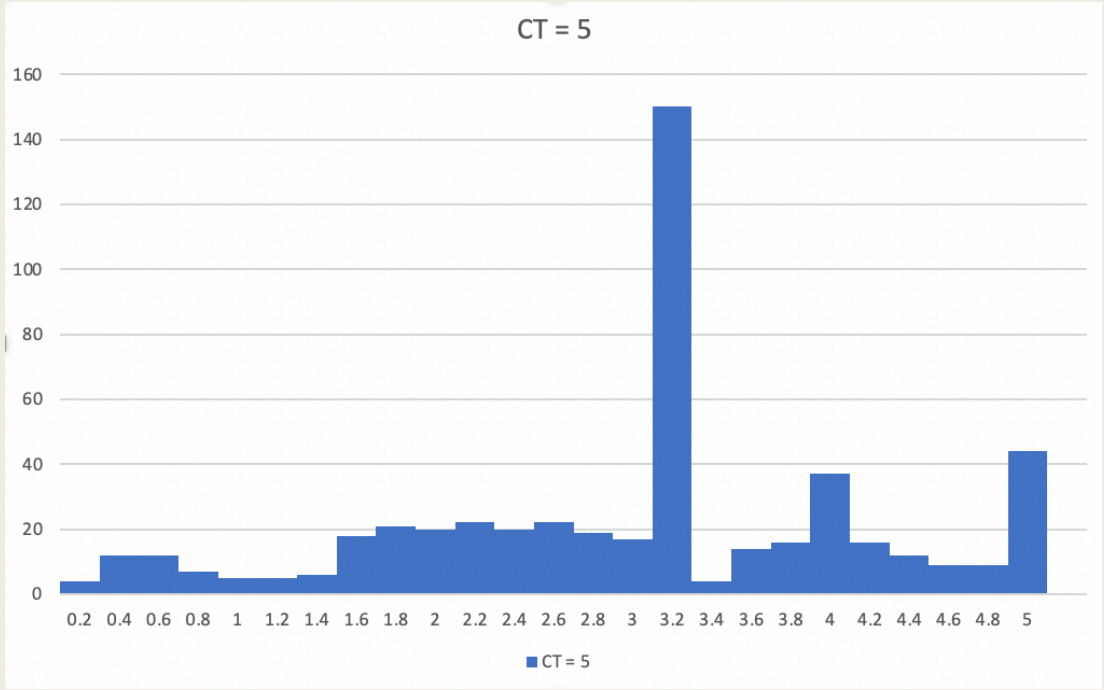
- Notice : 從 memory 讀取資料後，過早傳到下一級pipeline，像是 flip-flop 不 work，原因可能是用外部的module（ ？
- Solution : 不padding memory related flip-flop

PARAMETER

- Duty cycle : 20%
- Padding ratio : 20% (without memory related flipflop)
- Minimum cycle time (no edff) : 0.9
- Success padding cycle time (with edff) : 3.5ns & 5ns

Analysis : slack time distribution (critical)





Analysis : slack time distribution (critical)