Analysis of Soft Error Rate in Flip-Flops and Scannable Latches

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***Abstract*—Soft the critical charge by increasing the gate capacitance while errors are gaining importance as technology scales. Flip-flops, an important component of pipelined architectures, are becoming more susceptible to soft errors. This work analyzes soft error rates on a variety of flip-flops. The analysis was performed by implementing and simulating the various designs in 70 nm, 1V CMOS technology. First, we evaluate the critical charge for the susceptible nodes in each design. Further, we implement two hardening techniques and present the results. One attempts to increase the other improves the overall robustness of the circuit by replicating the master stage of the master slave flip-flops, which leads to reduced power and area overhead.**

I. Introduction

Soft errors pose a major challenge for the continued scaling of CMOS circuits. They result due to the excess charge carriers induced primarily by external radiations. The circuit however is not permanently damaged by such radiations. The rapid technology scaling has accelerated the reduction in the capacitance of storage nodes and supply voltages thus resulting in increased susceptibility of latches and flip-flops to soft errors. These circuits are more difficult to protect than memories by conventional logic methods like parity and error correcting codes. Also as frequency increases, the probability of a flip-flop to latch on to an error increases [7]. So analysis of traditional flip-flop designs for soft error rates and improvising them for protection against soft errors is of paramount importance.

In this paper, we present a detailed analysis of effect of soft errors in different styles of flip-flops designed in 70nm, 1V CMOS technology. A variety of flip-flop designs are analyzed and evaluated for critical charge on the susceptible nodes.

Earlier work on soft errors has focused on quantifying the circuit susceptibility radiations in terms of the critical charge required to charge or discharge a particular node and the sensitive node area [1]. Various methods for reducing soft error rate (SER) in deep sub-micron integrated circuits were discussed in [2]. Further soft error tolerant techniques like space and time redundancy were proposed [3]. Initially most of the work on soft errors focused on SRAM and DRAM memory cells as they are more susceptible to soft errors. But susceptibility of latches and flip-flops too has increased with scaling. So equal attention has been given to the protection of latches and register files recently [2], [4-6]. These works have focused on building new latches and register files that are protected against such errors. But in our work we concentrate on evaluating these effects in the existing flip-flops and propose optimizations to make these designs soft error tolerant.

The rest of the work is organized in the following way. Section II gives a brief background on how soft errors are caused, their importance in flip-flops and the metrics used in this work. Section III details on each of the different designs considered here. Optimizations are discussed in Section IV and the results are presented.

II. Background

A. Soft error metrics

Soft errors could be induced through three different radiation sources, alpha particles from the naturally occurring radioactive impurities in device materials, high-energy cosmic ray induced neutrons and neutron induced 10B fission [9]. Recent works [1], [10-11] have shown the effect of the technology scaling on soft errors. In [12], a study on the radiation flux noted that particles of lower energy occur far more frequently than particles of higher energy. Thus smaller CMOS device are easily affected by lower energy particles, leading to a much higher rate of soft errors. Soft errors occur when the collected energy Q at a particular node is greater than a critical charge $Q_{critical}$, which results in a bit flip at that node. This concept of critical charge is used for the estimation of soft error rate (SER). According to model proposed in [1]

$$\text{SER} \propto N_{flux} \times CS \times \exp\left(\frac{-Q_{critical}}{Q_s}\right)$$

Where N_{flux} is the intensity of the Neutron Flux, CS is the area of cross section of the node and Q_s is the charge collection efficiency which strongly depends on doping. $Q_{critical}$ is proportional to the node capacitance and the supply voltage.

B. Flip-flops

Flip-flops form important component of data path designs and have been studied and improved constantly for speed and power optimizations. Also latches and register files that are inherently hardened against SERs have been proposed [4-6]. It is also important to evaluate SER in the existing high performance and low power flip-flop designs.

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Latches and register files are more resilient to SER when compared to conventional memory cells but as seen earlier the recent scaling trends decrease the charge retaining capabilities of CMOS devices. Further with increased frequency in scaled designs, more number of clock edges occurs per second. The window of vulnerability for a flip-flop being around its clock edges makes it more susceptible to SER at increased frequencies. Due to the difficulties in implementing error correcting logic to flip-flops and latches, it is important to tackle this problem as a design issue.

III. DESIGNS AND EXPERIMENTAL SET-UP

The flip-flop designs studied here encompass many types of designs which include master-slave, pulse triggered, sense amplifier based flip-flops and a couple of scannable latches. These designs were implemented and simulated in HSPICE using 70 nm Berkley Predictive Model. The $Q_{critical}$ is estimated only at specific nodes having low $Q_{critical}$. Such nodes can be experimentally or intuitively identified. Once these nodes are identified, current pulses which model the charge generation due to the radiation are supplied to these nodes and the $Q_{critical}$ for both 0 to 1 and 1 to 0 bit flips of the output is estimated. This would give an accurate estimation of SER and can be used to modify the design accordingly.

A. *Master-Slave Designs*

Transmission gate flip-flops (TGFF) derived from the PowerPC603 [13] is the first flip-flop design analyzed for SER estimation here. The node "S1" (Fig 1) has very low $Q_{critical}$ at the positive edge of the clock when compared to the other nodes. During the positive edge of the clock, master stage transitions from "enable" mode to "hold" mode and the feed back inverter is enabled at this point. Here the node "S1", which is the output of the feedback inverter, is clearly most susceptible to SEU. Even if node "S2" has transistors connected to it similar to "S1", at the positive edge of the clock, the slave transitions from hold to evaluation mode thus enabling the transmission gates. This makes the $Q_{critical}$ at the node very high. The $Q_{critical}$ values for TGFF are in Table 1. It shows the $Q_{critical}$ for two bit flips (1 to 0 and 0 to 1). Note that the 0 to 1 bit flip never occurs at "S2".

The Double-edge triggered flip-flop (DET) [14] designed using two TGFF blocks is considered next. Here two nodes that are equally vulnerable ("S1" and "S2" in Fig 2) are tested. One node is affected at positive edge of clock and the other at the negative edge. Results (Table 2) show that the type of edge determine the $Q_{critical}$ required to flip the output contrary to the expectation that the two nodes must have similar $Q_{critical}$ as the design is fairly symmetric. This is due to difference in the mobility of holes and electrons as the PMOS and NMOS connected to this node are of same size.

C^2MOS(C2) flip-flop [13] is the next master-slave negative edge-triggered flip-flop design estimated for SER here. $Q_{critical}$ was estimated at "S" (Fig 3), output of master stage.

B. *Pulse Triggered Designs*

Pulse-triggered flip-flops generate pulses during the active edge of the clock, which in turn would result in a transition at the output. The pulse triggered designs have a higher $Q_{critical}$ than the master-slave designs discussed above. For example in the case of the Hybrid latch flip-flop [13] (HLFF) (Fig 4), the node "X", which is the most vulnerable node, has highly sized NMOS and PMOS connected to it. Here 1 to 0 bit flip have higher $Q_{critical}$ because "X" normally stays at 1 due to the PMOS device and thus needs higher negative pulse to bring it down to 0.

Another pulse-triggered design evaluated for SER here is the Semi-dynamic flip-flop (SDFF) [13]. They show very similar characteristics to the HLFF. The difference in the $Q_{critical}$ is more evident here. This is due to the presence of cross coupled inverters connected to "X" (Fig 5).

C. *Sense amplifier based design and scannable latches*

Sense-amplifier based flip-flops (SAFF) used in StrongArm100 [15] is evaluated for $Q_{critical}$. Since this is a differential input differential output flip-flop there are two outputs at the master stage, "S" and "R" (Fig 6) which are evaluated for SER. Results (Table 2) show that while one of the bit flips has a very low $Q_{critical}$ value, the other transition has a very high $Q_{critical}$. This is due to the presence of sized transistors connected to these nodes.

Both the scannable latches (LSSD and ETSA) [16] are built similar to the SAFF structure (Figs 7 & 8) and has very similar SEU characteristics. The results in Table 2 show the $Q_{critical}$ values when they function as flip-flops.

D. *Analysis*

Table 2 shows SER evaluated for only the nodes at which $Q_{critical}$ were the lowest for each flip-flop. It is observed that the pulse triggered has higher $Q_{critical}$. The SDFF, SAFF and the scannable latches has a higher $Q_{critical}$ for one kind of flip. This will be the preferred state for the flip-flop for lower SER. The node "S2" in DET has the least $Q_{critical}$.

IV. OPTIMIZATIONS

There are numerous optimization strategies discussed in the literature to harden CMOS devices [2-5]. Adding more gate capacitance to the node is one of the common methods. But care should be taken that the diffusion capacitance is not increased as this will increase the area of the node. In [20], gate capacitance is added by connecting the node to the gates of a MOS device whose drain and source are shorted to the supply rails. This has performance penalties. Gate capacitance of a specific node can also be improved by sizing the MOS devices to whose gates it is connected. For example, in the case of TGFF (Fig 1), sizing up the pull up and pull down transistors at "S1" will increase the diffusion capacitance thus making it more susceptible to SEU's. But sizing up the pull up and pull down transistors of the inverter at "Q_m" will improve the gate capacitance of S1also increasing diffusion capacitance at "Q_m". But $Q_{critical}$ at "Q_m" is much higher. With this method higher $Q_{critical}$ was achieved, thus was used to simulate each design with different sizing.

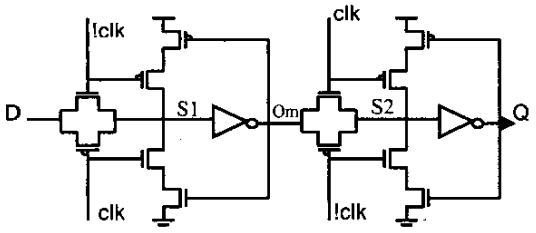

Fig 1. Transmission Gate Flip-Flop

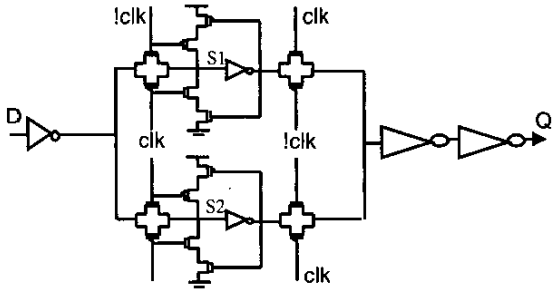

Fig 2.Double Edge Triggered Flip-Flop

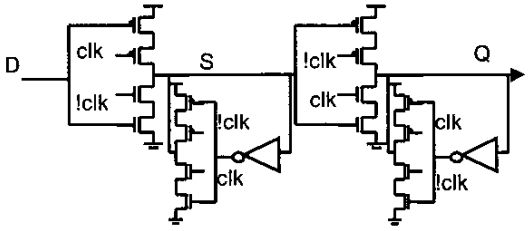

Fig 3. C2MOS Flip-Flop

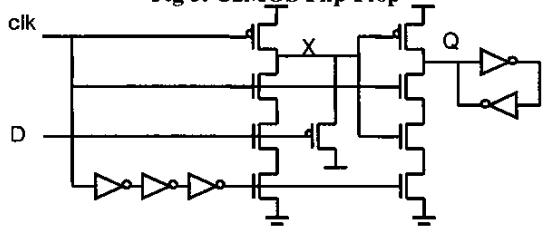

Fig 4. Hybrid Latch Flip-Flop

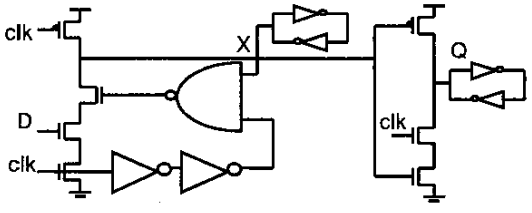

Fig 5. Semi-dynamic Flip-Flop

Node	S1	S2	Qm
0 to 1 flip	5.48	-	32.03
1 to 0 flip	2.06	16.67	10.17

Table 1. Critical charge values for TGFF

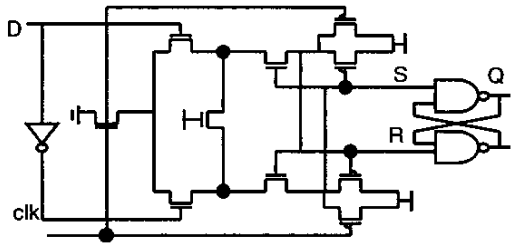

Fig 6. Sense Amplifier based Flip-Flop

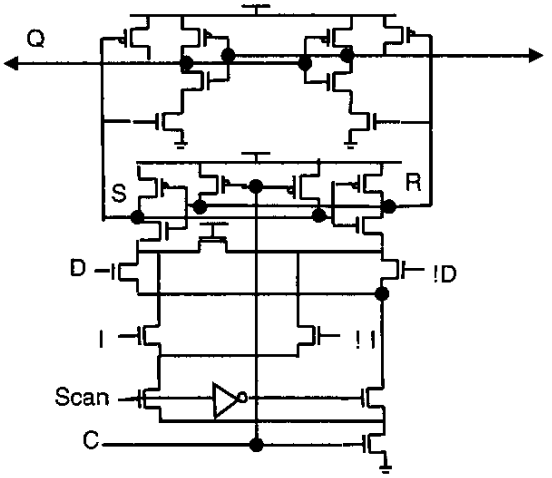

Fig 8. Level Sensitive Scannable SA based Latch

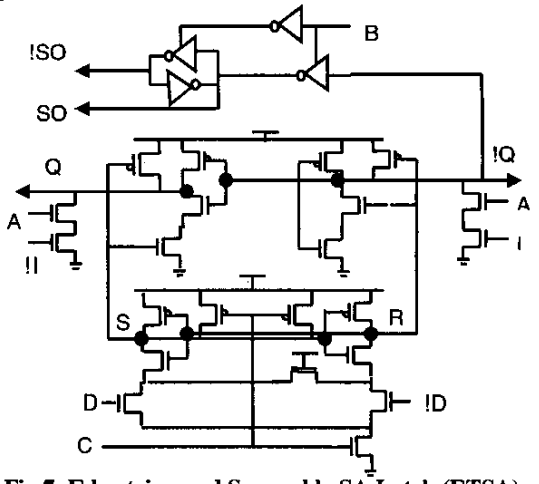

Fig 7. Edge triggered Scannable SA Latch (ETSA)

Type	Node	0 to 1 flip fC	1 to 0 flip fC	Type	Node	0 to 1 flip fC	1 to 0 flip fC
TGFF	S1	5.48	2.06	SAFF	R	4.38	1.52
C2	S	1.4	3.58		S	0.25	4.61
DET	S1	1.01	1.9	ETSA	R	9.52	1.21
	S2	0.79	0.87		S	2.15	6.60
HLFF	X	5.29	4.75	LSSD	R	5.31	2.77
SDFF	X	16.19	2.72		S	1.84	9.89

Table 2. Critical charge values

The results are presented for 0 to 1 and 1 to 0 output flips in Fig 9 and Fig 10 respectively. It compares the $Q_{critical}$ for each node with the pull up and pull down transistors of the next stage having progressively increased size (size 1 to 3). As expected, for most of the designs the $Q_{critical}$ increases as the size increases. A marked improvement is seen especially in some of the designs like DET and HLFF. While there are a few exceptions in which the $Q_{critical}$ actually reduces as it is sized up. For example in the case LSSD, the node "R" and "S" are connected to 4 gates (Fig 8). But sizing up transistors in the cross coupled inverters to increase the gate capacitance at these nodes would make the transitions from one state to the other faster. So a lower $Q_{critical}$ would be sufficient here to result in a flip. Similar reasoning could be given to other such designs where there is a decrease in $Q_{critical}$.

Another optimization that is done to improve robustness of the design is triple modular redundancy (TMR). The simplest implementation of TMR is obtained by replicating whole flip-flop design and using majority logic to determine the correct output. But this results in area and power overhead. We suggest a new method that will achieve TMR with a reduced overhead. It is achieved by replicating just the master stage of the flip-flop and using majority logic at the output of the master stage (Fig 11). This takes the advantage of the fact that the susceptible node is in the master stage as in TGFF where the node "S1" is the node with least $Q_{critical}$. This results in reduced area and power overhead. This can be used only in master slave flip-flops.

V. Conclusion

Addressing SER is becoming extremely important in flip-flops as technology scales. This work characterizes SER in terms of $Q_{critical}$ and discusses two simple optimization techniques. One attempts to increase the $Q_{critical}$ by increasing the gate capacitance while the other improves the overall robustness of the circuit by replicating the master stage of the master slave flip-flops, which results in a reduced power and area overhead. This work forms the basis for a detailed study of $Q_{critical}$ in deep sub-micron technology when a node cannot be modeled as an ideal capacitance.

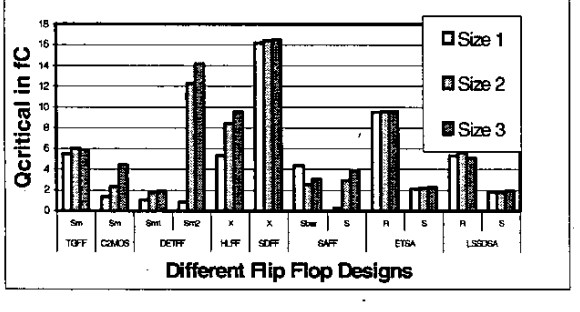

Fig 9. Critical charge for 0 to 1 flips

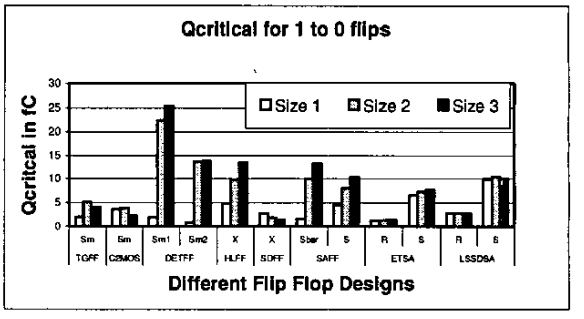

Fig 10. Critical charge for 1 to 0 flips

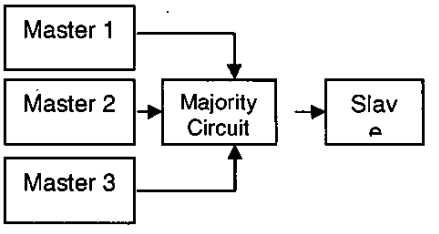

Fig 11. Proposed TMR design

VI. References

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