5/26 MEETING

Critical Path

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
ALUSrc_3_reg/CK (DFFSRHQX1)	0.00 #	0.00 r
ALUSrc_3_reg/Q (DFFSRHQX1)	0.18	0.18 r
U2222/Y (CLKINVX1)	0.20	0.38 f
U1709/Y (NOR2X1)	0.46	0.84 r
U1810/Y (AO21XL)	0.34	1.18 r
alu/B[38] (ALU)	0.00	1.18 r
alu/add_342/B[38] (ALU_DW01_add_1)	0.00	1.18 r
alu/add_342/U1032/Y (OR2X1)	0.13	1.30 r
alu/add_342/U674/Y (INVX1)	0.03	1.33 f
alu/add_342/U673/Y (OA21XL)	0.17	1.50 f
alu/add_342/U867/Y (OAI21XL)	0.13	1.63 r
alu/add_342/U866/Y (AOI21X1)	0.04	1.67 f
alu/add_342/U865/Y (OAI21XL)	0.09	1.76 r
alu/add_342/U702/Y (AOI21X1)	0.07	1.83 f
alu/add_342/U703/Y (NAND2X1)	0.08	1.91 r
alu/add_342/U701/Y (AOI21X1)	0.06	1.97 f
alu/add_342/U697/Y (OAI21XL)	0.14	2.11 r
alu/add_342/U704/Y (AOI21X1)	0.07	2.18 f
alu/add_342/U856/Y (OAI21XL)	0.16	2.34 r
alu/add_342/U729/Y (AOI21XL)	0.09	2.43 f
alu/add_342/U685/Y (OAI21XL)	0.18	2.61 r
alu/add_342/U731/Y (XNOR2XL)	0.14	2.74 f
alu/add_342/SUM[62] (ALU_DW01_add_1)	0.00	2.74 f
alu/U75/Y (AO22XL)	0.16	2.90 f
alu/U686/Y (OR3X2)	0.13	3.03 f
alu/Z[62] (ALU)	0.00	3.03 f
ALU_result_4_reg_62_0/D (DFFSRHQX1)	0.00	3.03 f
data arrival time		3.03

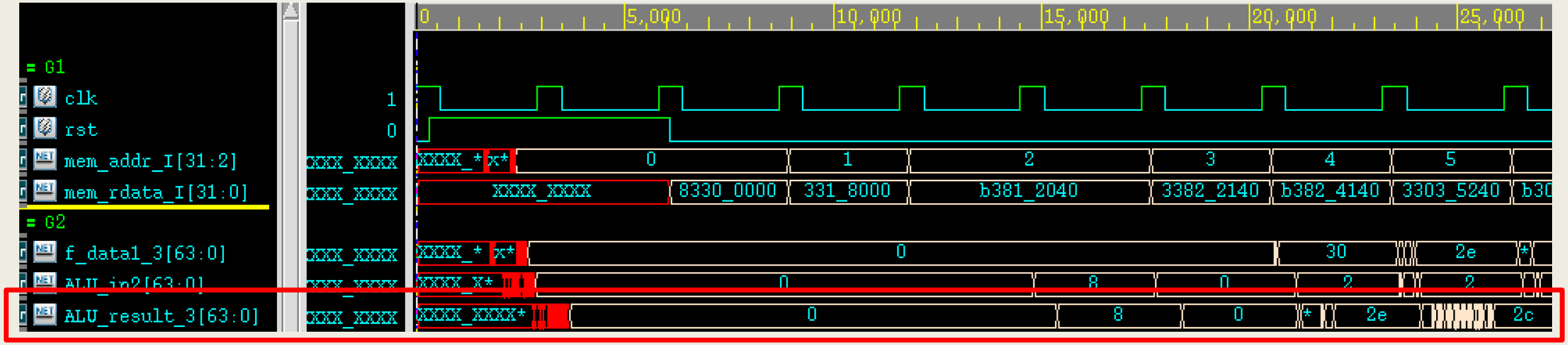
Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
MEM_forwd_in1_3_reg/CK (DFFSRHQX1)	0.00 #	0.00 r
MEM_forwd_in1_3_reg/Q (DFFSRHQX1)	0.19	0.19 r
U1720/Y (BUFX4)	0.08	0.27 r
U1678/Y (NAND2BX2)	0.07	0.34 r
U1689/Y (NOR2X2)	0.05	0.39 f
U2114/Y (CLKBUFX3)	0.15	0.54 f
U1759/Y (AO22XL)	0.22	0.77 f
U1723/Y (OR2X4)	0.11	0.88 f
BRANCH/r_data_1[6] (Branch_Unit)	0.00	0.88 f
BRANCH/U23/Y (NAND2X1)	0.05	0.93 r
BRANCH/U24/Y (NAND2X1)	0.05	0.98 f
BRANCH/U1/Y (OR4X4)	0.18	1.15 f
BRANCH/U6/Y (NOR4BX1)	0.13	1.28 r
BRANCH/U19/Y (AND3X2)	0.11	1.39 r
BRANCH/U33/Y (NAND2X2)	0.03	1.42 f
BRANCH/U4/Y (NAND2X1)	0.06	1.47 r
BRANCH/U41/Y (NAND2X2)	0.03	1.50 f
BRANCH/U2/Y (NOR2BX1)	0.06	1.56 r
BRANCH/U5/Y (NAND2X1)	0.05	1.61 f
BRANCH/U11/Y (NOR2X2)	0.05	1.66 r
BRANCH/Branch (Branch_Unit)	0.00	1.66 r
U1680/Y (OR2X1)	0.12	1.77 r
U1654/Y (BUFX6)	0.08	1.86 r
U1653/Y (NOR2X6)	0.04	1.90 f
U1736/Y (AO22XL)	0.19	2.09 f
U1735/Y (AO21XL)	0.16	2.25 f
sub_246_aco/A[0] (RISCV_DW01_sub_7)	0.00	2.25 f
sub_246_aco/U305/Y (NOR2X1)	0.08	2.33 r
sub_246_aco/U287/Y (NAND2X1)	0.05	2.38 f
sub_246_aco/U230/Y (NOR2X1)	0.07	2.45 r
sub_246_aco/U245/Y (NAND2XL)	0.05	2.51 f
sub_246_aco/U257/Y (CLKBUFX3)	0.14	2.65 f
sub_246_aco/U282/Y (NOR2X1)	0.07	2.72 r
sub_246_aco/U52/Y (XOR2X1)	0.06	2.78 r
sub_246_aco/DIFF[22] (RISCV_DW01_sub_7)	0.00	2.78 r
mem_addr_I_o_reg_24_0/D (DFFSRHQX1)	0.00	2.78 r
data arrival time		2.78

Critical Path

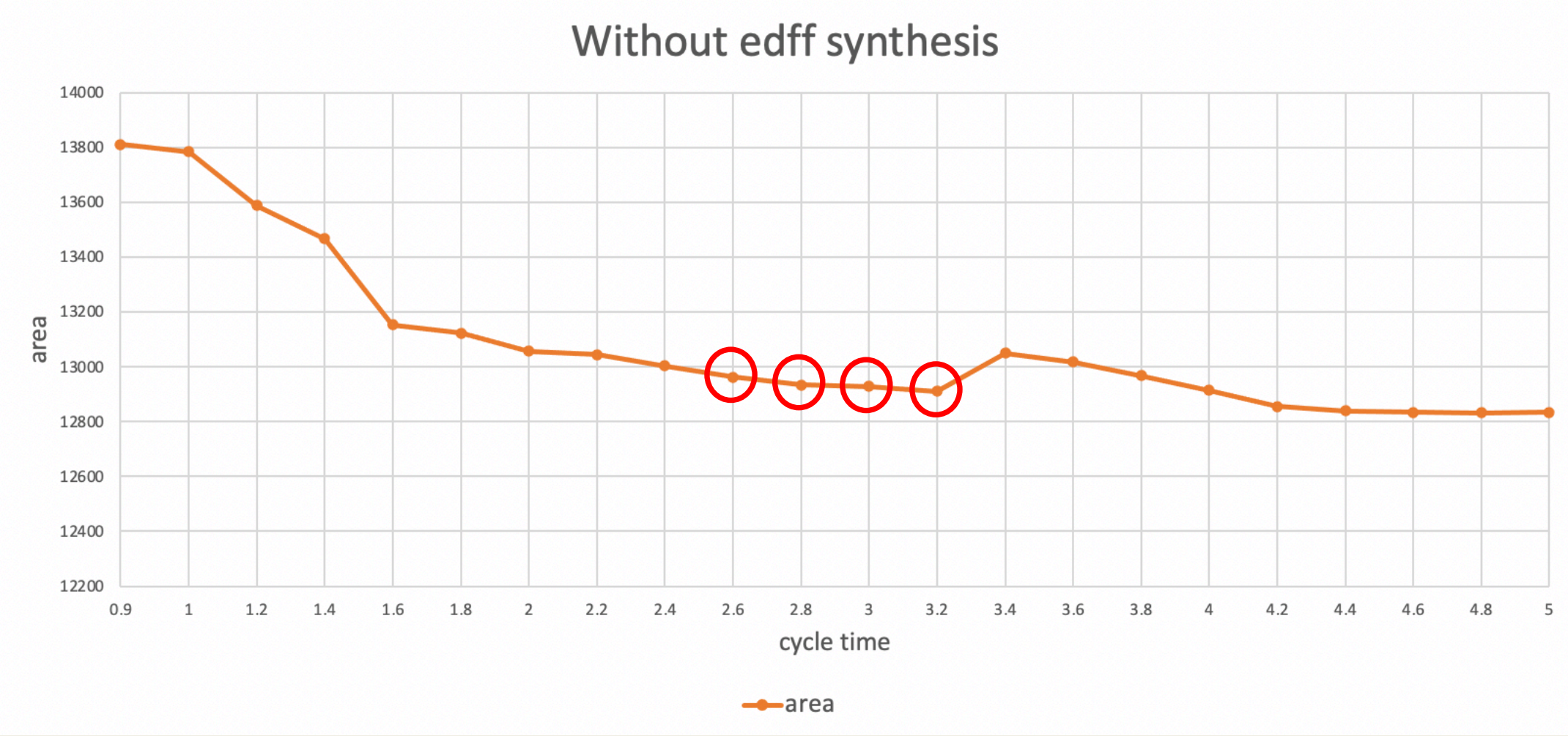
1. Instruction Fetch
2. Instruction Decode
3. Execute(ALU) : Forwarding + Subtraction / Forwarding + Branch
4. Memory
5. Write back to register

Design Benchmark

1. Load data
2. A sequence of subtraction
3. Branch



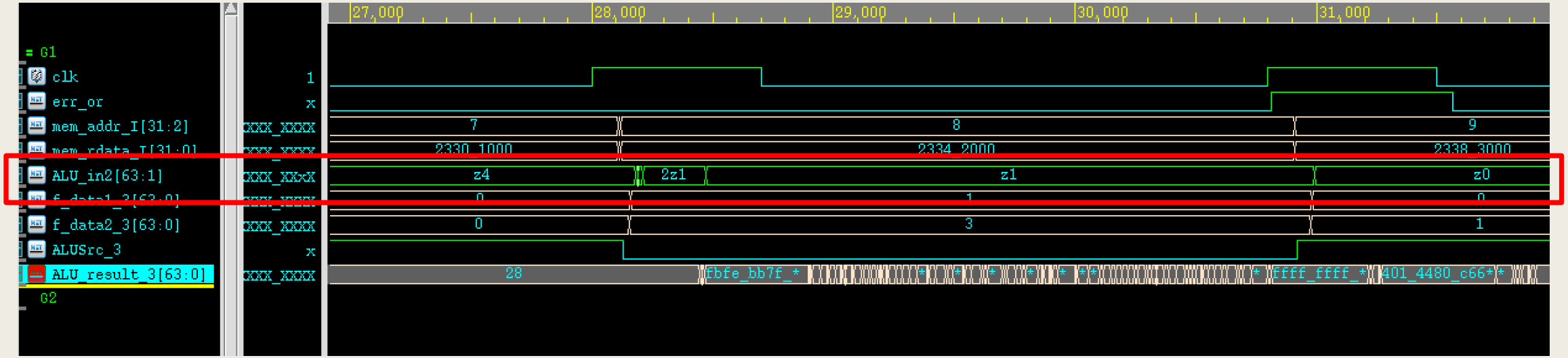
Choose cycle time



Experiment : test for benchmark

Synthesis Cycle Time	Pattern 1 limit	Pattern 2 limit	Pattern 3 limit	Benchmark limit
3.2 ns	2.6 ns	2.8 ns	2.2 ns	3.0 ns
3.0 ns	2.8 ns	2.8 ns	2.8 ns	2.8 ns
2.8 ns	2.5 ns	2.6 ns	2.3 ns	2.7 ns
2.6 ns	2.4 ns	2.4 ns	2.2 ns	2.5 ns

Problem： ALU_in2會有z出現




```
assign  ALU_in2 = (ALUSrc_3)? {{32{immediate_3[31]}},immediate_3} : f_data2_3;
assign  PC_4_out_3 = {32'b0,mem_addr_I_o, 2'b0} + 4;
assign  PC_imm_out = {32'b0,mem_addr_I_o, 2'b0} + {{32{immediate_3[31]}},immediate_3};
assign  Jalr_adder_out = f_data1_3 + {{32{immediate_3[31]}},immediate_3};
assign  nxt_mem_addr_I = (Branch || Jal_3)? (PC_imm_out-8) : (Jalr_3) ? Jalr_adder_out : PC_4_out_3;
```

Problem： ALU_in2會有z出現

- Only occur in certain synthesis