

## 2-Stage OpAMP Design (1<sup>st</sup> stage -> NMOS Diff Amp, 2<sup>nd</sup> stage -> PMOS CSA)

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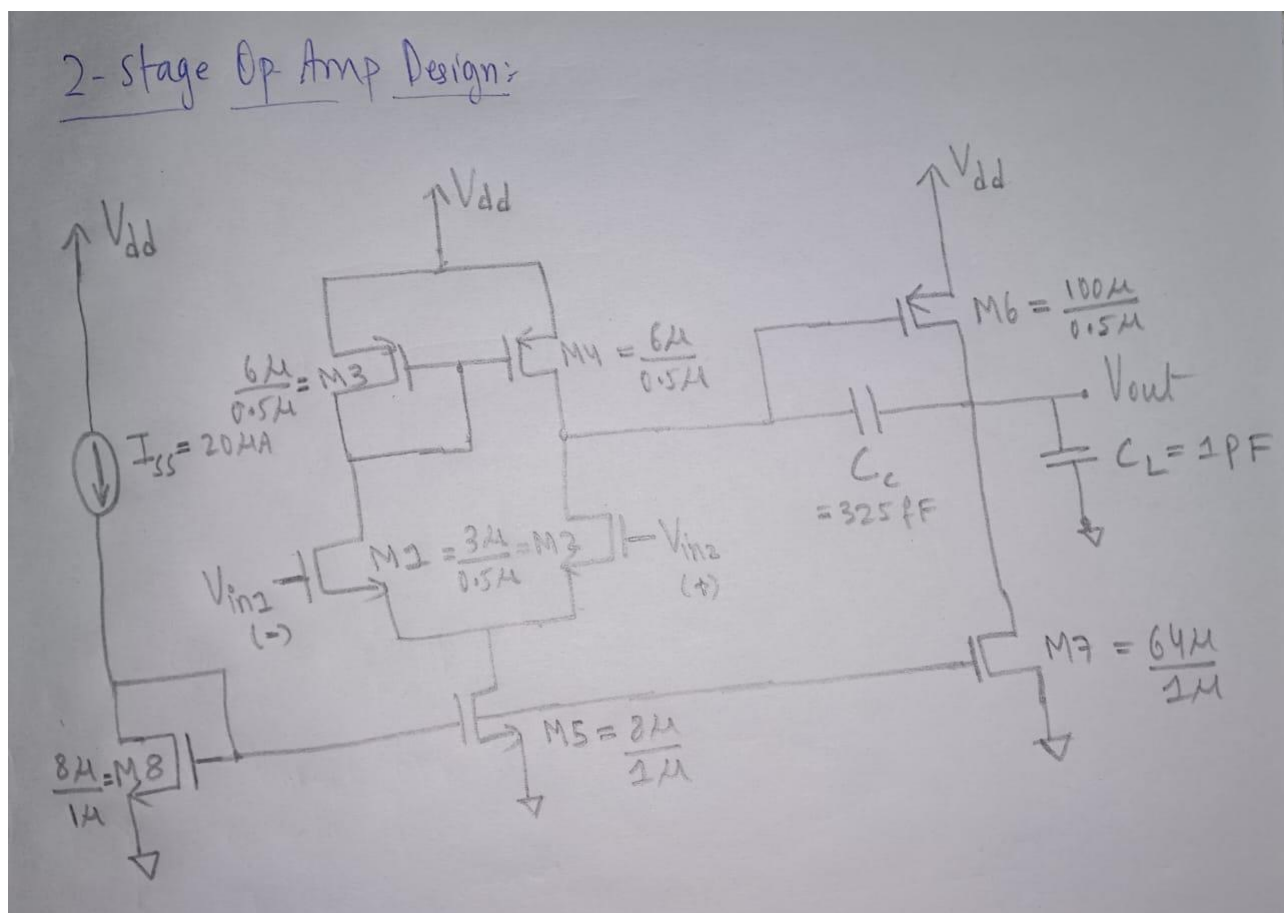
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### Required Specifications of the Design:

Low Frequency Gain (DC Gain)	1000 (60dB)
Gain x Bandwidth product	50 MHz
Phase Margin	60 deg
Slew Rate	30 V/usec
Load Capacitance	1 pF

VDD	1.8 V
ICMR(+)	1.6 V
ICMR(-)	0.8 V
Power	400 uW
Technology	UMC-180 nm



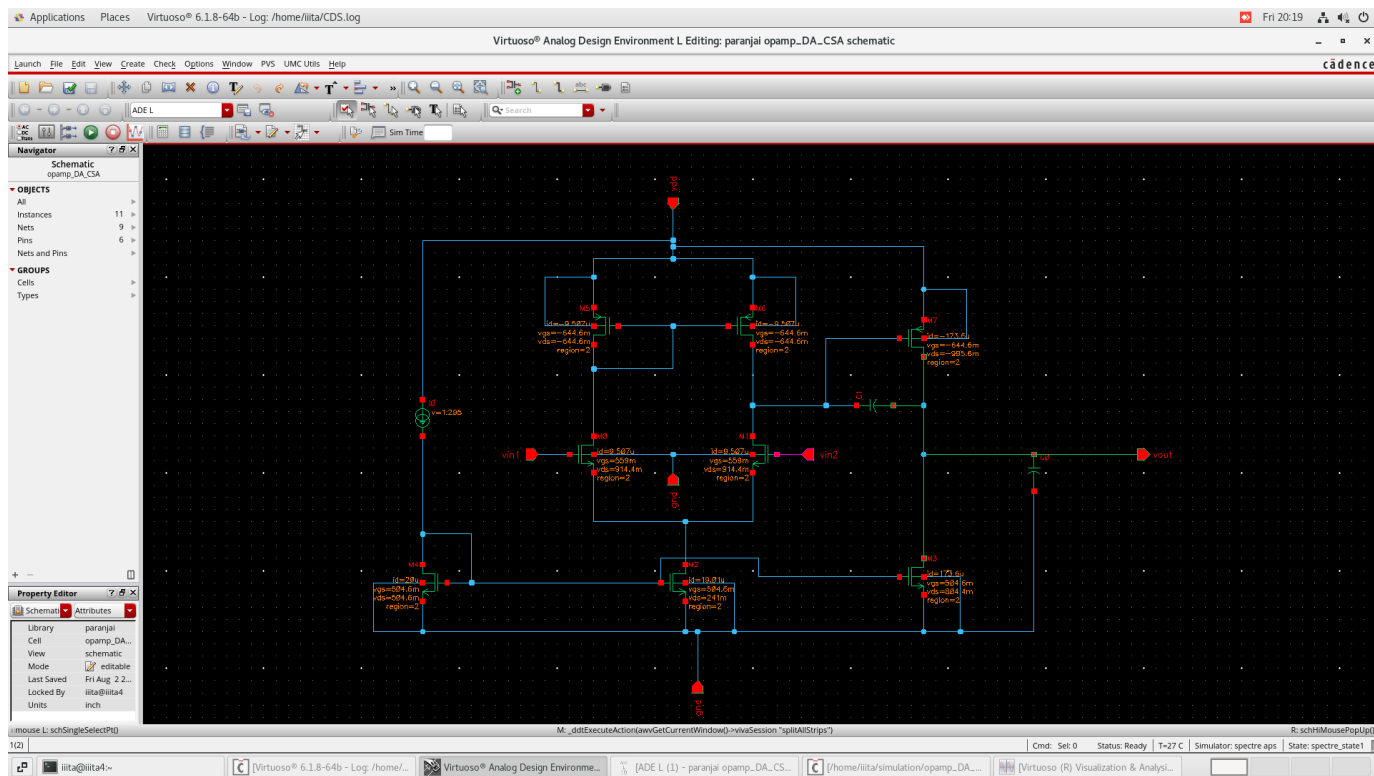
### Design Parameters after Final Tuning:

Channel Length (L)	500 nm
Compensation Capacitance ( $C_c$ )	325 fF
Tail Current ( $I_{SS}$ )	20 uA
M1, M2	$(w/l) = (3\mu/0.5\mu)$
M3, M4	$(w/l) = (6\mu/0.5\mu)$
M6	$(w/l) = (100\mu/0.5\mu)$
M7	$(w/l) = (64\mu/1\mu)$
M5, M8	$(w/l) = (8\mu/1\mu)$

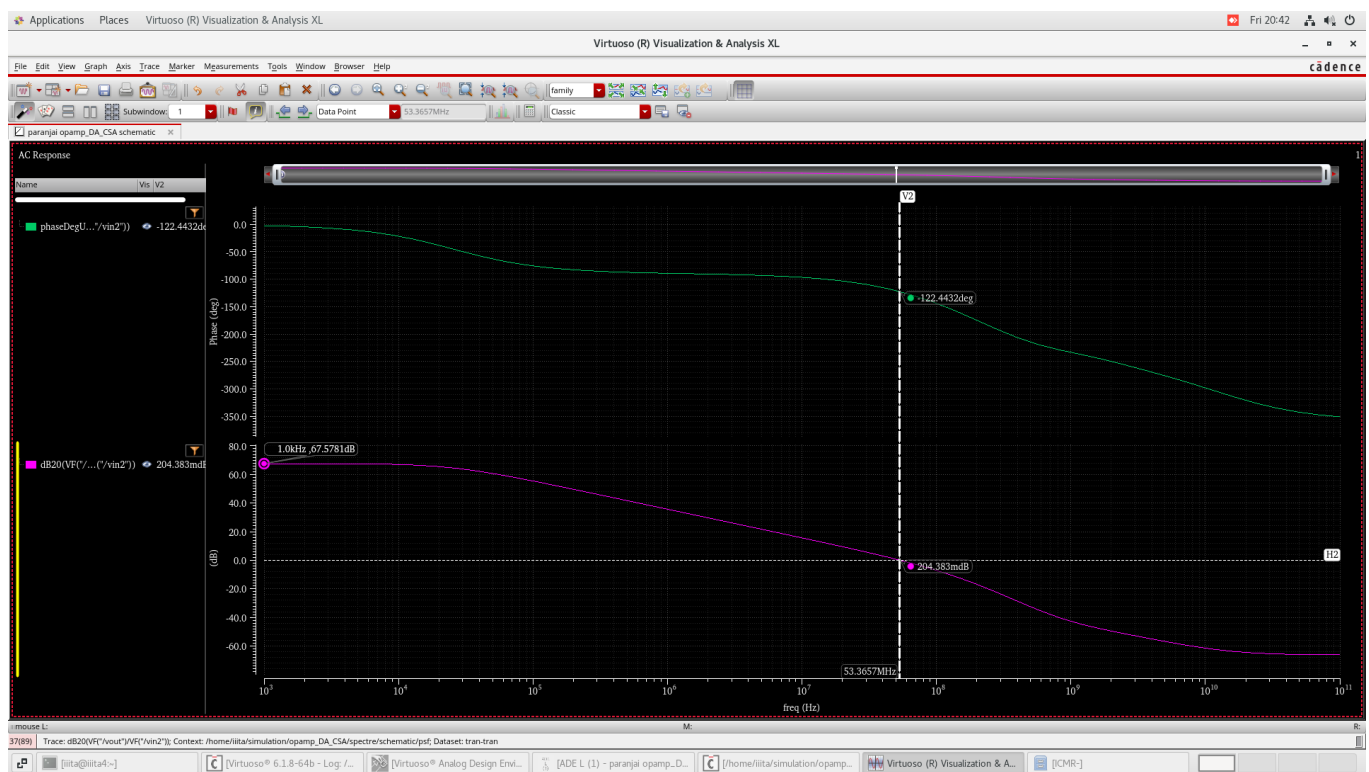
## Sample Outputs

### 1) $V_{in} = \text{ICMR}(-)$

**Schematic :** (The DC operating point of each MOSFET is annotated beside)



### Gain and Phase Plot:

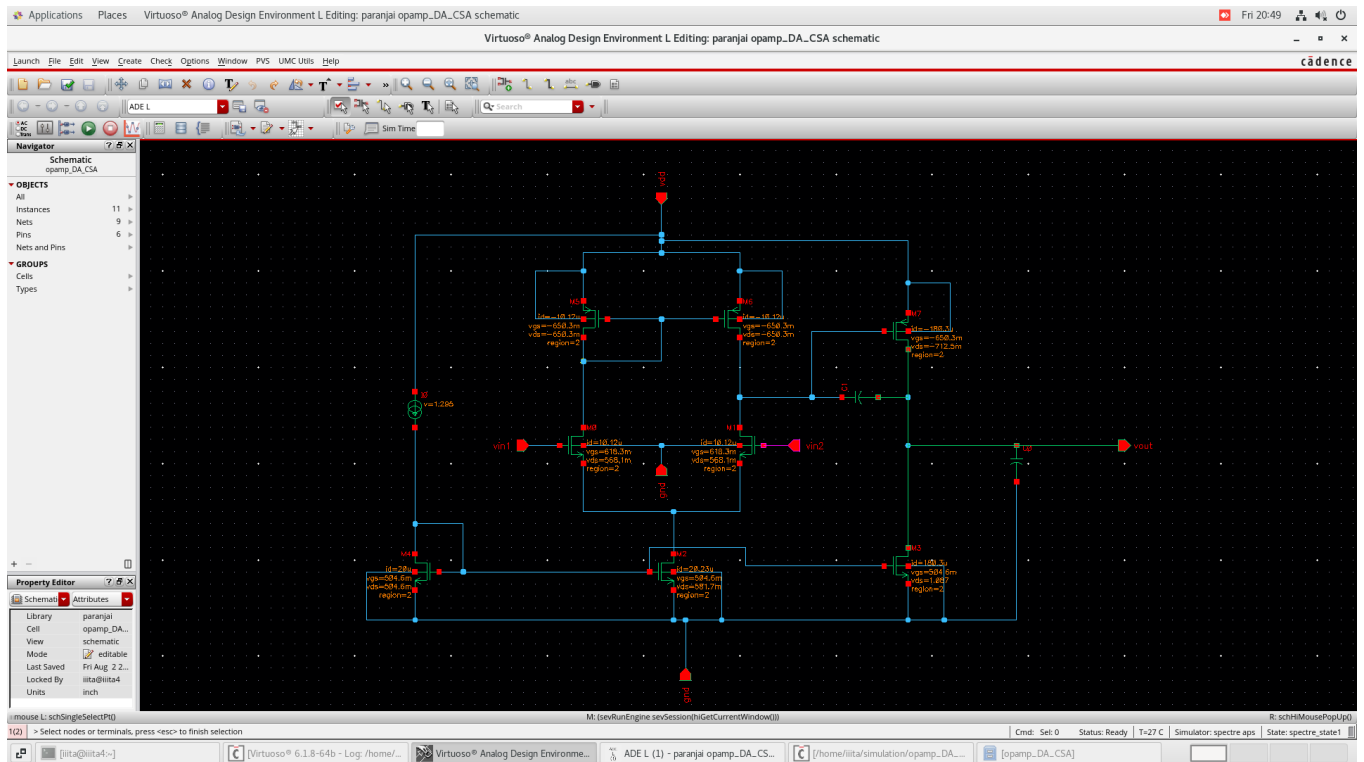


**Obtained:**

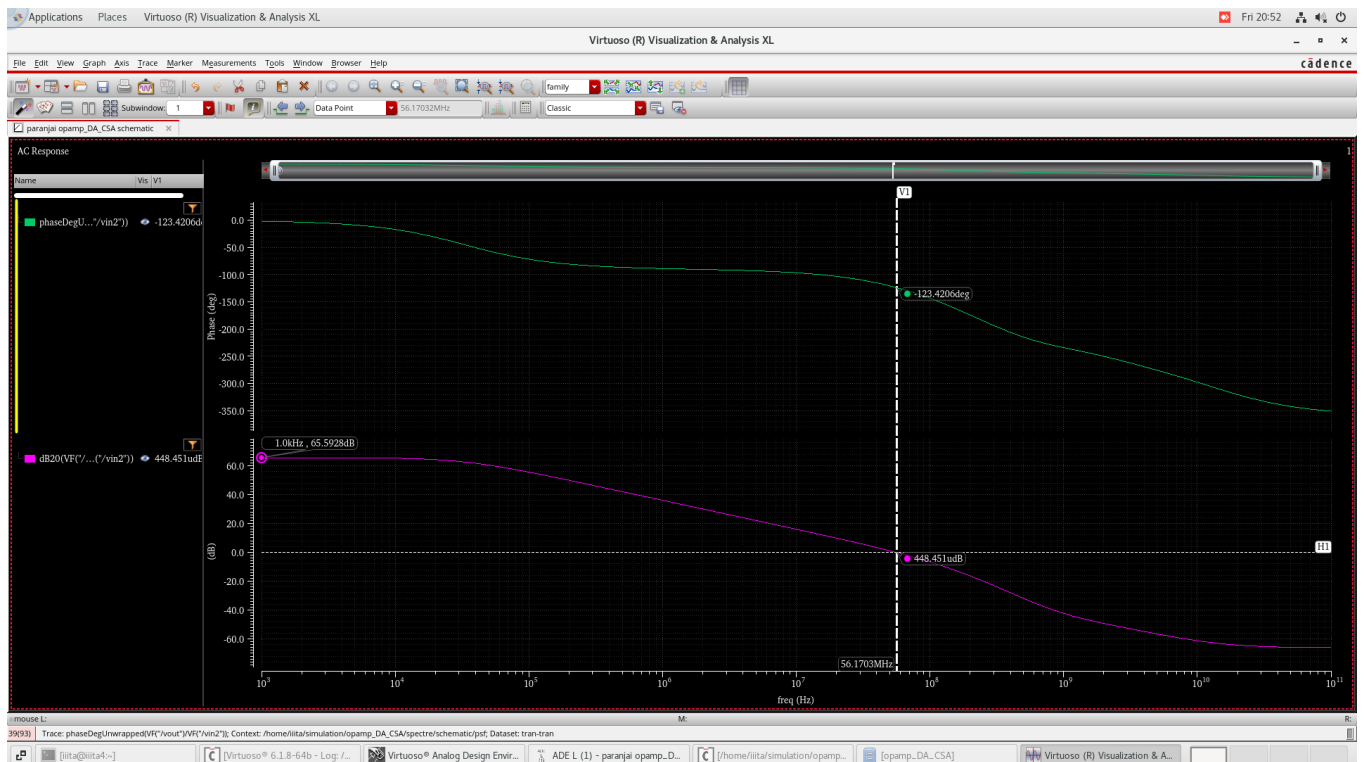
DC Gain = 67.5781 dB	Bandwidth = 53 – 54 MHz	Phase Margin = 57.5568 deg	Power = 346.698 uW
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2)  $V_{in} = 1.2\text{ V}$

**Schematic:** (The DC operating point of each MOSFET is annotated beside)



**Gain and Phase Plot:**

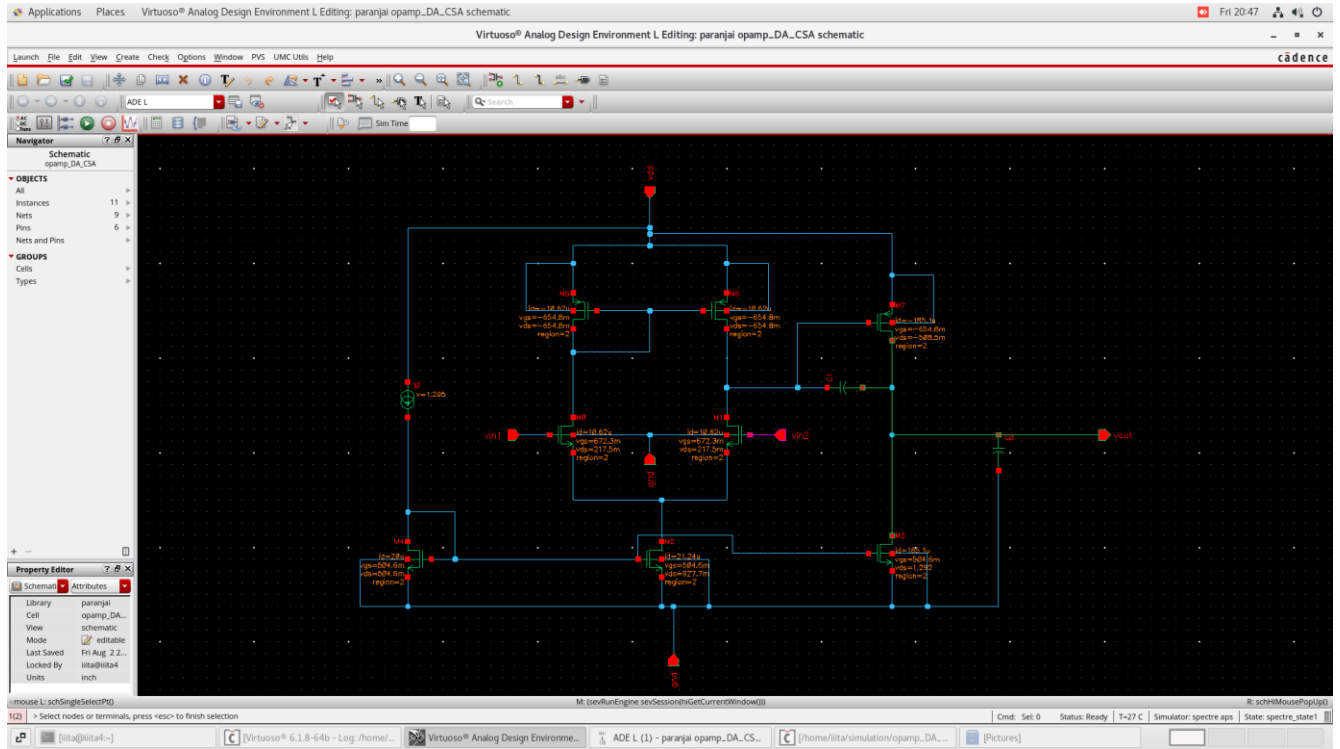


Obtained:

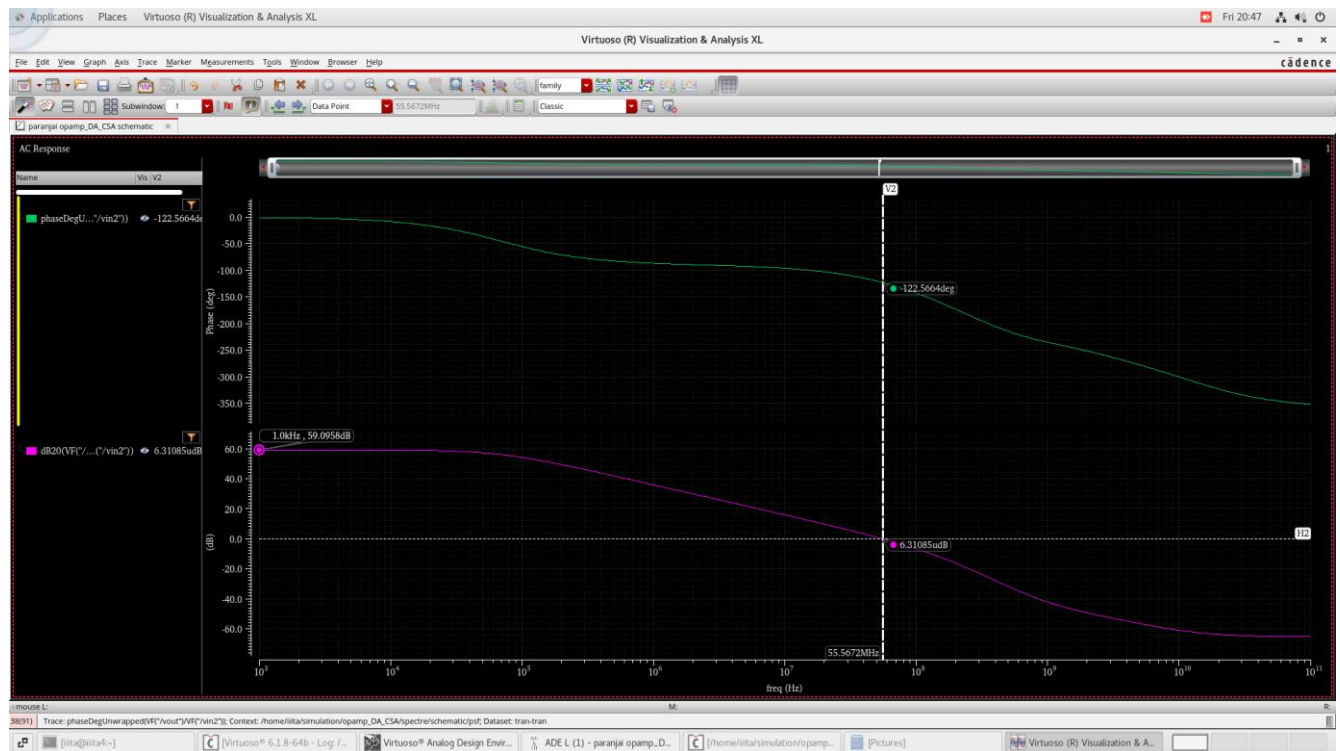
DC Gain = 65.5928 dB	Bandwidth = 56-57 MHz	Phase Margin = 56.5794 deg	Power = 360.954 uW
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### 3) $V_{in} = ICMR(+)$

**Schematic:** (The DC operating point of each MOSFET is annotated beside)



**Gain and Phase Plot:**



Obtained:

DC Gain = 59.0958 dB	Bandwidth = 55-56 MHz	Phase Margin = 57.434 deg	Power = 371.412 uW
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Obtained Slew Rate and Power of the Design:

Slew Rate	61.5 V/usec
Average Power	359.688 uW

Process Corner Analysis:

Setting up the outputs and desired specifications are mentioned:

Virtuoso® ADE Assembler Editing: paranjal opamp assembler														
Single Run, Sweeps and Corners														
Results														
Filter														
Test	Name	Type	Details	EvalType	Plot	Save	Spec	Weight	Units	Digits	Notation	Suffix		
Filter	filter	Filter	Filter	Filter			Filter	filter	Filter	filter	Filter	Filter		
ac		signal	/VDD	point										
ac		signal	/VIN1	point										
ac		signal	/VIN2	point										
ac		signal	/VOUT	point										
ac	Gain	expr	ymax(dB20((VF("VOUT") / VF("VIN2"))))	point			> 60							
ac	BW	expr	unityGainFreq((VF("VOUT") / VF("VIN2")))	point			> 50M							
ac	PM	expr	phaseMargin((VF("VOUT") / VF("VIN2")))	point			range 55 60							
trans	Average Power	expr	average(((IT("IM4/D") + IT("IM7/S")) * 1.8))	point			< 400u							

Results:

Corner analysis is setup for 3 processes typical, fast-fast and slow-slow, each at 3 different temperatures of -55°C, 27°C and 125°C.

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	typical_0	typical_1	typical_2	fast-fast_0	fast-fast_1	fast-fast_2	slow-slow_0	slow-slow_1	slow-slow_2
Filter	filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
ac	/VDD															
ac	/VIN1															
ac	/VIN2															
ac	/VOUT															
ac	Gain	65.59	> 60		pass	64.09	66.87	66.62	65.59	64.3	66.45	65.42	64.09	66.87	65.83	64.91
ac	BW	56.56M	> 50M		near	46.58M	73.29M	70.95M	56.56M	46.6M	73.29M	58.34M	47.9M	67.98M	54.43M	46.58M
ac	PM	56.97	range 55 60		near	54.38	58.85	54.43	56.97	58.85	54.55	57.03	58.82	54.38	56.95	58.48
trans	Average Power	360.2u	< 400u		pass	358.3u	364.1u	362.7u	360.2u	358.8u	361.7u	359.4u	358.3u	364.1u	361.4u	360u
trans	/M4/D															
trans	/M7/S															
dc	none															

Summary:

Test	Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
ac	Gain	64.09	66.87	65.57	65.59	888.9m	> 60	pass
ac	BW	46.58M	73.29M	57.92M	56.56M	9.383M	> 50M	near
ac	PM	54.38	58.85	56.74	56.97	1.667	range 55 60	near
trans	Average Power	358.3u	364.1u	360.7u	360.2u	1.7u	< 400u	pass

typical\_0, fast-fast\_0, slow-slow\_0 -> corresponding process corner at -55°C.

typical\_1, fast-fast\_1, slow-slow\_1 -> corresponding process corner at 27°C.

typical\_2, fast-fast\_2, slow-slow\_2 -> corresponding process corner at 125°C.

**Waveforms:**

