**2-Stage OpAMP Design (1st stage -> NMOS Diff Amp, 2nd stage -> PMOS CSA)**

**KARNATI PARANJAI**

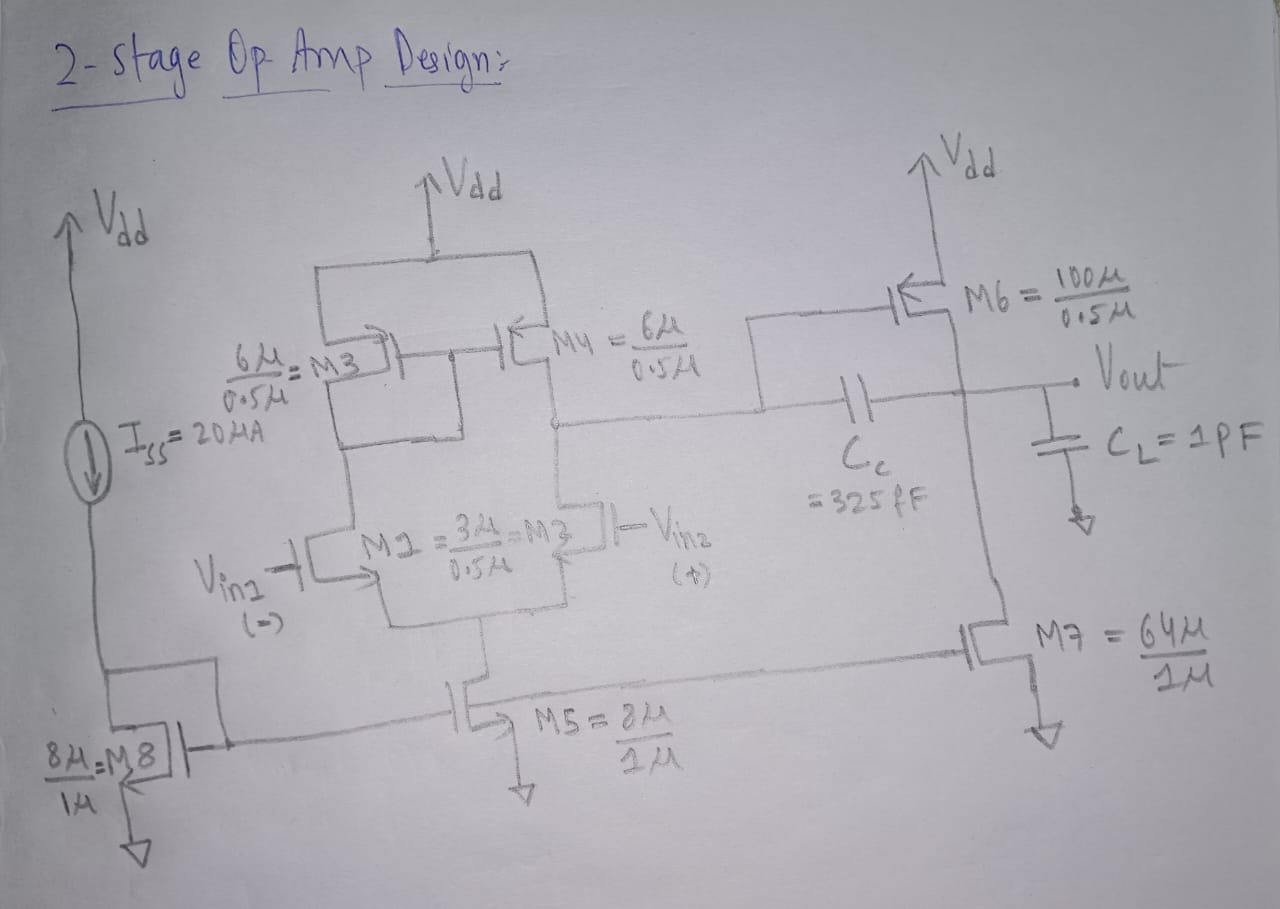
**IEC2021097**

**Final year student, B-Tech ECE, IIIT Allahabad**

**Required Specifications of the Design:**

|  |  |
| --- | --- |
| Low Frequency Gain (DC Gain) | 1000 (60dB) |
| Gain x Bandwidth product | 50 MHz |
| Phase Margin | 60 deg |
| Slew Rate | 30 V/usec |
| Load Capacitance | 1 pF |

|  |  |
| --- | --- |
| VDD | 1.8 V |
| ICMR(+) | 1.6 V |
| ICMR(-) | 0.8 V |
| Power | 400 uW |
| Technology | UMC-180 nm |

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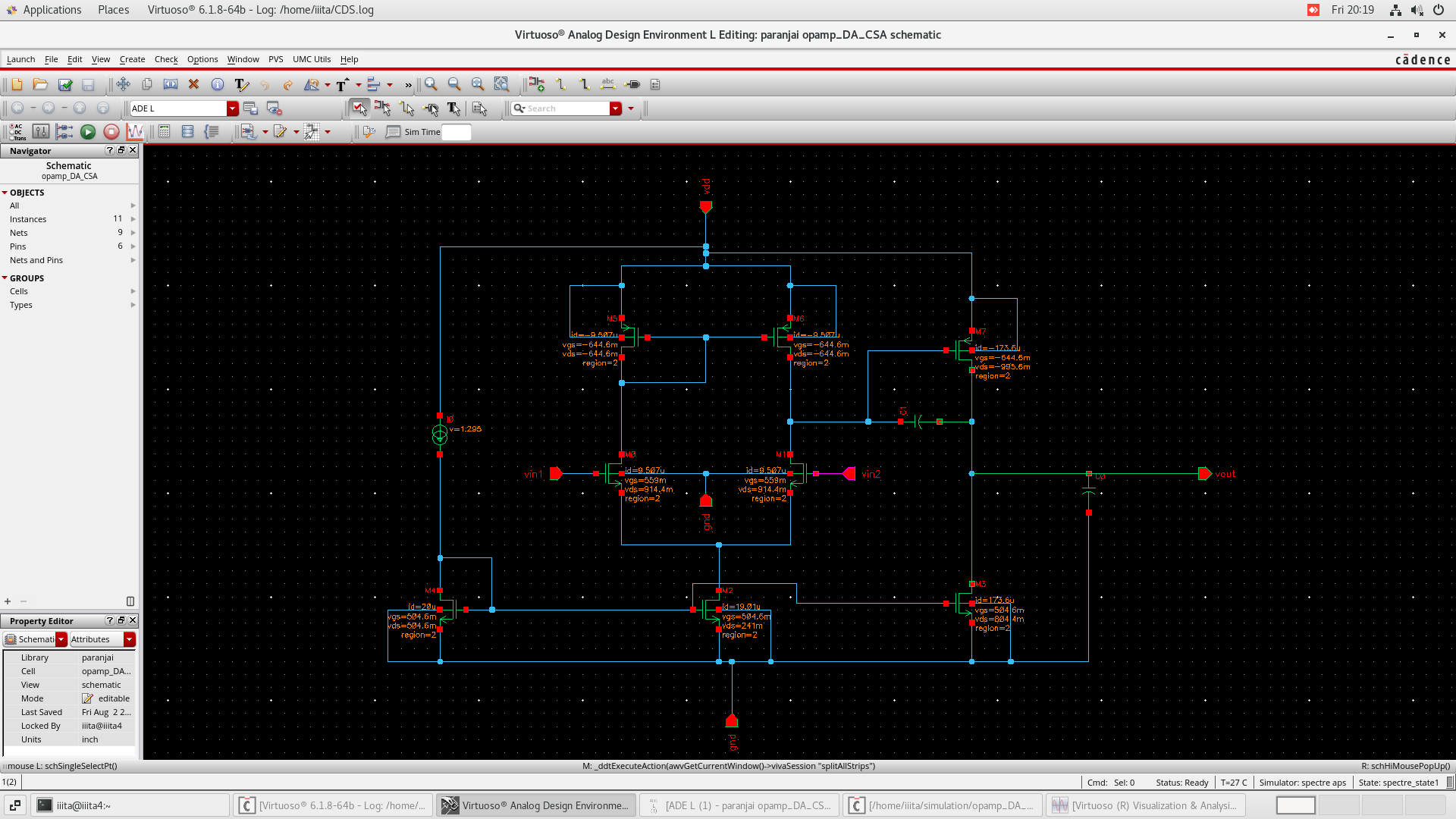
**Design Parameters after Final Tuning:**

|  |  |
| --- | --- |
| Channel Length (L) | 500 nm |
| Compensation Capacitance (Cc) | 325 fF |
| Tail Current (Iss) | 20 uA |
| M1, M2 | (w/l) = (3u/0.5u) |
| M3, M4 | (w/l) = (6u/0.5u) |
| M6 | (w/l) = (100u/0.5u) |
| M7 | (w/l) = (64u/1u) |
| M5, M8 | (w/l) = (8u/1u) |

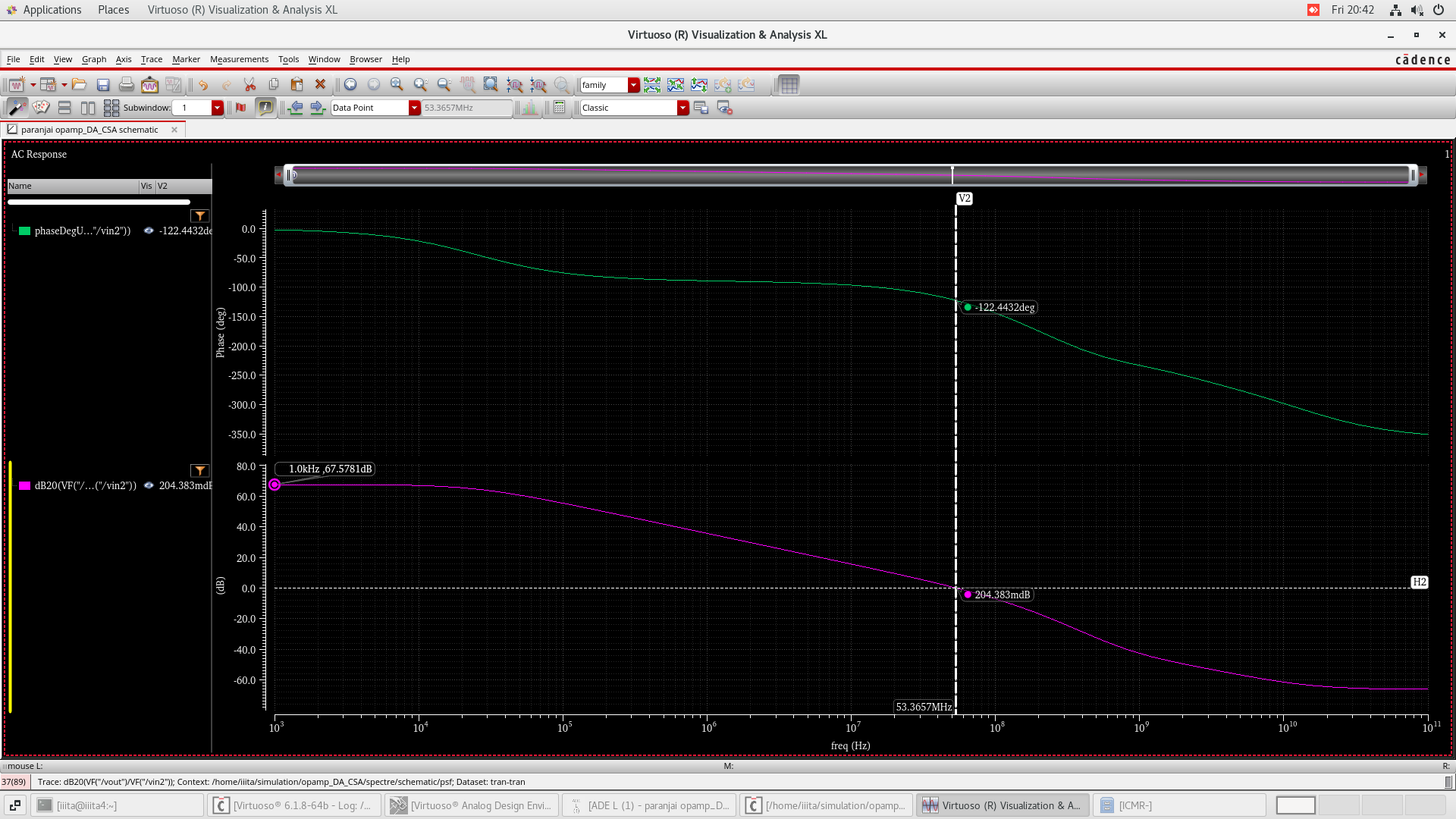
**Sample Outputs**

1. **Vin = ICMR(-)**

**Schematic :** (The DC operating point of each MOSFET is annotated beside)

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**Gain and Phase Plot:**

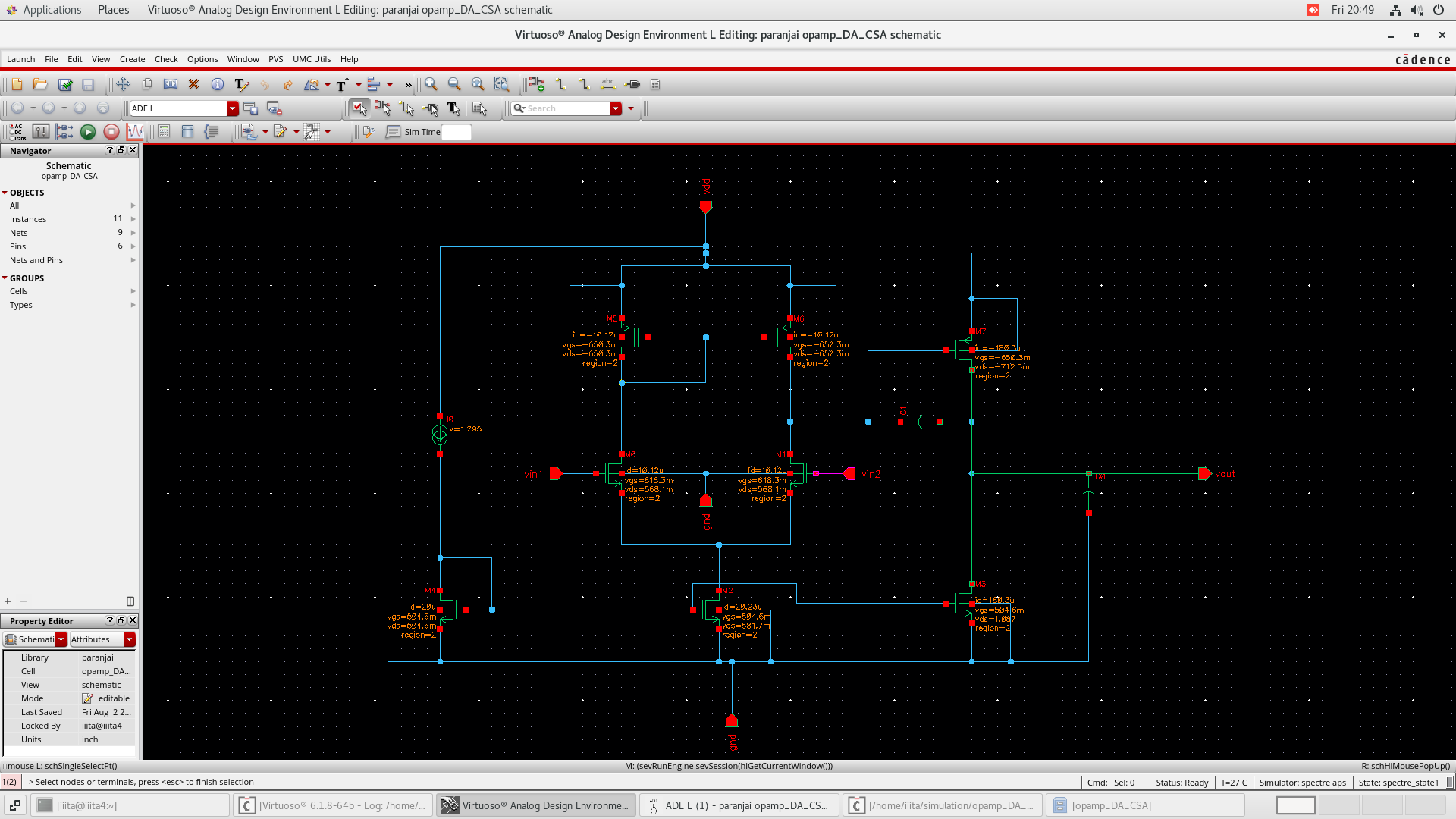
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**Obtained:**

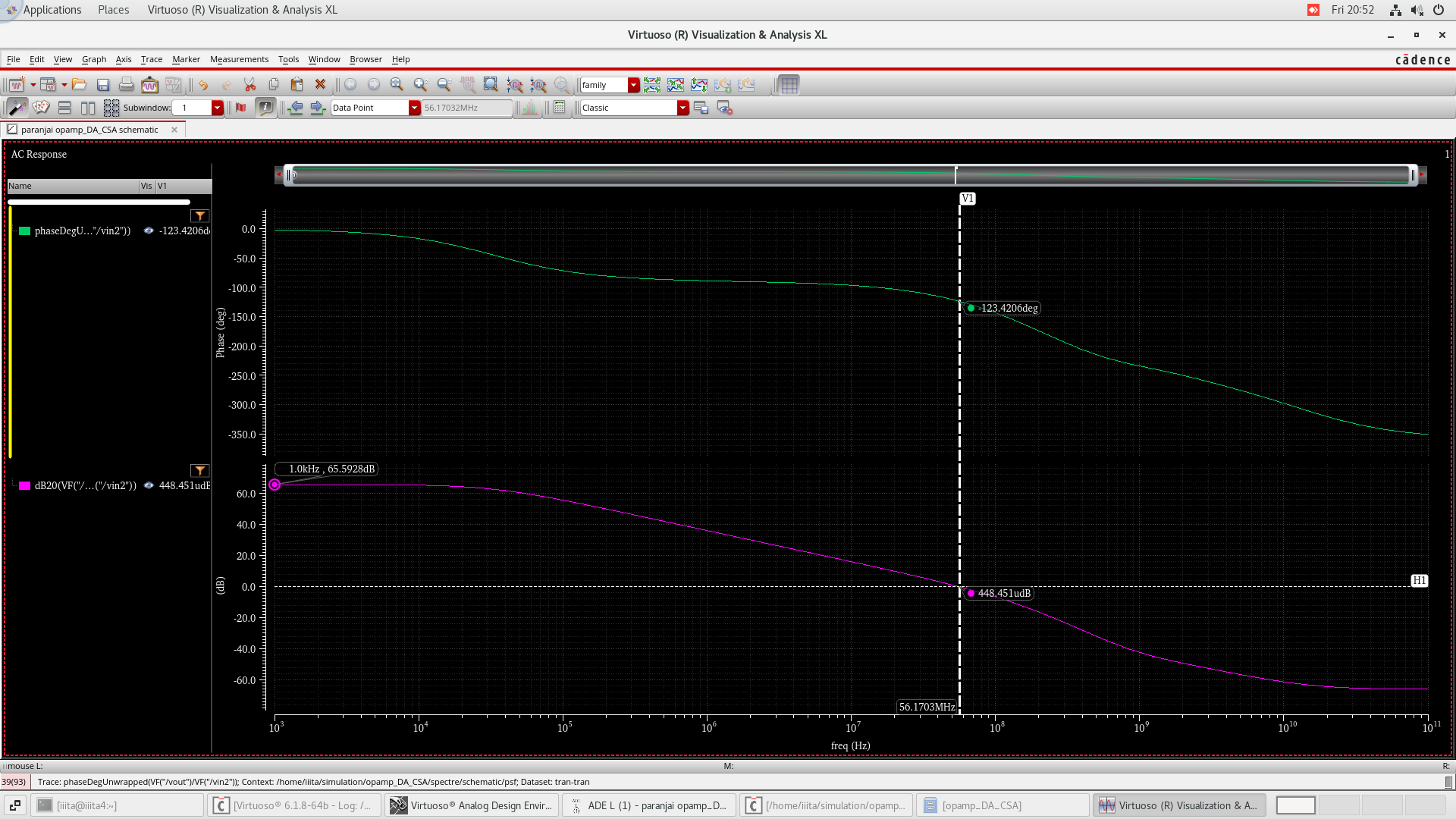
|  |  |  |  |
| --- | --- | --- | --- |
| DC Gain = 67.5781 dB | Bandwidth = 53 – 54 MHz | Phase Margin = 57.5568 deg | Power = 346.698 uW |

1. **Vin = 1.2 V**

**Schematic:** (The DC operating point of each MOSFET is annotated beside)



**Gain and Phase Plot:**

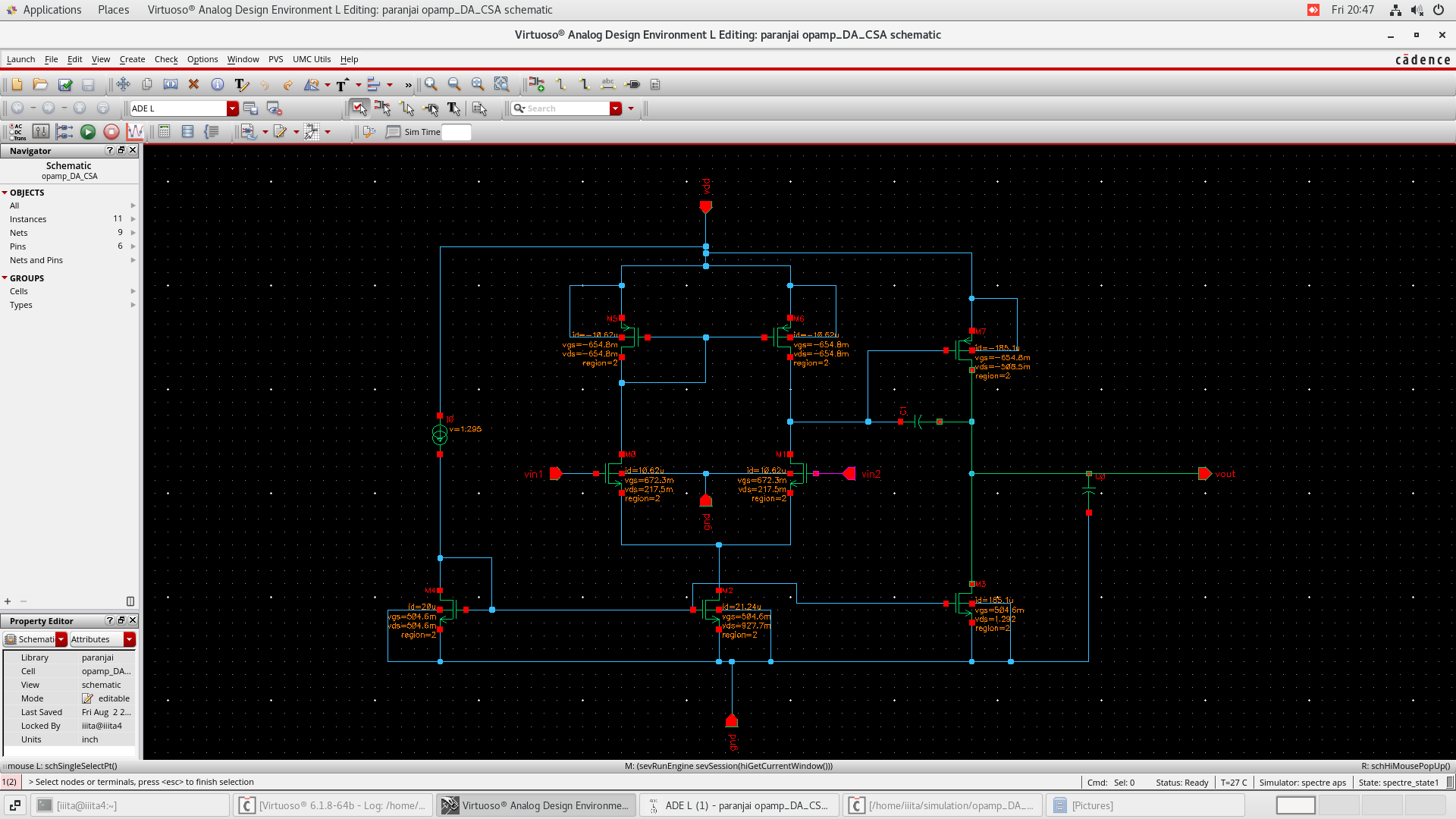
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|  |  |  |  |
| --- | --- | --- | --- |
| DC Gain = 65.5928 dB | Bandwidth = 56-57 MHz | Phase Margin = 56.5794 deg | Power = 360.954 uW |

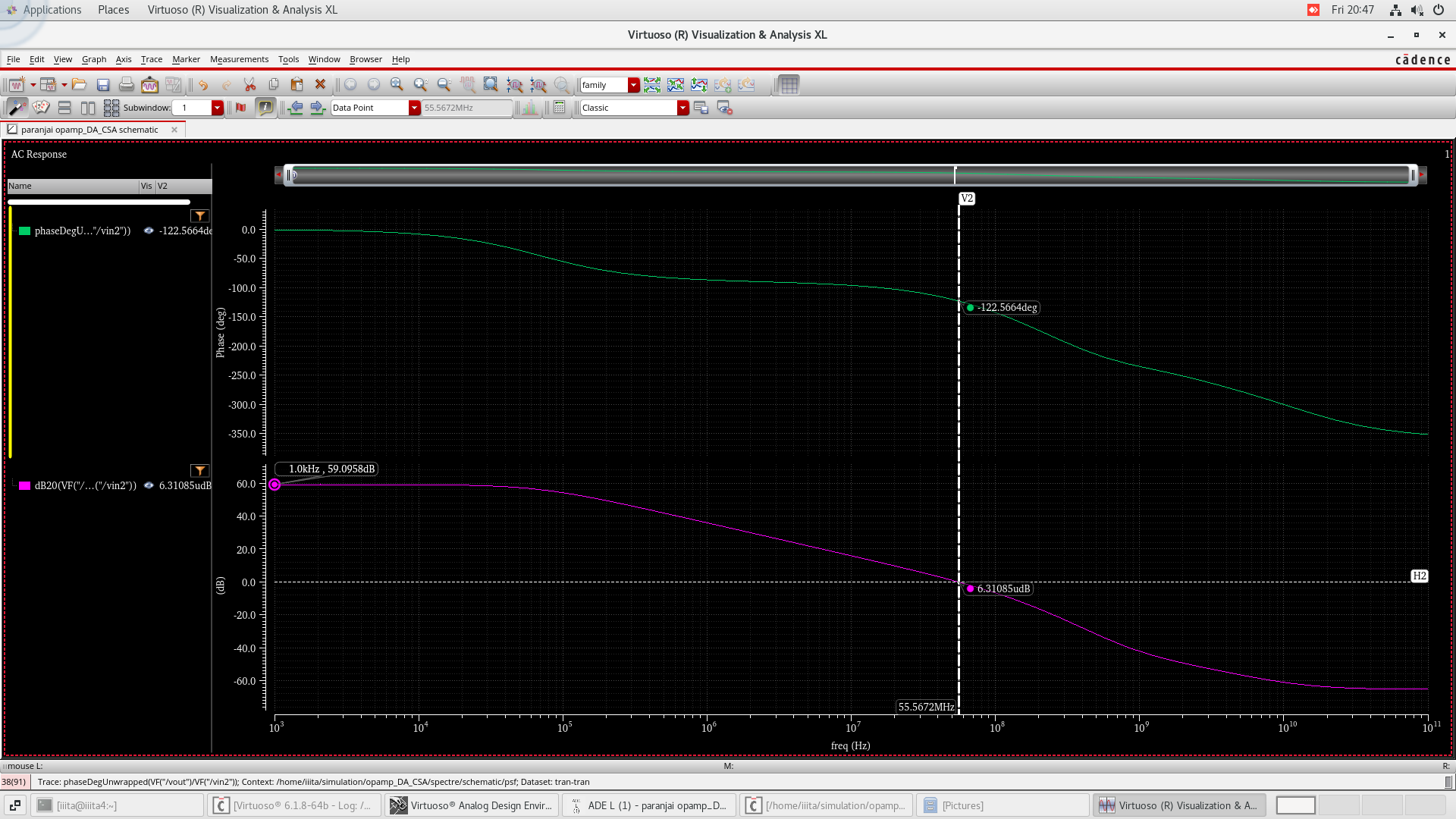
**Obtained:**

1. **Vin = ICMR(+)**

**Schematic:** (The DC operating point of each MOSFET is annotated beside)



**Gain and Phase Plot:**

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**Obtained:**

|  |  |  |  |
| --- | --- | --- | --- |
| DC Gain = 59.0958 dB | Bandwidth = 55-56 MHz | Phase Margin = 57.434 deg | Power = 371.412 uW |

**Obtained Slew Rate and Power of the Design:**

|  |  |
| --- | --- |
| Slew Rate | 61.5 V/usec |
| Average Power | 359.688 uW |