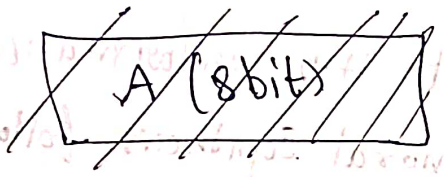
RTL :-

→ Describes the data flow from register to register at various time instants or clock cycle.

→ Carries timing information.

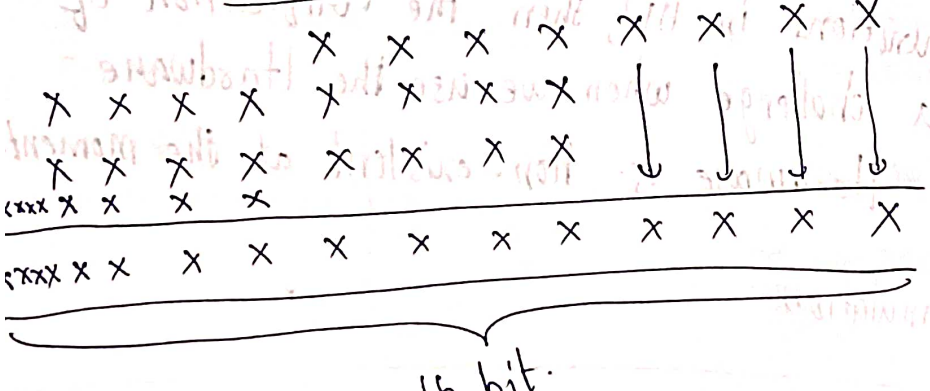
* Computation is done on the data path.
* FSM generates control signals.
* MUX passes the data based on control signals.

Vedic Multiplier (RTL Design) :-



Algorithm :-

$a_8\ a_7\ a_6\ a_5\ a_4\ a_3\ a_2\ a_1$
$\times\ b_8\ b_7\ b_6\ b_5\ b_4\ b_3\ b_2\ b_1$



16 bit.

Step 1 :-

$a_4\ a_3\ a_2\ a_1$
$\times\ b_4\ b_3\ b_2\ b_1$
q_0

Step 2 :-

$a_8\ a_7\ a_6\ a_5$
$\times\ b_4\ b_3\ b_2\ b_1$
q_1

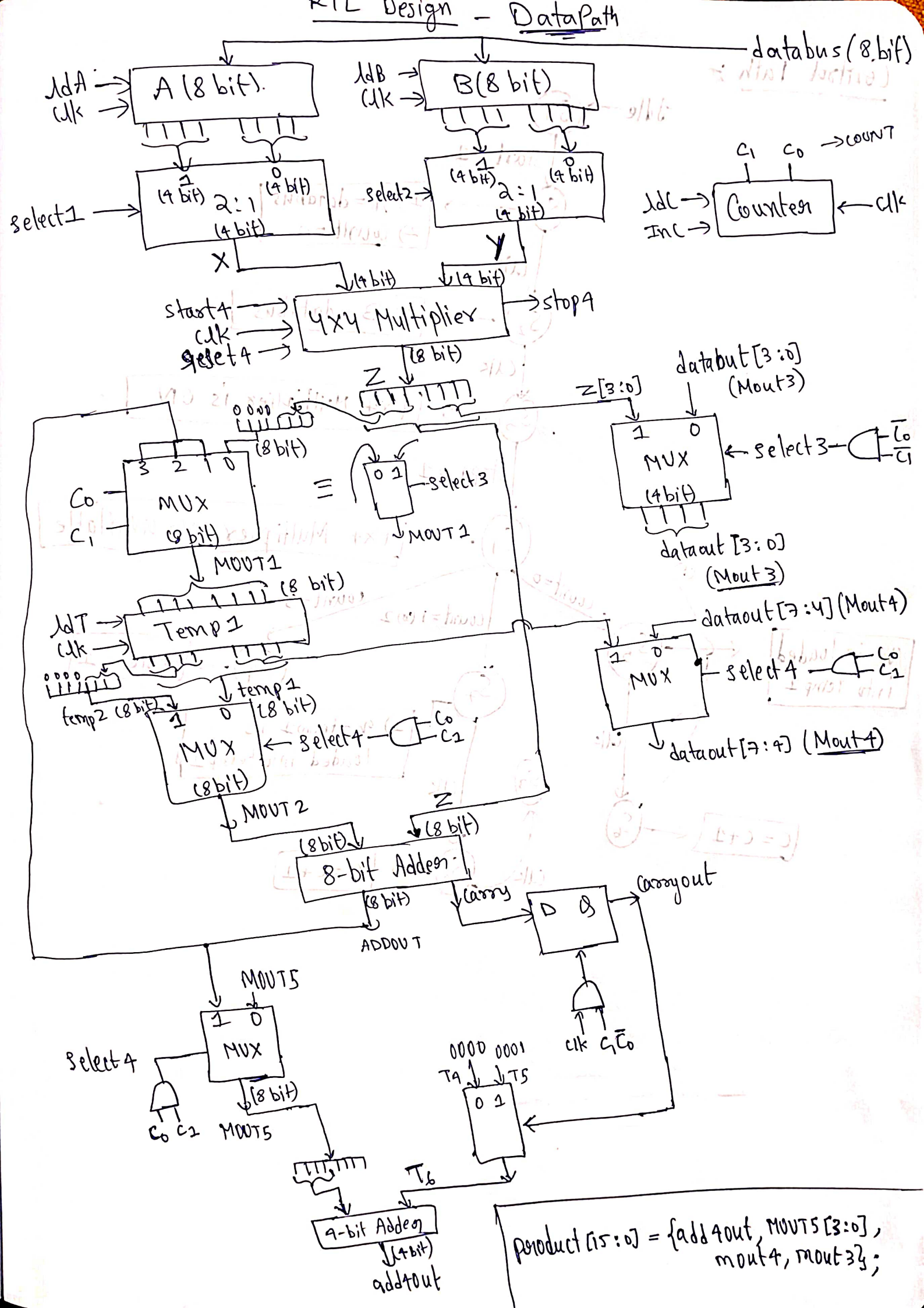
Step 3 :-

$a_4\ a_3\ a_2\ a_1$
$\times\ b_8\ b_7\ b_6\ b_5$
q_2

Step 4 :-

$a_8\ a_7\ a_6\ a_5$
$\times\ b_8\ b_7\ b_6\ b_5$
q_3

RTL Design - DataPath



Control Path :-