# FIFO [CDC]

Synchronizers :-

→ 2-FF Synchronizer :-

→ Toggle Synchronizer :-

→ First in First Out

→ For single bit Synchronization, we have 2-Flop synchronizer.

→ For pulse Synchronization with $f_{clk1} > f_{clk2}$ we have Toggle Synchronizer.

→ For multi-bit Synchronization we have, MUX Synchronizer, handshake Synchronizers, and FIFO, etc.

→ FIFO is not limited to CDC only. Even in a single clock domain, there can be cases when the read frequency is less than write frequency, even in those cases, we need FIFO to store the data

FIFO

- Synchronous
- Asynchronous
  - used when we want to transfer multibit of data from 1 clock domain to another.

Why Gray code?

→ Because there is only 1 bit difference b/w any number and its incremental next number, so we can avoid false full and false empty condition

FIFO depth :- The no. of slots or memory locations in a FIFO ~~are~~ is called FIFO depth.

** If Fifo depth = 8 ⇒ 3 bits sufficient for the address but to determine full and empty conditions, we need 1 (MSB) bit extra.

→ $2^3$

Binary ⇒ 000 001 010 011 100 101 110 111

Gray ⇒ 000 001 011 010 110 111 101 100

1 bit change.

→ In Sync FIFO:

9, 10, ...., Anything can be deep width.

In Async FIFO:

Only power of 2 ? [Not mandatory but need to follow some rules].

Ex: For Asyn FIFO with 6 deep.

0 to 5

⇒ Gray ⇒ 000 → 001 → 011 → 010 → 110 → 111

3 bits change (not acceptable)

$$\Rightarrow \left(\frac{2^n}{2} - \frac{\text{FIFO Depth}}{2}\right) \text{ to } \left(\frac{2^n}{2} + \frac{\text{FIFO Depth}}{2} - 1\right)$$

Ex: 520 deep

$$\Rightarrow \left(\frac{2^{10}}{2} - \frac{520}{2}\right) \text{ to } \left(\frac{2^{10}}{2} + \frac{520}{2} - 1\right)$$

⋮

252 to 771.

Gray ⇒ 0 10000 010 to 1 010000 010

1 bit change.

* Binary to Gray code Conversion :-

Binary → A

Gray → A_g ⇒ $\boxed{A\_g = A \wedge (A >> 1)}$

Overflow in Asynchronous FIFO : Overflow occurs when an attempt is made to write new data in a full FIFO.

Underflow : underflow occurs when ~~an~~ a there is no data to provide on a read request, because the FIFO is empty.