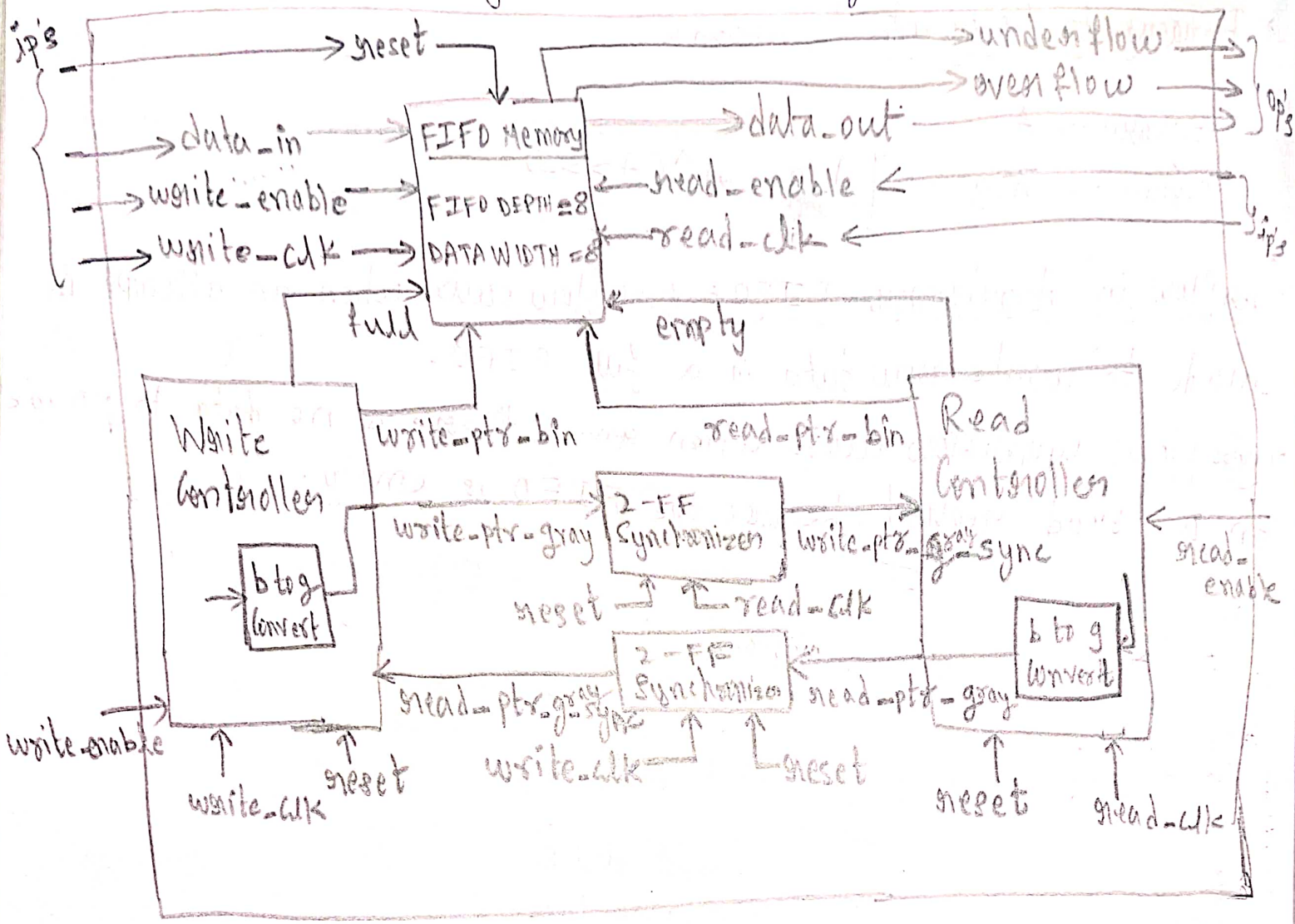
Asynchronous FIFO Design



→ FIFO Depth = 8

→ Data width = 8 bits

→ address width $= \log_2^{(\text{FIFO Depth})} + 1$

$= 4$

→ Actual memory addresses

$= 2 \times (\text{FIFO Depth}) - 1$

Synchronizer