UART – Hardware communication protocol design

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SAMPLE OUTPUTS

1) Sample testbench and the corresponding output for **uart module** :

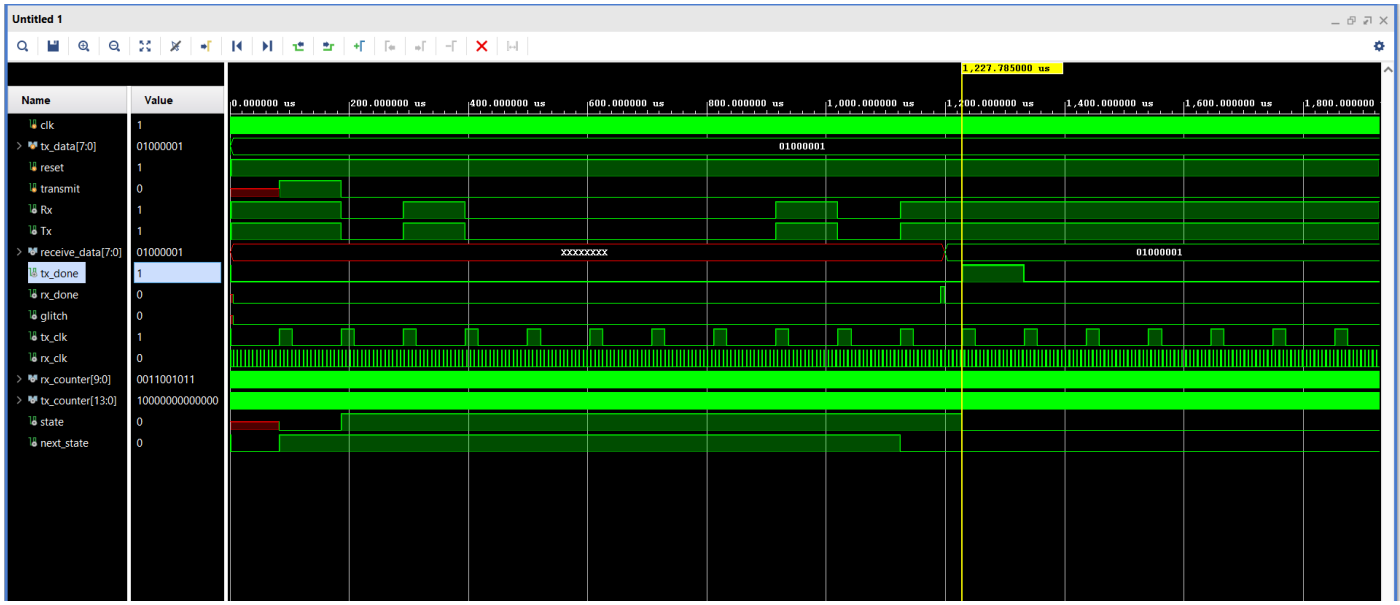
Testbench :

```
always #5 clk = ~clk;

assign Rx = Tx;

initial
begin
clk = 0;
#1 reset = 1;
#3 tx_data = 8'b01000001;
#82000              // for tx_clk and rx_clk to be generated
#10 transmit = 1;
#104160 transmit = 0;
end
```

Output :



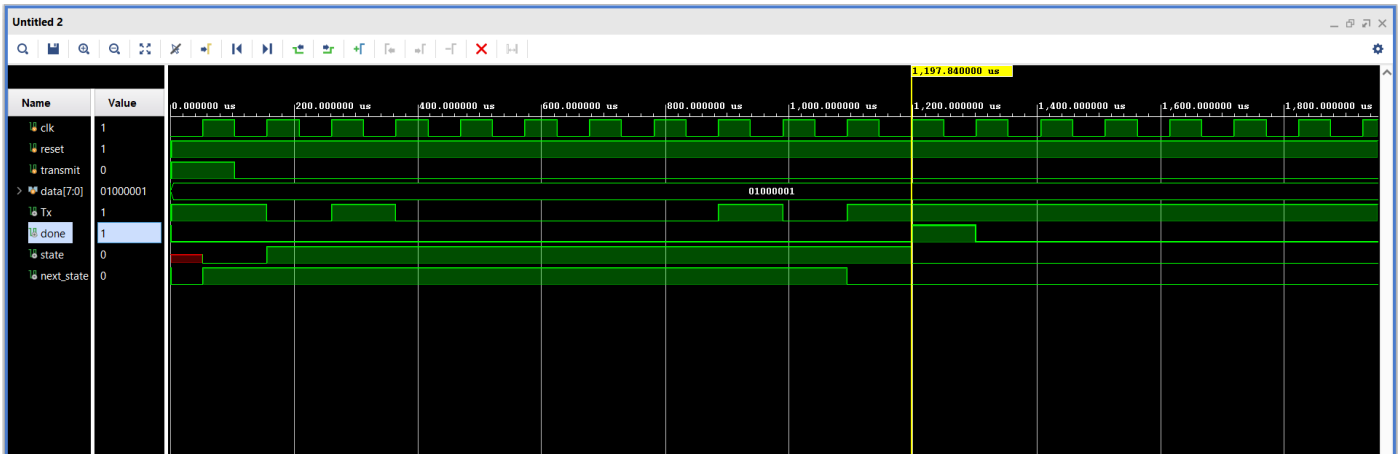
2) Sample Testbench and corresponding output for uart_transmitter (**uart_tx**) module :

Test Bench:

```
always #52080 clk = ~clk;  // 100 MHz clk/10416

initial
begin
clk = 0;
#1 reset = 1;
#3 data = 8'b01000001;
#10 transmit = 1;
#104160 transmit = 0;
end
```

Output:



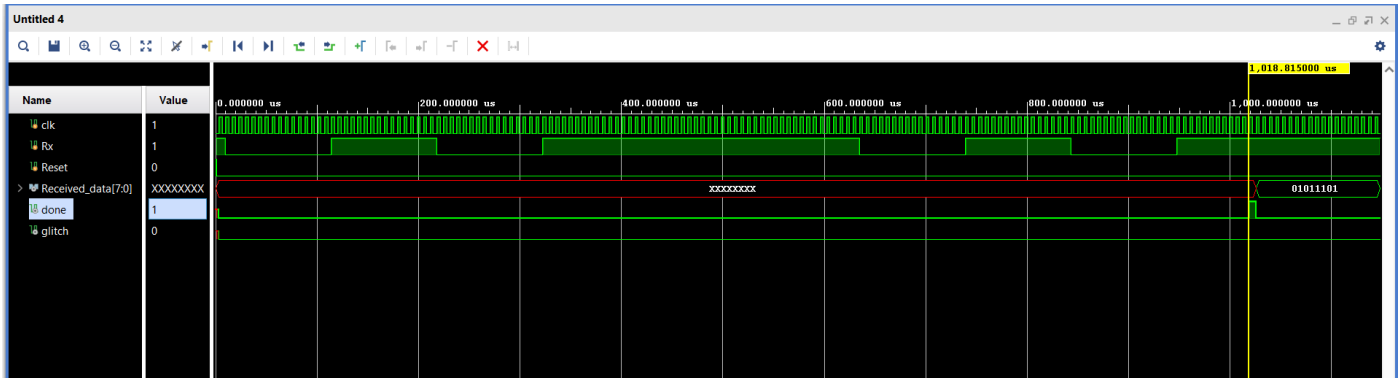
3) Sample Testbench and corresponding output for uart_receiver (**uart_rx**) module: (**without glitch**)

Testbench:

```
always #3255 clk = ~clk;

initial
begin
clk = 0;
Rx = 1;
Reset = 1;
#7 Reset = 0;
#10005 Rx = 0;
//#10000 Rx = 1; // if glitch
#104160 Rx = 1;
#104160 Rx = 0;
#104160 Rx = 1;
#104160 Rx = 1;
#104160 Rx = 1;
#104160 Rx = 0;
#104160 Rx = 1;
#104160 Rx = 0;
#104160 Rx = 1;
#200000 $finish;
end
endmodule
```

Output :



4) Sample Testbench and corresponding output for the **uart_rx** module **with a glitch** :

Test bench:

```
always #3255 clk = ~clk;

initial
begin
clk = 0;
Rx = 1;
Reset = 1;
#7 Reset = 0;
#10005 Rx = 0;
#10000 Rx = 1; // if glitch
//#104160 Rx = 1;
//#104160 Rx = 0;
//#104160 Rx = 1;
//#104160 Rx = 1;
//#104160 Rx = 1;
//#104160 Rx = 0;
//#104160 Rx = 1;
//#104160 Rx = 0;
//#104160 Rx = 1;
#200000 $finish;
end
```

Output :