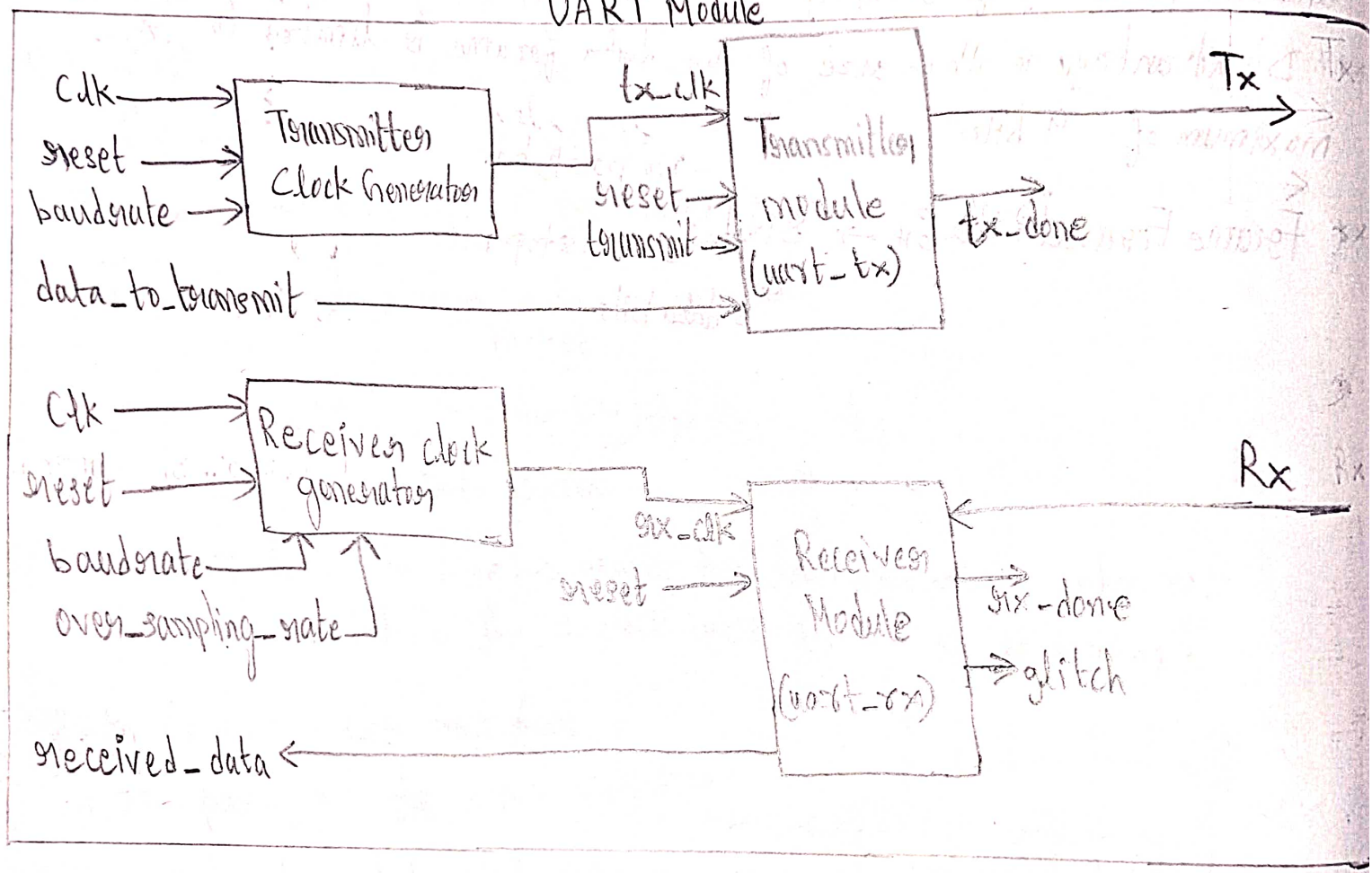
UART design :-

→ Format ⇒ 8N1
→ clock frequency ⇒ 100MHz
→ Baudrate ⇒ 9600 bps
→ Asynchronous Reset

Block diagram of UART Module



Transmitter module :-

→ Predefined baud rate = 9600 bps
→ clock freq = 100 MHz ⇒ Time period = 10ns

⇒ 1 bit duration = $\frac{100 \times 10^6}{9600}$ clock cycles = 10416.67 clock cycle.

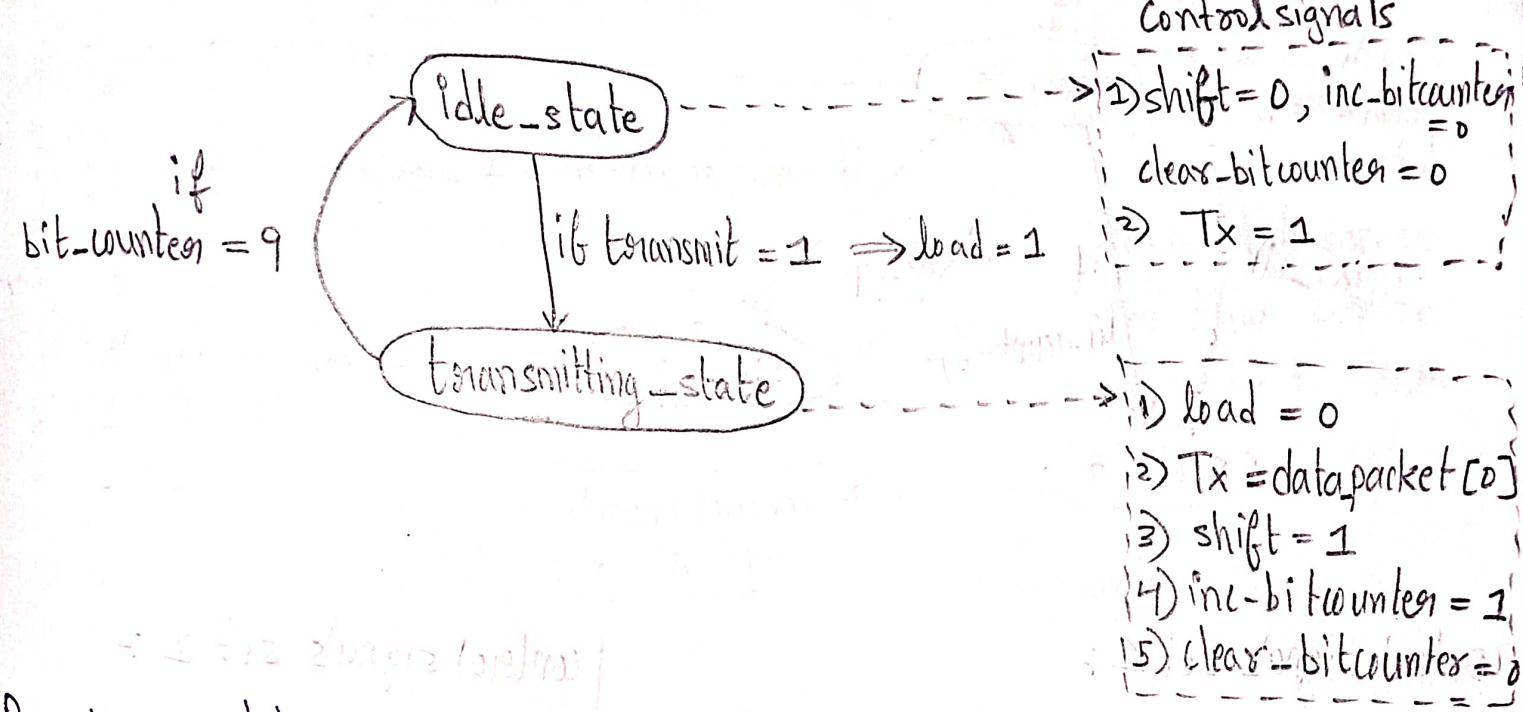
⇒ To meet the baud rate condition, 1 bit duration = 10416 clock cycle
= 104160 ns

* Generating a tx-clk, with Time period = 10416 × (T of 100 MHz clk)

⇒ frequency of tx_clk = $\frac{\text{freq of 100 MHz clk}}{10416}$

⇒ clock division by 10416 ⇒ MOD 10416 counter is used.

State diagram for Moore machine of Transmitter :



Receiver module :

→ Received bit duration = 104160 ns = 10416 clock cycles.

→ over sampling rate = 16 ⇒ 1 bit duration = 16 samples

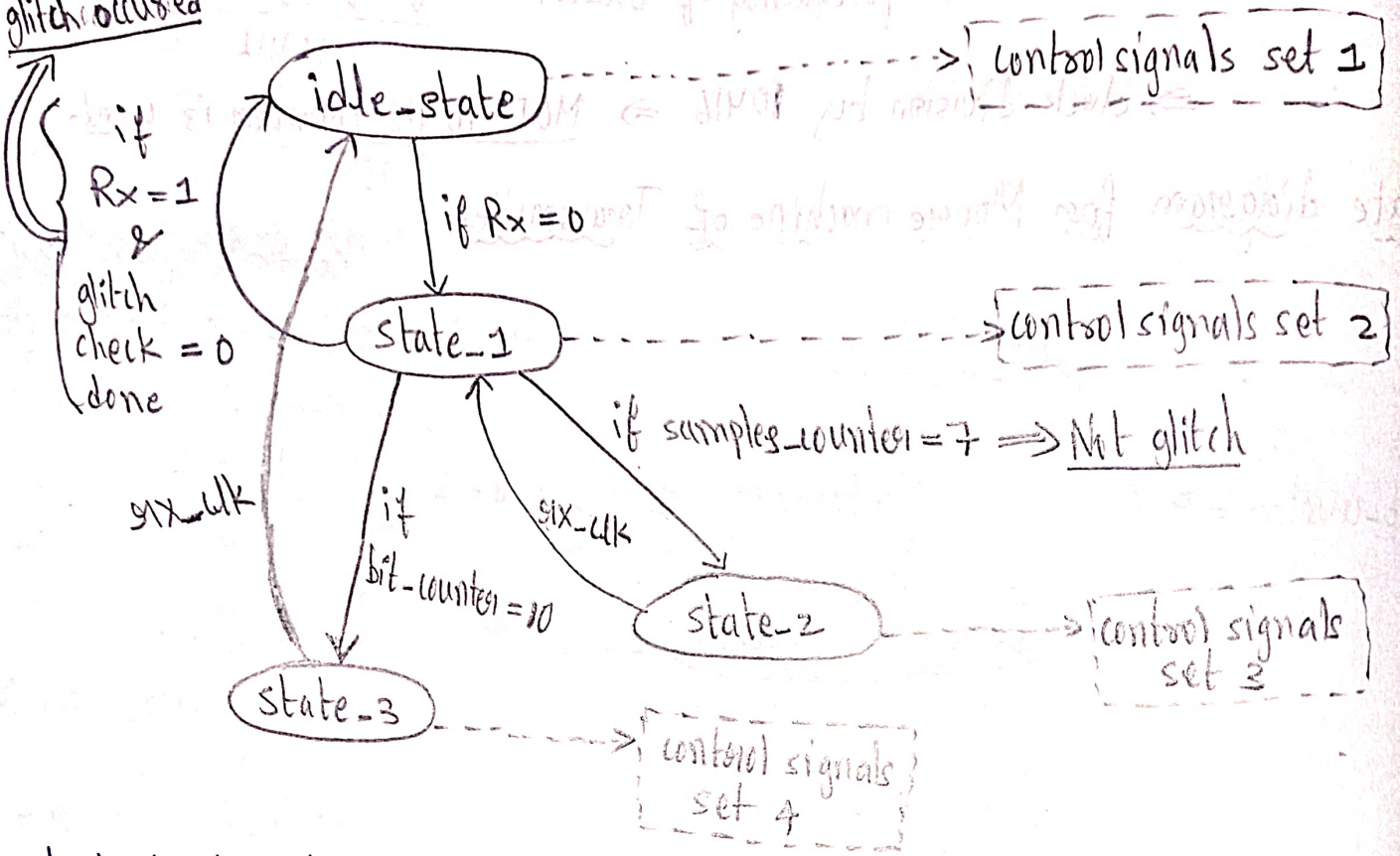
⇒ 1 sample duration = $\frac{10416}{16}$ = 651 clock cycles = 6510 ns

* Generating a rx-clk, with Time period = 651 × (T of 100 MHz clk).

⇒ frequency of rx_clk = $\frac{\text{freq of 100 MHz clk}}{651}$

⇒ clock division by 651 ⇒ MOD 651 counter is used.

State diagram of FSM for Receiver :



control signals set 1 :

load = 0 , done = 0, glitch_check_done = 0

inc_samplescounter = 0 , clear_samplescounter = 1

clear_bitcounter = 1

control signals set 2 :

inc_samplescounter = 1

shift = 0, inc_bitcounter = 0

clear_samplecounter = 0

clear_bitcounter = 0

control signals set 3 :

shift = 1, inc_bitcounter = 1,

glitch_check_done = 1

control signals set 4 :

load = 1

done = 1