

PARANJAI KARNATI

Undergraduate At Indian Institute of Information Technology Allahabad

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PARANJAIK

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Hyderabad, India

SKILLS

Verilog

C++

C

RTL Design

Python

Static Timing Analysis

Github

Assembly Language (8086)

DSA

SOFTWARES

Xilinx Vivado

LTspice

Cadence Virtuoso

Matlab

EDWinXP

Yosys

OpenSTA

Ansys Electronics

Multisim

KEY COURSES

Digital Electronics

CMOS Digital Design

MicroProcessors

Embedded Systems Design

Operating Systems

LANGUAGES

English: Conversational proficiency

Hindi,Telugu: Native Proficiency

OTHER HIGHLIGHTS

- Solved 220+ problems on Leetcode : [Leetcode Profile](#)
- 3-Star Coder At Codechef : [Codechef Profile](#)
- Pupil At Codeforces : [Codeforces Profile](#)

EDUCATION

B Tech - ECE | [Indian Institute of Information Technology Allahabad](#)

2021 - 2025

Prayagraj, UttarPradesh, India

- CGPA(Till Sem-4) : 8.4

Sr. Secondary Education | [Vijaya Ratna Junior College](#)

2021

Hyderabad, Telangana, India

- Percentage : 98.49

High School | [St.Martin's High School](#)

2019

Hyderabad, Telangana, India

- Percentage : 94.5

PROJECTS

1) Nexys-4-DDR FPGA implementation of **Booth Multiplier** using **Algorithmic State Machines** |

- Used **Datapath and Controller Design**. Implemented the **Controller using Finite State Machine**.
- No Warnings on **Synthesis and Implementation**. Total On-Chip Power is **0.107W** and Junction temperature is **25.5 °C** and no **DRC Violations**

2) RTL Design of a 8-bit Multiplier Using **Vedic Math Algorithm** with **Algorithmic State Machines** |

- Used **Datapath and Controller Design**. In **Datapath** used following **functional components for computation** : 8-bit Parallel Load registers,Counter,Quadruple 2:1 line Multiplexers, 8-bit and 4-bit adders, 4x4 Multipliers.
- Implemented the **Controller using Finite State Machine**, to generate control signals which control the computation in Datapath.
- Successfully verified** the functioning of 8-bit Multiplier using Vedic Algorithm.

3) Designed a **Sequence Detector** to detect "**10110**" using **Moore Machine** |

- Defined **6 states** from "" to "**10110**" with Moore Type Machine.Implemented the **structural model** using **4 8:1 MUXES** and **3 D Flip-Flops**.
- Implemented **Behavioral Model** using **switch cases**.And successfully verified the simulation outputs.

4) Designed a **16-bit Adder** using verilog. |

- Designed **behavioral model** of 16-bit adder using **switch cases**. Designed **structural model** of 16-bit adder using **4 4-bit ripple carry** adders.
- More **delay** for above model due to **Carry Propagation.Reduced delay** of above implementation by designing the 16-bit adder using **4 4-bit carry look-ahead** adders.Resulting **higher Speed**.
- A clear **trade off b/w speed and hardware complexity** is observed.