Designing & Programming Parallel Heterogeneous Architectures: a RISC-V perspective

Location: Room **Bianca A**

Scheduled time: **14:00 – 15:00**

Speaker: Luca Benini

Luca Benini holds the chair of digital Circuits and systems at ETHZ and is Full Professor at the Università di Bologna.
He served as chief architect in STmicroelectronics France.
Dr. Benini's research interests are in energy-efficient parallel computing systems, smart sensing micro-systems and machine learning hardware. He has published more than 1000 peer-reviewed papers and five books.
He is an ERC-advanced grant winner, a Fellow of the IEEE, of the ACM and a member of the Academia Europaea.
He is the recipient of the 2016 IEEE CAS Mac Van Valkenburg award and of the 2019 IEEE TCAD Donald O. Pederson Best Paper Award.

Abstract

The trend toward highly parallel and heterogeneous architecture has accelerated and gained momentum with the advent of the RISC-V ISA, thanks to its openness, extensibility and rapid adoption. In this talk I will detail our experience and the research insights gathered while designing hardware a software for a wide range of open heterogeneous architectures based on the risc-V cores developed in the context of the parallel-ultra low power (PULP) platform. I will conclude sharing my thoughts on short and long term research opportunities and challenges.