AN-9070

Smart Power Module Motion-SPM™ Products in µMini-DIP SPM® Packages

Table of Contents

Introduction

This application note supports the Motion-SPM™ product in a µMini-DIP SPM® package. It should be used in conjunction with the Motion-SPM product datasheets, Fairchild's SPM reference designs (*RD-344, RD-345*), and related application notes (*AN-9071: Thermal Performance Information*, *AN-9072: Mounting Guidance*).

Design Concept

The key design objective of Motion-SPM product in the µMini-DIP package is to create minimized package and a low-power-consumption module with improved reliability. This is achieved by applying new three-in-one HVIC (gate-driving High-Voltage Integrated Circuit), new IGBT of advanced silicon technology, and improved ceramics substrate base transfer mold package. The new µMini DIP SPM package can achieve 40% reduction in size and improved reliability as compared with existing Mini-DIP SPM package.

The second important design advantage is specialized in-product line-up regarding each application. Target applications of Motion-SPM products in µMini-DIP SPM packages are inverterized motor drives for household electric appliances such as air conditioners, washers, refrigerators, and fan motors.

FN**A**4XX60X Motion-SPM specializes in slow switching frequency (under 5kHz) applications; such as refrigerators and air conditioners, due to low $V_{CE(SAT)}$ of IGBT.

The FN**B**4XX60X Motion-SPM specializes in fast switching frequency (over 5kHz) applications; such as washing machines, dish washers, and fan motor drives; due to the low switching loss ($E_{SW(ON)}$, $E_{SW(OFF)}$) of IGBTs/FRDs. Customers can choose the product option that best meets the design specifications.

The third design advantage is the integrated NTC thermistor for temperature measuring of power chips (e.g. IGBTs, FRDs) on the same substrate. Most customers want to know the temperature of power chips precisely due to the impact on quality, reliability, and lifetime improvement. This desire is restricted because integrated power chips (e.g. IGBTs, FRD) inside modules are operated in high-voltage conditions. Therefore, instead of directly sensing the temperature of power chips, external NTC thermistors have been used for sensing the temperature of module or heat-sink. Although this method doesn't accurately reflect the temperature of power components; it is a simple and cost-effective method. However, the NTC thermistor of the µMini-DIP SPM package is integrated with power chips on the same ceramic substrate to more accurately measure the temperature of power chips.

The detailed features and integrated functions are:

- Exceptionally small package size (WxD: 39mmx23mm) in three-phase inverter bridge module
- Advanced silicon technology IGBTs, FRDs for low power loss and high ruggedness
- Built-in NTC thermistor for sensing temperature of power chips
- Easy PCB(print circuit board) layout due to built-in bootstrap diode and independent VS pin
- 600V/5A to 20A ratings in one package (with identical mechanical layouts)
- High reliability due to advanced ceramic substrate transfer mold package
- Three-phase IGBT inverter bridge, including control ICs for gate drive and protection
  - High-Side: UVLO (Under-Voltage Lockout) protection for control voltage without fault-out signal (V_{FO})
  - Low-Side: UVLO (Under-Voltage Lockout) and SCP (Short-circuit Current Protection) through external shunt resistor with fault-out signal (V_{FO})
- Soft turn-off function during protection functions
- Single-grounded power supply and opto-coupler-less interface due to built-in HVIC
- Minimized standby current of drive IC (HVIC/LVIC) for energy regulation
- Active-HIGH input signal logic resolves the startup and shutdown sequence restriction between V_{CC} (control supply voltage) and signal input, providing fail-safe operation with direct connection between the Motion-SPM product and a 3.3V MCU or DSP without additional external sequence logic
- Isolation voltage rating of 2000V_{rms} for one minute due to minimized package size

µMini-DIP SPM Package Technology

Power Devices

The µMini-DIP SPM package performance improvement is primarily the result of the technological advancement of the power devices (i.e., IGBT and FRD) in the three-phase inverter circuit. The design goal is reduction of power loss and increment of current density of the power devices.

IGBTs

The µMini-DIP SPM package includes Fairchild's new technology. Through advanced NPT (non-punch-through) technology of IGBT, the package keeps a suitable SOA (Safe Operating Area) for each motor control application, while dramatically reducing the on-state conduction loss or turn-on/off switching losses.

In the FN**A**4XX60X series, low $V_{CE(SAT)}$ is achieved by sacrificing turn-off switching power loss ($E_{SW(OFF)}$, IGBT turn off switching loss) because there is a trade-off between $V_{CE(SAT)}$ (collector-to-emitter voltage) and $E_{SW(OFF)}$.

In the FN**B**4XX60X series, minimization of turn-on/off switching power loss ($E_{SW(ON)}$, $E_{SW(OFF)}$) is accomplished by maximizing fast switching speed of the existing NPT IGBT.

Table 1 and Figure 1 show that the advanced NPT IGBT of FN**A**4XX60X series achieves almost 30% chip shrink with the same DC performance as compared with previous PT (Punch Through) IGBT and NPT (Non Punch Through) IGBT. The improved silicon technology enables the chip size to shrink while maintaining performance. The switching loss of the advanced NPT IGBT (especially, turn-off switching loss) is increased 60% as compared with that of NPT IGBT. Therefore, the main application of the FN**A**4XX60X series (applied advanced NPT IGBT) is low switching frequency applications, such as air conditioners and refrigerators.

Table 1. Collector-Emitter Saturation Voltage & IGBT Turn-On/Off Switching Loss

IGBT	Chip Size [pu]	$V_{CE(SAT)}$ [V] at I_C=10A, V_{CC}=15V		$E_{SW(OFF)}$ [μJ], I_C=10A, V_{CC}=15V	
		T_J=25°C	T_J=125°C	T_J=25°C	T_J=125°C
PT IGBT 10A	1.3	1.90	2.00	520	760
NPT IGBT 10A	1.3	1.60	1.85	240	330
Advanced NPT IGBT 10A	1.0	1.60	1.75	360	580

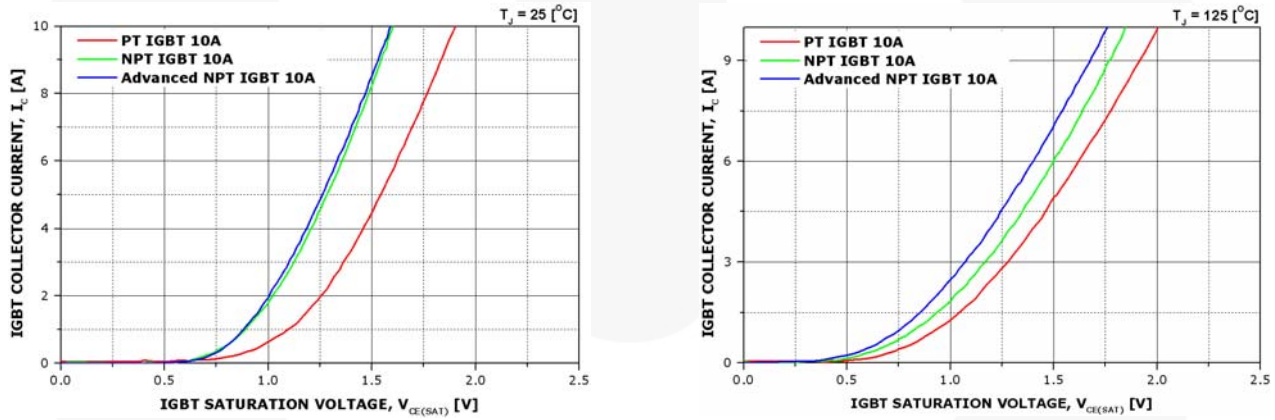


Figure 1. Typical $V_{CE(SAT)}$ (Collector-to-Emitter Voltage) Comparison of IGBT

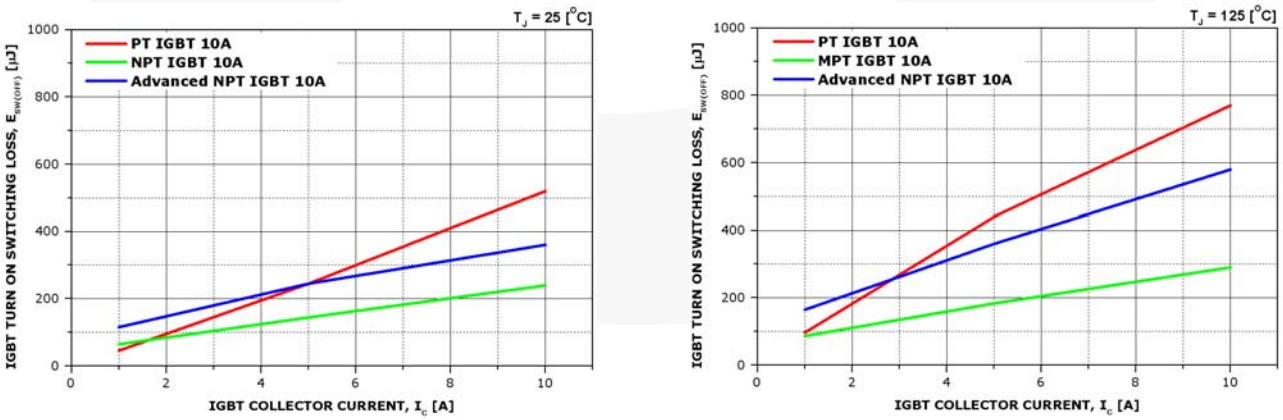


Figure 2. Typical Turn-Off Switching Power Loss (at T_J=25°C, 125°C) Comparison of IGBT

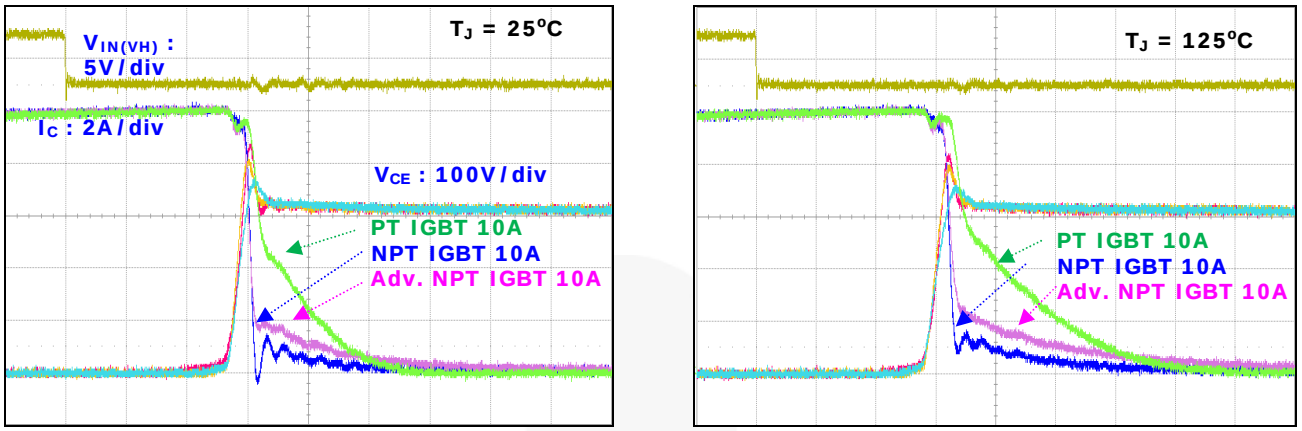


Figure 3. Turn-Off Switching Waveform of Advanced NPT IGBT and Existing IGBTs

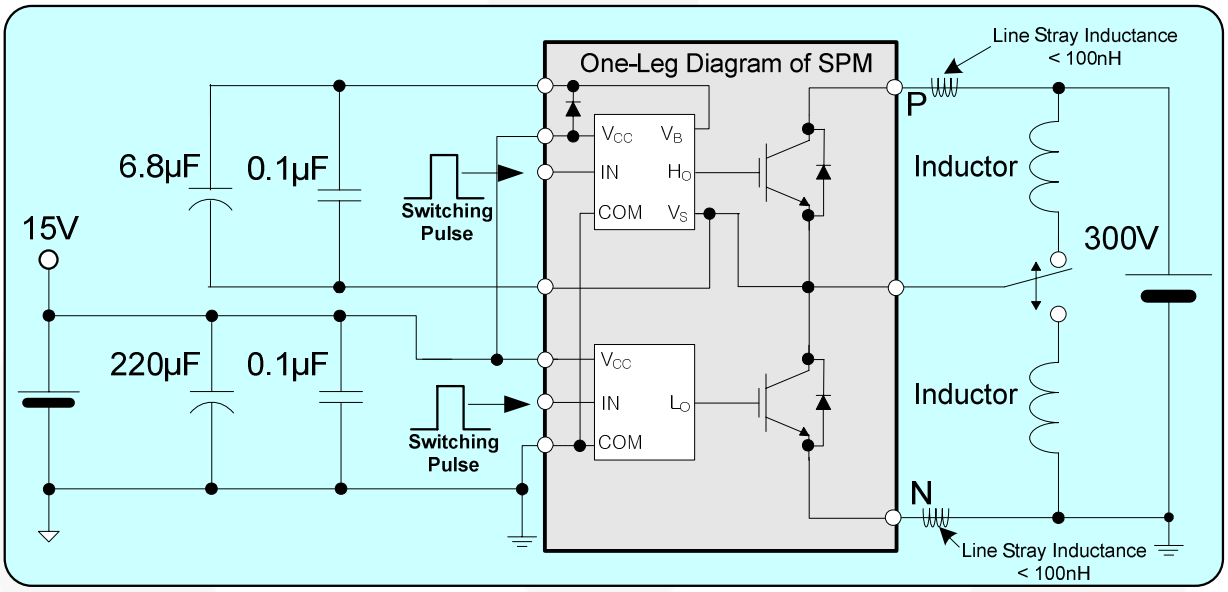


Figure 4. IGBT Switching Test Circuit Diagram
(Switching Conditions: V_{DC}=300V, V_{CC}=15V, C_{VBS}=6.8μF, C_{VCC}=220μF, Total Stray L<200nH)

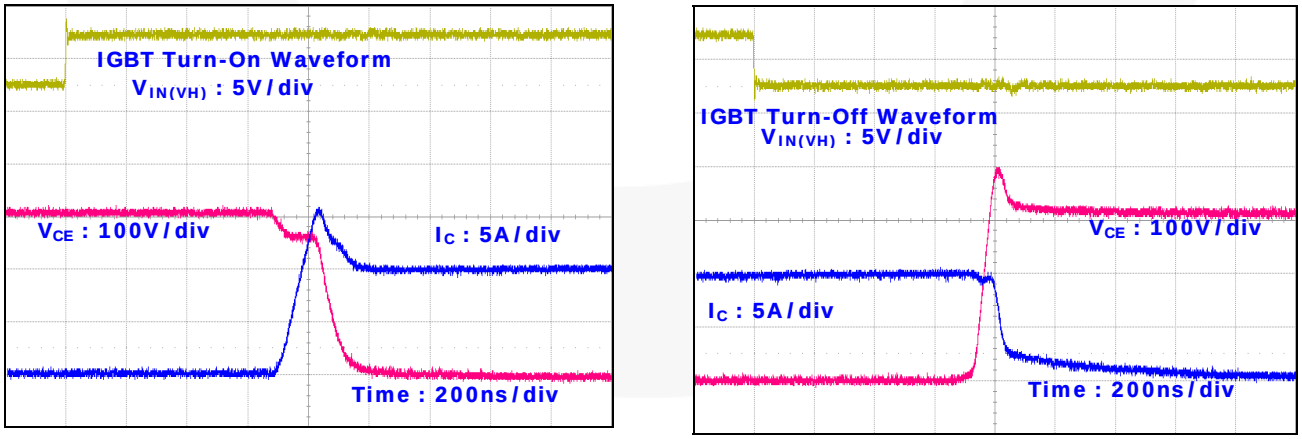


Figure 5. FNA41060 Typical Turn-On, Turn-Off Waveform at T_J=125°C

FRDs

The FRD apply an advanced STEALTH™ diode that has a low forward voltage drop and high breakdown voltage along with soft recovery characteristics.

The advanced STEALTH diode is optimized to low loss performance in high-frequency hard-switched conditions.

Advanced STEALTH™ diodes exhibit a low reverse recovery current ($I_{RM(REC)}$) and exceptionally soft recovery under typical operation conditions.

Table 2 shows the advantage of an advanced STEALTH™ diode in the µMini-DIP SPM package, compared with the existing version of ultrafast diode in the existing Mini-DIP SPM package.

Table 2. Characteristics Comparison between Ultrafast Diode and Advanced STEALTH™ Diode

	Test Conditions (T_J=125°C)	t_{rr} [ns]	t_a [ns]	t_b [ns]	Softness Factor	I_{rr} [A]
Ultrafast Diode	I_F=1A, dI_F/dt=100A/µs, V_R=30V	170.23	54.52	115.71	2.12	0.77
	I_F=15A, dI_F/dt=100A/µs, V_R=390V	147.44	52.75	94.69	1.80	5.43
Advanced STEALTH™ Diode	I_F=1A, dI_F/dt=100A/µs, V_R=30V	168.54	49.09	119.45	2.43	0.67
	I_F=15A, dI_F/dt=100A/µs, V_R=390V	188.25	45.44	142.81	3.14	4.40

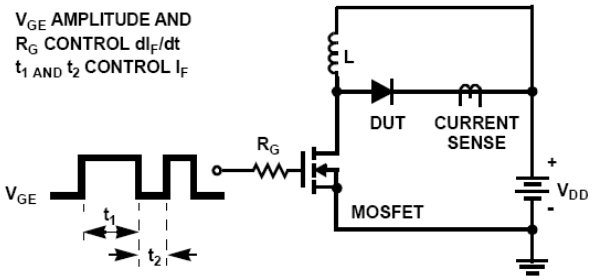


Figure 6. t_{rr} Test Circuit

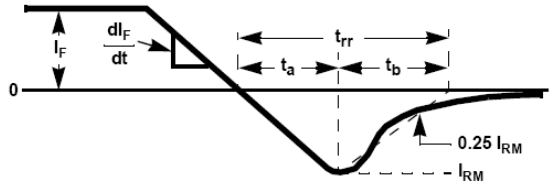
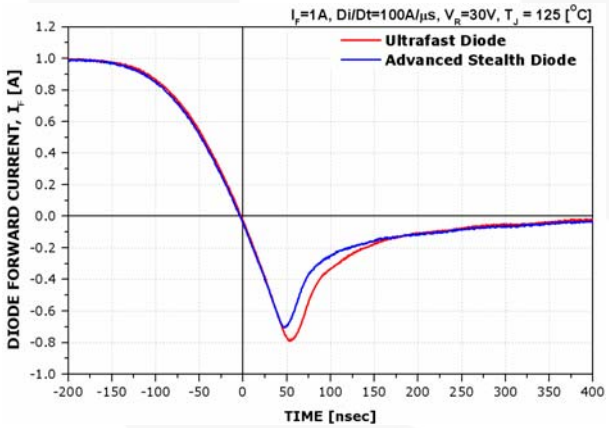


Figure 7. t_{rr} Waveforms and Definitions



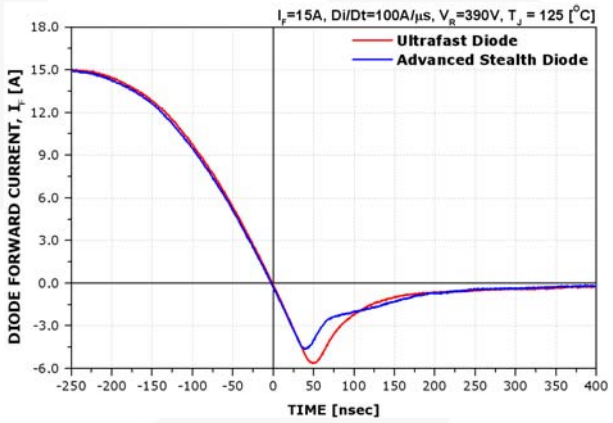
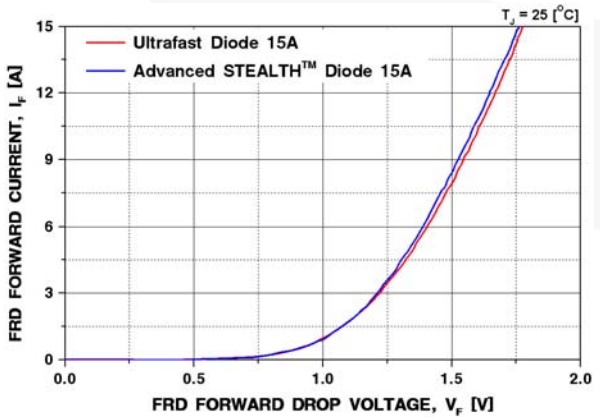


Figure 8. t_{rr} Waveform Comparison between Ultrafast Diode and Advanced STEALTH™ Diode



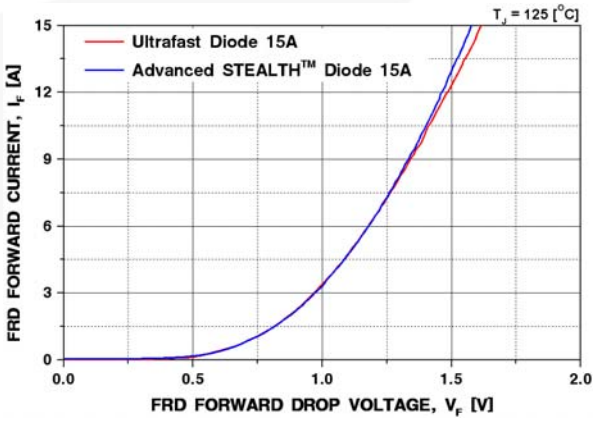


Figure 9. FRD Typical V_F (Forward Drop Voltage) Comparison

Gate Drive IC (HVIC, LVIC)

The HVIC (gate-driving high-voltage integrated circuits) and LVIC (gate-driving low-voltage integrated circuits) were designed as to have only the minimum necessary functionality required for low-power inverter drives.

HVIC

The µMini-DIP SPM package three-in-one HVIC includes the functions of three HVICs for optimized package design. The HVIC has a built-in high-voltage level-shift function that enables the ground referenced PWM signal to be sent directly to the Motion-SPM product's assigned high-side IGBT gate circuit, which enables opto-coupler-less interface and simplifies system design. The HVIC has built-in UVLO (under-voltage lockout) protection for V_{BS}. Because the bootstrap charge-pump circuit interconnects to the low-side V_{CC} bias external to the Motion-SPM product, the high-side gate drive power can be obtained from a single 15V control supply referenced to control ground. It is not necessary to have three isolated voltage sources for the high-side IGBT gate drive, as is required in inverter systems using conventional power modules. Recent progress in the HVIC technology includes chip downsizing through the introduction of wafer fine process technology. Logic input of HVIC is compatible with standard 3.3/5.0V CMOS/LSTTL outputs. HVIC's high-voltage process and common-mode noise cancellation technique provide stable operation in the high-side driver under high-dv/dt noise circumstances. All HVIC include prevention functions of malfunctions, such as latch by high-dv/dt.

LVIC

The new LVIC of µMini-DIP SPM package's low standby current and logic input of LVIC are compatible with standard 3.3/5.0V CMOS/LSTTL outputs. The LVIC has built-in UVLO (under-voltage lockout) for V_{CC} and SCP (Short-circuit Current Protection), as well as OCP (Over-Current Protection) for internal power components.

Package

Since heat dissipation is an important factor that limits the power module's current capability, the heat dissipation characteristics are critical in determining the µMini-DIP SPM package performance. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to a good package technology lies in the accomplishment of optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In the µMini-DIP SPM package, technology was developed in which bare ceramic with good heat dissipation characteristics is attached directly to the lead frame. This technology already applied in Mini-DIP SPM, but was improved through new adhesion methods. This made it possible to achieve improved reliability and heat dissipation, while maintaining cost effectiveness.

Figure 10 shows the package outline and the cross sections of the µMini-DIP SPM package.

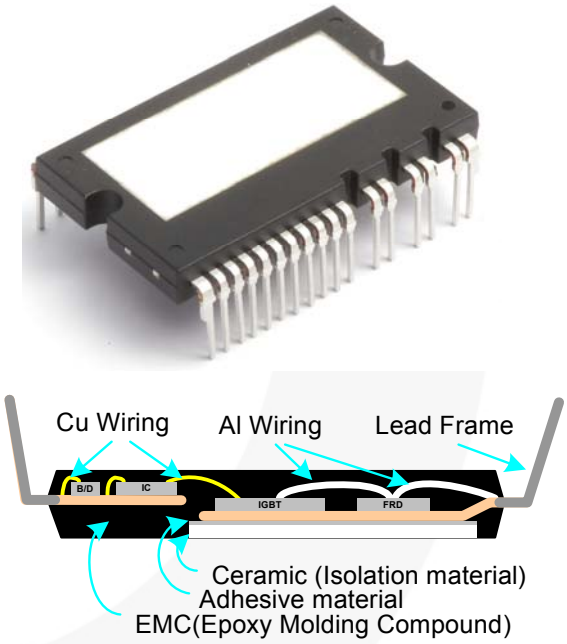


Figure 10.Vertical Structure of µMini-DIP SPM Package

Outline & Pin Description

Outline Drawings

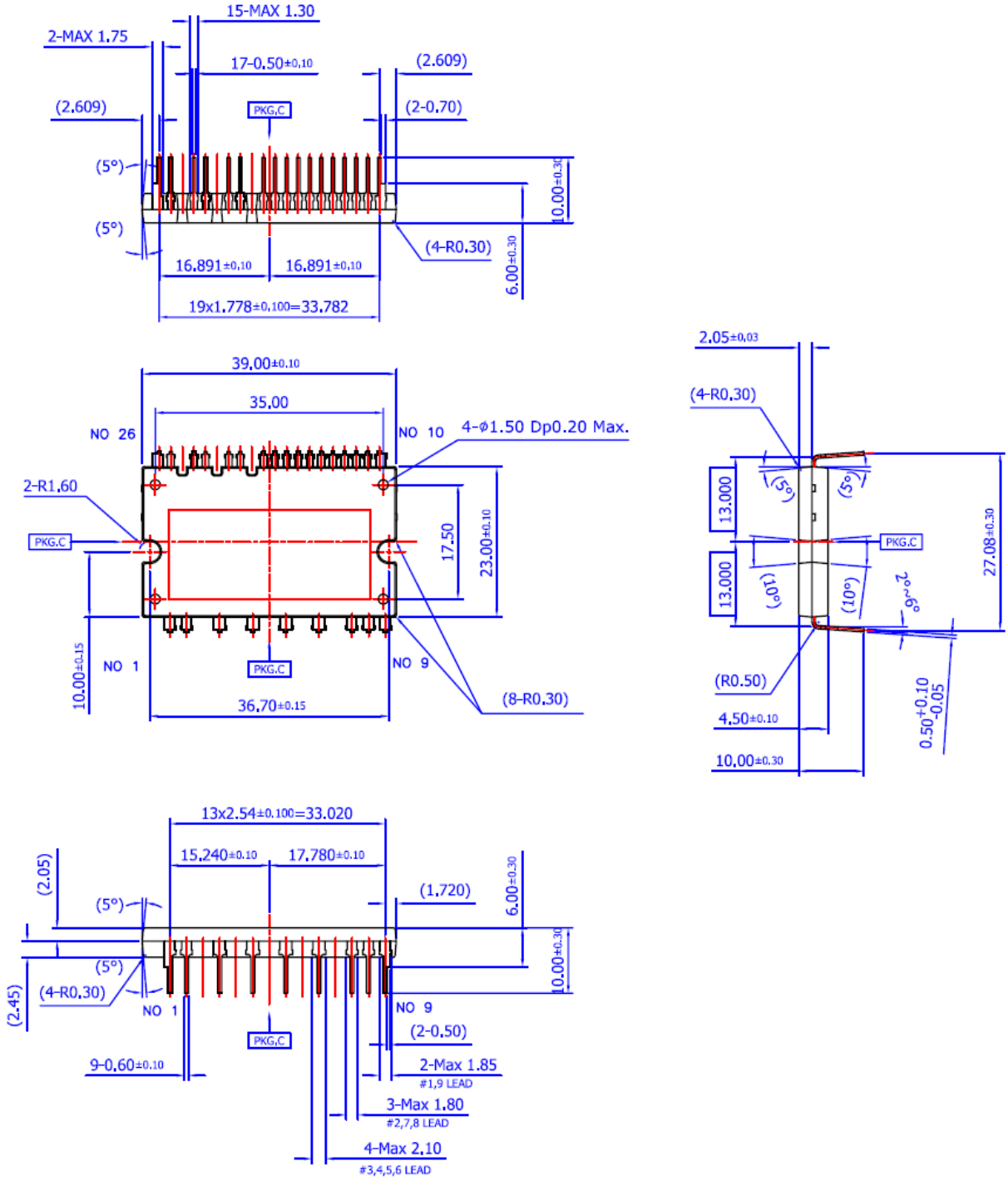


Figure 11.SPM26-AAA, Short-Lead & Normal Forming Option

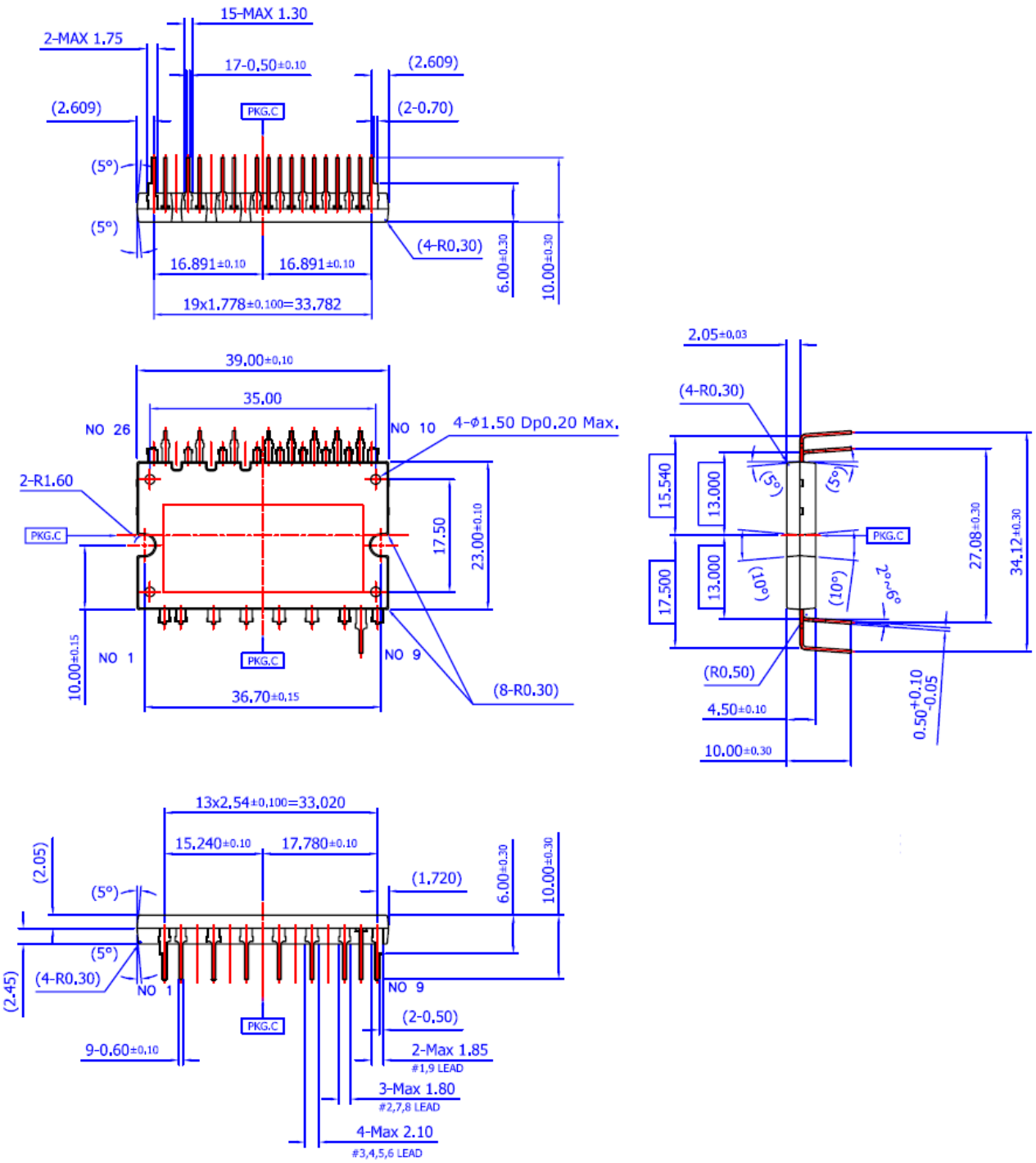


Figure 12.SPM26-AAB, Short-Lead & Signal and N terminal Double Forming Option

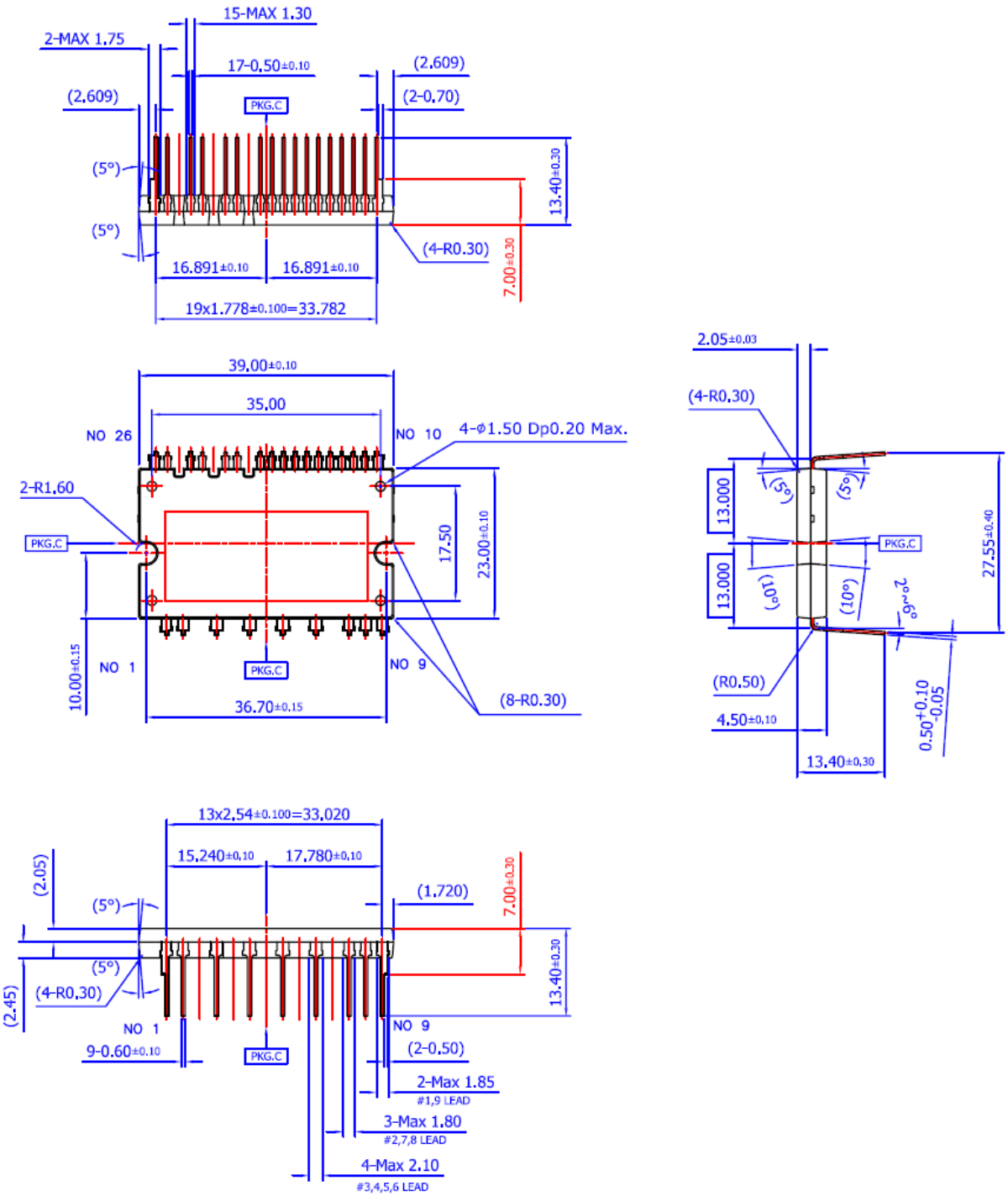


Figure 13.SPM26-AAC, Long-Lead & Normal Forming Option

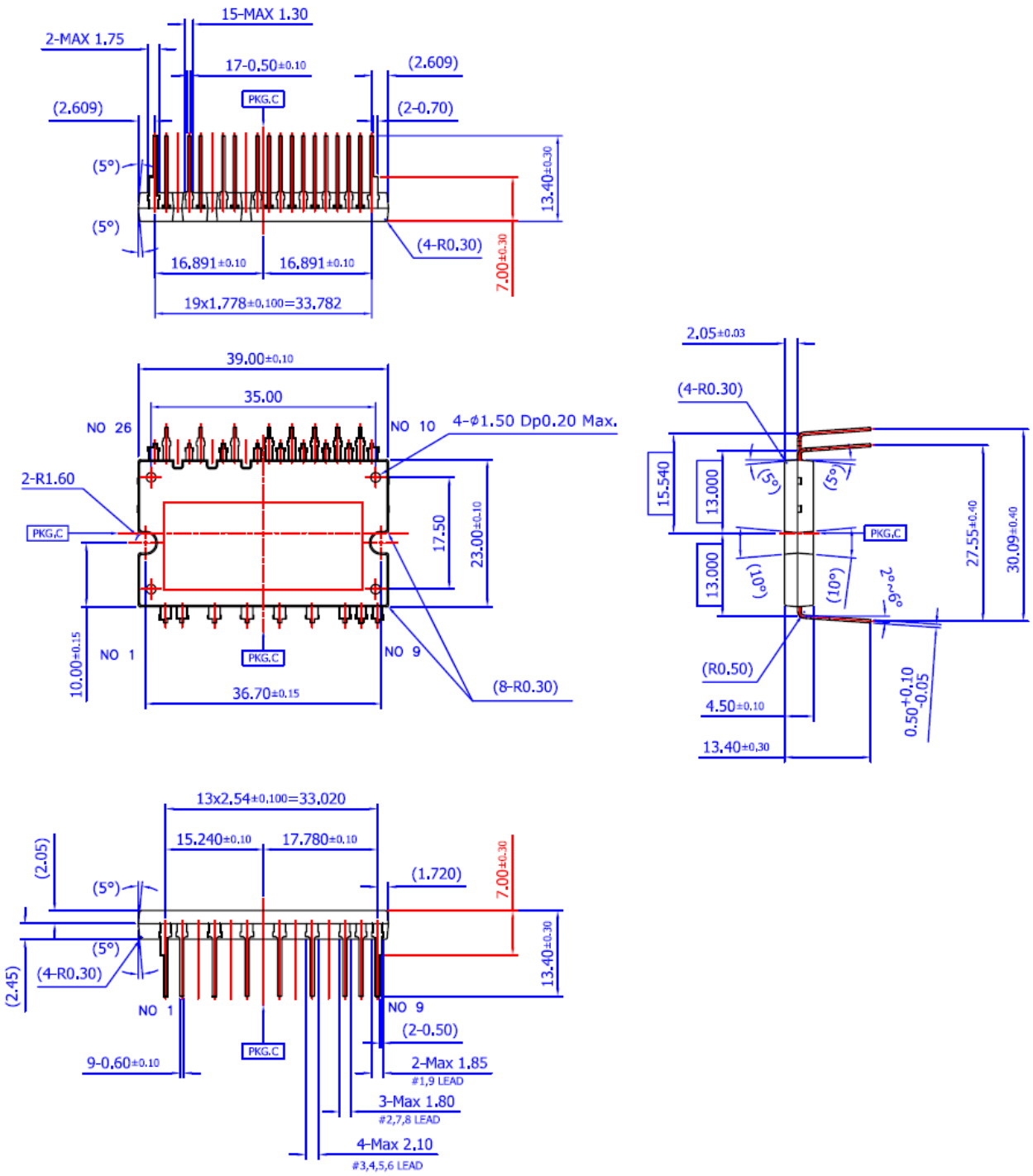


Figure 14.SPM26-AAD, Long-Lead & N terminal Double Forming Option

Descriptions of the Input and Output Pins

Table 3 defines the input and output pins of the Motion-SPM product in the µMini-DIP SPM package.

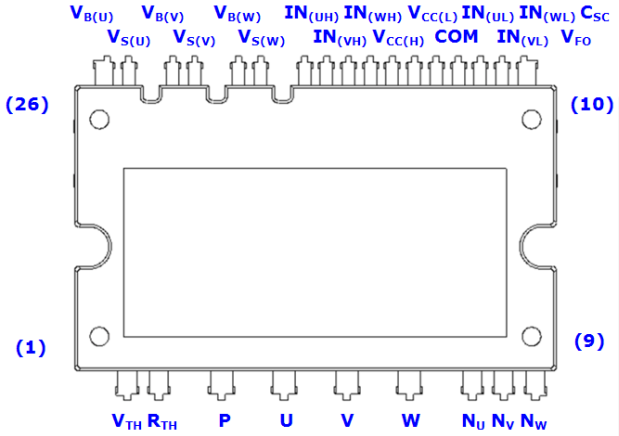


Figure 15. Pin Configuration

Table 3. Pin Descriptions

Pin #	Name	Pin Description
1	V_{TH}	Thermistor Bias Voltage
2	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
3	P	Positive DC-Link Input
4	U	Output for U Phase
5	V	Output for V Phase
6	W	Output for W Phase
7	N_U	Negative DC-Link for U Phase
8	N_V	Negative DC-Link for V Phase
9	N_W	Negative DC-Link for W Phase
10	C_{SC}	Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input
11	V_{FO}	Fault Output
12	IN(WL)	Signal Input for Low-Side W Phase
13	IN(VL)	Signal Input for Low-Side V Phase
14	IN(UL)	Signal Input for Low-Side U Phase
15	COM	Common Supply Ground
16	$V_{CC(L)}$	Low-Side Common Bias Voltage for IC and IGBTs Driving
17	$V_{CC(H)}$	High-Side Common Bias Voltage for IC and IGBTs Driving
18	IN(WH)	Signal Input for High-Side W Phase
19	IN(VH)	Signal Input for High-Side V Phase
20	IN(UH)	Signal Input for High-Side U Phase
21	$V_{S(W)}$	High-Side Bias Voltage Ground for W Phase IGBT Driving
22	$V_{B(W)}$	High-Side Bias Voltage for W Phase IGBT Driving
23	$V_{S(V)}$	High-Side Bias Voltage Ground for V Phase IGBT Driving
24	$V_{B(V)}$	High-Side Bias Voltage for V Phase IGBT Driving
25	$V_{S(U)}$	High-Side Bias Voltage Ground for U Phase IGBT Driving
26	$V_{B(U)}$	High-Side Bias Voltage for U Phase IGBT Driving

High-Side Bias Voltage Pins for Driving the IGBT/High-Side Bias Voltage Ground Pins for Driving the IGBTs

► Pins: $V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$

- These are drive power supply pins for providing gate drive power to the high-side IGBTs.
- The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
- Each bootstrap capacitor is charged from the V_{CC} supply during the on-state of the corresponding low-side IGBT.
- To prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.

Low-Side Bias Voltage Pin / High-Side Bias Voltage Pins

► Pins: $V_{CC(L)}$, $V_{CC(H)}$

- These are control supply pins for the built-in ICs.
- These two pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.

Low-Side Common Supply Ground Pin

► Pin: COM

- The Motion-SPM product common pin connects to the control ground for the internal ICs.
- **Important**! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

Signal Input Pins

► Pins: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These pins control the operation of the built-in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 5V-class CMOS.
- The signal logic of these pins is active HIGH. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the Motion-SPM product against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 32.

Short-Circuit Current Detection Pins

► Pin: C_{SC}

- The current-sensing shunt resistor should be connected between the pin C_{SC} and the low-side ground COM to detect short-circuit current *(reference Figure 20)*.
- The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the C_{SC} pin to eliminate noise.
- The connection length between the shunt resistor and C_{SC} pin should be minimized.

Fault Output Pin

► Pin: V_{FO}

- This is the fault output alarm pin. An active LOW output is given on this pin for a fault state condition in the SPM.
- The alarmed conditions are SCP (Short-Circuit Current Protection) or low-side bias UVLO (Under Voltage Lockout) operation.
- The V_{FO} output is open-drain configured. The V_{FO} signal line should be pulled up to the 5V logic power supply with approximately 4.7kΩ resistance.

Thermistor Bias Voltage

► Pin: V_{TH}

- This is the bias voltage pin of the internal thermistor. It should be connected to the 5V logic power supply.

Series Resistor for the Use of Thermistor (Temperature Detection)

► Pin: R_{TH}

- For case temperature (T_C) detection, this pin should be connected to an external series resistor.
- The external series resistor should be selected to meet the detection range matched for the specification of each application *(for details, refer to Figure 42)*.

Positive DC-Link Pin

► Pin: P

- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high-side IGBTs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (typically, metal film capacitors are used).

Negative DC-Link Pin

► Pins: N_U, N_V, N_W

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of the each phase.

Inverter Power Output Pin

► Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e.g. motor).

Internal Circuit

Figure 16 illustrates the block diagram of the Motion-SPM in µMini-DIP SPM. Note that the Motion-SPM consists of a three-phase IGBT inverter circuit power block, two drive ICs for control functions, one NTC thermistor for temperature detection, and three bootstrap diodes.

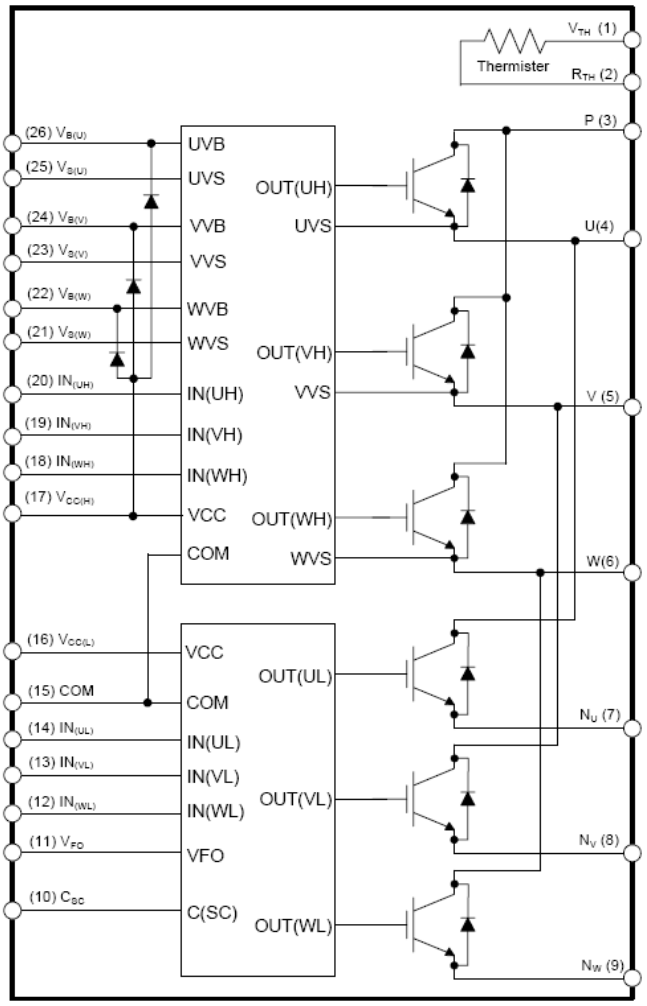


Figure 16.Internal Block Diagram

Ordering Information

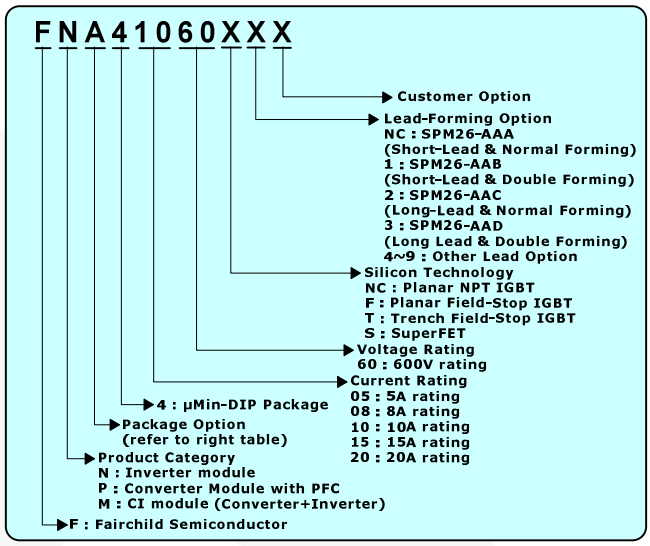


Figure 17.Top Mark Information

Table 4. Package Options

Suffix	Substrate	NTC Thermistor	Product Option
A	Ceramic	Yes	Normal
B	Ceramic	Yes	Fast
D	Ceramic	No	Normal
E	Ceramic	No	Fast

Key Parameter Design Guidance

Short-Circuit Current Protection (SCP)

µMini-DIP SPM packages use an external shunt resistor for the short-circuit current detection, as shown in Figure 18. The LVIC has built-in short-circuit current protection that senses the voltage to the C_{SC} pin and, if this voltage exceeds the $V_{SC(REF)}$ (the threshold voltage trip level of the short-circuit) specified in the devices datasheets($V_{SC(REF),Typ.}$ is 0.5V), a fault signal is asserted and the all lower arm IGBTs are turned off. Typically the maximum short-circuit current magnitude is gate voltage dependent. A higher gate voltage (V_{CC} & V_{BS}) results in a larger short-circuit current. To avoid this potential problem, the maximum short-circuit trip level is generally set to below 1.7 times the nominal rated collector current. The LVIC short-circuit current protection-timing chart is shown in Figure 19.

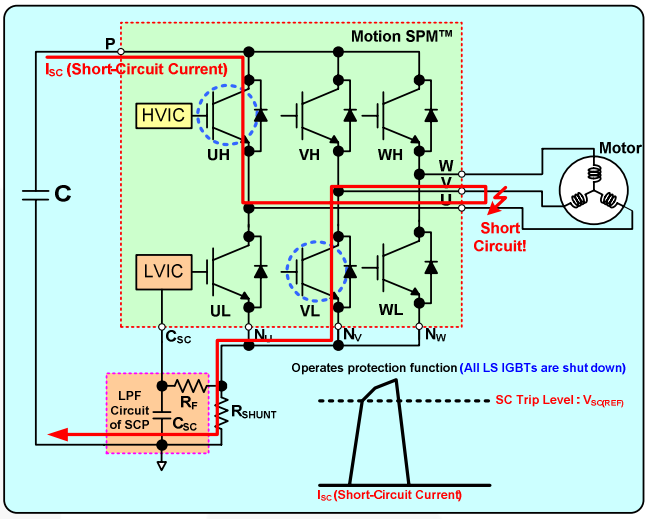


Figure 18.Operation of Short-Circuit Current Protection

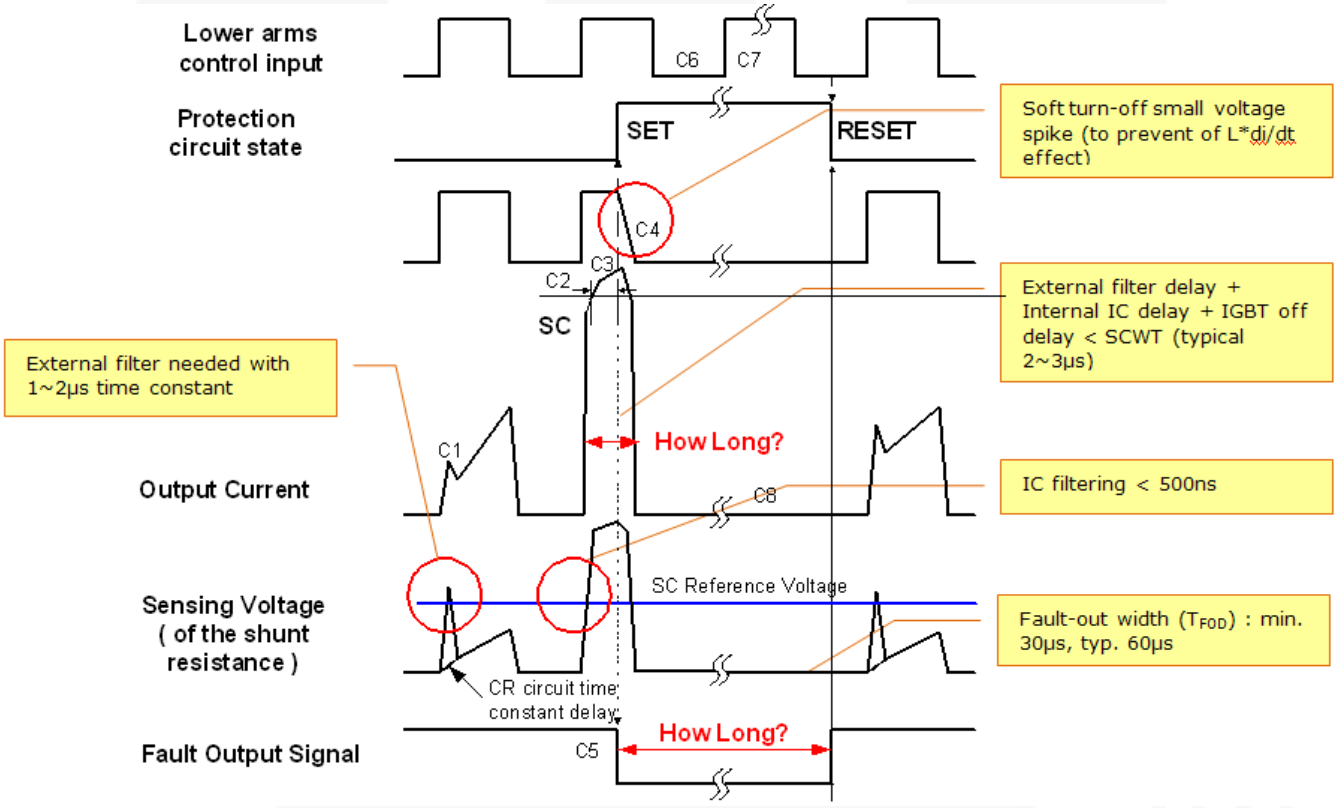


Figure 19.Timing Chart of Short-Circuit Current Protection Function

Notes:

C1. Normal operation: IGBT ON and carrying current
C2. Short-circuit current detection (SC trigger)
C3. Hard IGBT gate interrupt
C4. IGBT turns OFF
C5. Fault output timer operation start: Fault-out width (t_{FOD}) = min. 30µs
C6. Input “L”: IGBT OFF state
C7. Input “H”: IGBT ON state; but during the active period of fault output, the IGBT doesn’t turn ON
C8. IGBT OFF state

Selection of Shunt Resistor

Figure 20 shows an example circuit of the SC protection using one shunt resistor. The line current on the N-side DC-link is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N-side three-phase IGBTs are switched to OFF state and the F_O fault signal is transmitted to MCU. Since SC protection is non-repetitive, IGBT operation should be immediately halted when the F_O fault signal is given.

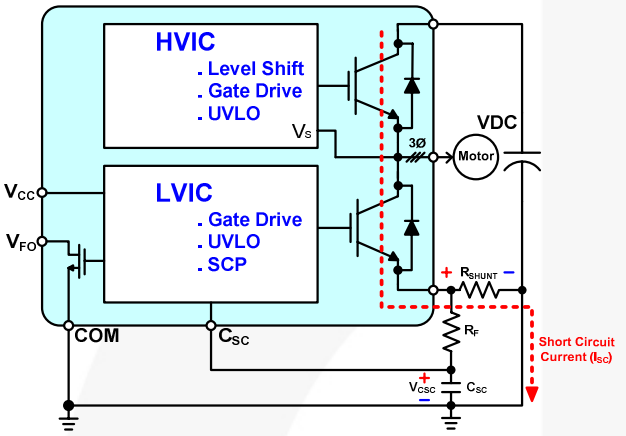


Figure 20. Example of Short-Circuit Current Protection Circuit with One Shunt Resistor

The value of shunt resistor is calculated by the following equations.

Maximum SC current trip level:

$I_{SC(max)}$=1.5 x I_C(rated current) (1)

SC trip referenced voltage:

V_{SC}=min. 0.45V, typ. 0.5V, max. 0.55V (2)

Shunt resistance:

$I_{SC(max)}=V_{SC(max)}/R_{SHUNT(min)} \rightarrow R_{SHUNT(min)}=V_{SC(max)}/I_{SC(max)}$ (3)

If the deviation of shunt resistor is limited below ±5%:

$R_{SHUNT(typ)} = R_{SHUNT(min)}/0.95$, $R_{SHUNT(max)} = R_{SHUNT(typ)}$ X 1.05(4)

And the actual SC trip current level becomes:

$I_{SC(typ)}=V_{SC(typ)} / R_{SHUNT(typ)}$, $I_{SC(min)} = V_{SC(min)} / R_{SHUNT(max)}$ (5)

The power rating of shunt resistor is calculated by the following equation:

$P_{SHUNT} = (I^2_{RMS}$ X R_{SHUNT} X Margin) / Derating Ratio (6)

- Maximum load current of inverter (I_{rms})
- Shunt resistor typical value at T_C=25°C (R_{SHUNT})
- Derating ratio of shunt resistor at T_{SHUNT}=100°C (from datasheet of shunt resistor)
- Safety margin (determined by customer)

The value of shunt Resistor calculation Examples: FNA41560, Shunt Resistor dispersion: ±5%.

Table 5. Specification for SCP Level ($V_{SC(ref)}$)

Conditions	Min.	Typ.	Max.	Unit
Specification at T_J =25°C, V_{CC} =15V	0.45	0.50	0.55	V

Table 6. Operating Short-Circuit Current Range (R_{SHUNT}=24.4mΩ (min.)(1), 25.7mΩ (typ.), 27.0mΩ (max.))

Conditions	Min.(2)	Typ.(3)	Max.(4)	Unit
Operating SC Level at T_J =25°C	16.66	19.43	22.50	A

Notes:

1. $R_{SHUNT(min)}$: $V_{SC(max)}/I_{SC(max)}$ = 0.55 / 22.5 = 24.4mΩ.
2. $I_{SC(min)}$: $V_{SC(min)}/R_{SHUNT(max)}$ = 0.45 / (0.0244/0.95x1.05) = 16.66A.
3. $I_{SC(typ)}$: $V_{SC(typ)}/R_{SHUNT(typ)}$ = 0.50 / (0.0244/0.95) = 19.43A.
4. Maximum SC trip level: 1.5 x IC = 1.5 x 15 = 22.5A.

Power rating of shunt resistor calculation examples:

- Maximum load current of inverter (I_{rms}): 5Arms
- Shunt resistor value at T_C=25°C (R_{SHUNT}): 24.8mΩ
- Derating ratio of shunt resistor at T_{SHUNT}=100°C: 70% *(refer to Figure 21)*
- Safety margin: 20%

P_{SHUNT} : (I^2_{rms} X R_{SHUNT} X Margin)/Derating Ratio = (5^2 X 0.0248 X 1.2)/0.7 = 1.1W (7)

Therefore, the proper power rating of shunt resistor is over 2.0W.

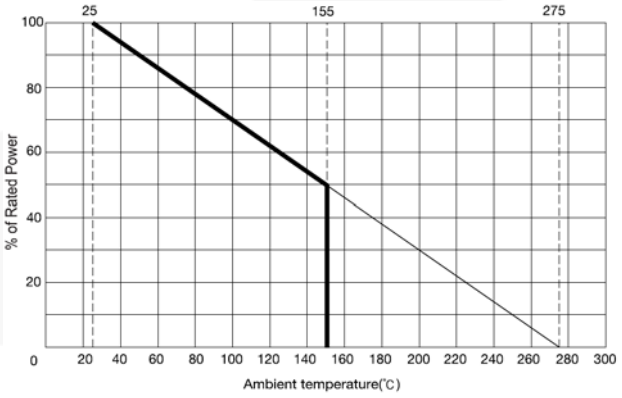


Figure 21. Derating Curve Example of Shunt Resistor (from RARA ELEC.)

Time Constant of Internal Time Delay

An RC filter (reference R_FC_{SC} in Figure 20) is necessary to prevent noise-related SCP (Short-circuit Current Protection) circuit malfunction. The RC time constant is determined by the applied noise time and the SCWT (Short-circuit Current Withstanding Time) of Motion-SPM products.

When the external shunt resistor voltage drop exceeds the SCP level, this is applied to the C_{SC} pin via the RC filter. The RC filter delay time (T1) is the time required for the C_{SC} pin voltage to rises to the referenced SCP level, Table 7 shows the specification of the SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: T2). Therefore, considered this filter time when designing the RC filter of V_{CSC}.

Table 7. Specification for SCP level ($V_{SC(ref)}$)

Conditions	Min.	Typ.	Max.	Unit
Specification at T_J =25°C, V_{CC} =15V	0.45	0.50	0.55	V

V_{IN}: Voltage of Input Signal
V_{CSC}: Voltage of C_{SC} Pin
L_{OUT}: V_{GE} of Low-Side IGBT
I_{SC}: Short-Circuit Current
V_{FO}: Voltage of V_{FO} Pin

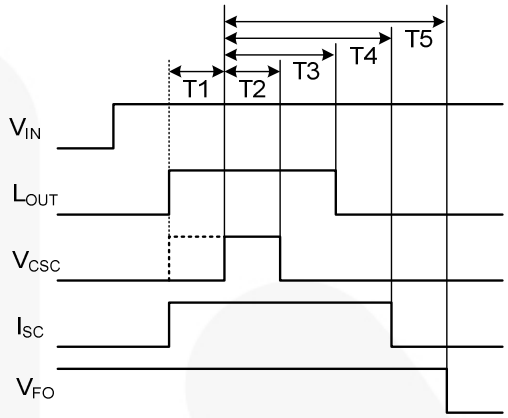


Figure 22. Timing Diagram

Notes:
T1: Filtering time of RC filter of V_{CSC}
T2: Filtering time of C_{SC}. If V_{CSC} width is less than T2, SCP does not operate.
T3: Delay from C_{SC} triggering to gate-voltage down
T4: Delay from C_{SC} triggering to short-circuit current
T5: Delay from C_{SC} triggering to fault-out signal

Table 8. Timetable on Short-Circuit Conditions: V_{CSC} to L_{OUT}, I_{SC}, V_{FO}

DUT	Typ. at T_J=25°C	Typ. at T_J=150°C	Max. at T_J=25°C
FNA40860	T2 = 0.40μs	T2 = 0.30μs	Considering ±20% Dispersion, T4=1.0μs
	T3 = 0.65μs	T3 = 0.60μs	
	T4 = 0.80μs	T4 = 0.75μs	
	T5 = 1.20μs	T5 = 1.75μs	

Notes:
5. To guarantee safe short-circuit protection under all operating conditions, C_{SC} should be triggered within 1.0μs after the short-circuit occurs (SCWT < 2.0μs, Conditions: V_{DC}=400V V_{CC}=16.5V, T_J=150°C, from datasheet of FNA40860).
6. It is recommended that the time delay from short-circuit to C_{SC} triggering should be minimized.

Figure 23 and Figure 24 show operating waveforms of SCP (Short-Circuit Current Protection) function. Normally, T (Tau, time constant of RC filter of C_{SC}) doesn't accurately operate due to fast di/dt of I_{SC} (short-circuit current). Therefore, consider this kind of situation when deciding time constant of RC filter of C_{SC}. Normally, T (time constant of RC filter of C_{SC}) accurately operates in OCP (Over-Current Protection).

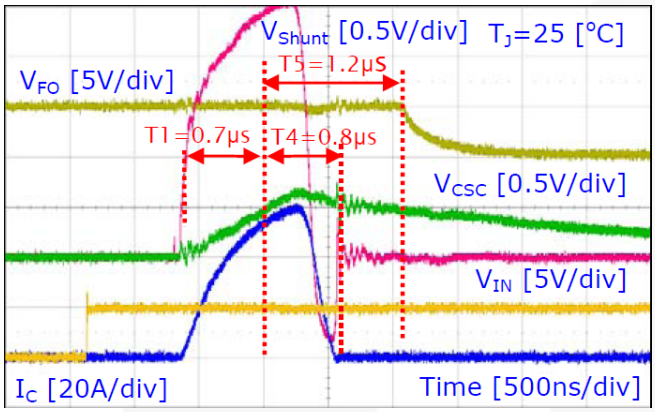


Figure 23. Waveform of SCP (Short-Circuit Current Protection) Function (Time Constant of RC Filter: 2μs (R_{SC}=62[Ω], C_{SC}=33[nF]), R_{SHUNT}=40[mΩ])

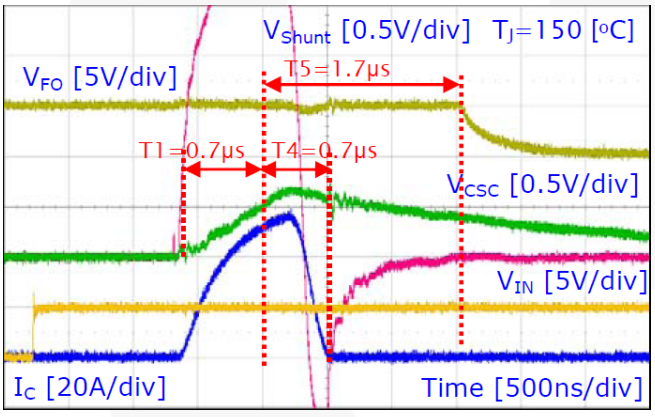


Figure 24. Waveform of SCP (Short-Circuit Current Protection) Function (Time Constant of RC Filter: 2μs (R_{SC}=62[Ω], C_{SC}=33[nF]), R_{SHUNT}=40[mΩ])

Therefore, the T_{TOTAL} (total time) from the detection of the SC trip current to the gate off of the IGBT becomes:

T_{TOTAL}=RC filter delay time (T1) + Delay from C_{SC} trigger to I_{SC} (T4) (8)

Therefore, total delay time (T_{TOTAL}) should be less than SCWT of SCSOA curve:

SCWT > T_{TOTAL} (T1 + T4) (9)

where SCWT = Short Circuit Withstanding Time.

It is recommended that the time constant of RC filter should be set in the range of 1.0 ~ 2.0μs to protect from destruction under most operating conditions.

Soft Turn-Off

The LVIC has a soft turn-off function to protect low-side IGBTs from over voltage of V_{PN} (supply voltage) by short-circuit hard off. "Short-circuit hard off" means IGBTs are turned off by short input signal before operation of SCP (Short-circuit Current Protection) function under short-circuit condition. In this case, V_{PN} (supply voltage) rapidly raises di/dt of I_{SC} (short-circuit current). This kind of rapid rise of V_{PN} causes destruction of IGBT by over voltage. The soft-off function prevents IGBT rapid turning off by slow discharging of V_{GE} (gate to emitter voltage of IGBT).

Block diagrams of LVIC and the operation sequence of the soft turn-off function are shown in Figure 25 and Figure 26. There are two internal protection functions, UVLO and SCP. When IGBT is turned off in normal conditions, LVIC turns off the IGBT immediately by a turn-off gate signal (V_{IN_L}) via gate driver block (pre-driver turn-on output buffer of gate driver block, path ① in Figure 26). However, when IGBT is turned off by a protection function, the gate driver is disabled by the protection function signal via the output of the protection circuit (disable output buffer, high-Z). Output of the protection circuit turns on the switch of soft-off function. Therefore, V_{GE} is discharged slowly via circuit of soft-off. (path ② in Figure 26).

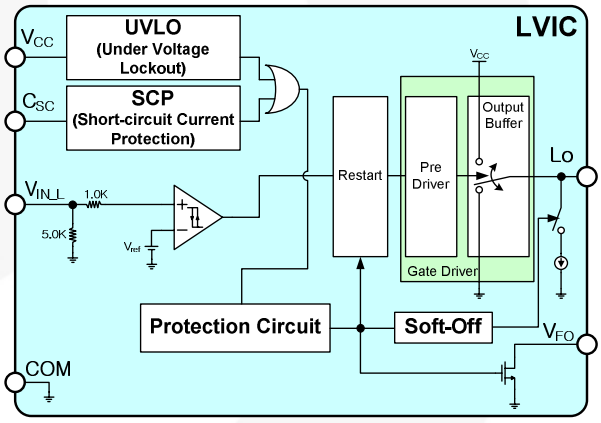


Figure 25. Internal Block Diagram

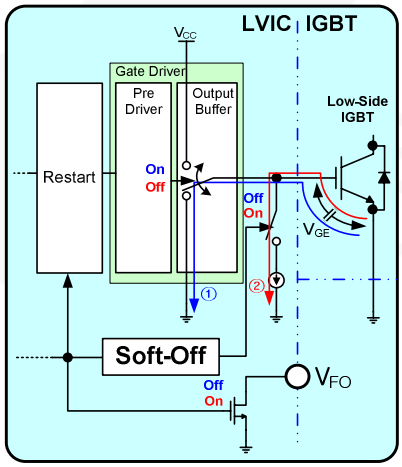


Figure 26. Operation Sequence of Soft Turn-Off

Figure 27 shows that the normal turn-off switching operations can be performed satisfactorily at a V_{PN}=450V, T_J=25, 150°C, with the surge voltage between P and N pins ($V_{PN(Surge)}$) limited to under 500V.

The difference between the hard and soft turn-off switching operation is shown in Figure 28. The hard turn-off of the IGBT makes a large overshoot (up to 100V). Hence, the DC-link capacitor supply voltage should be limited to 400V to protect the Motion-SPM product. A hard turn-off, with a duration of less than approximately 2μs, may occur in the case of a short-circuit fault. For a normal short-circuit fault, the protection circuit becomes active and the IGBT is turned off softly to prevent excessive overshoot voltage. An overshoot voltage of 40~70V occurs for this conditions.

Figure 277and Figure 28 are the experimental results of the safe operating area test. However, it is strongly recommended that the Motion-SPM product should not be operated under these conditions.

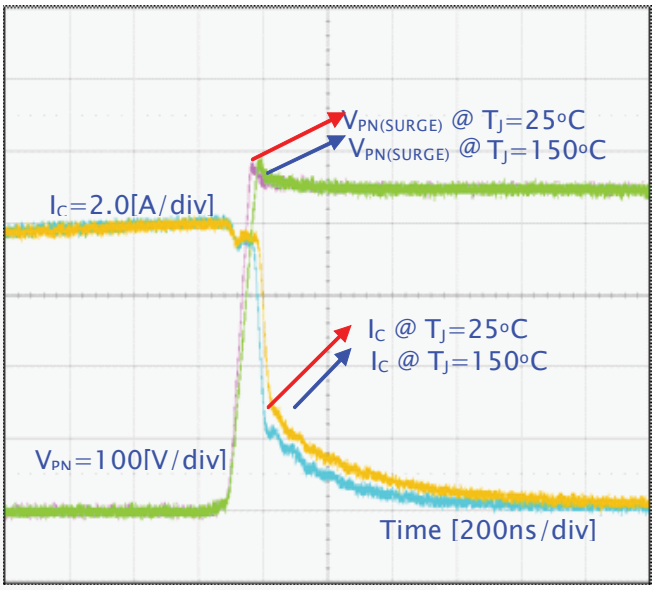


Figure 27. Normal Current Turn-Off Waveform of FNA40860 at V_{PN}=450V, T_J=25, 150°C

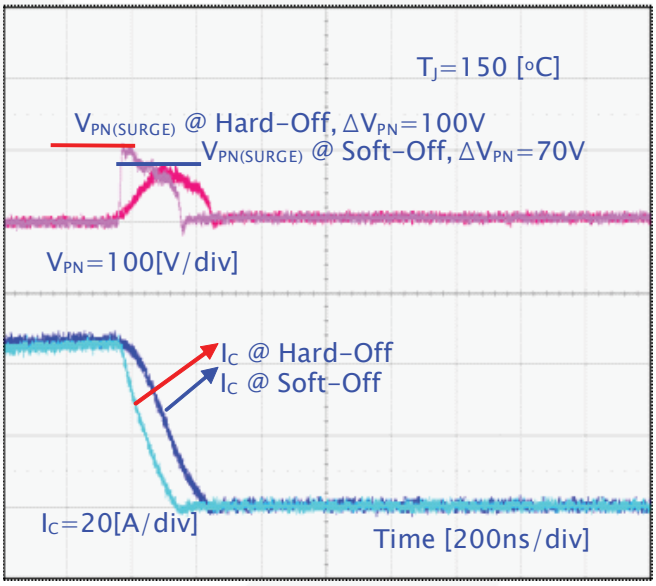


Figure 28. Short-Circuit Current Turn-Off Waveform of FNA40860 at V_{PN}=400V, T_J=150°C

Table 9. Detailed Description of Absolute Maximum Ratings *(FNA40860 Case, see Datasheet)*

Item	Symbol	Rating	Description
Supply Voltage	V_{PN}	450V	The maximum steady-state (non-switching mode) voltage between P-N. A brake circuit is necessary if P-N voltage exceeds this value.
Supply Voltage (Surge)	$V_{PN(surge)}$	500V	The maximum surge voltage (non-switching mode) between P-N. A snubber circuit is necessary if P-N surge voltage exceeds this value.
Collector-Emitter Voltage	V_{CES}	600V	The sustained collector-emitter voltage of built-in IGBT
Each IGBT Collector Current	$\pm I_C$	8A	The maximum allowable DC continuous IGBT collector current at T_C=25°C
Junction Temperature	T_J	-40~150°C	The maximum junction temperature rating of the power chips integrated within the Motion-SPM is 150°C. However, to ensure safe operation of the Motion-SPM, average junction temperature should be limited to 125°C. Although IGBT and FRD chip are not damaged immediately at T_J=150°C, its power cycles come to be decreased.
Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	$V_{PN(PROT)}$	400V	Under the conditions where V_{CC}=13.5 ~ 16.5V, non-repetitive, less than 2μs. The maximum supply voltage for safe IGBT turn-off under SC (Short-Circuit Current) or OC (Over Current) condition. The power chip may be damaged if supply voltage exceeds this specification.

Fault Output Circuit

Table 10. Fault-Output Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO}-COM	-0.3~V_{CC}+0.3	V
Fault Output Current	I_{FO}	Sink Current at V_{FO} Pin	1.0	mA

Table 11. Electric Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Fault Output Supply Voltage	V_{FOH}	V_{SC}=0V, V_{FO} Circuit: 4.7kΩ to 5V Pull-Up	4.5			V
	V_{FOL}	V_{SC}=1V, V_{FO} Circuit: 4.7kΩ to 5V Pull-Up			0.5	V

Because the F_O terminal is an open-drain type, it should be pulled up to 5V or 15V via a pull-up resistor. The resistor has to satisfy the above specifications.

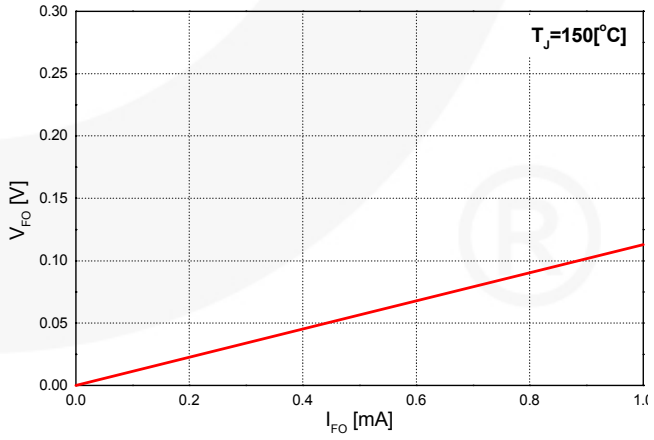


Figure 29.Voltage-Current Characteristics of V_{FO} Terminal

Under-Voltage Lockout Protection (UVLO)

The LVIC has an under-voltage lockout protection function to protect low-side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 30.

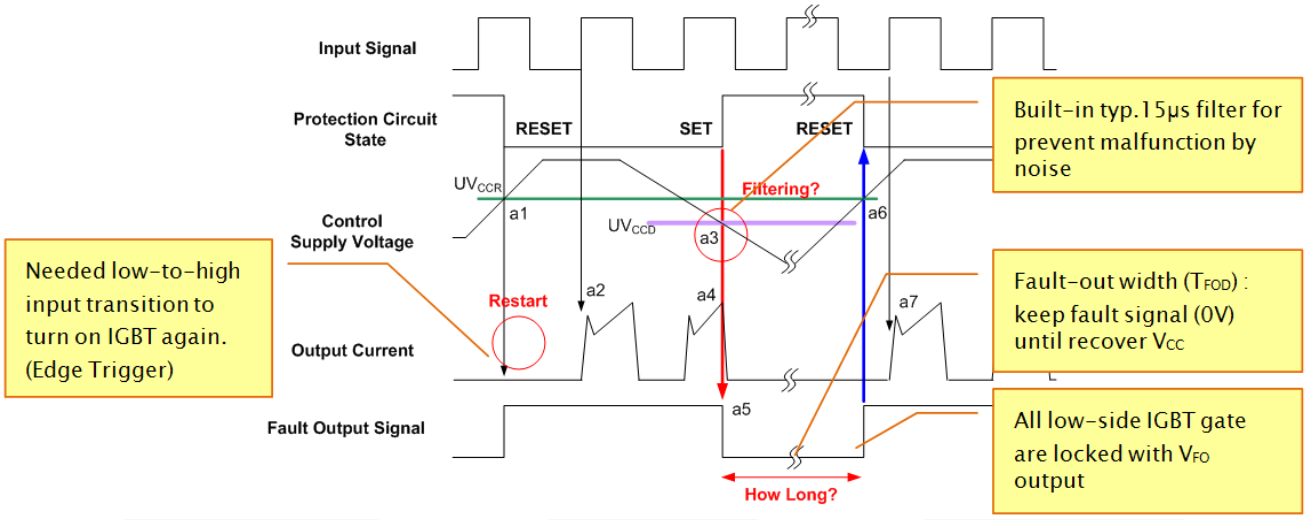


Figure 30. Timing Chart of Low-Side Under-Voltage Protection Function

Notes:

a1. Control supply voltage rise: After the voltage rises UV_{CCR}, the circuits start to operate when next input is applied.
a2. Normal operation: IGBT ON and carrying current
a3. Under-voltage detection (UV_{CCD})
a4. IGBT OFF in spite of control input condition
a5. Fault output operation starts
a6. Under-voltage reset (UV_{CCR})
a7. Normal operation: IGBT ON and carrying current

The HVIC has an under-voltage lockout function to protect the high-side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 31. A F_O alarm is not given for low HVIC bias conditions.

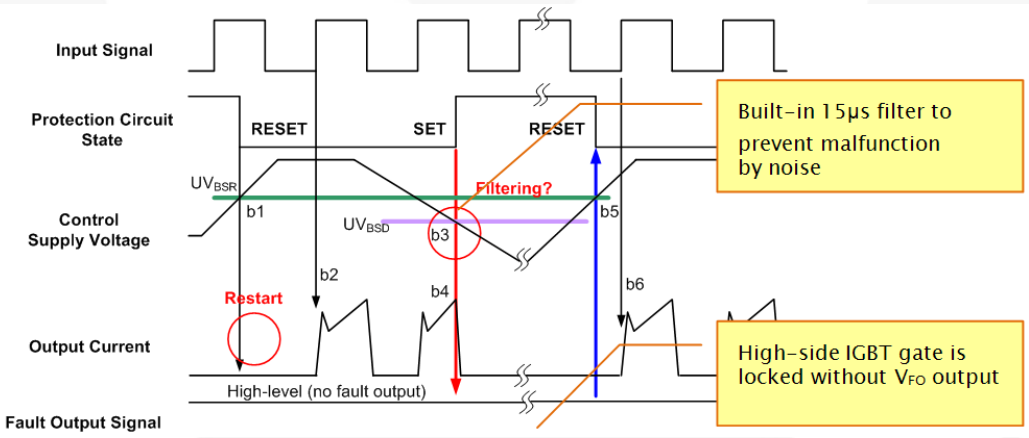


Figure 31. Timing Chart of High-Side Under-Voltage Protection Function

Notes:

b1. Control supply voltage rises: After the voltage reaches UV_{BSR}, the circuits start to operate when next input is applied.
b2. Normal operation: IGBT ON and carrying current
b3. Under-voltage detection (UV_{BSD})
b4. IGBT OFF in spite of control input condition, but there is no fault output signal.
b5. Fault output operation starts
b6. Under-voltage reset (UV_{BSR})
b7. Normal operation: IGBT ON and carrying current

Table 12. Specification for UVLO (Under-Voltage Lockout) Function

Item	Parameter	Conditions	Min.	Max.	Unit
UV_{CCD}	Supply Circuit Under-Voltage Protection	Detection Level	10.5	13.0	V
UV_{CCR}		Reset Level	11.0	13.5	V
UV_{BSD}		Detection Level	10.0	12.5	V
UV_{BSR}		Reset Level	10.5	13.0	V

Circuit of Input Signal ($V_{IN(H)}$, $V_{IN(L)}$)

Figure 32 shows the I/O interface circuit between the MCU and Motion-SPM products. Because the Motion-SPM input logic is active HIGH and there are built-in pull-down resistors, external pull-down resistors are not needed.

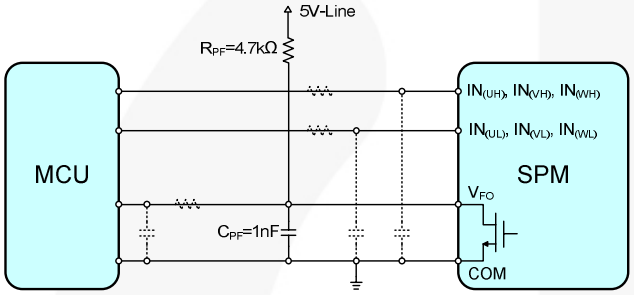


Figure 32.Recommended CPU I/O Interface Circuit

Table 13. Maximum Ratings of Input and F_O Pins

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	V_{CC}	Applied between $V_{CC(H)}$-COM, $V_{CC(L)}$-COM	20	V
Input Signal Voltage	V_{IN}	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$-COM $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$-COM	-0.3 ~ V_{CC} +0.3	V
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO}-COM	-0.3 ~ V_{CC} +0.3	V

The input and fault output maximum rating voltages are shown in Table 13. Since the fault output is open-drain configured, its rating is V_{CC}+0.3V, 15V supply interface is possible. However, it is recommended that the fault output be configured with the 5V logic supply, which is the same as the input signals. It is also recommended that the de-coupling capacitors be placed at both the MCU and Motion-SPM ends of the V_{FO} and the signal line as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 32 might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.

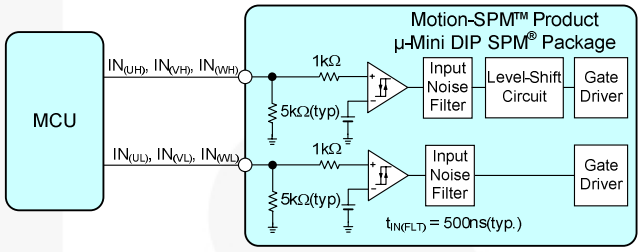


Figure 33.Internal Structure of Signal Input Terminal

The μMini DIP family of Motion-SPM products employs active-HIGH input logic. This removes the sequence restriction between the control supply and the input signal during startup or shutdown operation. Therefore, it makes the system fail-safe. In addition, pull-down resistors are built-in to each input circuit. External pull-down resistors are not needed, reducing external components. The input noise filter inside the Motion-SPM product suppresses short pulse noise and prevents the IGBT from malfunction and excessive switching loss. Furthermore, by lowering the turn-on and turn-off threshold voltages of the input signal, as shown in Table 14, a direct connection to 3.3V-class MCU or DSP is possible.

Table 14. Input Threshold Voltage Ratings (at V_{CC}=15V, T_J=25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Turn-On Threshold Voltage	$V_{IN(ON)}$	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$-COM		2.6	V
Turn-Off Threshold Voltage	$V_{IN(OFF)}$	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$-COM	0.8		V

As shown in Figure 33, the input signal section of μMini DIP package family in Motion-SPM products integrates a 5kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion-SPM input, attention should be given to the signal voltage drop at the Motion-SPM input terminals to satisfy the turn-on threshold voltage requirement. For instance, R=100Ω and C=1nF for the parts shown dotted in Figure 32.

Bootstrap Circuit Design

Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between $V_{B(U,V,W)}$ and $V_{S(U,V,W)}$, provides the supply to the HVIC within the µMini-DIP SPM package family in Motion-SPM products. This supply must be in the range of 13.0V~18.5V to ensure that the HVIC can fully drive the high-side IGBT. The µMini-DIP SPM package includes an under-voltage lockout protection for the V_{BS} to ensure that the HVIC does not drive the high-side IGBT, if the V_{BS} voltage drops below a specific voltage (*refer to the datasheet)*. This function prevents the IGBT from operating in a high-dissipation mode.

The V_{BS} floating supply can be generated a number of ways, including the bootstrap method described here *(refer to Figure 34)*. This method has the advantage of being simple and inexpensive; however, the duty cycle and on-time are limited by the need to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of and bootstrap diode, resistor, and capacitor as shown in Figure 35and Figure 36. The current flow path of the bootstrap circuit is show in Figure 35. When V_S is pulled down to ground (either through the low-side or the load), the bootstrap capacitor C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{CC} supply.

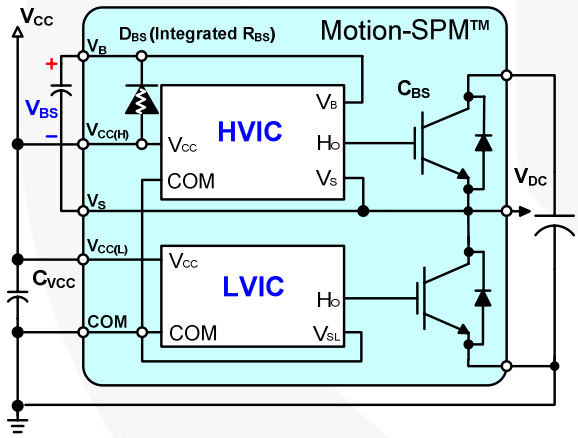


Figure 34. Bootstrap Circuit for the Supply Voltage (V_{BS}) of a HVIC

Initial Charging of Bootstrap Capacitor

Adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln \frac{V_{CC}}{V_{CC} - V_{BS(min)} - V_F - V_{LS}} \quad (10)$$

where:
V_F = forward voltage drop across the bootstrap diode;
$V_{BS(min)}$ = minimum value of the bootstrap capacitor;
V_{LS} = voltage drop across the low-side IGBT or load; and
δ = duty ratio PWM.

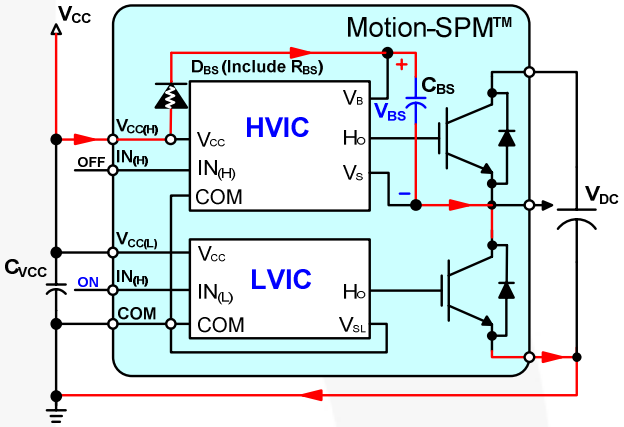


Figure 35.Bootstrap Circuit

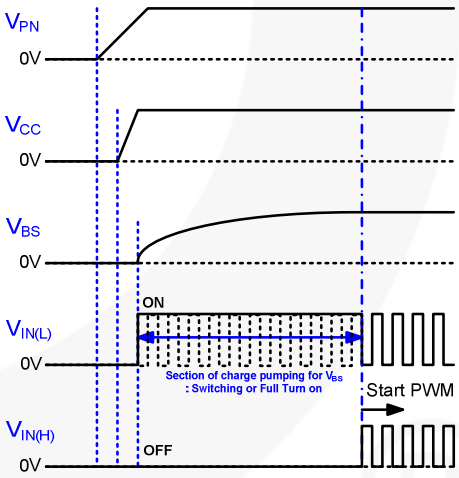


Figure 36.Timing Chart of Initial Bootstrap Charging

Figure 37 and Figure 38 show real waveforms of the initial bootstrap capacitor charging.

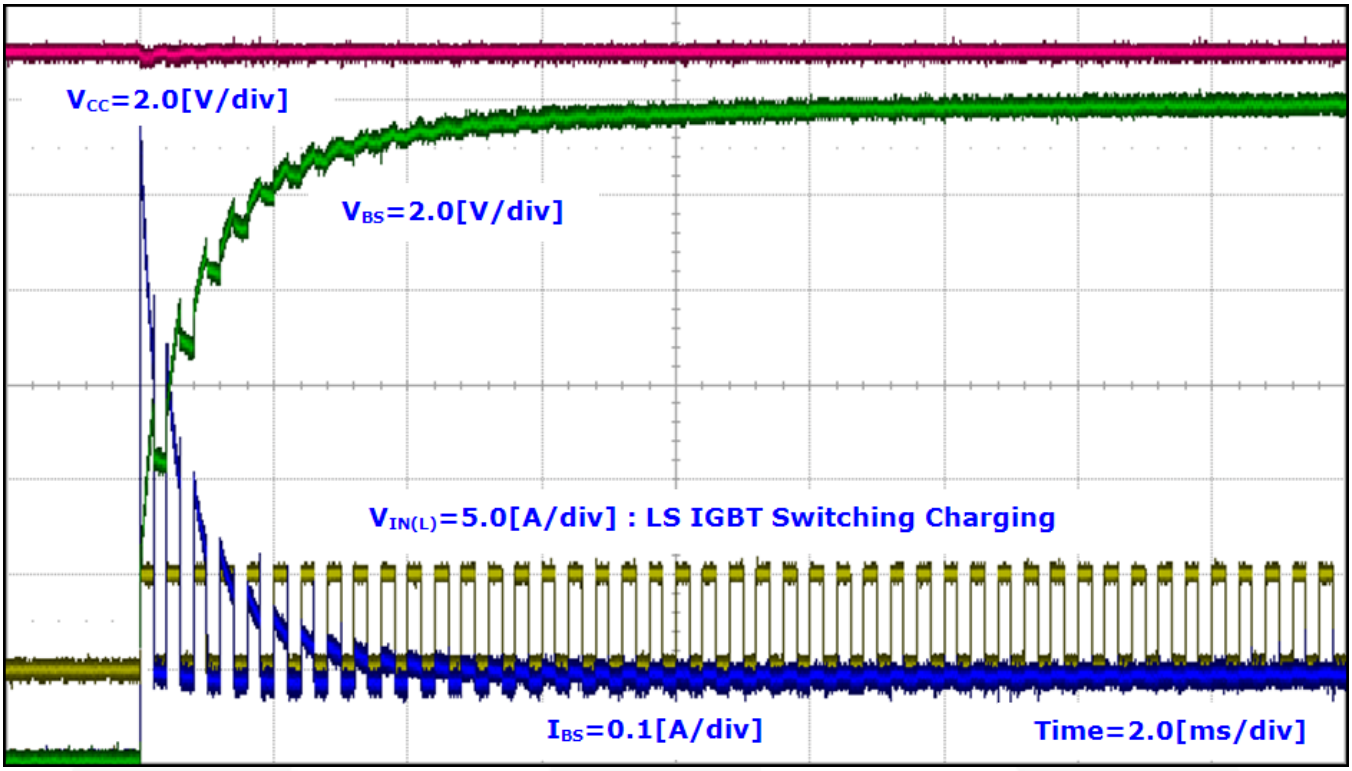


Figure 37.Each Part Initial Operating Waveform of Bootstrap Circuit
(Conditions: V_{DC}=300V, V_{CC}=15V, C_{BS}=22μF, LS IGBT Turn-on Duty=200μs)

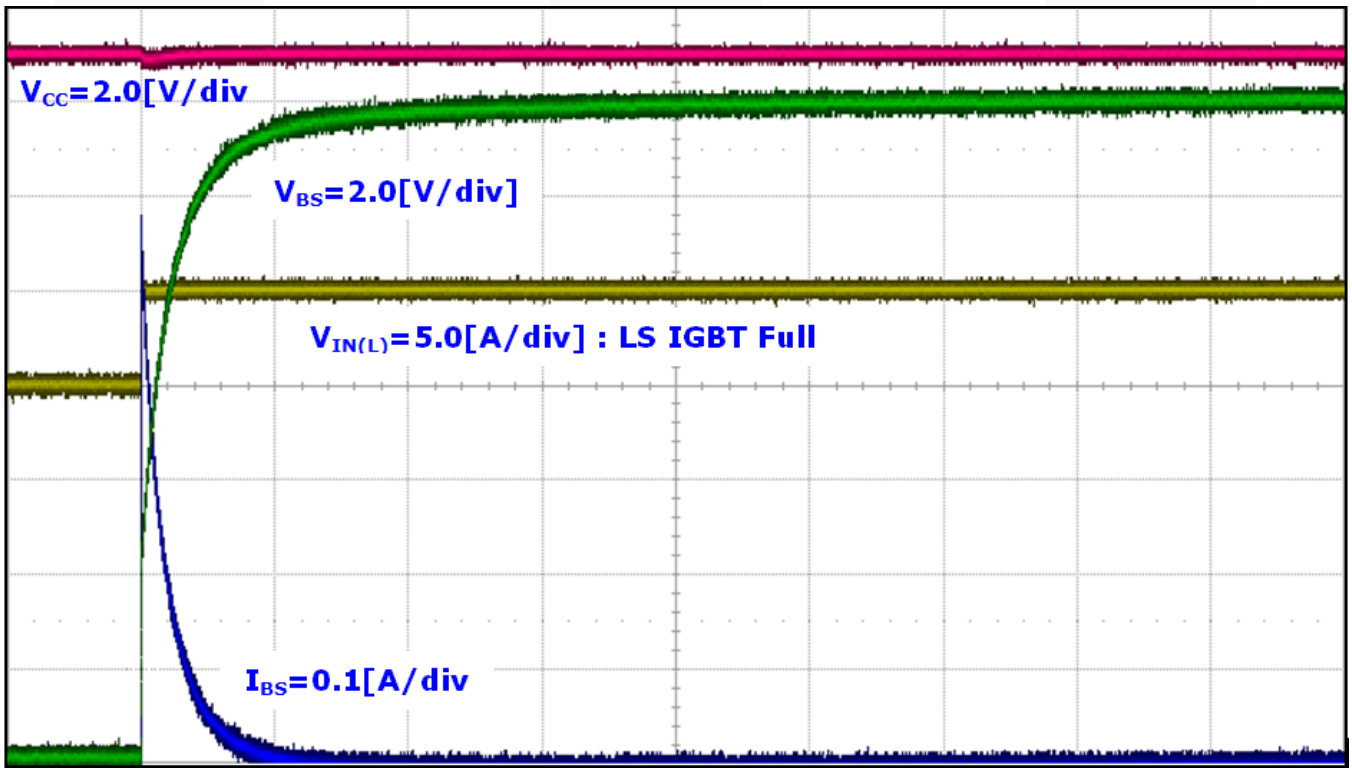


Figure 38.Each Part Operating Waveform of Bootstrap Circuit
(Conditions: V_{DC}=300V, V_{CC}=15V, C_{BS}=22μF, LS IGBT Full Turn-on)

Selection of Bootstrap Capacitor

The bootstrap capacitance can be calculated by:

$$C_{BS} = R\frac{I_{Leak} \times \Delta t}{\Delta V_{BS}} \quad (11)$$

where:
Δt = maximum on pulse width of high-side IGBT;
ΔV_{BS} = the allowable discharge voltage of the C_{BS} (voltage ripple); and
I_{Leak} = maximum discharge current of the C_{BS}.

Mainly via the following mechanisms:

- Gate charge for turning the high-side IGBT on…
- Quiescent current to the high-side circuit in the HVIC
- Level-shift charge required by level-shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
- Bootstrap diode reverse recovery charge.

Practically, 2mA of I_{Leak} is recommended for µMini-DIP SPM family in Motion-SPM products. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the V_S voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, there is an inherent minimum on-time for the low-side IGBT (or off-time of the high-side IGBT).

Calculation Examples of Bootstrap Capacitance

I_{Leak} = circuit current = 2.0mA (recommendation value)

ΔV_{BS} = discharged voltage = 0.1V (recommendation value)

Δt = Maximum on pulse width of high-side IGBT = 0.2ms. (depends on user system)

$$C_{BS\_min} = \frac{I_{Leak} \times \Delta t}{\Delta V_{BS}} = \frac{2mA \times 0.2ms}{0.1V} = 4.0 \times 10^{-6} \quad (12)$$

→ More than 2~3 times → 8µF.

Note:

7. This capacitance value can be changed according to the switching frequency, capacitor used, and recommended V_{BS} voltage of 13.0~18.5V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of component.

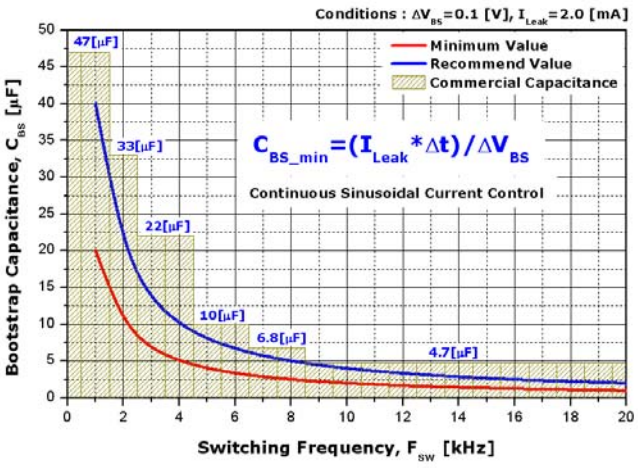


Figure 39. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Built-in Bootstrap Diode

When the high-side IGBT or FRD conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. Hence, a withstand voltage of more than 600V is recommended. It is important that this diode be fast recovery (recovery time < 100ns) to minimize the amount of charge fed back from the bootstrap capacitor into the V_{CC} supply. One role of the bootstrap resistor (R_{BS}) is to slow down the dV_{BS}/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.

Normally, bootstrap circuits consists of bootstrap diode (D_{BS}), bootstrap resistor (R_{BS}), and bootstrap capacitor (C_{BS}). The built-in bootstrap diode of µMini-DIP SPM package has bootstrap resistor characteristic by special V_F characteristics *(refer to Figure 40)*. Therefore, circuit engineers only need external bootstrap capacitor for bootstrap circuit.

The characteristics of the built-in bootstrap diode in the µMini-DIP SPM family are:

- Fast recovery diode: 600V/0.5A
- t_{rr}: 80ns (typical)
- Have a equivalent resistor characteristic (approximately 15Ω)

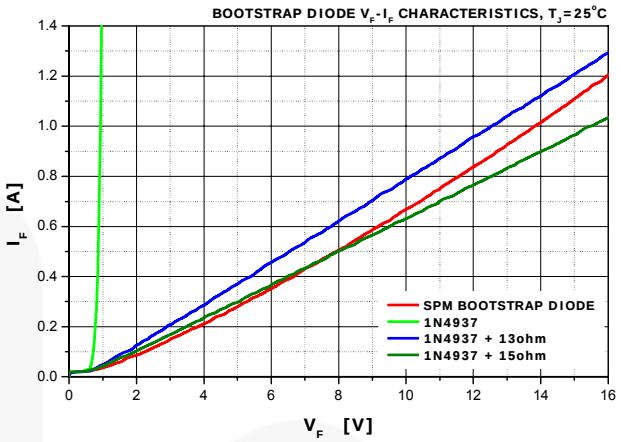


Figure 40. V-I Characteristics of Bootstrap Diode in µMini-DIP SPM Package

Table 15. Specification for Bootstrap Diode

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_F	Forward Drop Voltage	I_F=0.1A, T_C=25°C	~	2.5	~	V
t_{rr}	Reverse Recovery Time	I_F=0.1A, T_C=25°C	~	80	~	ns

Circuit of NTC Thermistor (Monitoring of T_C)

The µMini-DIP SPM package in the Motion-SPM family include a NTC (Negative Temperature Coefficient) thermistor for module case temperature (T_C) sensing. This thermistor is located in ceramic substrate with the power chip (IGBT/FRD). Therefore, the thermistor can accurately reflect the temperature of the power chip *(see Figure 41)*.

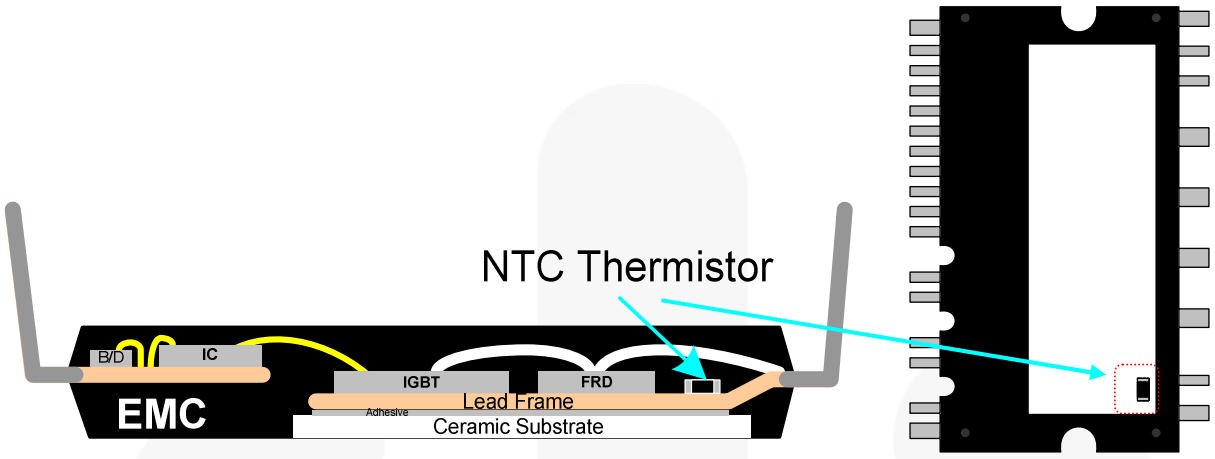


Figure 41.Location of NTC Thermistor in µMini-DIP SPM Package

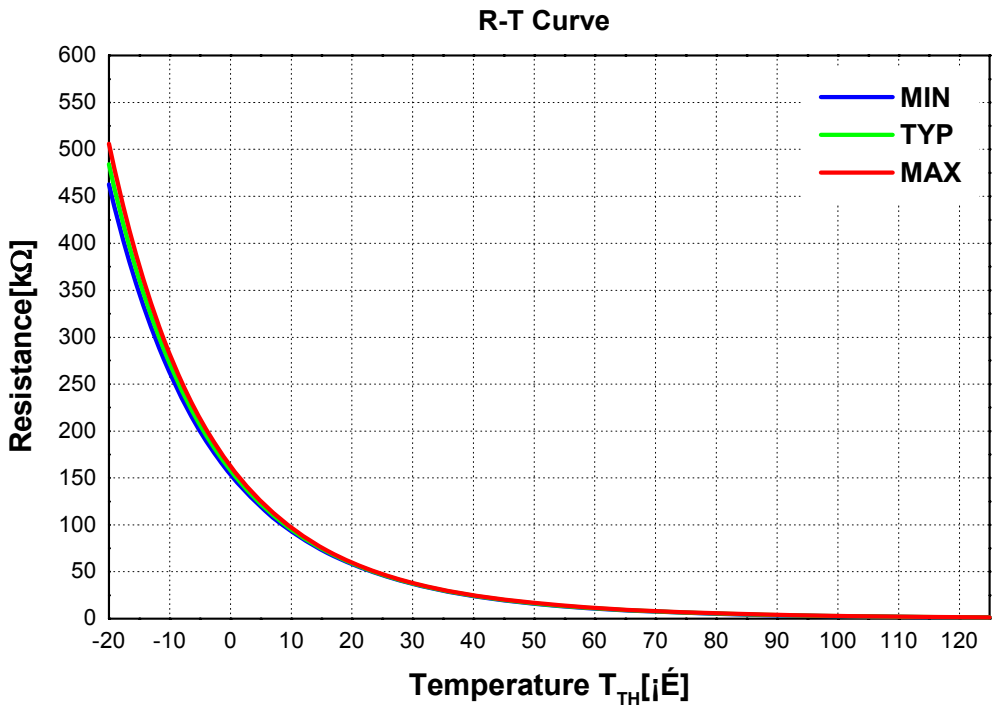


Figure 42.R-T Curve of NTC Thermistor in µMini-DIP SPM Package

Normally, circuit designers use two kinds of circuit for temperature protection (monitoring) by NTC thermistor. One is circuit by ADC (Analog-Digital Converter). The other is circuit by comparator. Figure 43 and Figure 44 show examples of application circuits with an NTC thermistor.

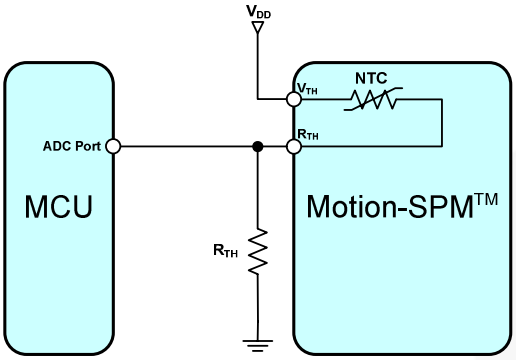


Figure 43.Over-Temperature Protection Circuit by MCU with NTC Thermistor

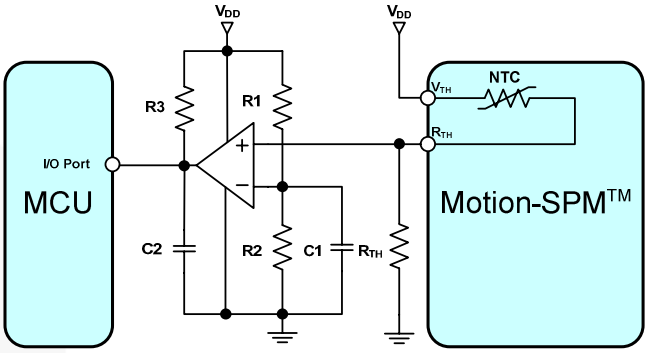


Figure 44.Over-Temperature Protection Circuit by Comparator with NTC Thermistor

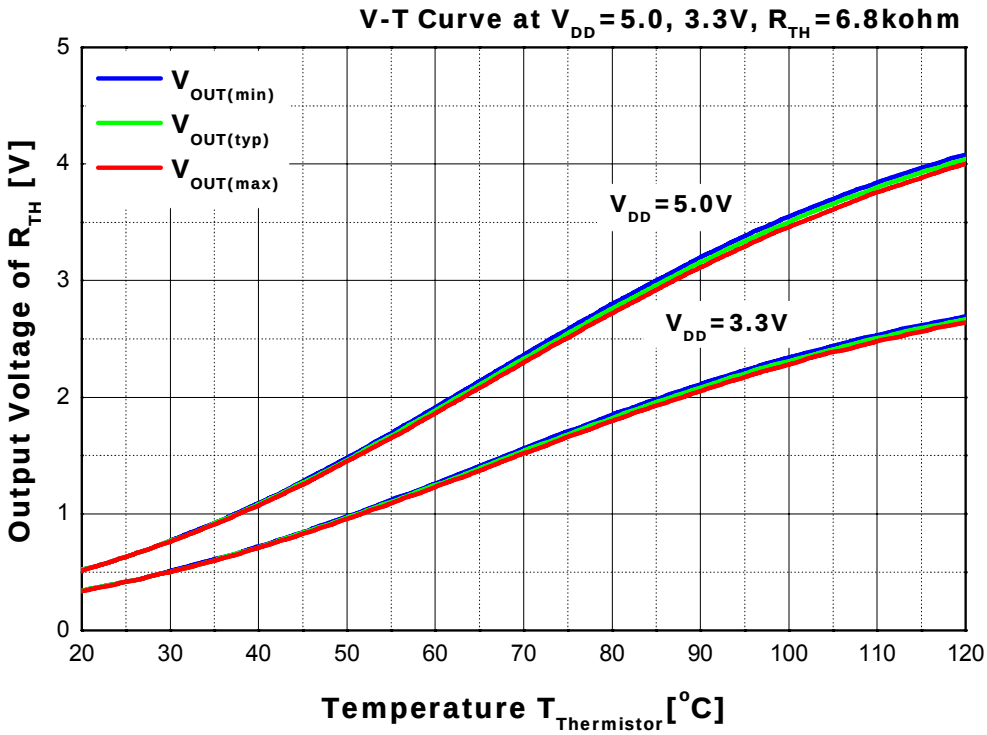


Figure 45.V-T Curve of Figure 43

Table 16. R-T Table of NTC Thermistor (1-1)]

T_{NTC}(℃)	R_{min}(kΩ)	R_{cent}(kΩ)	R_{max}(kΩ)	T(℃)	R_{min}(kΩ)	R_{cent}(kΩ)	R_{max}(kΩ)
0	153.8063	158.2144	162.7327	30	37.1428	37.6431	38.1463
1	146.0956	150.1651	154.3326	31	35.5329	36.0351	36.5408
2	138.8168	142.5725	146.4152	32	34.0011	34.5041	35.0111
3	131.9431	135.4081	138.9502	33	32.5433	33.0462	33.5534
4	125.4497	128.6453	131.9091	34	31.1555	31.6573	32.164
5	119.3135	122.2594	125.2655	35	29.834	30.3339	30.8392
6	113.5129	116.2273	118.9947	36	28.576	29.0734	29.5764
7	108.0276	110.5275	113.0739	37	27.3776	27.8717	28.372
8	102.8388	105.1398	107.4814	38	26.2356	26.726	27.2228
9	97.9288	100.0454	102.1974	39	25.1472	25.6332	26.1261
10	93.2812	95.2267	97.2031	40	24.1094	24.5907	25.0792
11	88.8803	90.6673	92.481	41	23.1198	23.596	24.0796
12	84.7119	86.3519	88.0148	42	22.1759	22.6466	23.1249
13	80.7624	82.2661	83.7894	43	21.2753	21.7401	22.2129
14	77.019	78.3963	79.7903	44	20.4158	20.8746	21.3416
15	73.47	74.7302	76.0043	45	19.5953	20.0478	20.5088
16	70.1042	71.2558	72.4189	46	18.812	19.258	19.7126
17	66.9112	67.962	69.0224	47	18.0638	18.5032	18.9514
18	63.8812	64.8386	65.8039	48	17.3492	17.7818	18.2234
19	61.005	61.8759	62.753	49	16.6663	17.0921	17.5269
20	58.2739	59.0647	59.8601	50	16.0137	16.4325	16.8605
21	55.6798	56.3961	57.116	51	15.3899	15.8016	16.2227
22	53.2152	53.8628	54.5127	52	14.7934	15.1981	15.6122
23	50.8732	51.4569	52.0422	53	14.223	14.6205	15.0277
24	48.6469	49.1715	49.6969	54	13.6773	14.0677	14.4678
25	46.53	47	47.47	55	13.1552	13.5385	13.9316
26	44.4567	44.936	45.4159	56	12.6556	13.0318	13.4178
27	42.4868	42.9737	43.4618	57	12.1774	12.5465	12.9255
28	40.6147	41.1075	41.6021	58	11.7195	12.0815	12.4536
29	38.8351	39.3323	39.8319	59	11.281	11.6361	12.0011
30	37.1428	37.6431	38.1463	60	10.861	11.2091	11.5673

Table 17. R-T Table of NTC Thermistor (1-2)

T_{NTC}(℃)	R_{min}(kΩ)	R_{cent}(kΩ)	R_{max}(kΩ)	T(℃)	R_{min}(kΩ)	R_{cent}(kΩ)	R_{max}(kΩ)
61	10.4594	10.8007	11.152	91	3.6675	3.8463	4.0334
62	10.0746	10.4091	10.7536	92	3.5505	3.7253	3.9084
63	9.7058	10.0336	10.3714	93	3.4377	3.6087	3.7879
64	9.3522	9.6734	10.0046	94	3.329	3.4963	3.6716
65	9.0133	9.3279	9.6525	95	3.2242	3.3878	3.5593
66	8.6882	8.9963	9.3145	96	3.1235	3.2836	3.4515
67	8.3764	8.6782	8.9899	97	3.0264	3.183	3.3473
68	8.0773	8.3727	8.6782	98	2.9328	3.086	3.2468
69	7.7902	8.0795	8.3787	99	2.8425	2.9923	3.1497
70	7.5147	7.7979	8.091	100	2.7553	2.9019	3.0559
71	7.2496	7.5268	7.8138	101	2.6712	2.8146	2.9654
72	6.995	7.2663	7.5474	102	2.5901	2.7303	2.8779
73	6.7505	7.016	7.2913	103	2.5117	2.6489	2.7933
74	6.5157	6.7755	7.045	104	2.436	2.5703	2.7117
75	6.2901	6.5443	6.8082	105	2.363	2.4943	2.6327
76	6.0739	6.3227	6.581	106	2.2921	2.4206	2.556
77	5.8662	6.1096	6.3624	107	2.2236	2.3493	2.4819
78	5.6665	5.9046	6.1521	108	2.1575	2.2805	2.4102
79	5.4745	5.7075	5.9498	109	2.0936	2.2139	2.3409
80	5.2899	5.5178	5.7549	110	2.0319	2.1496	2.2739
81	5.1129	5.3358	5.568	111	1.9725	2.0877	2.2094
82	4.9426	5.1607	5.3879	112	1.9151	2.0278	2.147
83	4.7788	4.9921	5.2145	113	1.8596	1.9699	2.0866
84	4.6211	4.8299	5.0475	114	1.806	1.9139	2.0282
85	4.4694	4.6736	4.8866	115	1.7541	1.8598	1.9716
86	4.3228	4.5226	4.731	116	1.7042	1.8076	1.9171
87	4.1817	4.3771	4.5811	117	1.6559	1.7572	1.8644
88	4.0459	4.2369	4.4366	118	1.6092	1.7083	1.8134
89	3.915	4.1019	4.2973	119	1.564	1.6611	1.7639
90	3.789	3.9717	4.1629	120	1.5203	1.6153	1.7161

General Application Circuit Example

Figure 46 shows a general application circuitry of interface schematic with control signals connected directly to an MCU.

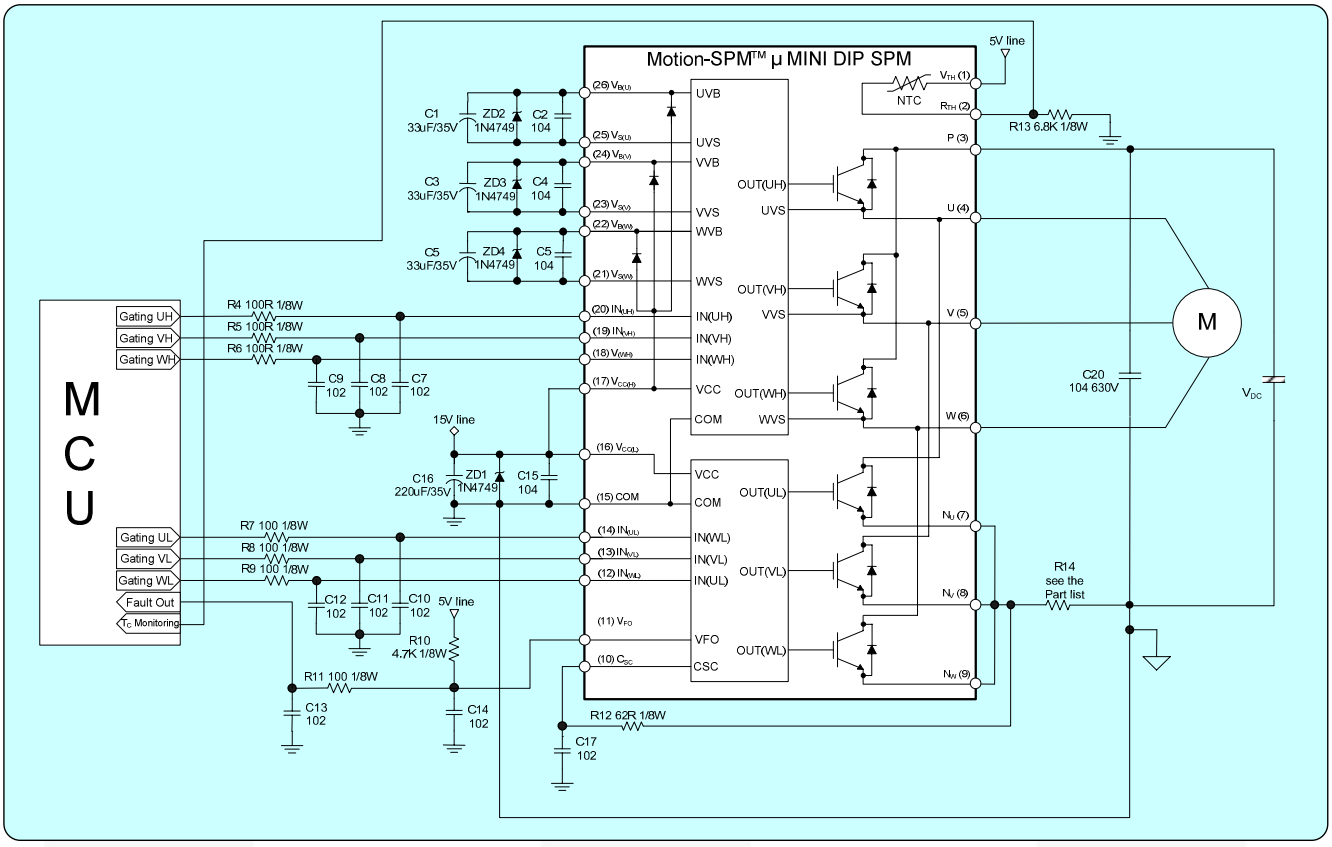


Figure 46. General Application Circuitry for µMini-DIP SPM Package (One-SHUNT Solution)

Print Circuit Board (PCB) Layout Guidance

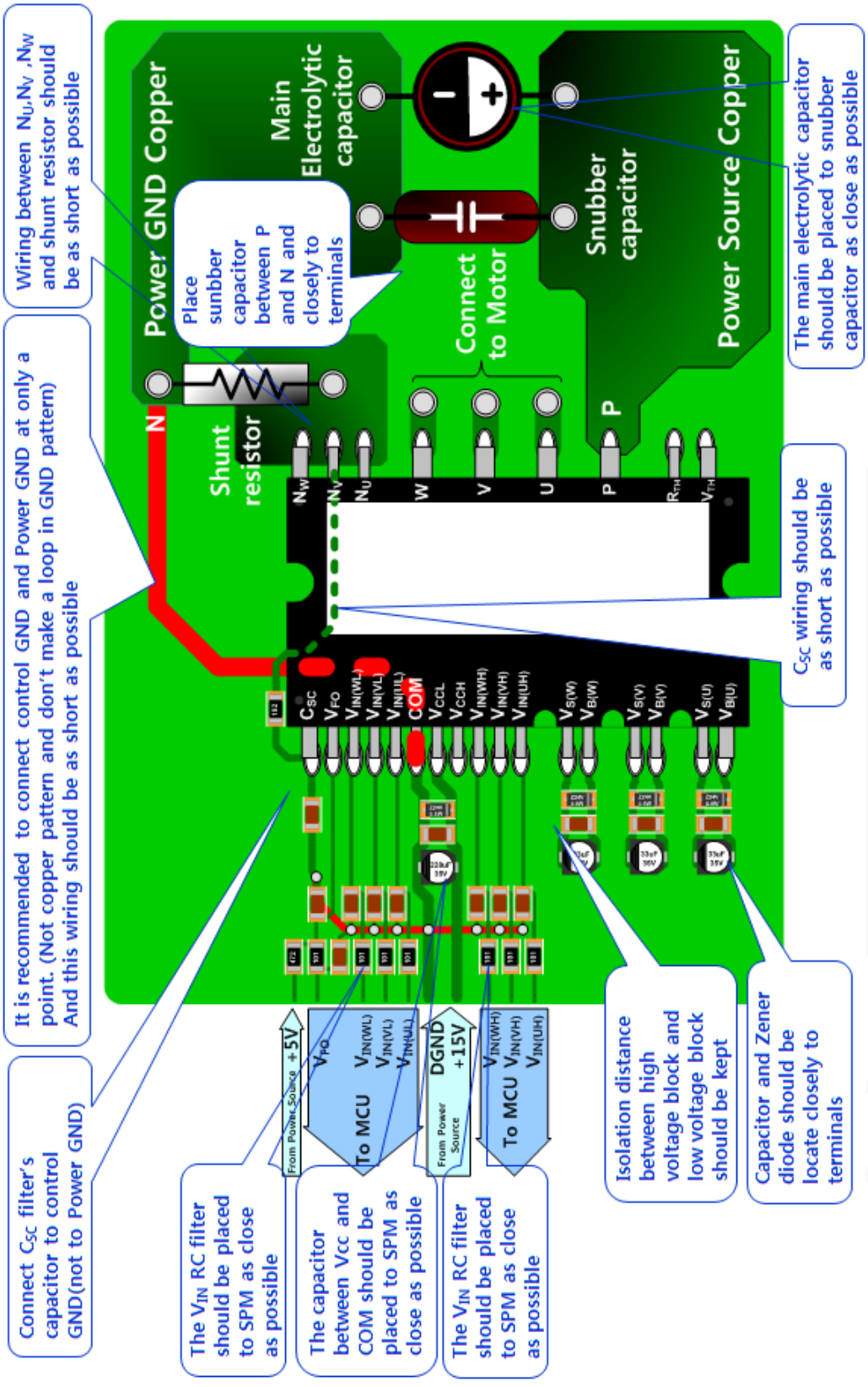


Figure 47.PCB Layout Guidance

Packaging Specification

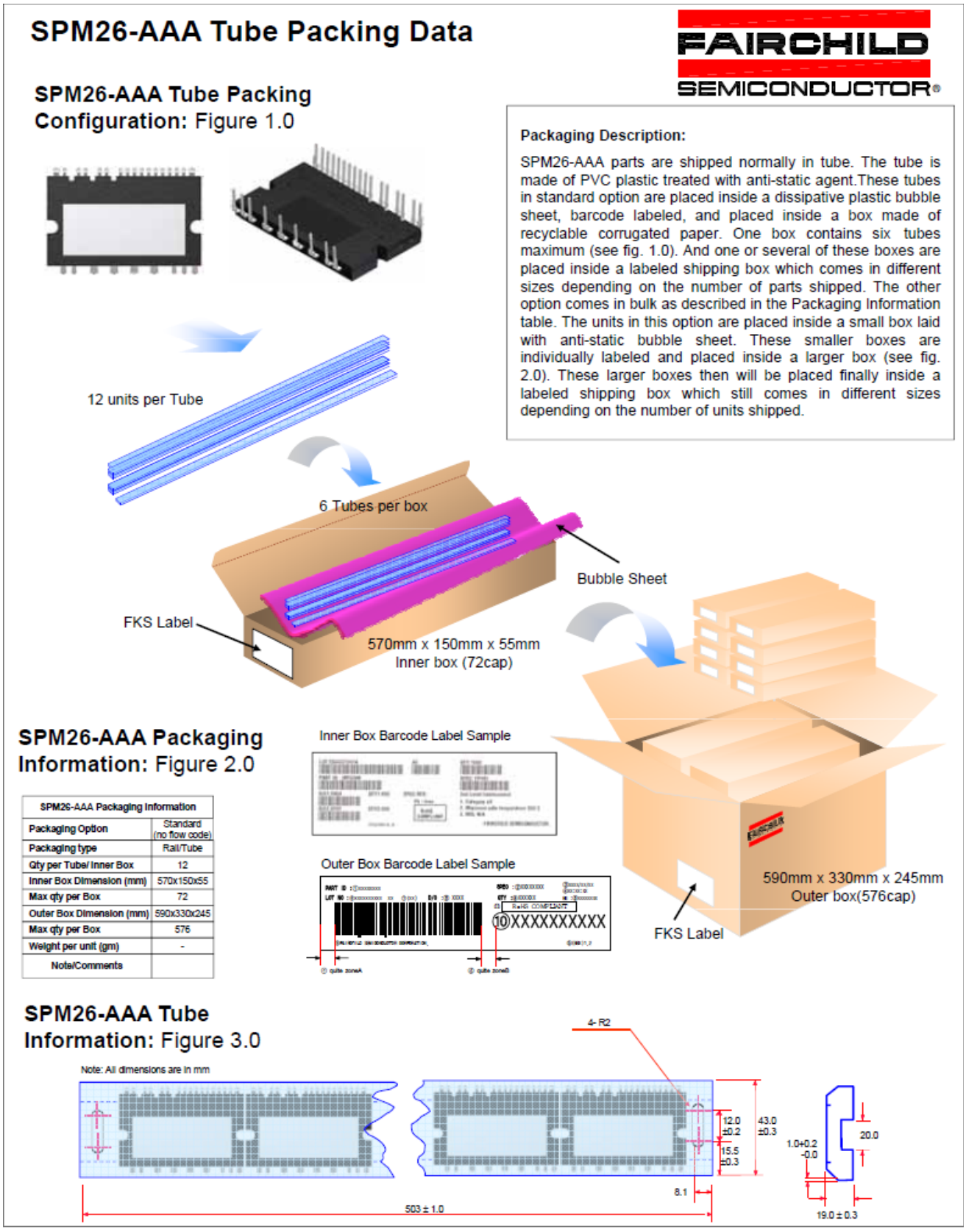
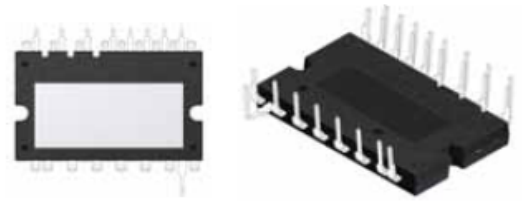


Figure 48.SPM26-AAA Packaging Specification

SPM26-AAB Tube Packing Data

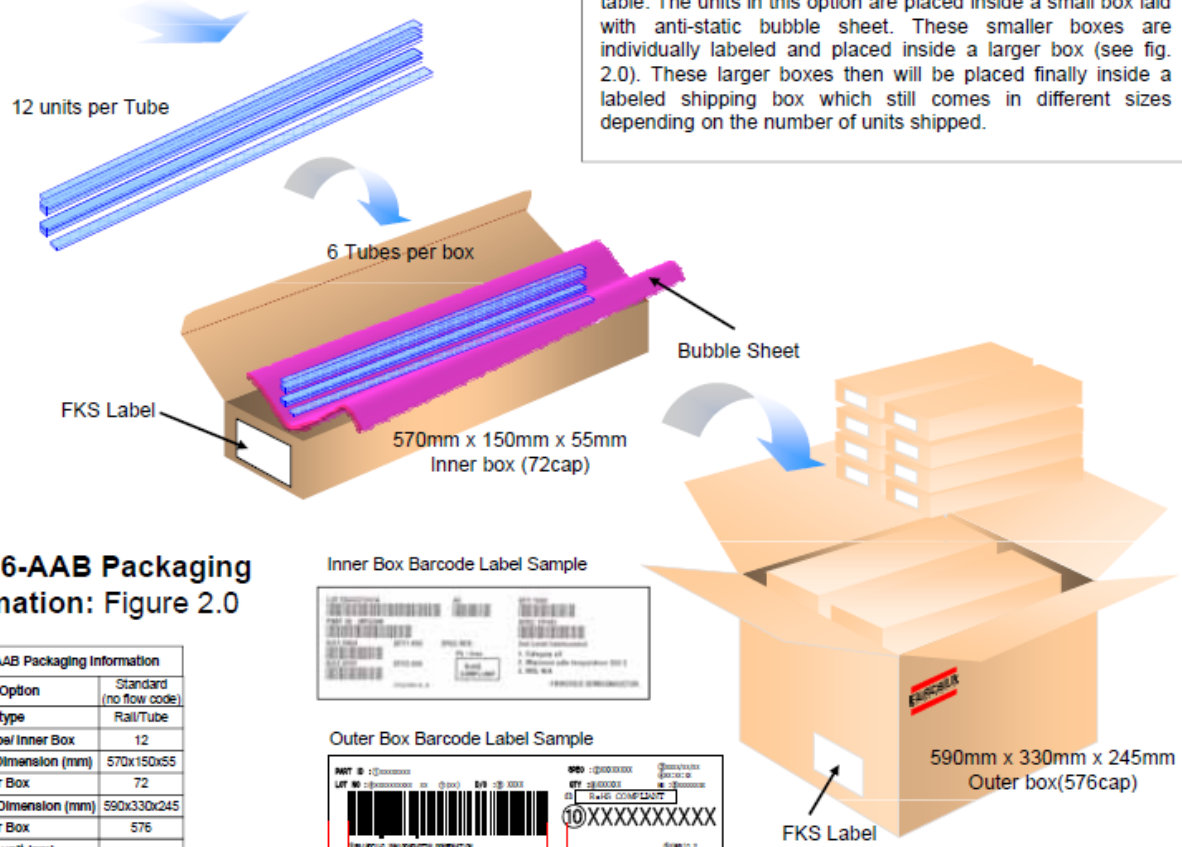
FAIRCHILD SEMICONDUCTOR®

SPM26-AAB Tube Packing Configuration: Figure 1.0



Packaging Description:

SPM26-AAB parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains six tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped. The other option comes in bulk as described in the Packaging Information table. The units in this option are placed inside a small box laid with anti-static bubble sheet. These smaller boxes are individually labeled and placed inside a larger box (see fig. 2.0). These larger boxes then will be placed finally inside a labeled shipping box which still comes in different sizes depending on the number of units shipped.



SPM26-AAB Packaging Information: Figure 2.0

SPM26-AAB Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	12
Inner Box Dimension (mm)	570x150x55
Max qty per Box	72
Outer Box Dimension (mm)	590x330x245
Max qty per Box	576
Weight per unit (gm)	-
Note/Comments	

Inner Box Barcode Label Sample

Outer Box Barcode Label Sample

SPM26-AAB Tube Information: Figure 3.0

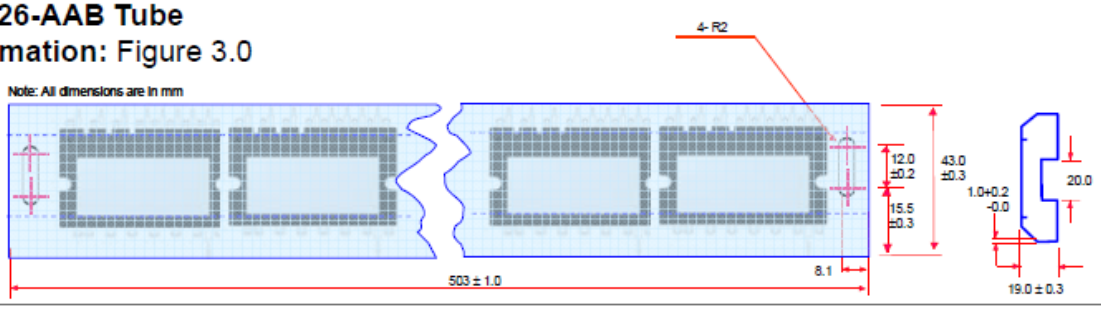


Figure 49.SPM26-AAB Packaging Specification

Related Resources

FNA40560 — Smart Power Module Motion-SPM™

FNA40860 — Smart Power Module Motion-SPM™

FNA41060 — Smart Power Module Motion-SPM™

FNA41560 — Smart Power Module Motion-SPM™

FNB40560 — Smart Power Module Motion-SPM™

FNB41060 — Smart Power Module Motion-SPM™

FNB41560 — Smart Power Module Motion-SPM™

AN-9071 — Smart Power Module Motion-SPM™ in µMini DIP SPM® Thermal Performance Information

AN-9072 — Smart Power Module Motion-SPM™ in µMini DIP SPM® Mounting Guidance

RD-344 — Reference Design for FNA41560 (One Shunt Solution)

RD-345 — Reference Design for FNA41560 (Three Shunt Solution)