

**PAN AFRICAN UNIVERSITY INSTITUTE FOR BASIC SCIENCES,
TECHNOLOGY AND INNOVATION**

Faculty of Engineering
Department Of
Computer Engineering

Assignment: 1

PUE 3141: ADVANCED DIGITAL SYSTEMS DESIGN

Submitted by: ALSHIMA ALWALI

Instructor: DR. MUTUGI KIRUKI

$$\square \quad y = \overline{ACD} + \overline{B(C + A(\overline{BD}))} + \overline{A}B\overline{C}\overline{D}$$

• firstly: $\overline{ACD} \Rightarrow \overline{A} + \overline{C} + \overline{D} \rightarrow \underline{(1)}$

• secondly: $\overline{B(C + A(\overline{BD}))}$

$$\Rightarrow \overline{B} + \overline{(C + A(\overline{BD}))}$$

$$\Rightarrow \overline{B} + C + A(\overline{BD})$$

$$\Rightarrow \overline{B} + C + A(\overline{B} + \overline{D})$$

$$\Rightarrow \overline{B} + C + A\overline{B} + A\overline{D} \rightarrow \underline{(2)}$$

• by applying the rules $\rightarrow \begin{cases} A + AB = A \\ A + \overline{A}B = A + B \end{cases}$ on (1) & (2)

\therefore

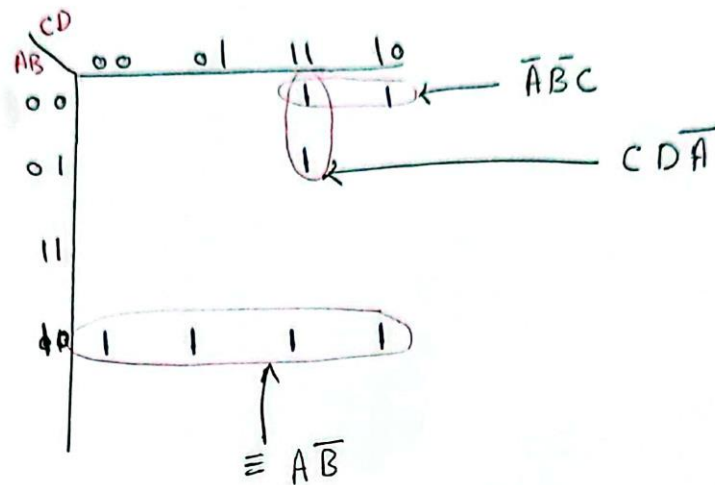
$$\Rightarrow (\overline{A} + A\overline{B}) + (\overline{D} + \overline{D}A) + \overline{B} + (C + \overline{C})$$

$$\Rightarrow (A + \overline{B}) + (\overline{D}) + (\overline{B}) + 1 \Rightarrow A + \overline{B} + \overline{D} + 1 \rightarrow \otimes$$

• Thirdly: add \otimes to the last term $\overline{A}B\overline{C}\overline{D}$

$$\therefore \overline{A}B\overline{C}\overline{D} + \underbrace{A + \overline{B} + \overline{D} + 1}_{=A} \Rightarrow \overline{A}B\overline{C}\overline{D} + \underbrace{A + \overline{B} + \overline{D}}_{\neq}$$

$$(2) Z = A\bar{B} + \bar{A}CD + \bar{A}\bar{B}C + A\bar{B}C\bar{D}$$



• $A\bar{B}$: Since it has only 2 terms it will cover 4 cells.

$\bar{A}CD$: // // // // 3 terms // // pair of cells

$\bar{A}\bar{B}C$: // // // // // // //

$$\therefore \text{From K-map above } Z = \bar{A}\bar{B}C + CDA\bar{A} + A\bar{B}$$

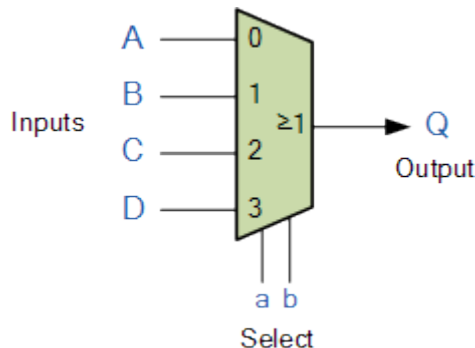
3\ Review the following combinational logic modules (symbols & brief description): Multiplexer, binary decoder, magnitude comparator, Adders (full & half-adder):

Multiplexer

Multiplexing is the generic term used to describe the operation of sending one or more analogue or digital signals over a common transmission line at different times or speeds and as such, the device we use to do just that is called a **Multiplexer**.

The *multiplexer*, shortened to “MUX” or “MPX”, is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple input lines called “channels” one at a time to the output.

Multiplexers, or MUX’s, can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analogue types using transistors, MOSFET’s or relays to switch one of the voltage or current inputs through to a single output.



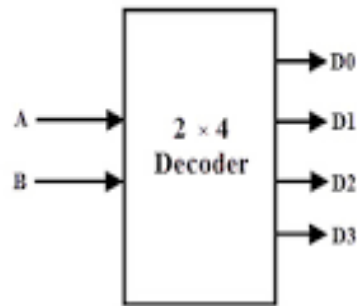
Binary Decoder

The name “Decoder” means to translate or decode coded information from one format into another, so a binary decoder transforms “n” binary input signals into an equivalent code using 2^n outputs.

Binary Decoders are another type of digital logic device that has inputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an n -bit code, and therefore it will be possible to represent 2^n possible values. Thus, a

decoder generally decodes a binary value into a non-binary one by setting exactly one of its n outputs to logic “1”.

If a binary decoder receives n inputs (usually grouped as a single Binary or Boolean number) it activates one and only one of its 2^n outputs based on that input with all other outputs deactivated



Magnitude Comparator

Magnitude comparators are mostly utilized in microcontrollers and CPUs to address data comparison, register and perform all other arithmetic operations. Magnitude comparators are implemented in many devices and every auto-turn-off device is surely designed using a comparator.

A comparator is a decision-making tool and it holds the ability to be executed in numerous control devices. Accepting two binary numbers as input (A and B), data comparison through magnitude comparators produces the output to indicate equality ($A=B$), logic 1 in two conditions when ($A>B$ or $A<B$).



Adders (full & half-adder)

➤ Full adders

A full adder circuit is central to most digital circuits that perform addition or subtraction. It is so called because it adds together two binary digits, *plus* a carry-in digit to produce a sum and carry-out digit.¹ It therefore has three inputs and two outputs.

➤ **Half adders**

A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The half adder is able to add two single binary digits and provide the output plus a carry value. It has two inputs, called A and B, and two outputs S (sum) and C (carry). The common representation uses a XOR logic gate and an AND logic gate.

