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Registration No: EE300-0012/2021

Assignment

1) simplify the following Boolean expression:

$$Y = \overline{\overline{A}CD} + \overline{B(C + \overline{A(\overline{B}\overline{D})})}$$

$$\overline{\overline{A}CD} = \overline{\overline{A} + \overline{C} + \overline{D}}$$

$$\overline{B(C + \overline{A(\overline{B}\overline{D})})} = \overline{B} + \overline{(C + \overline{A(\overline{B}\overline{D})})}$$

$$= \overline{B} + (C + \overline{A(\overline{B}\overline{D})})$$

$$= \overline{B} + C + A(\overline{B} + \overline{D})$$

$$= \overline{B} + C + A\overline{B} + A\overline{D}$$

$$= \overline{B}(1 + A) + C + A\overline{D}$$

$$= \overline{B} + C + A\overline{D}$$

$$Y = \overline{A} + \overline{C} + \overline{D} + \overline{B} + C + A\overline{D}$$

$$= \overline{A} + \overline{B} + (\overline{C} + C) + \overline{D}(1 + A)$$

$$= 1 + \overline{A}\,\overline{B} + \overline{D} = 1$$

$$Y = 1$$

2)

$$Z = A\overline{B} + \overline{A}CD + \overline{A}\,\overline{B}C + A\overline{B}C\overline{D}$$

$$A\overline{B} = A\overline{B}CD + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}\overline{C}D + A\overline{B}C\overline{D}$$

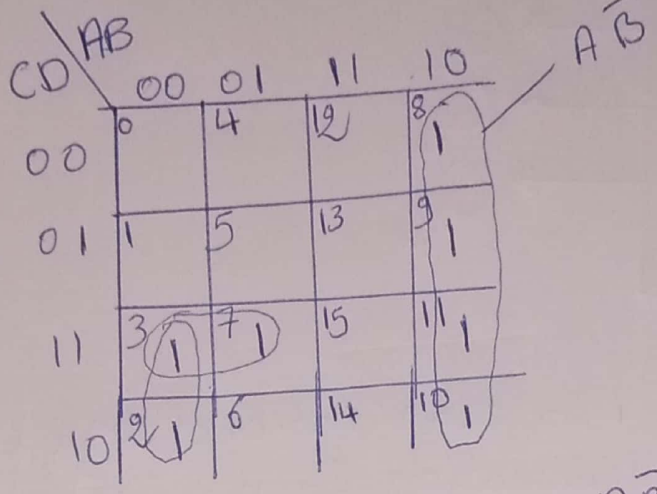
$$\overline{A}CD = \overline{A}BCD + \overline{A}\,\overline{B}CD$$

$$\overline{A}\,\overline{B}C = \overline{A}\,\overline{B}CD + \overline{A}\,\overline{B}C\,\overline{D}$$

$$A\overline{B}C\overline{D}$$

$Z = \Sigma m\,(11, 9, 8, 10, 7, 3, 2)$

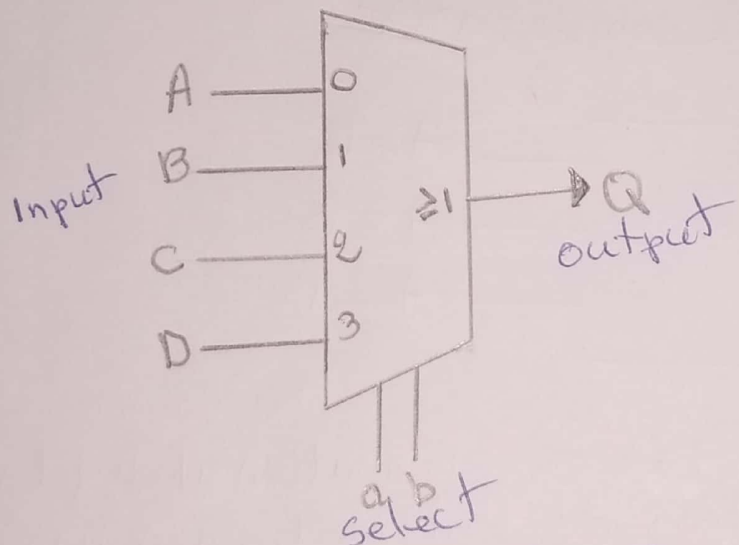
$Z = \Sigma m\,(2, 3, 7, 8, 9, 10, 11)$



$Z = \bar{A}CD + \bar{B}C + A\bar{B}$

2) Review of the combinational logic module

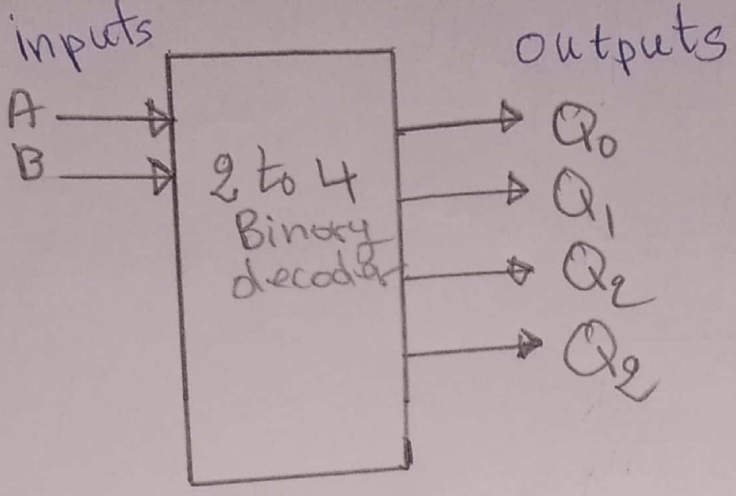
Multiplexer



Multiplexer: is a combinational circuit that has maximum of 2^n data input, n selection lines and single output lines. One of these data inputs will be connected to the output based on the value of selection lines.

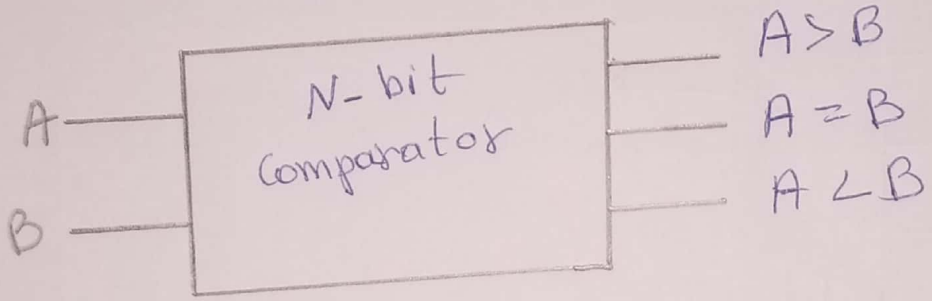
since there are n selection lines, there will be 2^n possible combinations of zero and ones, so each combination will select only one data input. Multiplexer is also called as Mux.

Binary decoder



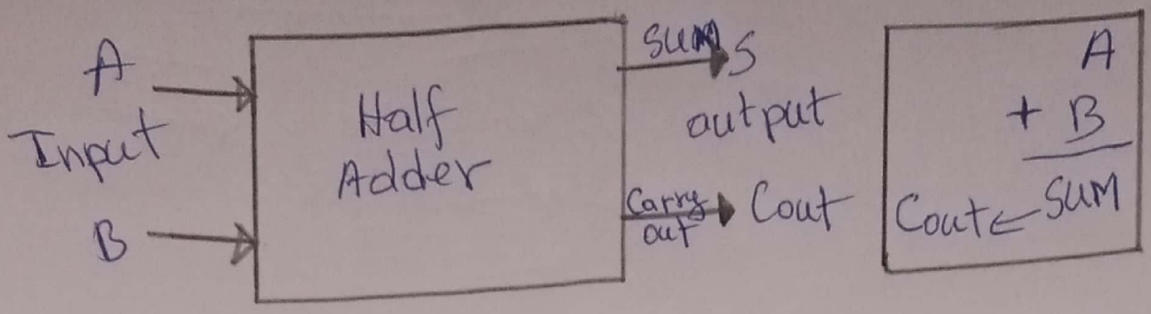
Binary decoder: is a combinational logic circuit that converts binary information from n coded inputs to a maximum of 2^n. They are used in wide variety of applications including instruction decoding, data demultiplexing, Sevent segment displays, and as address decoders for memory and port-mapped I/O

Magnitude comparator



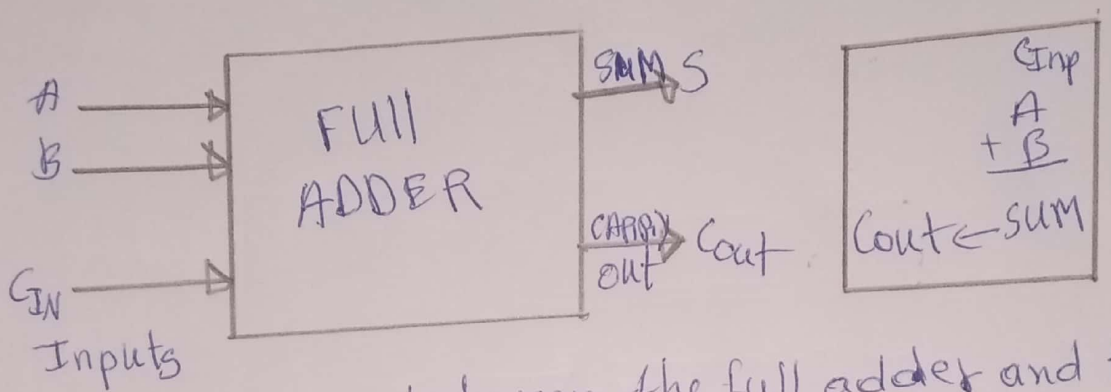
Magnitude comparator: is a combinational digital circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than, or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for A > B condition one for A = B condition, and one A < B condition

Half Adder circuit



Half Adder : is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits.

Full Adder Circuit



The main difference between the full adder and the previous half adder is that a full adder has three inputs. The same single bit data inputs A and B as before plus an additional carry-in (Cin) input to receive the carry from a previous stage as shown above.

4) The output signal waveforms Q_0 and Q_1 for 5 clock pulses