AN EFFICIENT CHANNEL CODING FOR FUTURISTIC CORDLESS APPLICATION

A PROJECT REPORT

Submitted by

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(AUTONOMOUS)

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K. RAMAKRISHNAN COLLEGE OF ENGINEERING SAMAYAPURAM TRICHY-621112

DEPARTMENT OF ECE

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M1. To equip the students with latest technical, analytical and practical knowledge

M2. To provide vibrant academic environment and Innovative Research culture.

M3. To provide opportunities for students to get Industrial Skills and Internships to meet out the challenges of the society.

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PEO2: Graduates will provide innovative ideas and management skills to enhance the standards of the society by individual and with team works through the acquired Engineering knowledge.

PEO3: Graduates will be successful professionals through lifelong learning and contribute to the society technically and professionally.

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PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and Team Work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large. Some of them are, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

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PO12: Lifelong learning: Recognize the need for, and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

CO-PO MAPPING FOR PROJECT WORK – UEC1811

After successful completion of this course, the students should be able to

CO1: Apply knowledge of basic science and engineering to electronics and communication engineering problems.

CO2: Identify, formulate real time problems and find solutions by applying engineering concepts.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	3	2	-	-	-	1	3	-	2	1	1	3
CO2	3	2	3	2	-	2	-	1	3	2	-	2	-	3
CO3	3	2	2	2	3	-	-	1	3	-	-	2	-	3

CO3: Implement the design in hardware and verify the performance of the design using modern simulation tools.

K.RAMAKRISHNAN COLLEGE OF ENGINEERING

BONAFIDE CERTIFICATE

Certified that this project report **"AN EFFICIENT CHANNEL CODING FOR FUTURISTIC CORDLESS APPLICATION"** is the bonafide work of **"MUTHULAXMI M, PAVITRA M, PRIYADHARSHINI S, RATI PRIYA C"** who carried out the project work under my supervision.

21/5/24

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INTERNAL EXAMINER

EXTERNAL EXAMINER

DECLARATION

We hereby declare that the work entitled "**AN EFFICIENT CHANNEL CODING FOR FUTURISTIC CORDLESS APPLICATION**" is submitted in partial fulfilment of the requirement of the award of the degree in B.E., K.Ramakrishnan College of Engineering, Trichy, is a record of our own work carried out by us during the academic year 2023-2024 under the supervision and guidance of **Ms.RADHA N** Assistant Professor, Department of ELECTRONICS AND COMMUNICATION ENGINEERING, K.RAMAKRISHNAN COLLEGE OF ENGINEERING. The extent source of information that are derived from the existing information are derived from the existing literature and have been indicated through the dissertation at the appropriate places. The matter embodied in this work is original and has not been submitted for the award of any degree or diploma, either in this or any other University.

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ABSTRACT

This paper presents an efficient error detection and correction code to detect and correct 50% of the errors during wireless transmission. The proposed novel Minimal Intricacy Parity Check Code (MIPC), Channel coding scheme offers minimum power consumption, less propagation delay, lesser area occupation, and minimum computational complexity through cadence 90nm technology. When compared to the low complexity parity check code, the power consumption, area occupation, and propagation delay of the proposed MIPC decrease by 38.60%, 36.06%, and 42.14% respectively. The proposed channel coding scheme requires less complexity to add parity bits with the information bits. The proposed decoding algorithm also requires less complexity to retrieve the original message bits. Simulation results using MATLAB reveal that the proposed channel code exhibits better BER performance. The proposed MIPC code has a reduction in BER of 78.79% to the LCPC code respectively at 2 dB. The aforementioned advantages show that the proposed channel coding scheme is the best suitable for next generation wireless communication.

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LIST OF ABBREVIATIONS

ACRONYM	ABBREVIATION
MIPC	Minimal Intricacy Parity Check Code
LCPC	Low Complexity Parity Check Code
LDPC	Low Density Parity Check Code
FEC	Forward Error Correction
BPSK	Binary Phase Shift Keying
AWGN	Additive White Gaussian Noise
FPGA	Field Programmable Gate Array
NOMA	Non-Orthogonal Multiple Access
ARQ	Automatic Repeat Request
BER	Bit Error Rate
ISI	Inter Symbol Interference
PDR	Packet Delivery Radio
SNR	Signal To Noise Ratio
PED	Parity Error Detection
RTL	Register Transfer Level

CHAPTER 1

INTRODUCTION

Channel coding means how we encode and decode a message in order to make wireless communication error free. It is helpful to know that received data is correct. The noise present in the channel creates unwanted errors between input and output sequences. The error probability should be very low for a reliable communication. Channel coding techniques fall into two main categories: error control coding and data compression coding. Error control coding is concerned with adding redundancy to transmitted data to detect and correct errors that occur during transmission. This redundancy allows the receiver to identify and correct errors, improving the reliability of the communication system.

The performance is measured by signal to noise ratio or SNR. A channel coding solution is primarily measured by its ability to correct errors at a given SNR, but it also important to understand the maximum possible throughput and the latency as well as resources and power consumed. Channel coding involves trade-offs between data rate, error correction capability, and complexity. Channel coding also known as forward error control coding (FECC).

Channel coding is performed both at the transmitter and at the receiver. At the transmit side, channel coding is referred to as encoder, where extra bits (parity bits) are added with the raw data before modulation. At the receive side, channel coding is referred to as the decoder. In Channel coding it has pure information with structured redundancy. The structured redundancy added in channel coding is called parity or check sum. The distance measure used depends on the channel over which we transmit our code words. It is a key component of modern communication systems and is essential for achieving high data rates and reliability in various applications. There are some applications in channel coding.

1.1 APPLICATIONS

Wireless Communications In wireless communication systems such as Wi-Fi, Bluetooth, 4G LTE, and 5G, channel coding techniques like convolutional codes, turbo codes, and LDPC (Low-Density Parity-Check) codes are employed to improve the reliability of data transmission over noisy wireless channels. These codes help combat fading, interference, and other impairments characteristic of wireless communication environments.

Satellite Communications Channel coding is crucial in satellite communication systems to ensure reliable transmission of data over long distances and through noisy space channels. Error-correcting codes are used to protect data transmitted between satellites and ground stations, as well as between satellites themselves.

Digital Television and Broadcasting In digital television broadcasting standards such as ATSC (Advanced Television System Committee) and DVB (Digital Video Broadcasting), channel coding techniques are utilized to enable robust transmission of audio and video content over terrestrial, cable, and satellite networks. These codes help maintain signal quality and minimize errors caused by noise and interference.

Storage Systems Channel coding is employed in storage systems such as hard disk drives (HDDs), solid-state drives (SSDs), optical discs, and flash memory devices to enhance data reliability and integrity. Error-correcting codes are used to detect and correct errors that may occur due to media degradation, read/write errors, or other storage-related issues.

Deep Space Communications In deep space exploration missions, where communication links suffer from extreme distances and weak signal strengths, channel coding techniques are indispensable. Codes with powerful error-correction capabilities, such as Reed-Solomon codes, are utilized to ensure reliable communication between spacecraft and ground stations, even in highly challenging environments.

Digital Audio and Video Streaming Channel coding is utilized in digital audio and video streaming applications to ensure uninterrupted playback and high-quality media delivery over the internet and other networks. Error-resilient coding schemes help mitigate packet loss and errors introduced during data transmission, enhancing the user experience for streaming services.

Mobile and IOT Devices In mobile communication networks and Internet of Things (IOT) devices, channel coding techniques are employed to improve spectral efficiency and increase the reliability of data transmission over wireless channels. Efficient coding schemes help conserve battery power and enable seamless connectivity for mobile devices and IOT sensors.

Error Correction in Data Transmission Channel coding is utilized in various data transmission systems, including Ethernet, optical communication, and point-to-point communication, to detect and correct errors introduced by noise, interference, and other impairments during transmission.

Fiber Optic Communication In fiber optic communication systems, channel coding is utilized to mitigate the effects of optical noise and dispersion, allowing for high-speed and reliable transmission of data over long distances.

Underwater Communication Channel coding plays a vital role in underwater communication systems used for applications like oceanographic research and offshore industries, where communication is challenged by the harsh underwater environment.

These applications highlight the versatility and importance of channel coding to ensure reliable communication across diverse technology.

1.2 WIRELESS COMMUNICATION BLOCK DIAGRAM

A wireless communication block diagram typically consists of several key components. At its core, there's a transmitter section responsible for encoding, modulating, and amplifying the input signal. This modulated signal is then transmitted through an antenna. On the receiving end, another antenna picks up the signal, which is then passed through a receiver section. Here, the signal undergoes demodulation, decoding, and amplification processes to extract the original information. Both transmitter and receiver sections are often accompanied by filters, amplifiers, and oscillators to ensure signal integrity and proper functioning.

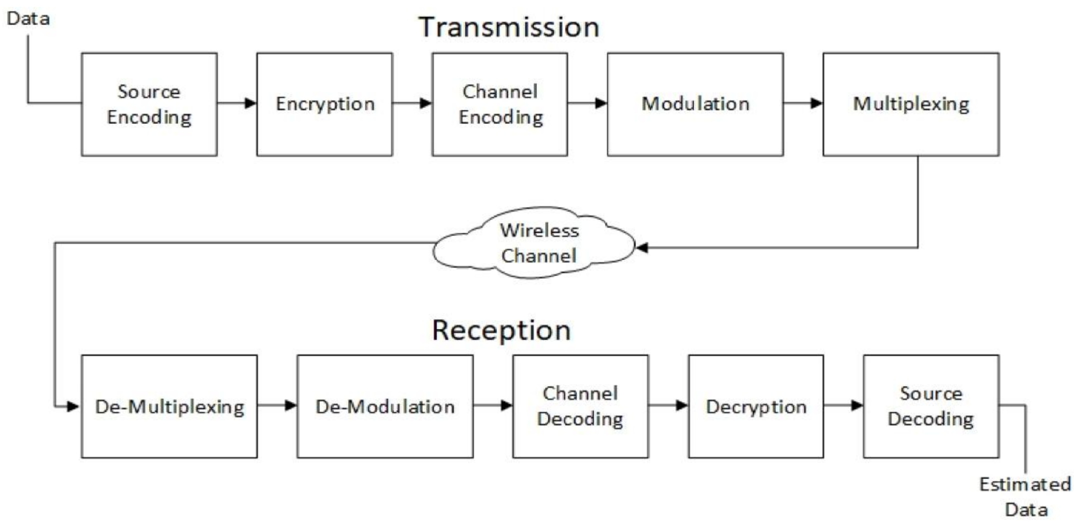

Figure 1.1: Block Diagram of Wireless Communication

Figure 1. shows the block diagram of wireless communication. Source encoding, also known as source coding or data compression, is a process in

which data is represented using fewer bits than the original representation, while still preserving the essential information content. The primary objective of source encoding is to reduce redundancy and minimize the amount of data required for storage or transmission, thereby saving storage space, reducing transmission bandwidth, and improving efficiency in data handling. Lossy and Lossless compression are two main types.

Encryption is a process of converting plaintext (ordinary text or data) into ciphertext (encoded text or data) using cryptographic algorithms and keys. The primary purpose of encryption is to ensure data confidentiality and protect sensitive information from unauthorized access or interception during storage, transmission, or processing.

Channel encoding, also known as error control coding or forward error correction (FEC), is a technique used in communication systems to enhance the reliability of data transmission over noisy or error-prone channels. It involves adding redundant information to the transmitted data stream in such a way that the original message can be accurately reconstructed at the receiver, even if errors occur during transmission.

The primary goal of channel encoding is to detect and correct errors introduced by noise, interference, distortion, or other impairments in the communication channel. By adding redundancy to the data stream, channel encoding allows the receiver to identify and correct errors, thereby improving the overall reliability of the communication system.

Modulation is a fundamental process in communication systems that involve modifying a carrier signal's properties, such as its amplitude, frequency, or phase, in accordance with the information signal being transmitted. The primary purpose of modulation is to encode the information signal onto the carrier signal in a form suitable for efficient transmission over a communication channel.

Multiplexing is a technique used in telecommunications and networking to combine multiple signals or data streams into a single transmission medium, such as a cable, Fiber optic line, or wireless channel. The primary goal of multiplexing is to efficiently utilize the available bandwidth and resources of the communication channel, allowing multiple users or devices to share the transmission medium simultaneously.

A wireless channel refers to the medium through which wireless communication signals propagate between the transmitter and the receiver in a wireless communication system. Unlike wired communication channels, which rely on physical cables or optical fibers, wireless channels transmit signals through the air or free space.

De-multiplexing is the process of separating multiple signals or data streams that have been combined or multiplexed onto a single transmission medium or channel. It is essentially the reverse process of multiplexing, which combines multiple signals into one.

In the context of data communication and networking, de-multiplexing is crucial for correctly routing and delivering individual data streams or packets to their respective destinations after they have been transmitted over a shared communication channel.

Demodulation is the process of extracting the original information signal from a modulated carrier signal at the receiver end of a communication system. Modulation, as mentioned earlier, involves altering the properties of a carrier signal to encode information for transmission over a communication channel. Demodulation reverses this process to recover the original information signal from the modulated carrier.

Channel decoding, also known as error correction decoding, is the process of recovering the original data or message sent over a noisy communication channel. It is a critical component of communication systems, especially in scenarios where the transmitted signal is corrupted by noise, interference, or other impairments during transmission.

Channel decoding algorithms are designed to detect and correct errors introduced during data transmission over unreliable communication channels. These errors may result from various factors, such as noise, attenuation, interference, distortion, and fading.

Decryption is the process of converting encrypted or encoded data back into its original, readable form, using a decryption algorithm and the appropriate decryption key. It is the reverse operation of encryption, where plaintext is transformed into ciphertext to secure it from unauthorized access during transmission or storage.

Source decoding is a process used in various fields such as data compression, digital communications, and signal processing to reconstruct the original source or message from its encoded or compressed representation. Its primary objective is to reconstruct the original source or message from its encoded or compressed representation. This intricate process plays a pivotal role in efficiently restoring information to its initial form, ensuring accurate communication and optimal data utilization.

1.3 SIGNIFICANCE OF CHANNEL CODING

Channel coding is essential in communication systems for several reasons:

Improved Reliability By adding redundancy to the transmitted data, channel coding improves the reliability of communication systems. Error-correcting codes can reconstruct the original data even if some bits are corrupted or lost during transmission, thereby minimizing the impact of channel impairments on the overall communication quality.

Increased Data Integrity Channel coding enhances the integrity of transmitted data by reducing the likelihood of data corruption or loss. By detecting and correcting errors at the receiver end, channel coding helps ensure that the received data accurately represents the original information sent by the transmitter.

Extended Communication Range In wireless communication systems, channel coding techniques enable communication over longer distances and in challenging environments. By mitigating the effects of signal attenuation and fading, error-correcting codes extend the effective communication range of wireless networks, improving coverage and reliability.

Spectral Efficiency Channel coding contributes to spectral efficiency by allowing for the transmission of more data within the available bandwidth. By incorporating error-correcting codes, communication systems can achieve higher data rates while maintaining reliable communication performance.

Standardization and Interoperability Channel coding schemes are often standardized to ensure interoperability and compatibility between different communication systems and devices. Standardized error-correcting codes facilitate seamless communication across diverse networks and platforms, enabling widespread adoption and deployment of communication technologies.

1.4 ERROR DETECTION

Error detection is a fundamental concept in communication and information theory. It refers to the process of detecting errors that occur during the transmission or storage of data. Error detection techniques are employed to determine whether the received data is error-free or if it has been corrupted during transmission. There are several common methods for error detection:

- Parity Check
- Checksum
- Cyclic Redundancy Check
- Hamming distance

1.5 ERROR CORRECTION

Error correction is a process used in communication and information theory to automatically detect and correct errors that occur during the transmission or storage of data. Unlike error detection, which only identifies the presence of errors, error correction techniques have the ability to not only detect but also recover from errors, thus ensuring data integrity. There are several methods for error correction**:**

- Forward error correction
- Automatic Repeat request
- Turbo codes
- LDPC codes

Error correction techniques play a crucial role in ensuring the reliability of data transmission in various communication systems. By automatically detecting and correcting errors, these techniques help minimize the need for retransmissions and enhance the overall efficiency of communication systems.

To further explore error detection and correction mechanisms, this paper presents a novel parity check code architecture. This prudent channel coding MIPC has a high level of error correction capability that detects and corrects all errors in the message bits that occur. It also has less computational complexity when compared to other error correction codes, without compromising its power consumption, area consumption, and propagation delay. A unique method is proposed in this paper to lower the bit error rate while also enhancing transmission quality.

The remainder of this report is formulated as follows: Chapter 2 reviews the earliest error correction and detection methods. Chapter 3 explains the existing low complexity parity check code. Chapter 4 explains the Proposed Minimal Intricacy Parity Check Code and its performance analysis found in Chapter 5 and Chapter 6 concludes the report.

CHAPTER 2

LITERATURE SURVEY

There are many ways to design and implement a channel coding scheme. This chapter covers various literature studies that provide implementations of channel coding using different techniques and the main drawbacks observed in each technique.

In 2000, Paterson K.G and Jones A.E proposed **An Efficient decoding algorithms for generalized Reed-Muller codes** [1]. Reed-Muller codes, constructed from Boolean functions, are distinguished by their order (r) and dimension (m), providing flexibility in error correction. To ensure effective error correction, it's crucial to identify and analyze the type and distribution of errors anticipated within the system. This involves assessing various error scenarios, including random errors, burst errors, and specific channel characteristics. By understanding these potential error patterns, appropriate error correction strategies can be implemented, enhancing the overall reliability and performance of the system. The merit of this paper lies in low complexity and effective error correction. The limitation of this paper is increased computational demands for longer codes and decoding complexity versus performance balance.

In 2005, Zhong He and Zhang T introduced **A practical LDPC coding system design approach** [2]. The method employed for implementing LDPC codes is Bloom Filtering, known for its speed and efficiency in determining whether a given element belongs to a set. This approach facilitates the detection and correction of errors within their corresponding data set. Leveraging Bloom Filtering in practical designs enables effective error mitigation with minimized overhead. This method offers a promising solution for addressing errors in various applications, contributing to improved reliability and performance in data transmission and storage systems. The advantage lies in enhanced handling, quick identification, and streamlined data. The disadvantage lies in increased complexity involving memory, computation, and communication.

In 2006, **S. M. Elengical, F. Takawira** and **H. Xu,** proposed **Reduced complexity maximum likelihood decoding of linear block codes** [3], implementing a simpler decoding method for linear block codes, inspired by the Kaneko decoder, involves integrating skip conditions to eliminate redundant steps. This approach, tested through simulations using BPSK signalling over an AWGN channel, aims to streamline the decoding process while maintaining accuracy. The advantage of this paper provides maintained performance comparable to that of the original decoder. The main drawbacks include dependency on signal-to-noise ratio (SNR) affecting effectiveness in low SNR scenarios and initial complexity.

In 2009, Lee C.M and Su Y.T proposed the **Stochastic erasure-only list decoding algorithms for Reed-Solomon codes** [4], are widely used in communication and storage for error correction. Popular erasure decoding algorithms like Berlekamp-Welch and Guru swami-Sudan are specifically designed for Reed-Solomon codes. They excel in recovering missing or corrupted symbols, ensuring reliable error recovery in different applications. The main advantage is that tailored algorithms effectively handle erasures in received codewords. The main drawbacks are Stochastic decoding can increase computational complexity compared to deterministic methods.

In 2011, Y. Luo and J. Li introduced **Optimal and suboptimal structured algorithms of binary linear block codes** [5], presenting novel approaches for implementing optimal and suboptimal algorithms tailored to linear block codes. These algorithms leverage geometric principles, supported by established lemmas and theorems concerning minimum distance and weight properties. However, owing to their inherent complexity, practical implementation often resorts to suboptimal methods. Comparatively, when contrasted with BCH codes, these structured algorithms demonstrate equivalent minimum distance properties, affording greater flexibility in code design. The main advantage lies in providing structured algorithms for binary linear block codes, aiding systematic design and highlighting equivalence in minimum distance with BCH codes, demonstrating algorithm effectiveness. The disadvantage of this paper provides lacks empirical validation.

In 2014, Lu E.H, Chen T.C. and Lu P.Y Suggested **A new method for evaluating error magnitudes of Reed-Solomon codes** [6]. Implementing this solution on conducting a comprehensive review of the existing methods for evaluating error magnitudes of Reed-Solomon codes is essential. By scrutinizing these methods, we can better understand the complexities involved in assessing error magnitudes within Reed-Solomon codes. It is crucial to clearly define the problem associated with evaluating error magnitudes in Reed-Solomon codes magnitudes than current techniques, and it could also demonstrate greater resilience to various error scenarios, such as burst errors, random errors, or erasures. The drawback of this paper entails implementation hindrance and computational limits.

In 2014, Reviriego, P., Martínez, J., Pontarelli, S proposed **A method to design SEC-DED-DAEC codes with optimized decoding** [7]. The method utilized is Decision Feedback Equalization, employed specifically for detecting and correcting errors within bursts of data. Decision Feedback Equalization is a signal processing technique commonly applied in communication systems to mitigate the effects of Intersymbol interference (ISI) caused by transmission through dispersive channels. By analyzing received data and incorporating feedback from previously detected symbols, Decision Feedback Equalization aims to accurately reconstruct the transmitted symbols, thereby correcting errors introduced during transmission. The merit of this paper lies in its enhanced signal quality and low latency. The drawback lies in convergence, training, and sensitivity to channel estimation.

In 2014, Sarangi S and Banerjee S proposed **An Efficient hardware implementation of encoder and decoder for Golay code** [8]. An efficient implementation of the encoding algorithm for both the binary Golay code and extended binary Golay code. Specifically designed and implemented in Virtex-4 FPGA, this encoding algorithm aims to enhance the performance and efficiency of error correction in communication systems. Additionally, the paper presents an optimized decoding architecture (24,12,8) based on an Incomplete Maximum Likelihood Decoding (IMLD) algorithm. This decoding architecture offers improved error correction capabilities, contributing to enhanced reliability and accuracy in data transmission and reception processes. A notable feature of this paper is its high-speed, efficient, compact, and low-latency solution. The challenges with this paper include limited scalability with longer codes and susceptibility of IMLD to decoding errors.

In 2015, Chang T.C.Y and Su Y.T posited **Dynamic weighted bit-flipping decoding algorithms for LDPC codes** [9], enacting this procedure on Redundant Residue Number System (RRNS), which serves as the foundation for the analysis and implementation. RRNS operates on the principle of multiple residue digit error detection and correction, offering robustness in handling errors within the numerical system. The merit of this paper is RRNS offers fault tolerance through redundancy. The drawback of this paper is that increased storage and complexity pose challenges in error handling.

In 2015, Reviriego P, Liu S, Xiao L, and Maestro J.A introduced **An efficient single and double-adjacent error correcting parallel decoder for the (24, 12) extended golay code** [10]. The proposed approach involves the implementation of a dual-decoder system aimed at efficiently correcting various error patterns. Specifically, a fast parallel decoder is utilized to address the most common error patterns, such as single and double adjacent errors. This parallel decoder operates swiftly and simplifies the correction process, thereby enhancing the overall decoding speed and efficiency. In contrast, for error patterns beyond the capability of the parallel decoder, a slower serial decoder is employed. A key benefit is the achieved reductions in area, delay, and power consumption, along with the cost reduction in SEC-DAEC implementation. The drawbacks of this paper include compatibility limitations with platforms/systems and the requirement for specialized expertise for implementation.

In 2016, S. A. Alabady and F. Al-Turjman proposed **Low Complexity Parity Check Code for Futuristic Wireless Networks Applications** [11]. The proposed low-complexity parity-check (LCPC) codes present a solution for efficient error detection and correction in futuristic wireless networks. These codes offer shorter code word lengths and lower complexity compared to turbo and LDPC codes, while still delivering up to 3-dB coding gain. In simulation tests, LCPC codes outperform Hamming and Reed-Solomon codes, showcasing their effectiveness in practical scenarios. The advantage of this paper is low complexity in both encoding and decoding processes. The main disadvantage in performance as more complex codes like LDPC in certain scenarios.

In 2018, M. Zhang, Z. Li, L. Xing and N. Tang proposed **A Construction of Some New Quantum BCH Codes** [12]. It involves the examination of various properties of cyclotomic cosets deemed suitable for specific purposes. The implementation strategy relies on Steane's enlargement of nonbinary Calderbank-Shor-Steane codes and the Hermitian construction method. By leveraging these techniques, the study aims to enhance the efficiency and effectiveness of error correction in communication systems. Through an in-depth analysis of cyclotomic cosets and the application of advanced coding methods, the research endeavors to contribute valuable insights into improving the reliability and robustness of data transmission processes. A notable feature of this paper is its improved minimum distance, optimality for quantum BCH codes, and versatile construction. The drawback is its high complexity.

In 2020, Yu N.Y introduced **A Binary Golay spreading sequences and Reed-Muller codes for uplink grant-free** [13]. Grant-free NOMA introduces a novel concept wherein multiple users transmit their data without the prior allocation of orthogonal resources like time slots or frequency bands. This approach aims to enhance spectral efficiency by allowing simultaneous transmissions from multiple users. In the context of uplink transmission in grant-free NOMA, the design of Golay spreading sequences becomes pivotal. These sequences need to be carefully selected to possess low cross-correlation properties, enabling reliable multi-user detection. By choosing suitable Golay spreading sequences, the system can effectively mitigate interference and ensure accurate data detection, thereby optimizing the performance of grant-free NOMA in the uplink scenario. The benefit of this paper lies in both interference reduction and bandwidth expansion. The drawback of this paper is Hardware complexity and code length limitation.

In 2022, B. Gong, C. Ding and C. Li proposed **The Dual Codes of Several Classes of BCH Codes** [14]. This study delves into the exploration of primitive narrow-sense BCH codes and projective narrow-sense ternary BCH codes. Through rigorous investigation, the research introduces novel bounds on the minimum distances of dual codes, surpassing the classical Sidel'nikov and Carlitz-Uchiyama bounds. By pushing the boundaries of theoretical constraints, the study contributes valuable insights into the performance and capabilities of these codes, shedding light on potential advancements in error correction techniques and coding theory. The advantage of this paper is that it improves the performance assessment of codes and provides conditions for subclass identification. The drawbacks include increased complexity and restricted flexibility, as well as limited scope leading to a shortfall in covering a broader range of BCH codes.

Linear block codes encounter challenges such as limited error correction capability, particularly with burst errors. Their fixed block size can lead to inefficiencies in handling varying error patterns. They often exhibit high encoding and decoding complexity, demanding significant computational resources. Our novel proposed MIPC overcomes these challenges and detects and corrects all the message bit errors with less complexity, with efficient area and power consumption. It results in lower bit error rate.

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CHAPTER 3

EXISTING SYSTEM

The unreliable wireless links, broadcast nature of wireless transmissions, interference and noisy transmission channels, frequent topology changes, and the various quality of wireless channel. There are challenges in providing high data rate service, high throughput, high packet delivery ratio (PDR), low end to end delay and reliable services.

3.1 LOW COMPLEXITY PARITY CHECK CODE

There are challenges in providing high data rate service, high throughput, high packet delivery ratio (PDR), low end to end delay and reliable services. In wireless network and real time application systems, low complexity and shorter codeword length in channel coding scheme are preferred. Low Complexity Parity Check (LCPC) codes are a class of error-correcting codes used in digital communication systems. They are designed to provide a good balance between error correction performance and computational complexity, making them suitable for applications where computational resources are limited, such as in mobile devices or low-power communication systems.

In order to address these challenges, a novel error detection and correction codes called the Low Complexity Parity Check (LCPC) codes with short codeword lengths for futuristic wireless networks applications. The proposed codes have less complexity and lower memory requirement in comparison to Turbo and Low-Density Parity Check (LDPC) codes. Simulation results demonstrated that the proposed LCPC codes outperform the Hamming and Reed-Solomon (RS) codes, in addition to the renowned LDPC codes. It offers up to 3 dB coding gain.

The LCPC code is defined a block code (n, k), where n is the codeword length and k is the information length, respectively. In LCPC, three different kinds of LCPC codes are presented. In order to explain how the LCPC codes work, the encoding and decoding of the LCPC (9, 4) code in the next subsections. The encoding/decoding of the LCPC (8, 3) and LCPC (7, 3) codes is identical with the LCPC (9, 4) code.

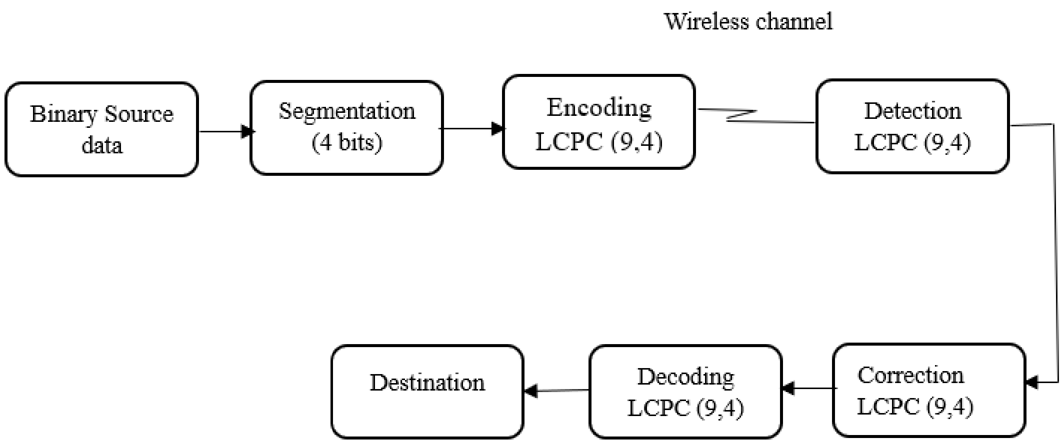

Figure 3.1 LCPC block diagram

Figure 3.1 represents the block diagram of Low Complexity Parity Check Code. The block diagram consists of binary source data and a segmentation block where data is divided into four-bit segments. In the encoding process, the segmented four bits are converted into a code word of length 9. After the decoding process is completed, the original message is retrieved.

(i) LCPC ENCODING

The LCPC code is a block code which takes the data stream from the source encoder, divides it into four-bit symbol (i.e., k), and then encodes each four-bit symbol (depending on the number of rows in G matrix) into a nine-bit codeword (i.e., n), before the transmission. The symbol of source data is denoted as SD_i = (v1, v2, ...vk), where $1 \leq i \leq j$, and j is the number of symbols of the source data, v is a binary bit, and k = 4 is the length of the symbol. Each k-bits symbol is then encoded into an n bits codeword before the transmission. The encoding process is implemented using the generator matrix G.

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \end{bmatrix} \tag{1}$$

In the encoding unit the redundant bits r is then added to each symbol to make the length of the codeword equal to n, where n = k + r, and r = 5. The codeword of the symbol corresponds to CD_{Ti}= (β1, β2 ... βn), where n = 9, and βi is a binary bit. A codeword CD_{Ti} given, that is used for encoding the symbols data which is defined as a multiplication between $SD_i$and G

$$CD_{Ti} = SD_i \times G \tag{2}$$

Where, SD_i is an information symbol, CD_{Ti} is the transmitted codeword and G is the proposed generator matrix. In LCPC (9, 4) code, the number of redundant parity bits is 5, so the maximum number of syndrome vector obtained is 32 and this makes the LCPC (9, 4) code can detect and correct single and many cases of double bit errors.

$$\beta 1 = v1 \tag{3}$$

$$\beta 2 = v2 \tag{4}$$

$$\beta 3 = v3 \tag{5}$$

$$\beta 4 = v4 \tag{6}$$

$$\beta 5 = \gamma 1 = v1 \oplus v2 \oplus v3 \oplus v4 \tag{7}$$

$$\beta 6 = \gamma 2 = v1 \oplus v2 \oplus v3 \tag{8}$$

$$\beta 7 = \gamma 3 = v1 \oplus v2 \oplus v4 \tag{9}$$

$$\beta 8 = \gamma 4 = v1 \oplus v3 \oplus v4 \tag{10}$$

$$\beta 9 = \gamma 5 = v2 \oplus v3 \oplus v4 \tag{11}$$

Where, the five bits ($\gamma 1$, $\gamma 2$, ... $\gamma 5$) are the parity bits, and the four bits (v1, v2, ... v4) are the symbol bits.

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{12}$$

(ii) LCPC CODE DECODING

The decoding algorithm is of three stages. Firstly, is the error detection which is implemented by compute the syndrome vector. Secondly, is the determine of the error pattern. Thirdly, is the error correction.

a) LCPC ERROR DETECTION

The detection process detects errors in the received codeword CD_{Ri}that is defined as the transmitted codeword CD_{Ri} with errors pattern (EP). The parity check matrix H of LCPC code is used for this purpose. After the codeword is received, the syndrome vectors (SY) are obtained from the (CD_{Ri}).

$$CD_{Ri} = c + \mathrm{EP} \tag{13}$$

$$\mathrm{SY} = \mathrm{H} \times CD_{Ri}^{T} \tag{14}$$

Where, SY = (γ1, γ2, ... γr) is the syndromes binary vector. The SY can be expressed as

$$\mathrm{SY} = \mathrm{H} \times (CD_{Ti} + \mathrm{EP})^{\mathrm{T}} \tag{15}$$

$$\mathrm{SY} = \mathrm{H} \times CD_{Ti}^{T} + \mathrm{H} \times \mathrm{EP}^{\mathrm{T}} \tag{16}$$

Since any row in the H matrix is orthogonal to the rows of the G matrix, and the inner product of a row in G with a row in H will be zero, the result of multiplication H by the CD_{Ti} is zero if there are no bit errors in the codeword. Where the CD_{Ti} is the transpose of the transmitted codeword.

$$H \times (CD_{Ti})^T = 0 \quad (17)$$

$$SY = H \times (EP)^T \quad (18)$$

The number of error pattern can be computed in the below equation, where, n is the codeword length (in the proposed code n = 9), and e ∈ (1, 9) is the number of bit errors that may occur in the codewords.

$$NoEP = \frac{n!}{e!(n-e)!} \quad (19)$$

b) LCPC ERROR CORRECTION

In the error correction process, the EP is chosen (depending on the SY value) and is fetched from the lookup tables in memory. The correction process is achieved as shown in the Equation (20).

$$\overline{CD_{Ti}} = CD_{Ri} \oplus EP \quad (20)$$

The correction is achieved by adding the specific EP to error received codeword CD_{Ri}. Next, the decoding of the corrected received codeword is carried out. The decoder is implemented by masking the last four bits on the left side of the codeword. After correction process is completed, SD_i can be obtained by implementing the decoding process on the $\overline{CD_{Ti}}$.

The third process is the decoder, which is used to decode the $\overline{CD_{Ti}}$ and obtain the original source symbol data sent.

$$SD_i = \text{AND}\ (\overline{CD_{Ti}}, 111100000) \qquad (21)$$

The masking process for the last left four bits of the correct received codeword must be done by AND operation for the $\overline{CD_{Ti}}$ with (111100000) as given in equation (21).

3.2 CHALLENGES IN EXISTING SYSTEM

(i) Latency and Delay Sensitivity

Existing systems face challenges with latency and delay sensitivity, impacting real-time applications and requiring optimization for swift data transmission.

(ii) Interference and Inter-Symbol Interference (ISI)

Systems contend with interference from various sources, complicating signal reception, and leading to inter-symbol interference, necessitating robust interference mitigation strategies.

(iii) High Power Consumption

Significant energy usage in devices and networks poses challenges, demanding efficient power management solutions to prolong battery life and enhance environmental sustainability

The proposed system aims to design a high-speed, energy-efficient error detection and correction code with minimal bit error rate for futuristic wireless communications. This innovative approach seeks to enhance the reliability and efficiency of data transmission in advanced wireless networks. By minimizing errors and optimizing energy consumption, it promises to significantly improve the performance and stability of future communication systems.

CHAPTER 4

PROPOSED SYSTEM

This chapter explains the proposed system architecture for error detection and correction codes. The scope of this project is to reduce the bit error rate with less delay, less power consumption and less area occupied. This can be achieved by Minimal Intricacy Parity Check Code (MIPC). The proposed architecture improves their error correction performance by an optimal error correction scheme.

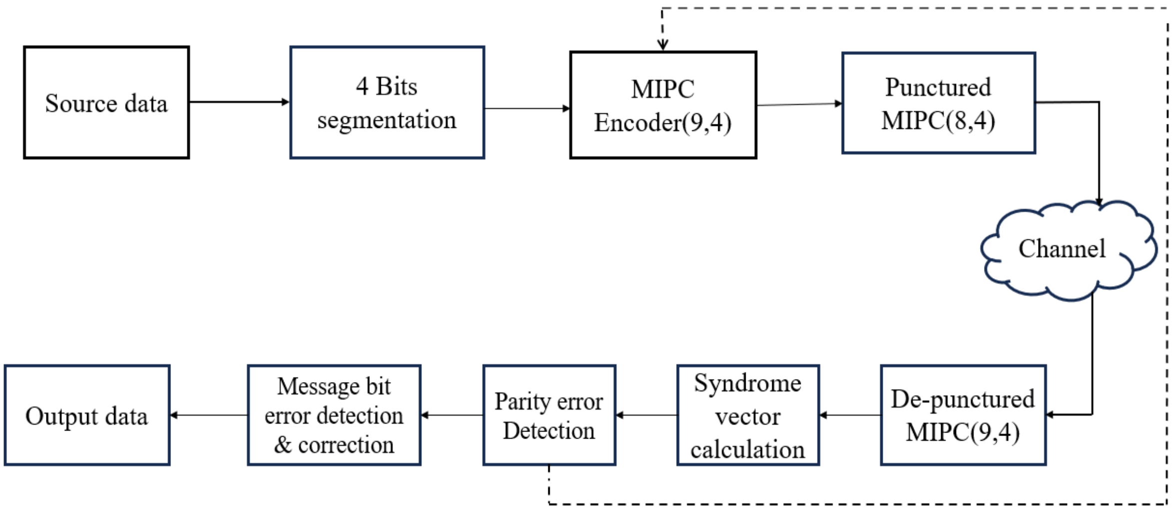

Figure 4.1 Minimal Intricacy Parity Check Code system

As shown in Figure 4.1, The source data undergoes segmentation in the segmentation block, where it is divided into four-bit segments. Subsequently, encoding occurs through the MIPC encoder, followed by the puncturing of data before transmission through the channel to the MIPC decoder. De-puncturing is performed prior to sending the data to the decoder, which comprises three sections. The first involves the calculation of the syndrome vector to determine the syndrome vector based on the received data and the parity check matrix.

In the second section, the emphasis is placed on the implementation of parity error detection mechanisms, which play a pivotal role in identifying and isolating errors within the received data through the meticulous application of parity checks. This stage involves the scrutiny of parity bits accompanying the data to detect any anomalies that may have occurred during transmission. Following this, the final section is exclusively dedicated to the intricate process of message bit error correction and detection. Here, the system meticulously locates and rectifies errors within the original message bits, ensuring the integrity and accuracy of the transmitted information. This sophisticated error correction mechanism guarantees a high level of reliability in data transmission. Post the decoding process in these sections, the output data is meticulously obtained, free from any potential errors that may have been introduced during the communication process. This comprehensive approach underscores the commitment to achieving data accuracy and reliability in the face of potential transmission errors.

The proposed Minimal Intricacy Parity Check Code is a error detection and correction code. On the transmitter side, the error detection and correction code(MIPC encoder (n, k)) encodes the input data and generates the code word. Puncturing is employed before transmitting through the channel. Due to the presence of noise, the information may become erroneous when delivered via a wireless channel. De-puncturing is employed before entering the decoder. The MIPC decoder receives the code word and uses a parity check matrix to calculate the syndrome vector on the receiver side. When the calculated syndrome vector equals to zero, that means there was no error in the received code word. If the syndrome vector is not zero, it means the received code word has been corrupted. The decoder will then compare the received code word to the calculated syndrome vector to check for parity mistakes. If no parity faults are found, the decoder will look for and correct flaws in the message bits.

4.1 MIPC Encoder

Breaking the original data stream into equal-length symbols is the first step in the MIPC encoding process (i.e., k bits). Then, for each symbol (k bits), a code word c is used to convert it to n bits, where n > k. The redundant bits for detecting and fixing faults are the n-k parity check bits. Before transmission, the proposed MIPC code separates the data stream into four-bit symbols (k) and then encodes each four-bit symbol into a nine-bit code word (n). The symbol for the original data stream is $SD_i = (m_1,m_2,m_3, \ldots .m_k)$, where $1 \leq i \leq j$, and j is the number of symbols in the source data, m is a binary bit, and k=4 is the symbol length. Before transmission, each k bit symbol is encoded into a n bit code word. The following shows the parity bit calculation.

$$P1 = M1 \oplus M2 \oplus M3 \tag{1}$$

$$P2 = M1 \oplus M2 \oplus M3 \oplus M4 \tag{2}$$

$$P3 = M1 \oplus M2 \oplus M4 \tag{3}$$

$$P4 = M2 \oplus M3 \oplus M4 \tag{4}$$

$$P5 = M3 \oplus M1 \oplus M4 \tag{5}$$

After encoding the code word would be given in Figure 4.2. Figure 4.4 shows the flow diagram of the proposed encoder.

M1	M2	M3	M4	P1	P2	P3	P4	P5

Figure 4.2 MIPC Code word

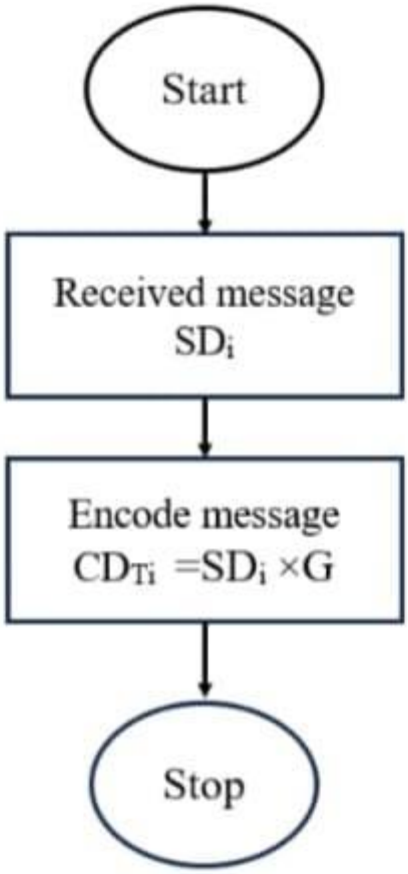

Figure 4.3 Flow chart for MIPC encoder

4.2 PROPOSED PUNCTURING AND DE-PUNCTURING TECHNIQUE

Puncturing is the process of removing some of the parity bits after encoding with an error-correction code. This has the same effect as encoding with an error-correction code with a higher rate, or less redundancy. However, with puncturing the same decoder can be used regardless of how many bits have been punctured. Thus, puncturing considerably increases the flexibility of the system without significantly increasing its complexity.

Table 4.1 Proposed Puncturing Technique

M1	M2	M3	M4	P1	P2	P3	P4	P5
0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1	1
0	0	1	0	1	1	0	1	1
0	0	1	1	1	0	1	0	0
0	1	0	0	1	1	1	1	0
0	1	0	1	1	0	0	0	1
0	1	1	0	0	0	1	0	1
0	1	1	1	0	1	0	1	0
1	0	0	0	1	1	1	0	1
1	0	0	1	1	0	0	1	0
1	0	1	0	0	0	1	1	0
1	0	1	1	0	1	0	0	1
1	1	0	0	0	0	0	1	1
1	1	0	1	0	1	1	0	0
1	1	1	0	1	1	0	0	0
1	1	1	1	1	0	1	1	1

Table 4.1 depicts the proposed puncturing process. The code word of 9 bits is reduced to 8 bits by puncturing the M4 bit. The de-puncturing technique is done by taking XOR between P1 and P2. It is found from the Table 4.2 that the M4 bit can be recovered from the P1 and P2 parity bits thereby producing the output of 8 bits.

Table 4.2 Proposed De-puncturing Technique

M4	P1	P2
0	0	0
1	0	1
0	1	1
1	1	0
0	1	1
1	1	0
0	0	0
1	0	1
0	1	1
1	1	0
0	0	0
1	0	1
0	0	0
1	0	1
0	1	1
1	1	0

De-puncturing is the process of retrieving the parity bits. This action effectively reverses the effect of puncturing, increasing redundancy and potentially improving the code rate. De-puncturing allows for greater flexibility in the system while maintaining the use of the same decoder, without substantially increasing complexity.

4.3 MIPC Decoder

The main purpose of this proposed MIPC decoder is to lower the bit error rate during wireless transmission. Only one-bit errors are corrected by a single error correction hamming code. The MIPC code has been proposed for the detection and repair of all bit defects in message bits at the receiver end, in order to improve its dependability. The message bits of length 4 will be broadcast as 7 bits in (7,4) Hamming coding, with 3 superfluous parity bits attached, and it can only rectify single-bit errors. The size (9,4) MIPC code will detect 9 bits and correct up to 4 bits of error, with a message bit length of four bits. There are three phases to MIPC decoding.

(i) Syndrome vector calculation

The syndrome vector (SY1, SY2, SY3, SY4, SY5) is generated in the first stage. This is achieved using code word at the receiver end. It follows the same XOR operation used in the encoder. The syndrome vector is calculated by

$$SY = H \times CD \tag{6}$$

Let the received code word be (CD1, CD2, ……..,CD9)

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{7}$$

Let the syndrome vector be parity of 0,1,2,3,4,5 (SY1,SY2,SY3,SY4,SY5)

In syndrome vector calculation, the focus lies on determining the parity bits associated with the intended message bits. This process involves utilizing a parity check matrix to assess errors and facilitate error correction. By computing the syndrome vector, deviations from the intended message can be identified, enabling efficient error detection and correction mechanisms. Depending on the severity of errors, retransmission protocols may be initiated to ensure accurate message transmission. Through this systematic approach, the integrity of the transmitted data is upheld, ensuring reliable communication channels.

The Figure 4.5 represents the Flow Chart of Minimal Intricacy Parity Check Code Decoder for puncturing and de-puncturing the received code bits. The received code bits, possibly corrupted during transmission. Using the syndrome information, the decoder performs error correction to correct any detected errors in the received code sequence. This process may involve iterative decoding algorithms designed for Minimal Intricacy Parity Check Code Decoder codes.

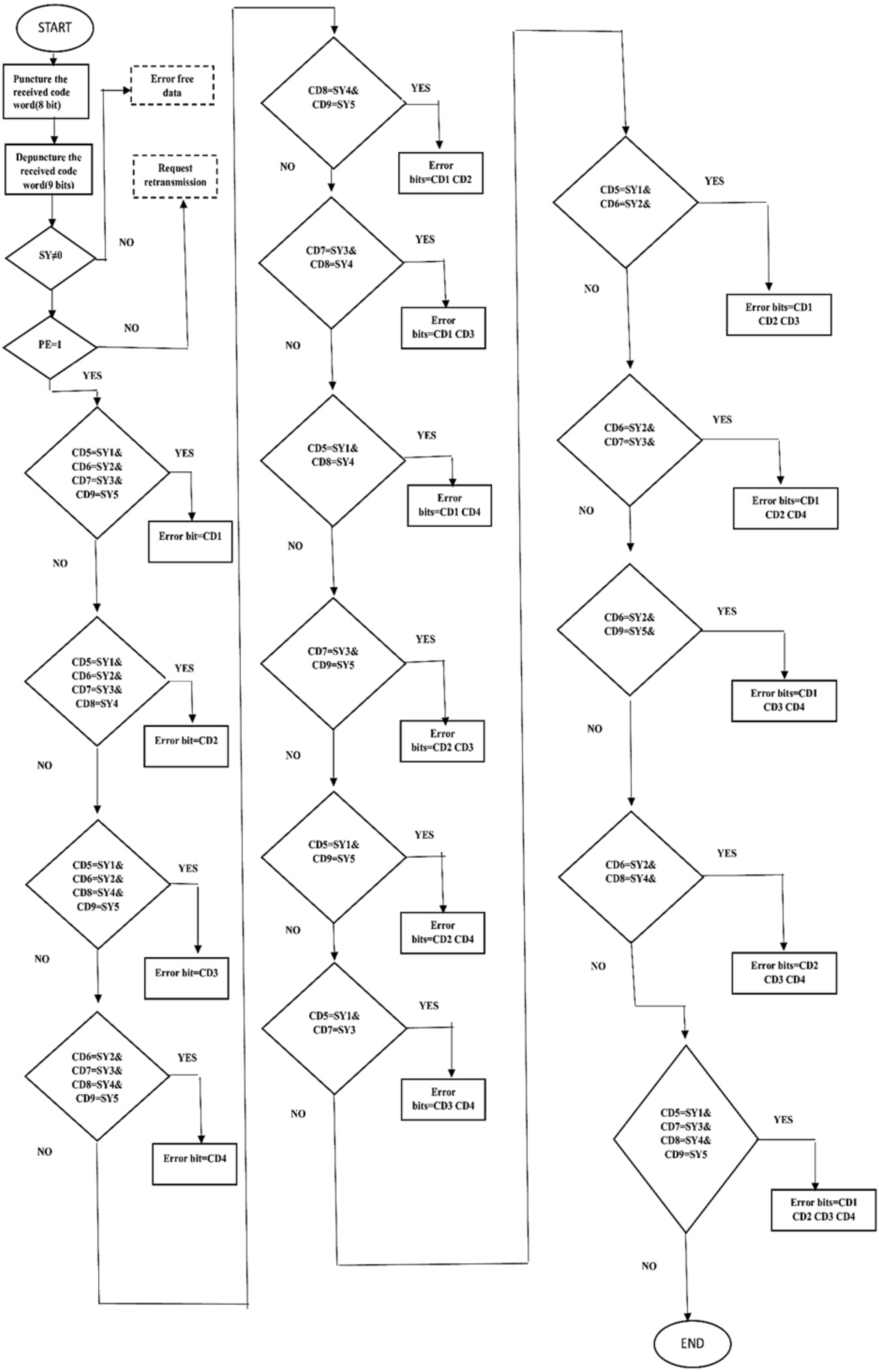

Figure 4.4 Flow chart for MIPC Decoder

(ii) Parity error detection

The second stage entails detecting errors in parity bits. This is accomplished using the following equation.

$$PE = (SY1 \odot P1)(SY2 \odot P2)(SY3 \odot P3)$$

$$(SY4 \odot P4)(SY5 \odot P5) \quad (8)$$

Where SY1 $= CD1 \oplus CD2 \oplus CD3$ (9)

SY2 $= CD1 \oplus CD2 \oplus CD3 \oplus CD4$ (10)

SY3 $= CD1 \oplus CD2 \oplus CD4$ (11)

SY4 $= CD2 \oplus CD3 \oplus CD4$ (12)

SY5 $= CD3 \oplus CD1 \oplus CD4$ (13)

If PE=1, it indicates that no errors in parity bits and if PE$\neq 1$, it indicates that parity error exists. Therefore, the decoder request retransmission by sending HARQ signal.

(iii) Message error detection and correction

The third stage entails detecting and automatically repairing any faults found in message bits. This is accomplished using the following equations. Equation (1), (2), (3) and (4) are used to detect and correct single bit error (Errorcorrect1), double bit error (Errorcorrect2), triple bit error (Errorcorrect3) and four-bit error (Errorcorrect4) in the message bit respectively.

$$Errorcorrect1=\{\sim CD1,CD2,CD3,CD4\}*\{CD5\oplus SY1\}.\{CD6\oplus SY2\}.\{CD7\oplus SY3\}.\{CD9\oplus SY5\}+\{CD1,\sim CD2,CD3,CD4\}*\{CD5\oplus SY1\}.\{CD6\oplus SY2\}.\{CD7\oplus SY3\}.\{CD8\oplus SY4\}+\{CD1,CD2,\sim CD3,CD4\}*\{CD5\oplus SY1\}.\{CD6\oplus SY2\}.\{CD8\oplus SY4\}.\{CD9\oplus SY5\}+\{CD1,CD2,CD3,\sim CD4\}*\{CD6\oplus SY2\}.\{CD7\oplus SY3\}.\{CD8\oplus SY4\}.\{CD9\oplus SY5\} \quad (14)$$

$$Errorcorrect2=\overline{Errorcorrect1}*\{\sim CD1,\sim CD2,CD3,CD4\}*\{CD8\oplus SY4\}.\{CD9\oplus SY5\}+\overline{Errorcorrect1}*\{\sim CD1,CD2,\sim CD3,CD4\}*\{CD7\oplus SY3\}.\{CD8\oplus SY4\}+\overline{Errorcorrect1}*\{\sim CD1,CD2,CD3,\sim CD4\}*\{CD5\oplus SY1\}.\{CD8\oplus SY4\}+\overline{Errorcorrect1}*\{CD1,\sim CD2,\sim CD3,CD4\}*\{CD7\oplus SY3\}.\{CD9\oplus SY5\}+\overline{Errorcorrect1}*\{CD1,\sim CD2,CD3,\sim CD4\}*\{CD5\oplus SY1\}.\{CD9\oplus SY5\}+\overline{Errorcorrect1}*\{CD1,CD2,\sim CD3,\sim CD4\}*\{CD5\oplus SY1\}.\{CD7\oplus SY3\} \quad (15)$$

$$Errorcorrect3=\overline{Errorcorrect2}*\{\sim CD1,\sim CD2,\sim CD3,CD4\}*\{CD5\oplus SY1\}.\{CD6\oplus SY2\}+\overline{Errorcorrect2}*\{\sim CD1,\sim CD2,CD3,\sim CD4\}*\{CD6\oplus SY2\}.\{CD7\oplus SY3\}+\overline{Errorcorrect2}*\{\sim CD1,CD2,\sim CD3,\sim CD4\}*\{CD6\oplus SY2\}.\{CD9\oplus SY5\}+\overline{Errorcorrect2}*\{CD1,\sim CD2,\sim CD3,\sim CD4\}*\{CD6\oplus SY2\}.\{CD8\oplus SY4\} \quad (16)$$

$$Errorcorrect4=\overline{Errorcorrect3}*\{\sim CD1,\sim CD2,\sim CD3,\sim CD4\}*\{CD5\oplus SY1\}.\{CD7\oplus SY3\}.\{CD8\oplus SY4\}.\{CD9\oplus SY5\} \quad (17)$$

4.4 BIT OVERHEAD

Bit Overhead Bit overhead refers to the additional bits added to the original data for error correction purposes. These extra bits increase the overall size of the transmitted data, impacting bandwidth utilization and efficiency. However, they are necessary to implement error correction codes effectively. With four data bits and four parity bits, the calculation results in a bit overhead of one. This means that for every four data bits, one parity bit is included in the transmission for error correction.

$$\text{Bit Overhead}=\frac{\text{Number of Parity Bits}}{\text{Number of Data Bits}}=\frac{4}{4}=1 \tag{18}$$

4.5 HAMMING DISTANCE

Hamming Distance Hamming distance is a measure of the difference between two binary strings of equal length. In the context of error correction codes, it represents the minimum number of bit changes required to convert one valid codeword into another valid codeword. A higher Hamming distance implies greater error detection and correction capability since it allows for more robust error detection and correction.

$$d_{min} \leq \text{n-k+1} \tag{19}$$

$$d_{min} \leq 9\text{-}4\text{+}1 \tag{20}$$

$$d_{min} \leq 6 \tag{21}$$

Therefore, the proposed MIPC code detects 5 bits error and corrects upto 4-bit errors.

4.6 CODE RATE

Code Rate The code rate of an error correction code represents the ratio of the number of information bits to the total number of bits in a codeword. A higher code rate indicates that a larger portion of the transmitted data consists of actual information, reducing the overhead associated with error correction. However, higher code rates typically come at the expense of error correction capability, as fewer redundant bits are available for error detection and correction. With 4 data bits and 8 codeword, the calculation results in a code rate of 0.5.

$$\text{Code Rate} = \frac{\text{Number of Data Bits}}{\text{Number of Codeword}} = \frac{4}{8} = 0.5 \tag{22}$$

Error correction capability refers to the ability of an error correction code to detect and correct errors in the transmitted data. This capability is influenced by factors such as the Hamming distance and code rate. Codes with higher Hamming distances and lower code rates tend to have better error correction capabilities since they can detect and correct a greater number of errors. However, achieving a balance between code rate, overhead, and error correction capability is crucial in designing efficient error correction systems.

Table 4.3 Error Correction Code

ERROR CORRECTION CODE	DATA BITS	PARITY BITS	CODEWORD LENGTH	BIT OVERHEAD	CODE RATE
Hamming Code	32	6	38	0.1875	0.8421
Golay Code	32	31	63	0.9688	0.5079
BCH Code	32	31	63	0.9688	0.5079
LCPC Code	32	40	72	1.25	0.4444
MIPC Code	32	32	64	1	0.5

In Table 4.3 represents the table of different error correction codes, such as Hamming, Golay, Bose-Chaudhuri-Hocquenghem, Low Complexity Parity Check, and Minimal Intricacy Parity Check, offer distinct configurations for various applications. For instance, the Hamming code employs 32 data bits and 6 parity bits, resulting in a codeword length of 38 with a minimal bit overhead of 0.1875 and a code rate of 0.8421. The Golay code utilizes 32 data bits and 31 parity bits, creating codewords of length 63 with a bit overhead of 0.9688 and a code rate of 0.5079. The Bose-Chaudhuri-Hocquenghem code features 32 data bits and 31 parity bits, maintaining a codeword length of 63 with identical bit overhead and code rate as the Golay code. The low complexity parity check code incorporates 32 data bits and 40 parity bits, resulting in codewords of length 72 with a bit overhead of 1.25 and a code rate of 0.4444. Lastly, the minimal intricacy parity check code employs 32 data bits and 32 parity bits, generating codewords of length 64 with a bit overhead of 1 and a code rate of 0.5.

These are the various parameters in error correction across different communication systems and scenarios.

4.6 ADVANTAGES

(i) Addressing Challenges of Futuristic Wireless Networks The paper acknowledges the challenges inherent in futuristic wireless networks such as unreliable links, interference, noisy channels, and frequent topology changes. By proposing MIPC codes, the paper aims to mitigate these challenges effectively.

(ii) Comparison with Existing Coding Schemes The paper compares LCPC codes with other well-known error detection and correction codes such as Hamming, Reed-Solomon (RS), and Low-Density Parity Check (LDPC) codes. The simulation results demonstrate the superiority of LCPC codes, offering up to 3 dB coding gain over these existing schemes.

(iii) Lower Memory Requirement MIPC codes are claimed to have lower memory requirements compared to Turbo and LDPC codes. This is an advantage, especially in scenarios where memory resources are limited, such as embedded systems or IoT devices.

(iv) Performance Improvement The proposed MIPC codes outperform traditional error correction codes such as Hamming and Reed-Solomon codes, as well as the widely used LDPC codes. This indicates a significant performance improvement in terms of error detection and correction capabilities.

CHAPTER 5

RESULTS AND DISCUSSION

The performance of the proposed Minimal Intricacy Parity Check Codes is analysed in terms of power consumption, propagation delay, and area consumption. The proposed codes are simulated using Xilinx and Cadence 90 nm technology. The Bit Error Rate with respect to its propagated signal power are also analysed using MATLAB.

5.1 MODULE DESCRIPTION

The overall project in divided into the following modules.

Module 1: Design of MIPC Encoder.
Module 2: Design of Puncturing.
Module 3: Design of De puncturing.
Module 4: Design of MIPC Decoder.
Module 5: Power, Area and Delay Analysis.
Module 6: BER Analysis.

In Module 1, the input to the MIPC Encoder consists of message bits of size 32 divided into 8 chunks, each comprising 4 bits. This results in a 72-bit codeword, with each chunk containing 9 bits. To optimize the code rate, puncturing is implemented in Module 2, reducing the 72 bits to 64 bits. The modulated code word is then transmitted over the AWGN channel using BPSK modulation. In Module 3, before the code word reaches the decoder at the receiver side, depuncturing of the punctured bits occurs by retrieving the bits. Module 4 involves decoding the received code word using the MIPC decoder, which decodes the 72 bits into 32 bits divided into 8 chunks. The MIPC decoder process is divided into three stages, including syndrome vector calculation, parity error detection, and message error detection & correction. Module 5 measures power consumption, area utilization, and propagation delay using Cadence 90nm technology, conducting a comparative analysis against existing codes. Module 6 performs BER analysis using MATLAB.

The transmitter side output such as Module 1 and Module 2 are shown in Figure 5.1 and Figure 5.2 respectively. The receiver side output such as Module 3 and Module 4 are shown in Figure 5.3 and Figure5.4(a,b,c,d) respectively. The overall implementation output and its RTL schematic is shown in Figure 5.5 and Figure 5.6 respectively. The results of Module 5 is tabulated in Table 5.1 and the BER analysis done in Module 6 is shown in Figure 5.10.

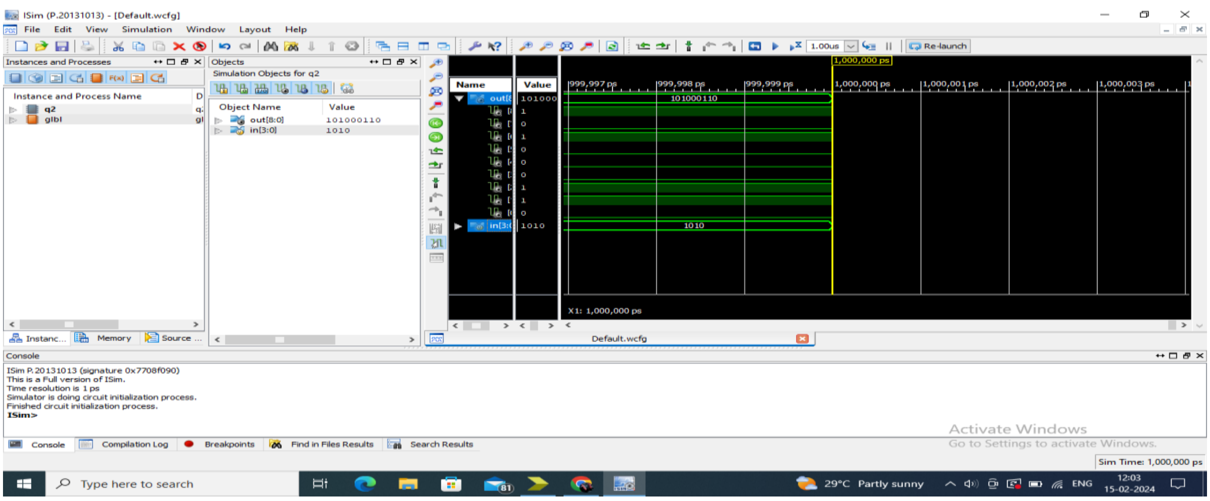

Figure 5.1: Minimal Intricacy Parity Check Encoder output

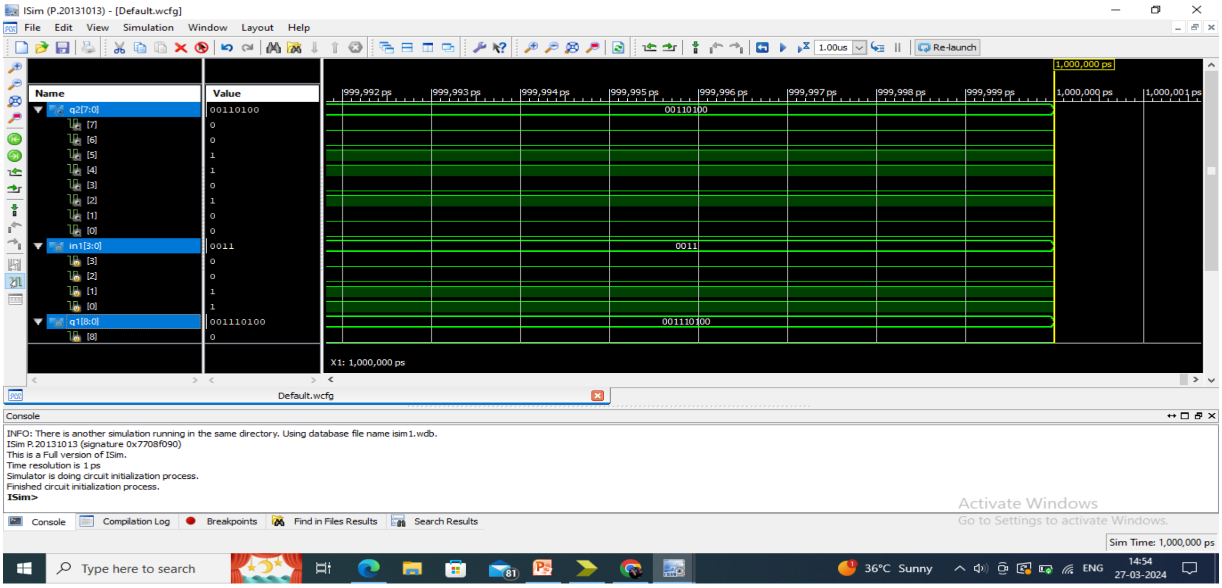

Figure 5.2: Punctured Minimal Intricacy Parity Check Encoder output

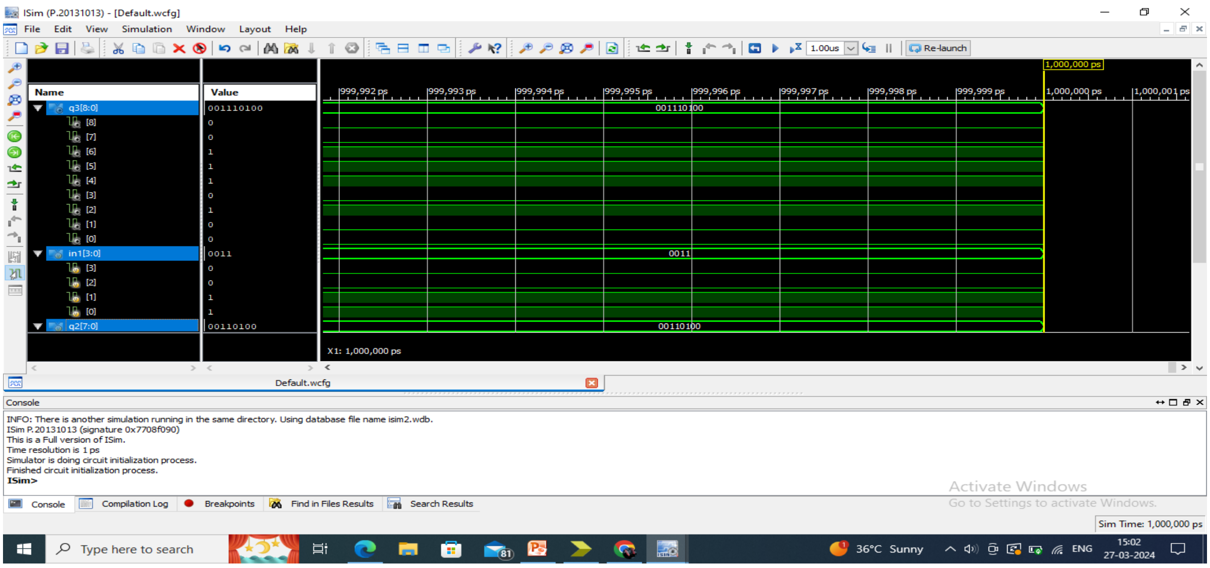

Figure 5.3 De-Punctured Minimal Intricacy Parity Check Decoder output

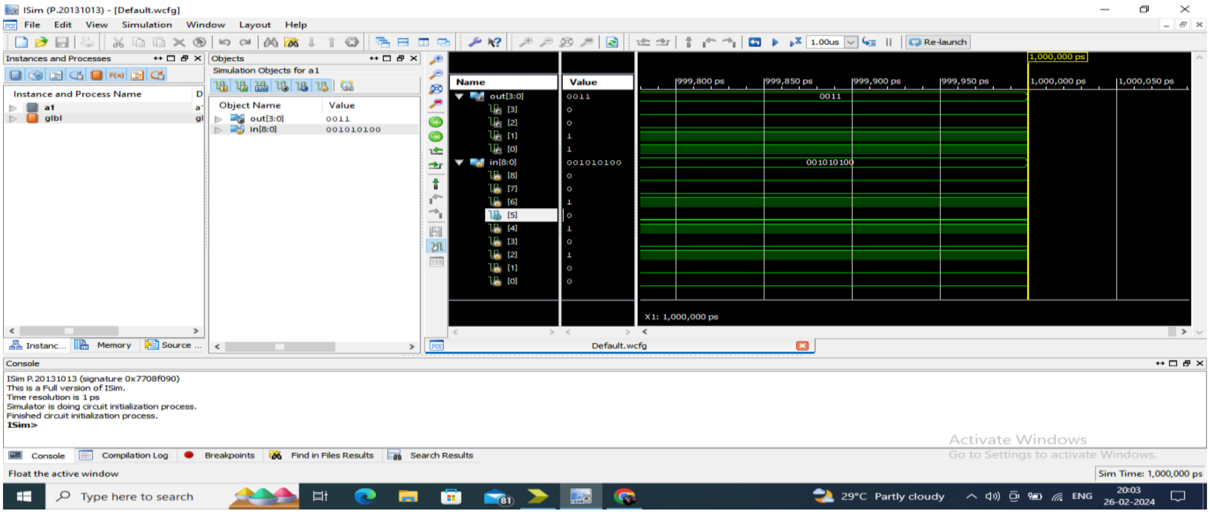

Figure 5.4(a) Minimal Intricacy Parity Check Decoder output (Single bit error Correction)

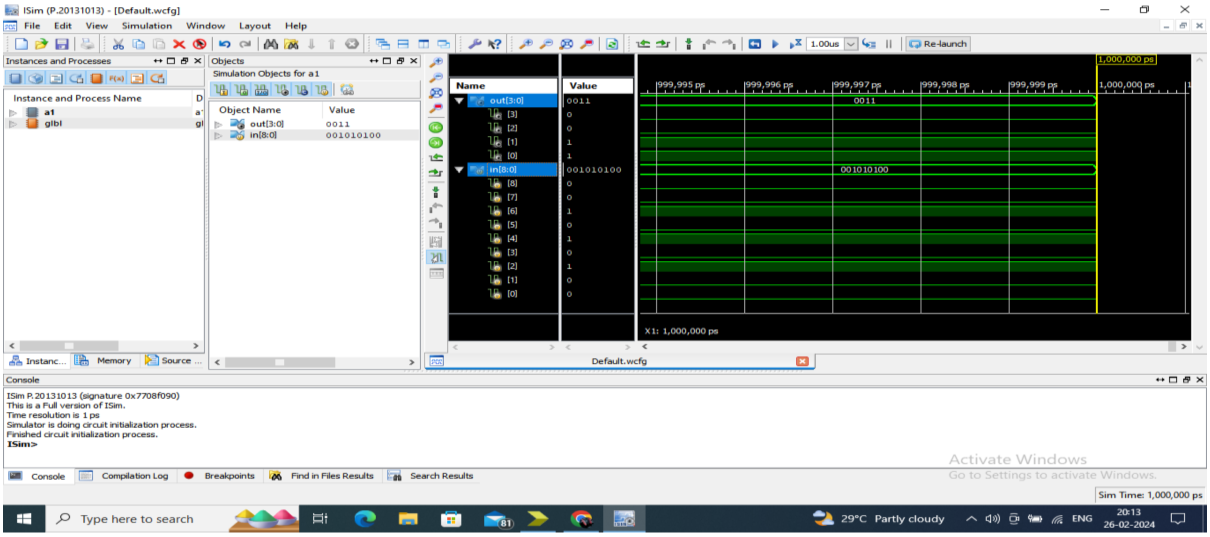

Figure 5.4(b) Minimal Intricacy Parity Check Decoder output (Double bit error Correction)

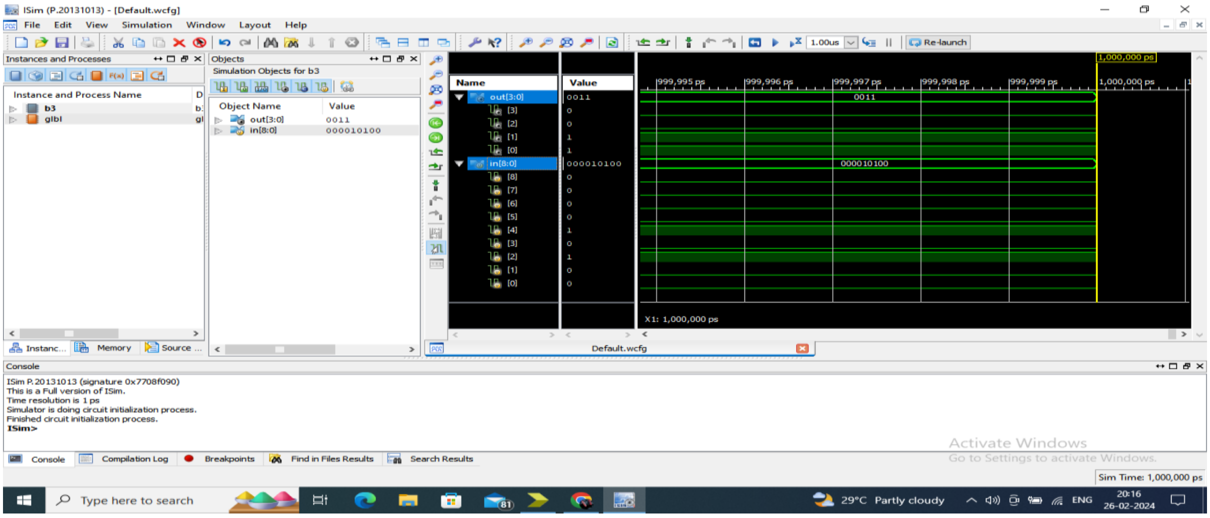

Figure 5.4(c) Minimal Intricacy Parity Check Decoder output (Triple bit error Correction)

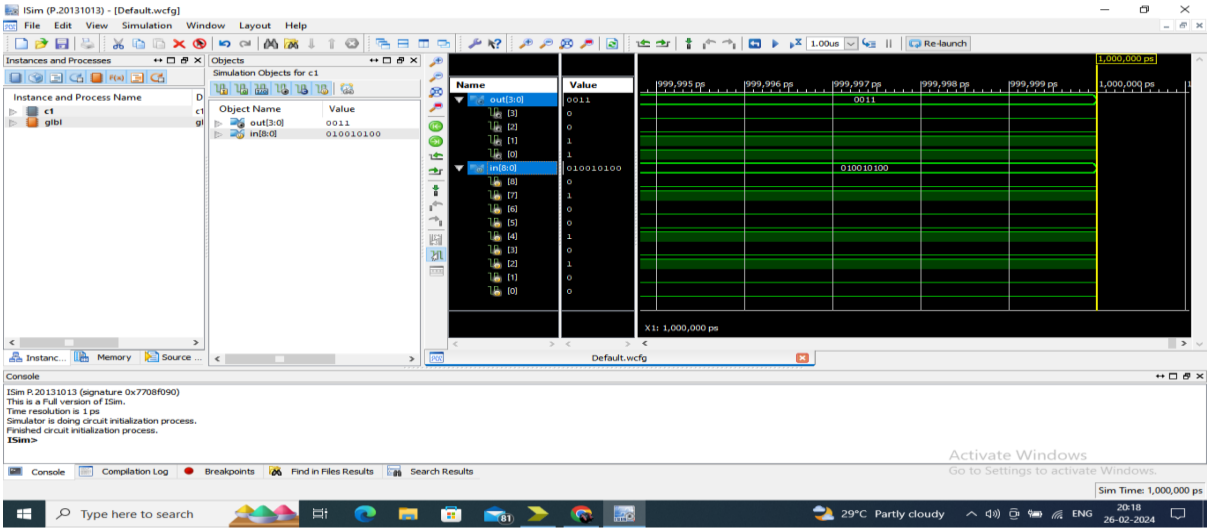

Figure 5.4(d) Minimal Intricacy Parity Check Decoder output (Four bit error Correction)

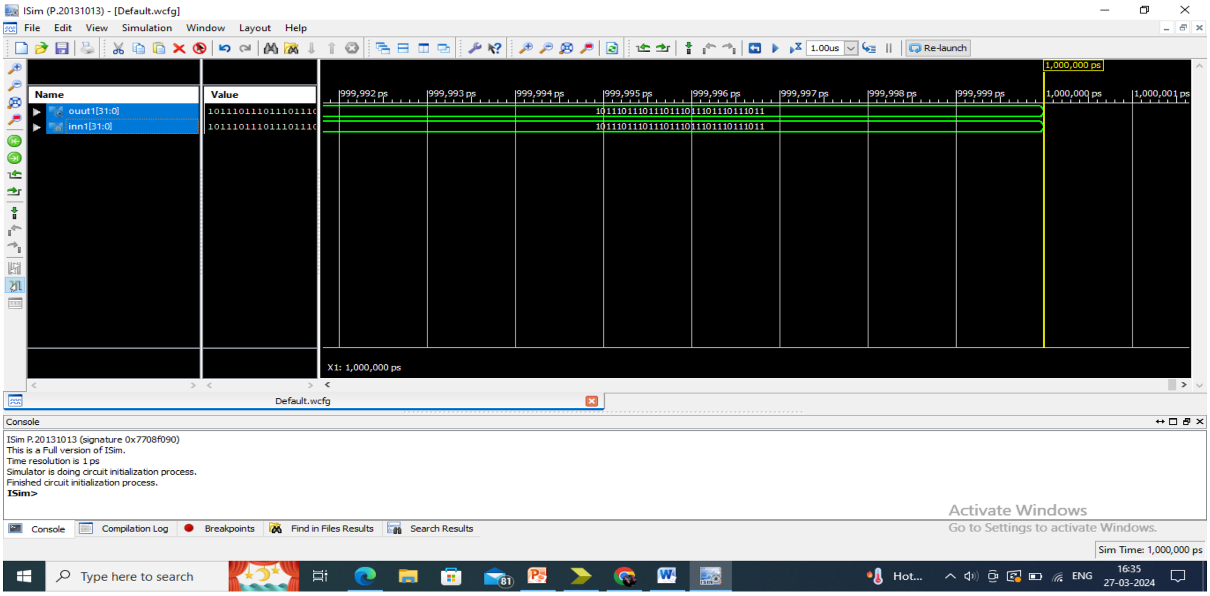

Figure 5.5 Minimal Intricacy Parity Check Code Output

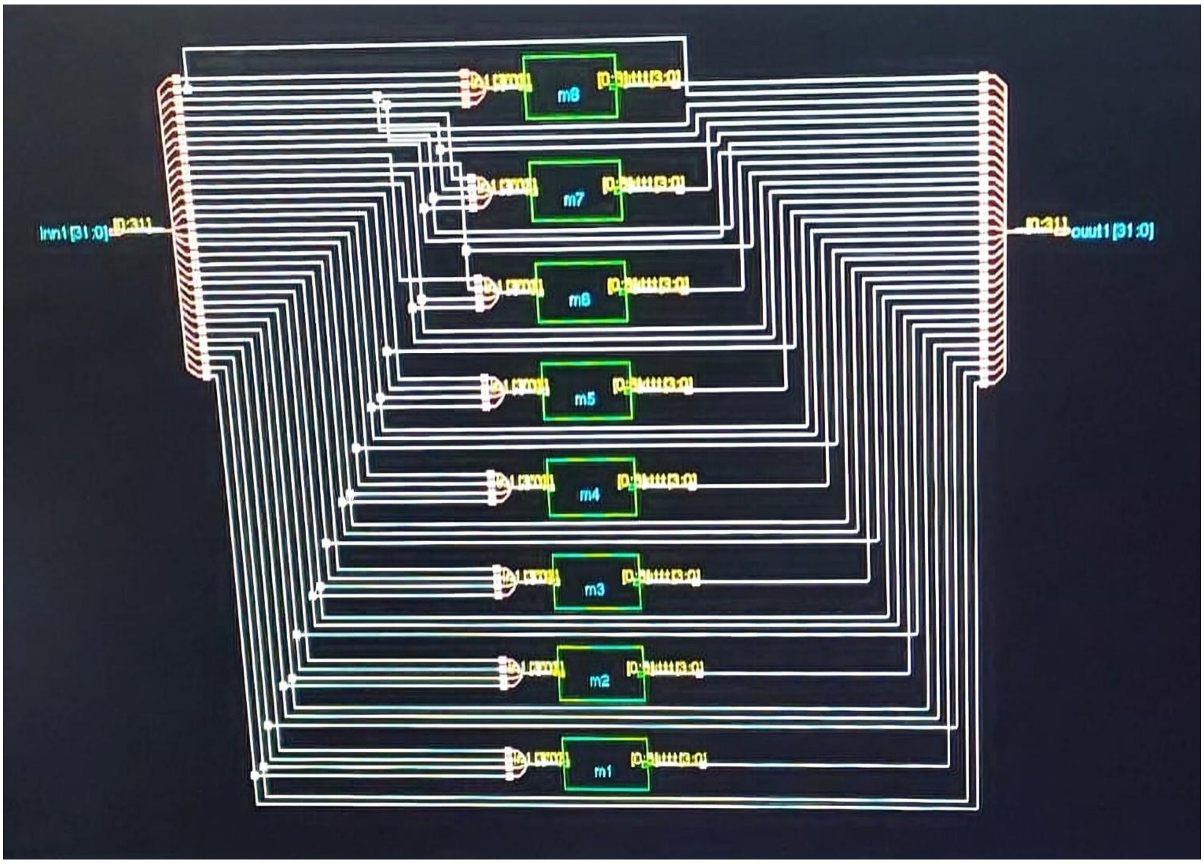

Figure 5.6 RTL Schematic of Minimal Intricacy Parity Check Code

The proposed error correction code is simulated using Cadence 90 nm technology and its performance evaluation matrices such as power consumption, area, and propagation delay are measured. Table 5.1 depicts the comparison of performance evaluation matrices of various Code architectures.

Table 5.1 Comparative Analysis

CODE	POWER CONSUMPTION(μW)	AREA (μm^2)	DELAY (nS)
Hamming code (38,32)	152.2	1080.1	0.705
Golay code (63,32)	235.7	3655.2	1.72
BCH code (63,32)	268.9	4067.5	1.9
LCPC code (72,32)	221.8	3537.6	1.63
MIPC code (64,32)	136.175	2262	0.943

Figure 5.7 shows the power comparison chart of various existing code architectures and proposed MIPC code architecture. Figure.5.8 and Figure 5.9 depicts the comparative analysis of Area and Delay. The proposed MIPC architecture presents significant enhancements across various existing coding structures. In comparison to the Golay code architecture, it achieves notable reductions of 42.22%, 38.11%, and 45.17% in power consumption, area utilization, and delay, respectively. Conversely, when contrasted with the Hamming code, the MIPC architecture sees an increase of 109.425% in area consumption and 33.75% in delay, alongside a favorable decrease of 10.53% in

power consumption. Moreover, in relation to the BCH code architecture, it showcases decreases of 49.36%, 44.39%, and 50.37% in power consumption, area utilization, and delay, respectively. Similarly, compared to the LCPC code architecture, it demonstrates declines of 38.60%, 36.06%, and 42.14% in power consumption, area usage, and delay, respectively. These findings underscore the hardware-friendly attributes of the proposed Channel coding scheme, rendering it well-suited for next-generation wire communication systems.

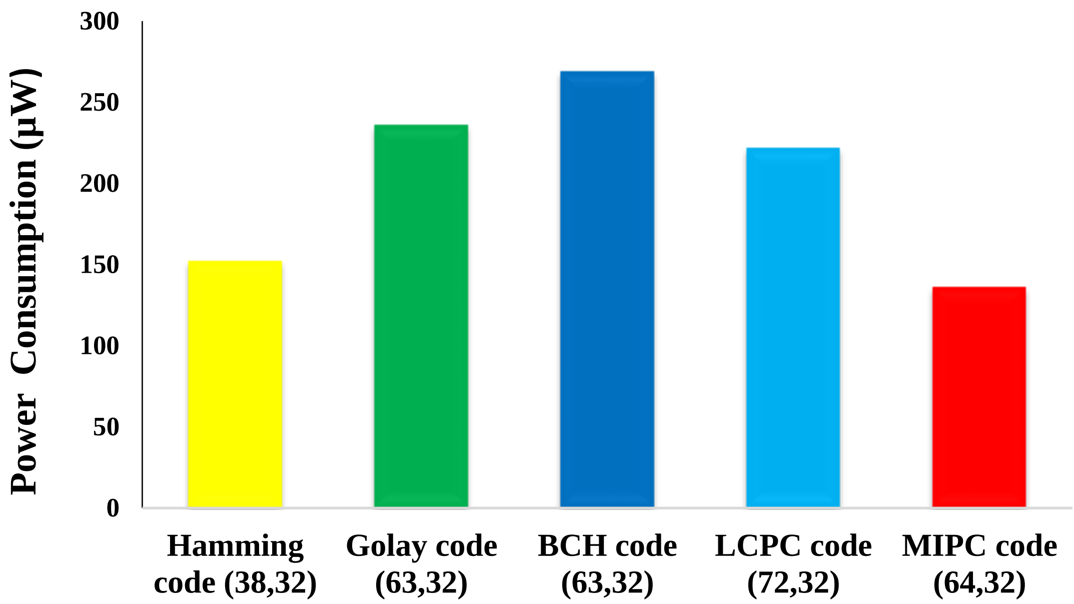

Figure 5.7 Power analysis

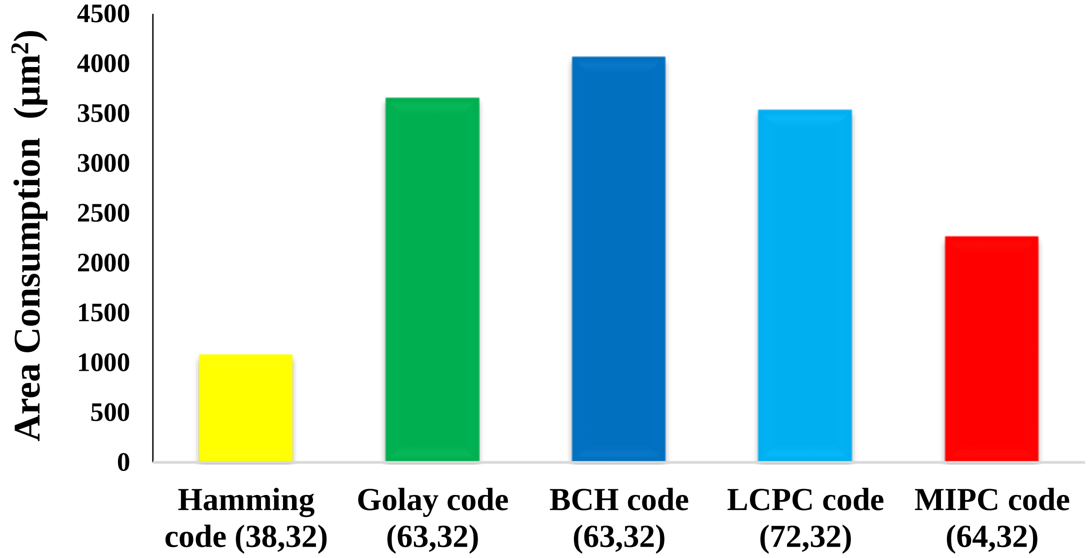

Figure 5.8 Area analysis

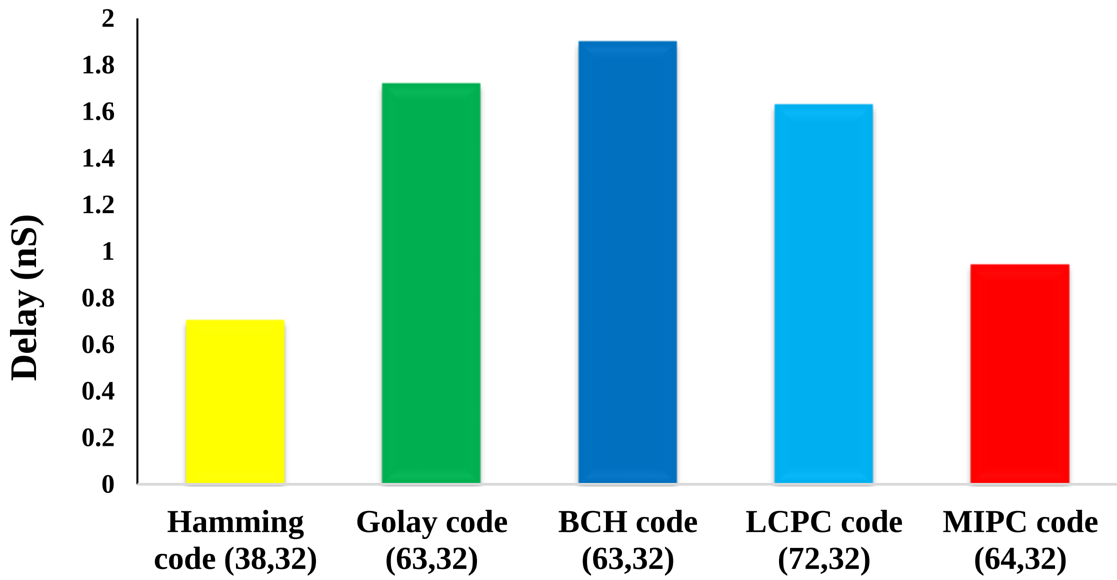

Figure 5.9 Delay analysis

(ii) BIT ERROR RATE ANALYSIS

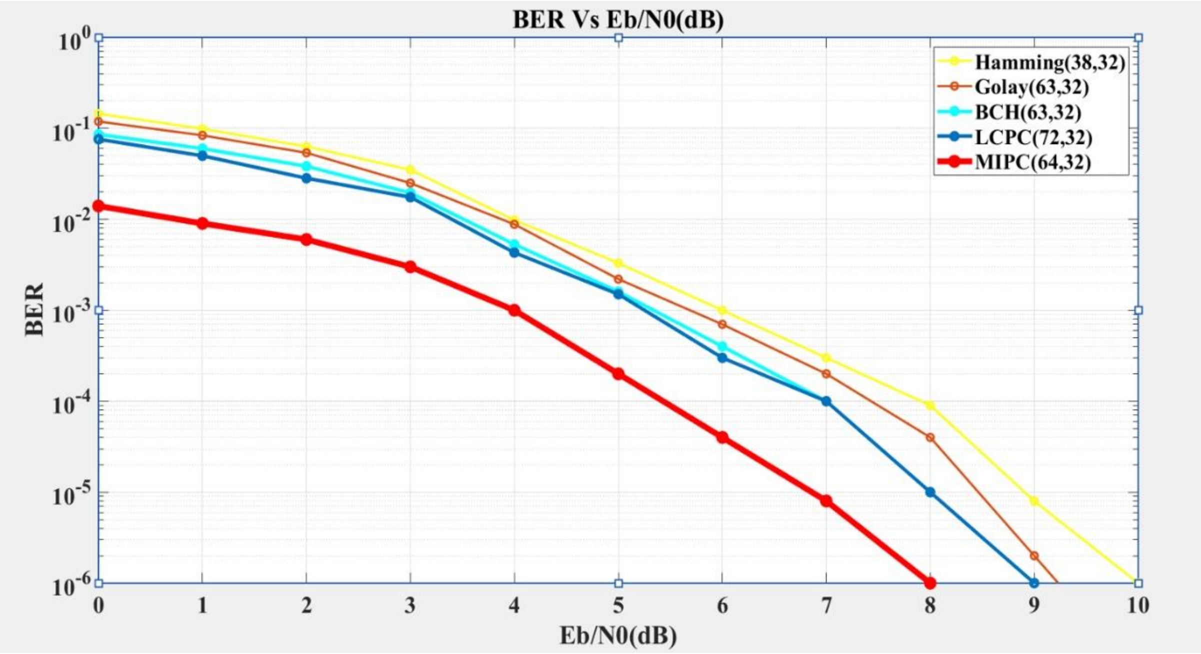

Figure 5.10 BER VS SNR through BPSK modulation over AWGN Channel

Compared to the other error correcting codes in the literature, the proposed MIPC code performs well, which is observed in Figure 5.10. While the Hamming code (38,32) can deliver BER = 0.0631 at the SNR of 2 dB, the MIPC code can deliver BER = 0.006 at the same SNR. The proposed MIPC code (64,32) has a reduction in BER of 90.49 % to the Hamming code (38,32) at a 2 dB Gain. It is also observed from figure that the proposed MIPC code (64,32) has a reduction in BER of 88.84 %, 84.33 % and 78.79 % to the Golay code (63,32), BCH code (63,32) and LCPC code (72,32) respectively at 2 dB.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

The systematic analysis of Minimal Intricacy Parity Check Codes (MIPC) is presented in this work. The analysis revealed that the proposed MIPC architecture consume less power, occupy less area, and operate at a higher speed when compared with other error correcting codes. The reason behind this lesser hardware complexity lies in the optimal error correction code method. With fewer hardware requirements, this MIPC can detect and correct the greatest number of errors that occurred during transmission. This effective error correction scheme leads to less complexity, less delay, less power and area consumption, and improved BER performance. This project concludes that the MIPC architecture will be the suitable error correction code for next-generation wireless communication.

6.2 FUTURE SCOPE

The deployment of interleaved codes can improve the Bit Error Rate further. The Bit Error Rate can also be improved by the implementation of the Minimal Intricacy Parity Check Code that further detects and correct parity bits as well.

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