**Multiplexer 4:1 using dataflow Model**

1. **Code**

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity mux\_data is

Port ( a,b,c,d : in STD\_LOGIC;

s : In STD\_LOGIC\_VECTOR(1 Downto 0);

y : out STD\_LOGIC);

end mux\_data;

architecture Dataflow of mux\_data is

begin

Y<= a WHEN S(1)='0' AND S(0)='0' ELSE

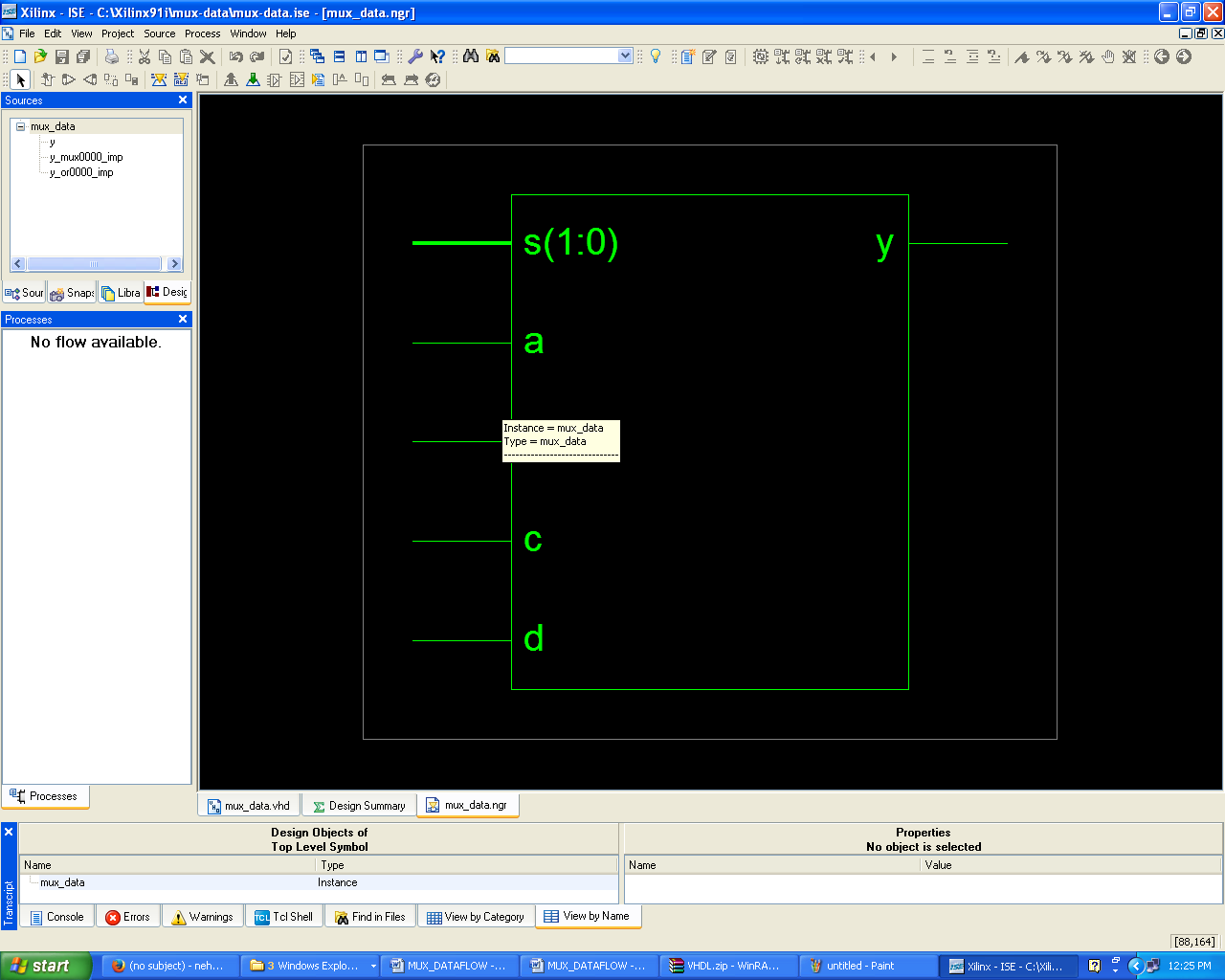
b WHEN S(1)='0' AND S(0)='1' ELSE

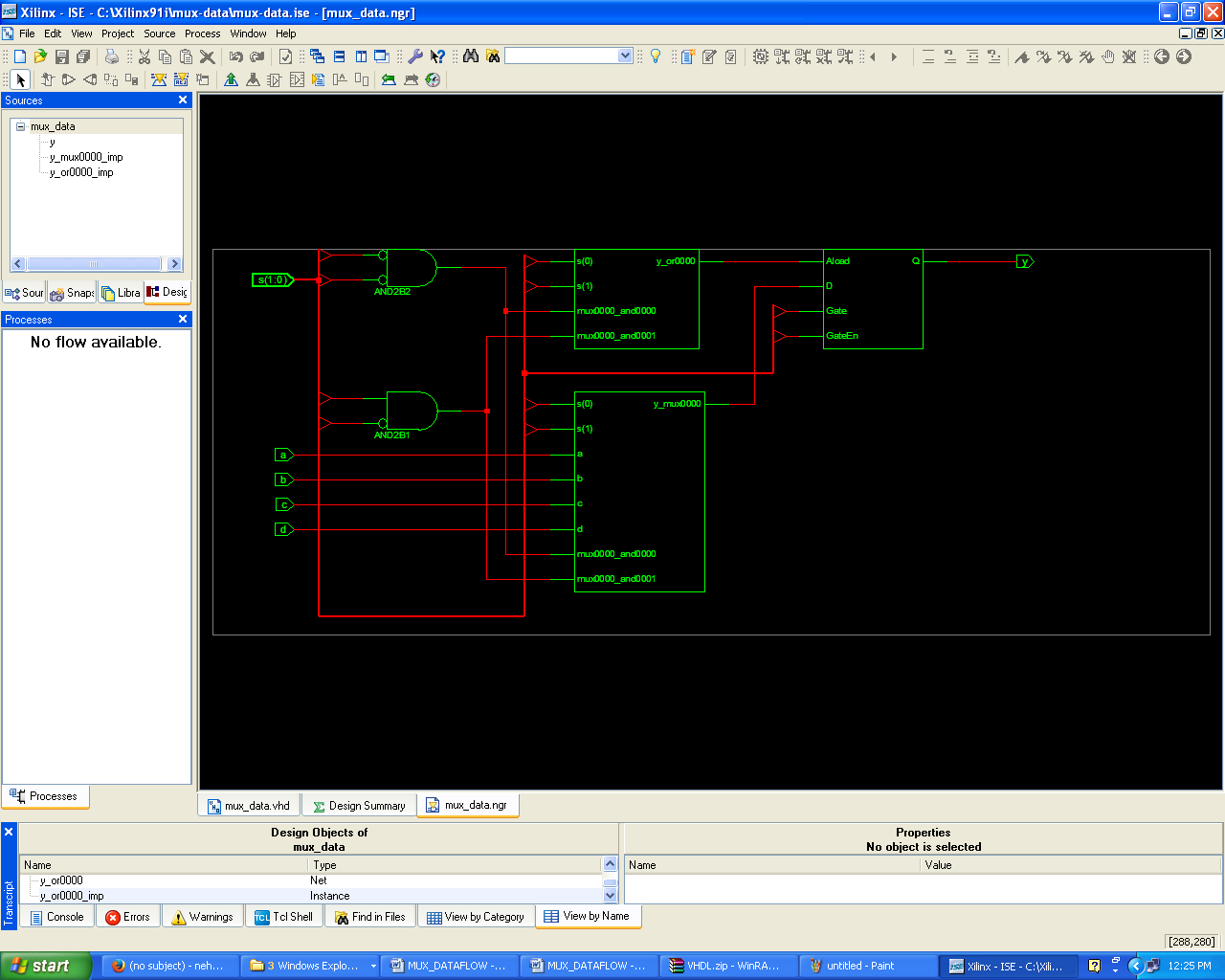
c WHEN S(1)='1' AND S(0)='0' ELSE

d WHEN S(1)='1' AND S(0)='1' ;

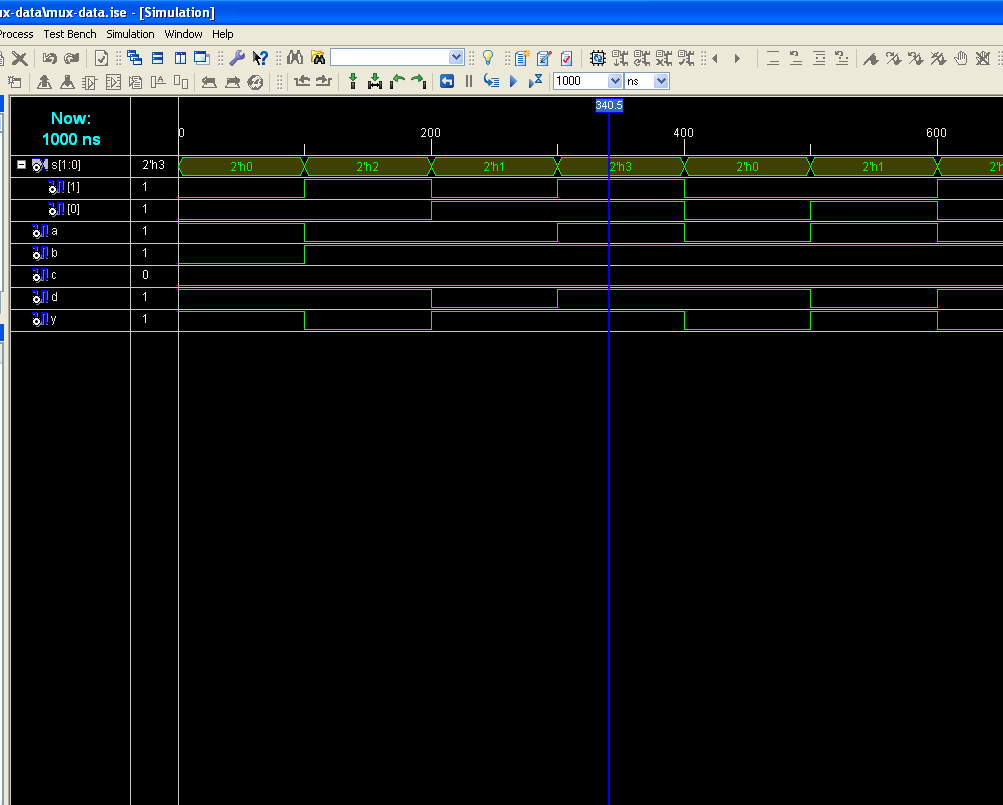
end dataflow;

1. **RTL Schematic**

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1. **Simulation Output**

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