LIST OF EXPERIMENTS:

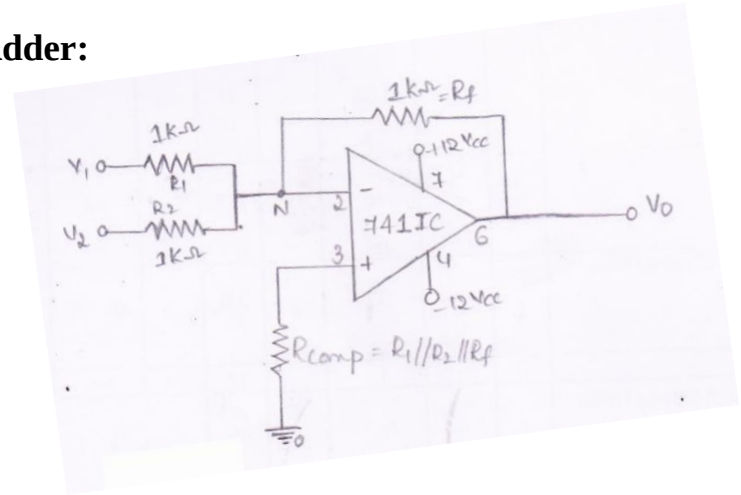
1. Construct basic Applications of Op-Amp-Adder, Subtractor, and Comparator Circuit.
2. Design of an Integrator and Differentiator Circuit using Op-Amp IC 741.
3. Construct Waveform Generator using single Op-Amp with variable Duty Cycle.
4. Design Schmitt Trigger Circuit using Single Op-Amp with Reference Voltage.
5. Design a Function Generator using Op-Amp.
6. Design an Active Filters 1- LPF,HPF (first order) using Op-Amp IC 741.
7. Design an Active Filters 2-BPF, Band reject (Wideband) and Notch Filters using Op-Amp IC 741.
8. Construct Astable Multivibrator using IC 555 Timer.
9. Construct Monostable Multivibrator using IC 555 Timer.
10. Evaluate Capture range and Lock range Using PLL IC 565.

Augmented Experiments:

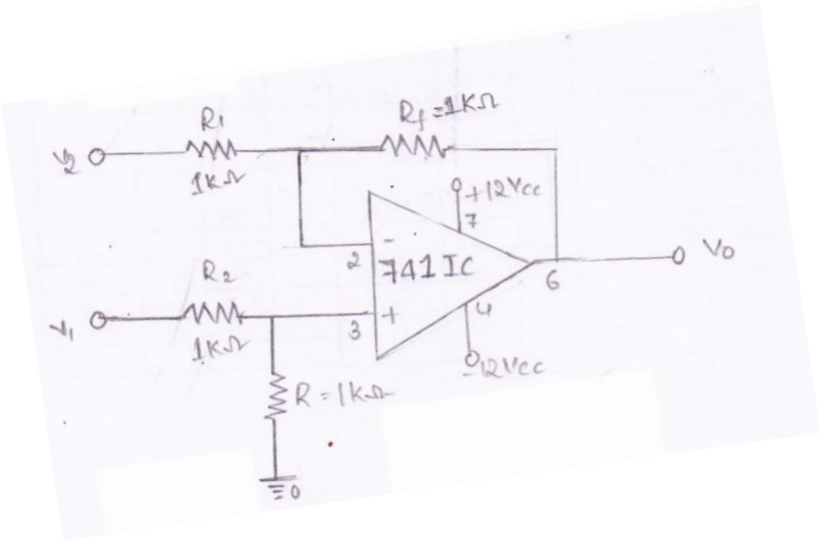
1. Design a 4 bit R-2R Ladder Network with Op-Amp Buffer and measure the Output Waveform for various Input combinations.
2. Digital of Oscillator Circuits - Phase Shift and Wien Bridge Oscillators using Op-Amp IC 741.
3. Design of Dual Power Supply Using 78XX and 79XX and Full Wave Bridge Rectifier with Shunt Capacitance Filters.

CIRCUIT DIAGRAMS:

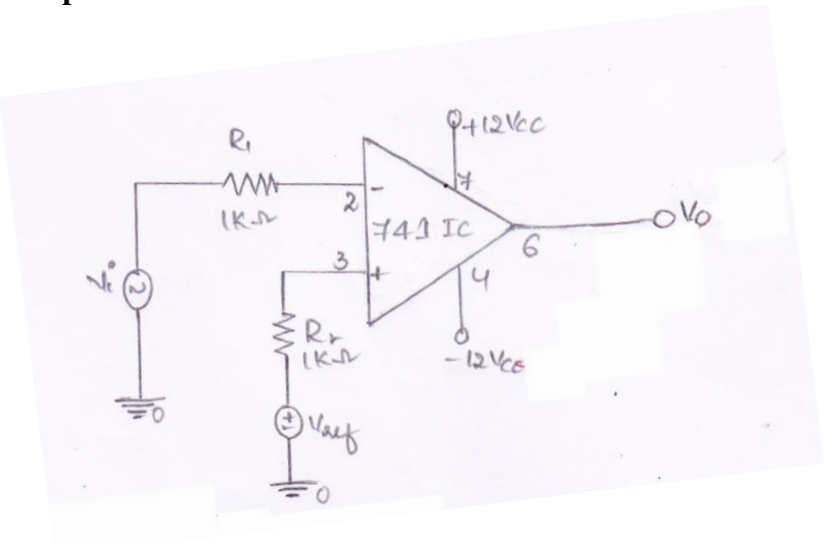
Adder:



Subtractor:



Comparator:



OP-AMP APPLICATIONS (ADDER , SUBTRACTOR , COMPARATOR)

AIM:

1. To design Adder circuit that will add given no. of input signals.
2. To design subtractor circuit that will subtract input signals.
3. To design a comparator circuit that will compare given input signal with reference signal.

APPARATUS:

S.No.	Device / Instrument	Type /Range	Quantity
1.	Cathode Ray Oscilloscope	Dual trace	1 No.
2.	Signal generator		1 No.
3.	Regulated power supply	0-30V	3 No.
4.	OP-AMP	IC μA 741	1
5.	Resistors	1KΩ	4

THEORY:

A**DDER:**

Op-Amp may be used to design a circuit whose output is the sum of several input signals such as circuit is called a summing amplifier or summer. We can obtain either inverting or non-inverting summer.

The circuit diagrams shows a two input inverting summing amplifier .It has two input voltages V_1 and V_2, two input resistors R_1, R2and a feedback resistor R_f.Assuming that op-amp is in ideal conditions and input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the noninverting input terminal is at ground potential.

By taking nodal equations.

$V_1/R_1+V_2/R_2+V_0/R_f=0$

$V_0=-[(R_f/R_1)\ V_1+(R_f/R_2)\ V_2]$

And here $R_1=R_2=R_f=1K\Omega$

$V_0=-(V_1+V_2)$

Thus output is inverted and sum of input.

Observations:

Adder circuit:

S.NO	INPUT 1	INPUT 2	INPUT 3	OUTPUT

Subtractor circuit:

S.NO	INPUT 1	INPUT 2	OUTPUT

Comparator circuit:

INPUT		V_{REF}	OUTPUT	
AMPLITUDE	FREQUENCY		AMPLITUDE	FREQUENCY

SUBTRACTOR:

A basic differential amplifier can be used as a subtractor. It has two input signals V1and V2 and two input resistances R1andR2 and a feedback resistor R_f. The input signals scaled to the desired values by selecting appropriate values for the external resistors.

From the figure, the output voltage of the differential amplifier with a gain of'1' is
V_0=-R/R_f(V_2-V_1)
V_0=V_1-V_2.
Also R_1=R_2=R_f=1KΩ.

Thus ,the output voltage V_0 is equal to the voltage V_1 applied to the noninverting terminal minus voltage V_2 applied to inverting terminal.
Hence the circuit is sub tractor.

COMPARATOR:

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp with output ±V satas in the ideal transfer characteristics. Itis clear that the change in the output state takes place with an increment in input Vi of only 2mv.This is the uncertainty region where output cannot be directly defined There are basically 2 types of comparators.

1. Non inverting comparator and.
2. Inverting comparator.

The applications of comparator are zero crossing detector ,window detector, time marker generator and phase meter.

Design procedure:

Adder circuit:

Output of the summing amplifier: $V_O = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$

When $R_1=R_2=R_3=R_f$ we have $V_0 = -(V_1+V_2+V_3)$

For averaging circuit $R_1=R_2=R_3 = 3\,R_f$

$$V_O = -\left(\frac{V_1+V_2+V_3}{3}\right)$$

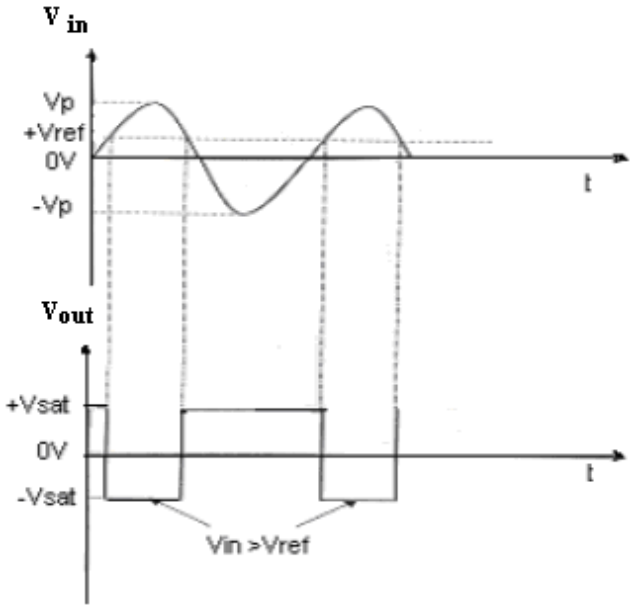
Subtractor circuit:

Output of the differential amplifier $V_O = -\frac{R_f}{R_1}(v_1 - v_2)$

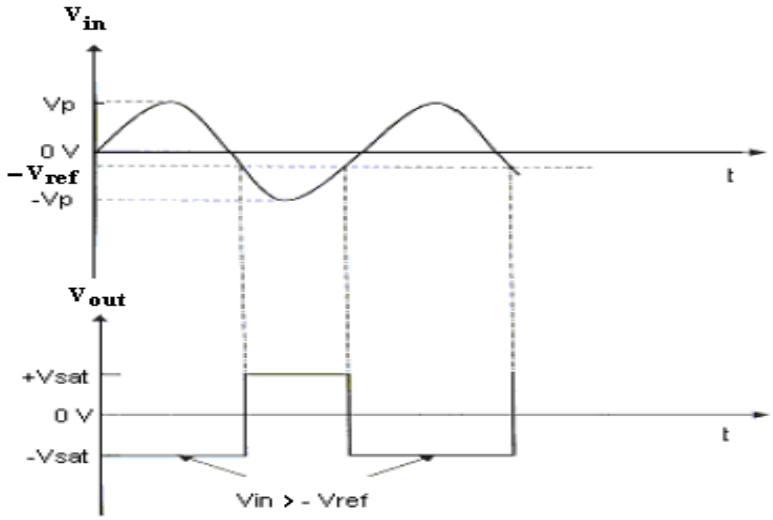
When $R_f = R_1$ $V_0 = -(V_1 - V_2)$

Model waveforms:

i) Inverting Comparator with Positive V_{ref}



ii) Inverting Comparator with Negative V_{ref}



Procedure:

Adder circuit:

1. Connect the circuit as per the circuit diagram.
2. Apply 1V, DC as a first input V_1 and 2 V DC as a second input , and 3 V DC as a third input at the inverting terminal of the op-amp.
3. Observe the input and output wave forms on the two channels of the CRO. Measure amplitude.

Subtractor circuit:

1. Connect the circuit as per the circuit diagram.
2. Apply 4V DC at the Non inverting terminal of the Op-Amp and 2V DC at the inverting terminal of the OP-AMP.
3. Observe the input and output waveforms on the two channels of the CRO. Measure the amplitude.

Comparator circuit:

1. Connect the circuit as per the circuit diagram.
2. Apply 4Vp-p, 1 KHz sine wave at the Non inverting terminal of the Op-Amp and 1V (Vref) at the inverting terminal of the OP-AMP.
3. Observe the input and output waveforms on the two channels of the CRO. Measure the amplitude and frequency.
4. Repeat step3 for different values of reference voltage.

Applications of comparator:

1. Zero crossing detector
2. window detector
3. Time marker generator.
4. Phase detector.

Result:

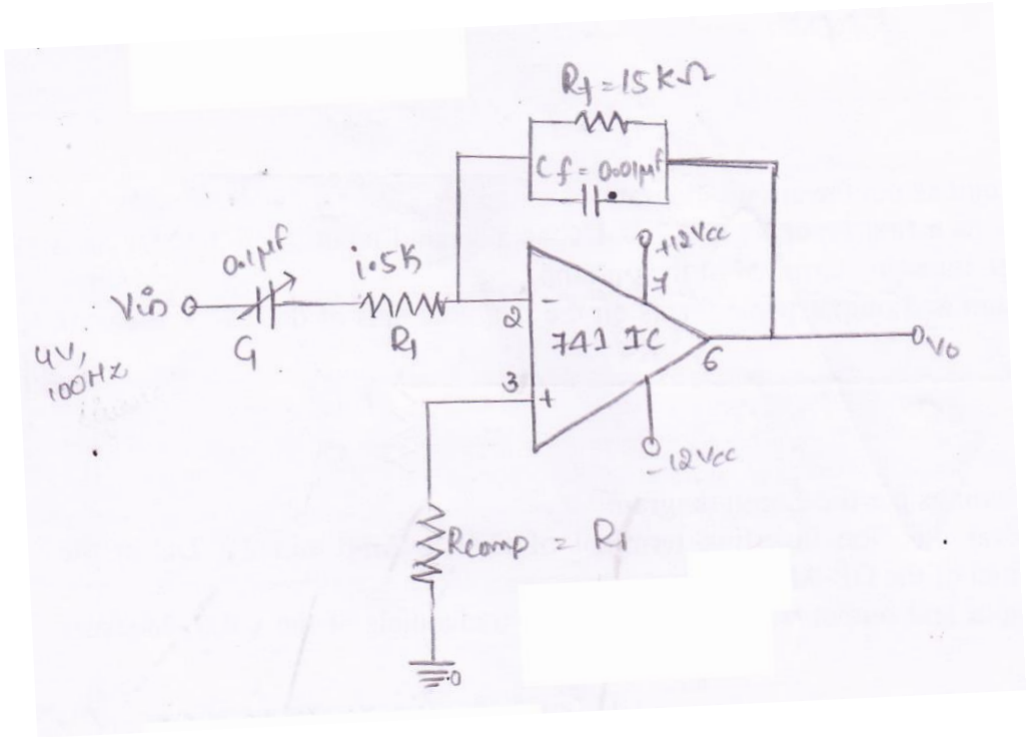
Hence the required circuit of adder , subtractor, comparator are designed and these output is verified

VIVA QUESTIONS :

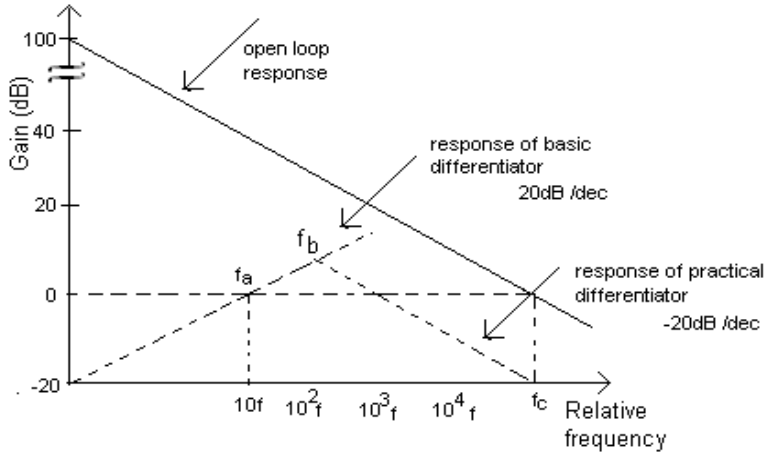
1. What is a mixed adder (Summing Amplifier)?
2. How do you construct Summing Amplifier using Op-Amp IC 741?
3. List the different types of comparators?
4. What are the differences between ideal and practical comparator?
5. In which mode Op-Amp used as a subtractor?

CIRCUIT DIAGRAMS:

DIFFERENTIATOR



Frequency response



INTEGRATOR AND DIFFERENTIATOR CIRCUITS USING IC 741

AIM:

1. To design differentiator circuit that will differentiate input signal at a frequency of 100Hz.
2. To design an integrator circuit using 741 Op-Amp to integrate input signal square wave of 1 KHz.

APPARATUS:

S.No.	Device/instrument	Type /Range	Quantity
1.	Cathode Ray Oscilloscope	Dual trace	1 No.
2.	Signal generator		1 No.
3.	Regulated power supply	0-30V	1 No.
4.	OP-AMP	IC μA741	1
5.	Resistors	1.5KΩ, 15KΩ, 10KΩ, 100KΩ	Each 1
6.	Capacitors	0.1μF, 1μF, 0.01μF	Each 1
7.	DCB	---	1No.

THEORY:

Differentiator:

One of the simplest of the OP-AMP circuits that contain capacitor is the differentiating amplifier, or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiator that is, the output waveform is the derivative of input waveform.
A differentiator circuit is shown in figure:

Analysis:

The node 'N' is at virtual ground potential i.e, V_N=0. The circuit current i_c through the capacitor is $i_{c=}\ c_1 \frac{d}{dt}(v_i - v_N) = c_1(\frac{dv_i}{dt})$.

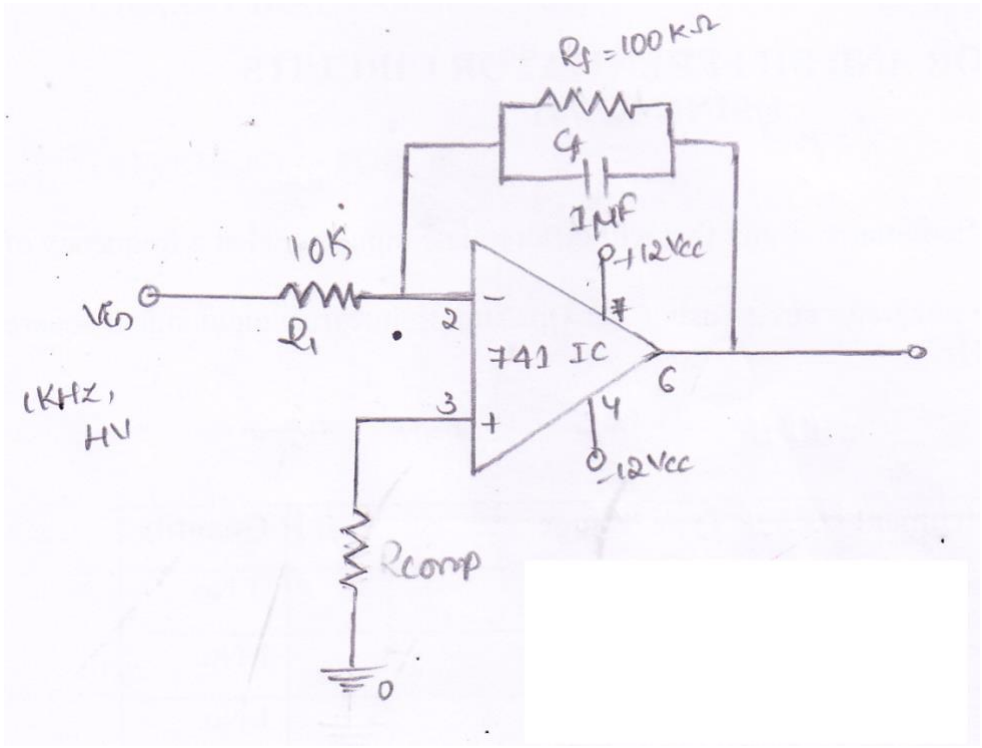
The current if through the feedback resistor is V_0/R_f and there is no current into the OP-AMP. Therefore the nodal equation at node N is

$$c_1(\frac{dv_i}{dt}) + \frac{v_0}{R_f} = 0 \quad \text{from which we have}$$

$$v_0 = -R_f C_1 \frac{dv_i}{dt} \quad \rightarrow 1$$

Thus the O/P voltage Vo is a constant ($-R_fC_1$) times the derivative of the input voltage V_i and the circuit is a differentiator. The minus sign indicates a 180^0 phase shift of the O/P waveform Vo with respect to the input signal.

INTEGRATOR:



Frequency response

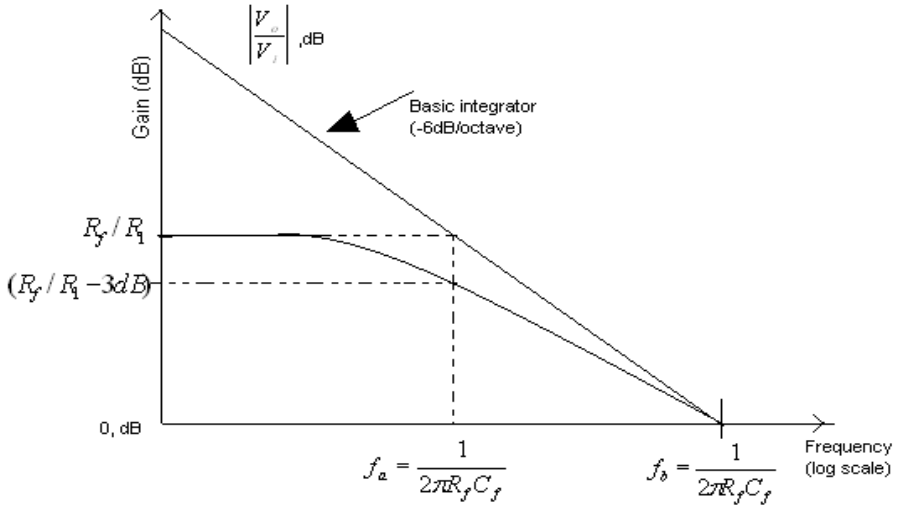


Figure (b)

The phasor equivalent of above equation is

$$Vo(s) = -R_fC_1SV_i(s) \rightarrow 2$$

In steady state $S = j\omega$.

We may now write the magnitude of gain (A) of differentiator is

$$|A| = \left|\frac{v_0}{v_i}\right| = |-j\omega R_f C_1| = \omega R_f C_1 \text{ ------> } 3$$

$$|A| = f / f_a \text{ ---> } 4 \text{ where } f_a = \frac{1}{2\pi R_f C_1}$$

At f =fa, $|A|$=1 i.e, 0 dB and the gain increases at a rate of +20dB/dec

From equation 7 it is evident that the gain increases at +20dB/dec for frequency $f<f_b$ and decreases at –20dB/dec for $f>f_b$ as shown by dashed lines in figure. This 40dB/dec change on gain caused by R_1C_1 and R_fC_f factors.

For the basic differentiator the frequency response would have increased continuously at the rate of frequency +20dB/dec even beyond f_b causing stability problem at high frequency. Thus the gain at high frequency is reduced significantly. There by avoiding the high frequency noise and stability problems. The value of f_b should be selected such that fa < fb < fc.
where fc is the unity gain bandwidth of the Op-Amp in open loop configuration.

For good differentiation, one must ensure that the time period T of the input signal is larger than or equal to R_fC_1 that is $T \geq R_fC_1$.

Design procedure:

1. Choose 'fa' equal to the highest frequency of the input signal.
   Assume a practical value C_1 (<1μF) and then calculate R_f by using
   $R_f = 1/2\pi f_aC_1$.
2. Choose fb = 10 f_a. now calculate the value of R_1 by using $R_1 = 1/2\pi f_bC_1$.
3. Calculate C_f by using $R_1C_1 = R_fC_f$.

Differentiator:

$f_a = \frac{1}{2\pi R_f C_1}$

$C_1 = 0.1\mu F$

$f_a = 100Hz$

$\Rightarrow R_f = \frac{1}{2\pi f_a C_1} = \frac{1}{2\pi \text{ x } 100 \text{ x } 0.1 \text{ x } 10^{-6}} = 15.9K\Omega$

$R_1 = 1.59K\Omega$

$R_1C_1 = R_fC_f$

$\Rightarrow C_f = \frac{R_1C_1}{R_f} = \frac{1.59K \text{ x } 0.1\mu}{15.9K}$

$C_f = 0.01\mu F$

f_b=10f_a

$f_b = \frac{1}{2\pi R_1 C_1}$, R_1 = 1.59KΩ, Rf = 15.9 KΩ, C_1 = 0.1μF, Cf = 0.01 μF

OBSERVATIONS: Differentiator

Condition	C_1 (μF)	INPUT WAVEFORM			OUTPUT WAVEFORM		
		Type	Amplitude	Frequency	Type	Amplitude	Frequency
R_fC_1 <<T	0.1uf	Square					
R_fC_1 =T		Square					
R_fC_1 >>T		Square					
R_fC_1 <<T	0.1uf	Sine wave					
R_fC_1 <<T	0.1uf	Triangular					

OBSERVATIONS: Integrator

Condition	C_f (μF)	INPUT WAVEFORM			OUTPUT WAVEFORM		
		Type	Amplitude	Frequency	Type	Amplitude	Frequency
R_1C_f >>T	1uf	Square					
R_1C_f =T		Square					
R_1C_f <<T		Square					
R_1C_f >>T	1uf	Sine wave					
R_1C_f >>T	1uf	Triangular					

Applications:

The differentiator is most commonly used in wave shaping circuits to detect high frequency components in a signal and also as a rate of change detection in FM modulations.

Integrator:

If we interchange the resistor and capacitor of differentiator, we have the circuit called as an integrator. The nodal equation at node 'N' is

$$\frac{V_i}{R_1} + C_f \frac{dV_o}{dt} = 0$$

$$or \quad \frac{dV_o}{dt} = -\frac{1}{R_1 C_f} V_i$$

Integrating both sides we get,

$$\int_0^t dV_o = -\frac{1}{R_1 C_f} \int_0^t V_i dt$$

$$V_o(t) = -\frac{1}{R_1 C_f} \int_0^t V_i(t) dt + V_o(0) \rightarrow 9$$

Where $V_{(o)}$ is the initial output voltage.

The circuit, thus provides an output voltage which is proportional to the time integral of the input and R_1C_f is the time constant of the integrator. It may be noted that there is a negative sign in the output voltage, and therefore, this integrator is known as an inverting integrator. A resistance, $R_{comp}=R_1$ is usually connected to the (+) input terminal to minimize the effect of input bias current.

A simple low pass RC circuit can also work as an integrator when time constant is very large. This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations. However, in the Op-amp integrator of fig, by miller's theorem, the effective time constant of the op-amp integrator becomes very large which results in perfect integration.

The operation of the integrator can also be studied in the frequency domain. In phasor notation, Equation 8 can be written as

$$V_o(s) = -\frac{1}{sR_1 C_f} V_i(s) \rightarrow 10$$

In steady state, put s=jω and we get

$$V_o(j\omega) = -\frac{1}{j\omega R_1 C_f} V_i(j\omega) \rightarrow 11$$

So, the magnitude of the gain or integrator transfer function is

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega R_1 C_f}\right| = \frac{1}{\omega R_1 C_f} \rightarrow 12$$

The frequency response (or Bode plot of this basic integrator is shown in fig (b). The Bode plot is a straight line of slope –6B/octave (or equivalently –20dB/decade). The frequency f_b in fig (b) is the frequency at which the gain of the integrator is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_f}$$

It can further be seen from equation 11 that at ω=0, the magnitude of the integrator transfer function is infinite. At dc, the capacitor C_f behaves as an open circuit and there is no negative feedback. The op-amp thus operates in open loop, resulting in an infinite gain. In practice, of course, output never becomes infinite, rather the output of the amplifier saturates at a voltage close to the op-amp positive or negative power supply depending on the polarity of the input dc signal.

As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in a differentiator. However, at low frequencies such as at dc (ω=0), the gain becomes infinite (or saturates). The solution to this problem is discussed in the following.

DESIGN PROCEDURE:

$$R_1 C_f \geq T$$

$$Assume\ C_f = 0.1\mu F$$

$$f = 1KHz$$

$$T = 1m\sec$$

$$R_1 C_f = T$$

$$R_1 = \frac{T}{C_f} = \frac{1 \text{ x } 10^{-3}}{0.1 \text{ x } 10^{-6}} = 10K\Omega$$

$$R_f = 10R_1$$

$$\therefore R_f = 100K\Omega$$

R_1 =10 KΩ , R_f = 100KΩ, C_f = 0.1 μF

Applications:

The integrator is most commonly used in analog computers and analog to digital converters (ADC) and signal wave shaping circuits.

Procedure for differentiator

1. Connect the circuit as per the circuit diagram except do not apply the signal from the function generator yet.

2. Set the function generator for a square wave output and adjust its amplitude 2Vp-p also set the frequency of the square wave at 100Hz. Apply the square wave o/p of the function generator to the circuit as Vin.

3. Connect one channel of the oscilloscope at the input and the other at the output terminal of the op-Amp. Measure the frequency of the input waveform and record it in Tabular form. Also measure the amplitude and frequency of the output waveform and record them on tabular form.

4. Repeat step3 to satisfy the conditions $R_fC_1 = T$ and $R_fC_1 > T$.

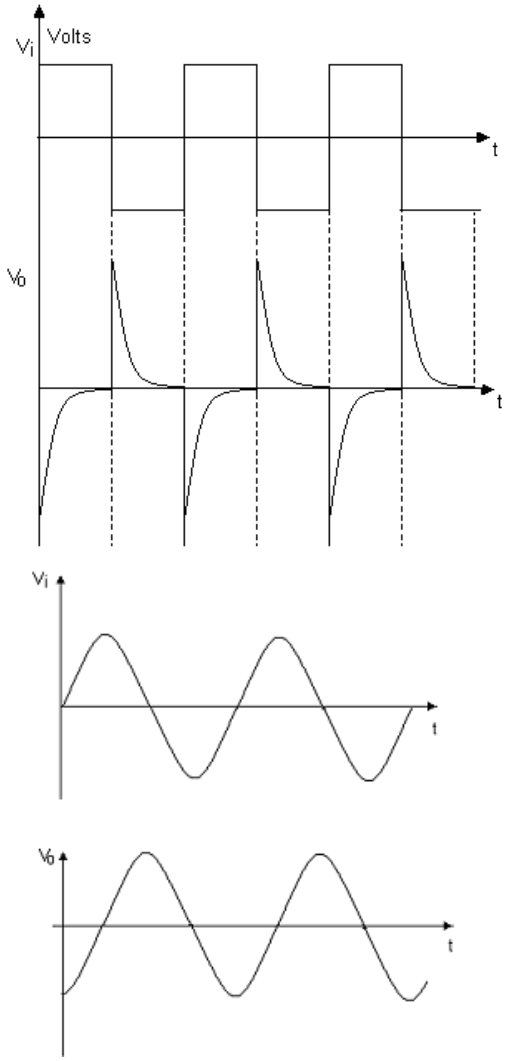
5. Next set the function generator for sine wave output. Adjust the amplitude of the sine wave to 1Vp-p and set the frequency at 100Hz for the condition $R_fC_1 << T$.

6. Connect one channel of the oscilloscope at the input and the other at the output terminal of the OP-AMP. Measure amplitude and frequency of input and output wave forms and record them on Table.

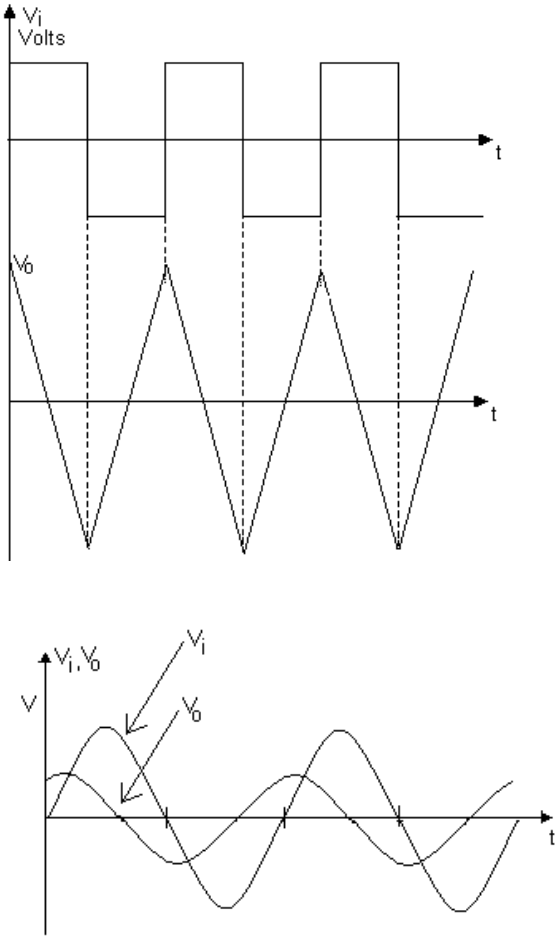
7. Also observe the output waveform for triangular input.

MODEL WAVEFORMS:

Differentiator:



Integrator:



Procedure for integrator:

1. Connect the circuit as per the circuit diagram except do not apply the signal from the function generator yet.
2. Set the function generator for a square wave output and adjust its amplitude 2Vp-p also set the frequency of the square wave at 1KHz. Apply the square wave o/p of the function generator to the circuit as V_{in}
3. Connect one channel of the oscilloscope at the input and the other at the output terminal of the op-Amp. Measure the frequency of the input waveform and record it in Tabular form. Also measure the amplitude and frequency of the output waveform and record them on tabular form.
4. Repeat step3 to satisfy the conditions $R_1C_f = T$ and $R_1C_f < T$.
5. Next set the function generator for sine wave output. Adjust the amplitude of the sine wave to 2Vp-p and set the frequency at 1 KHz for the condition $R_1C_f >> T$.
6. Connect one channel of the oscilloscope at the input and the other at the output terminal of the OP-Amp. Measure amplitude and frequency of input and output wave forms and record them on table.
7. Also observe the output waveform for triangular input.

RESULT:

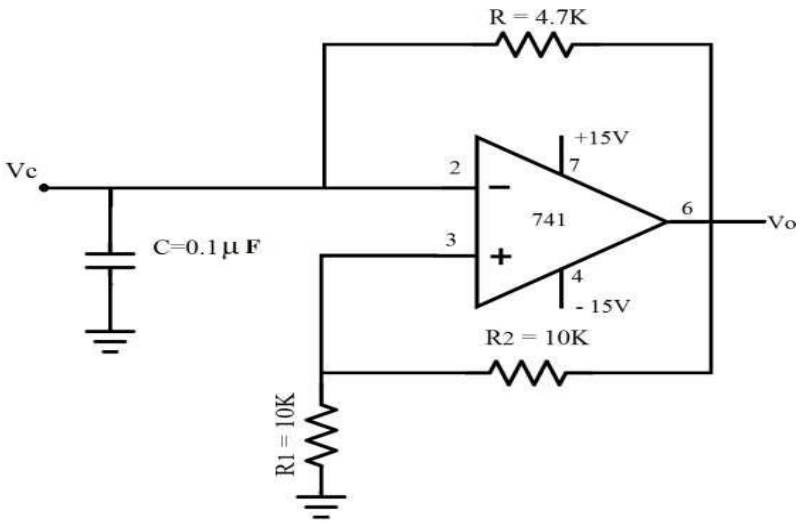
Hence the differentiator circuit that will differentiator input signal at 100hz and the integrator circuit that will integrator a square wave of 1khz is designed

VIVA QUESTIONS :

1. What are the limitations of ideal differentiator?
2. What is the need for R_1in the circuit of integrator?
3. What are the applications of integrator and differentiator?
4. What are the differences between integrator and differentiator?
5. Which filter does act as a differentiator?
6. Which filter does act as an integrator?

a) SYMMETRICAL ASTABLE MULTIVIBRATOR

Circuit Diagram:



SYMMETRICAL ASTABLE MULTIVIBRATOR

Note: Use 10KΩ pot instead of R = 4.7KΩ resistor and vary it for accurate time period.

Design:

Given f = 1 KHz

So T = 1/f = 1ms

And β = R1 / (R1+R2)

Let R1 = 10KΩ , and R2 =10KΩ

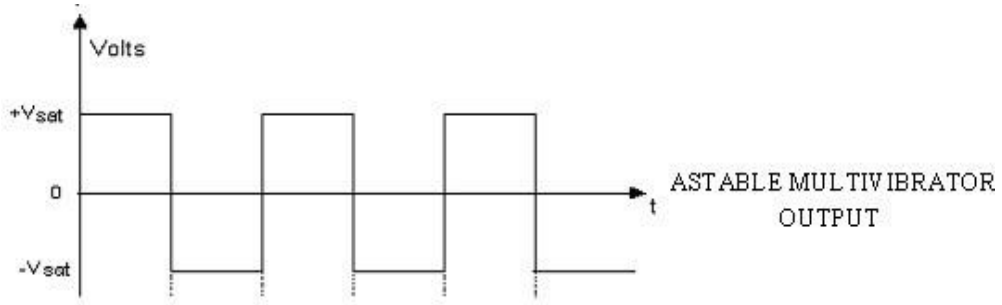
Then β = 0.5

Therefore T= 2.2RC

=1msLet C = 0.1μF

Then R = 4.7KΩ

MODEL WAVE FORMS:



Construct Waveform Generator using single Op-Amp with variable duty cycle.

AIM:

To generate the Square waveform by using 741 OP-AMP with variable duty cycle**.**

APPARATUS:

S.No.	Name and Specifications	Quantity Required
1.	CRO	1 No.
2.	IC 741	1 No.
3.	Diode IN 4007	2 Nos.
4.	Resistors- 4.7kΩ	1 No.
5.	10kΩ	2 Nos.
6.	3.3kΩ	1 No.
7.	5.6kΩ	1 No.
8.	Capacitor (0.1μF)	1 No.
9.	Probes and Connecting Wires	As requird

THEORY:

Square wave generator (Astable multivibrator)

A simple op-amp square wave generator is shown in figure 1(a), also called as free running oscillator. The principle of generation of square wave output is to force an op-amp to operate in the saturation region. In fig 1(a) a fraction β =R2 / (R1+R2) of the output is fed back to the (+)input terminal. Thus the reference voltage Vref is βV0 and may take values as +βVsat or -βVsat. The output is also feedback to the (-) input terminal after integrating by means of alow pass RC combination. Whenever input at the (-)input terminal just exceeds Vref ,switching takes place resulting in a square wave output. In astable multivibrator , both thestates are quasi stable.

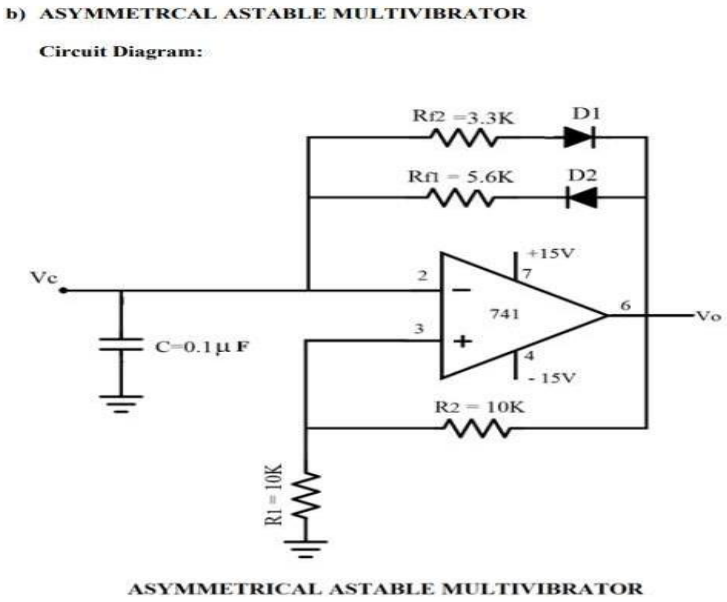
Consider an instant of time when the output is at +Vsat . The capacitor now starts charging towards +Vsat through resistance R as shown in fig 1(b). The voltage at (+) input terminal is held at +βVsat, by R1 and R2 combination. This condition continues as the charge on C rises, until it has just exceeded +βVsat, the reference voltage. When the voltage at the (-)input terminal becomes just greater than this reference voltage , the output is driven to -Vsat. At this instant, the voltage on the capacitor is +βVsat. It begins to discharge through R,that is charges towards –Vsat. When the output voltage switches to –Vsat, the capacitor charges.

Principle:

In this circuit, the opamp is operated in saturation mode and the output swings between +Vsat and –Vsat giving square wave output. This circuit is also called free running oscillator or square wave generator . A positive feedback with feedback factor β = R1 / (R1+R2) isprovided to the non-inverting terminal. When Vo= +Vsat, the capacitor C starts to charge to + Vsat through R. when the capacitor voltage cross

b) ASYMMETRCAL ASTABLE MULTIVIBRATOR

Circuit Diagram:



ASYMMETRICAL ASTABLE MULTIVIBRATOR

Note: Use two 10KΩ potentiometers instead of Rf1 and Rf2 resistor and vary it foraccurate time period.

Design:

Given f = 1 KHz

So T = Ton + Toff = 1/f = 1ms

Also Duty cycle = Ton/(Ton+Toff) = 0.66

or 66% Solving above two equations, Ton = 0.66ms

Toff = 0.33ms

For β=0.5,

Ton= 1.1Rf1C = 0.66ms

Let C = 0.1µF

Then Rf1 = 6.2KΩ = 5.6KΩ (Std)

Similarly Toff = 1.1Rf2C = 0.33ms

Then Rf 2 = 3KΩ = 3.3 KΩ (Std)

+βVsat, output switches from +Vsat to – Vsat. Now the voltage appearing at the non-inverting terminal is –βVsat and capacitor discharges through R towards -Vsat. When the capacitor voltage crosses –βVsat, the output switches from –Vsat to + Vsat and this process continues to generate square wave output with time period T=Ton + Toff= 2RC ln[(1+β)/(1-β)]. In asymmetrical astable multivibrators, the charging and discharging time of capacitor is made unequal to get asymmetrical square wave with different Ton and Toff

Procedure:

1. Check the components.
2. Setup the symmetric astable multivibrator circuit on the breadboard and heck he connections.
3. Switch on the power supply.
4. Observe output and capacitor voltage on two channels of the oscilloscope simultaneously.
5. Draw the waveforms on the graph.
6. Measure the frequency of oscillation and duty cycle .
7. Repeat the procedures for asymmetric astable multivibrator.

(Note: The experiment may be repeated for different values of frequency and duty cycle)

Observation:

a) Symmetrical astable multivibrators

Vo(p-p)= ?

f = ?

Duty cycle = ?

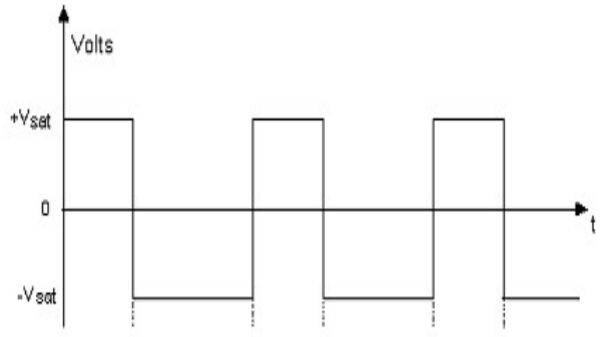
b) Asymmetrical astable multivibrators

Vo(p-p)= ?

f = ?

Duty cycle = ?

MODEL WAVE FORMS:



ASYMMETRICAL ASTABLE MULTIVIBRATOR

OBSERVATIONS:

S.NO	Type of the Circuit	Amplitude	T on pulse width	T off pulse width	Timeperiod	Frequency
1	Symmetrical Astable multivibrator					
2	Asymmetrical Astable multivibrator					

DESIGN OF ASTABLE MULTIVIBRATOR:

$$\beta = \frac{R_2}{R_1 + R2} \Rightarrow R_1 = R_2 \Rightarrow \beta = \frac{1}{2} = 0.5.$$

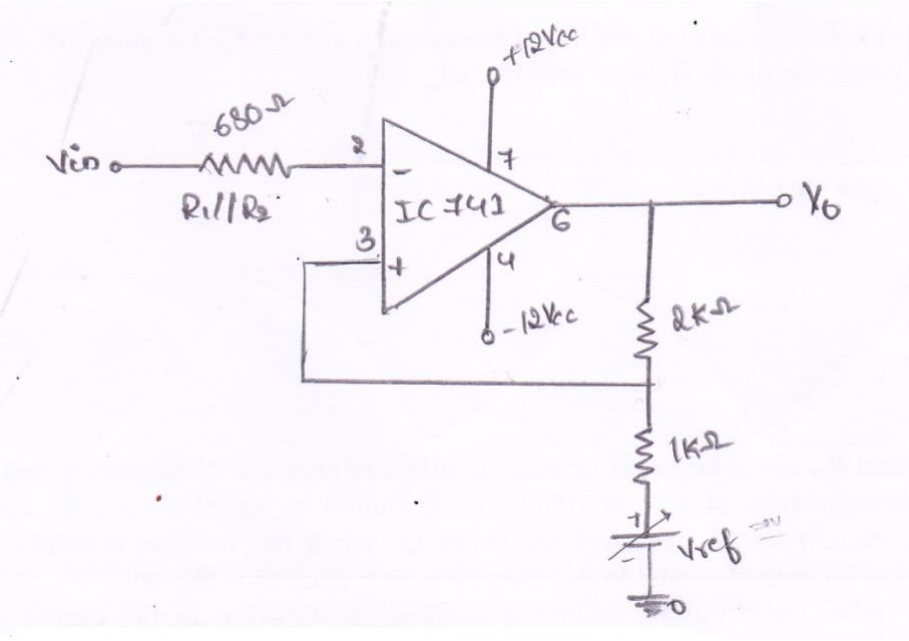
$$T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

T = $2RC$ = 2 x 10K x 0.1μ = 2msec

RESULT: Hence the generation of square wave with variable duty is done using IC 741.

CIRCUIT DIAGRAMS:

SCHMITT TRIGGER CIRCUIT USING IC 741



SCHMITT TRIGGER CIRCUITS - USING IC 741

AIM:

1. To convert any periodic waveform into a square wave and calculate UTP and LTP values .
2. To study the operations of Schmitt trigger using IC 741.

APPARATUS:

S.No.	DEVICE / INSTRUMENT	TYPE /RANGE	QUANTITY
1.	Cathode Ray Oscilloscope	Dual trace	1 No.
2.	Signal generator		1 No.
3.	Regulated power supply	0-30V	1 No.
4.	Op-amp, Timer	IC μA 741,	1 No. .
5.	Resistors	1KΩ, 2KΩ	1 No.each
		680Ω	1 No.
		100KΩ	2 No.
6.	Capacitors	0.01μF	2 No.

THEORY:

Using IC 741:

Schmitt trigger circuit is an inverting comparator with positive feedback. This circuit converts irregular shaped waveforms into square wave. Schmitt trigger circuit is also known as regenerative comparator. The input voltage is applied to the inverting input terminal and feedback voltage to the non-inverting input terminal.

The input voltage Vi triggers the output Vo every time . it exceeds certain voltage levels. These voltage levels are called Upper Threshold voltage (V_{UT}) and Lower Threshold voltage (V_{LT}). The hysteresis width is the difference between these two threshold voltages ie, $V_{UT} - V_{LT}$. These threshold voltages are calculated as follows.

Design procedure:

$$R_i = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

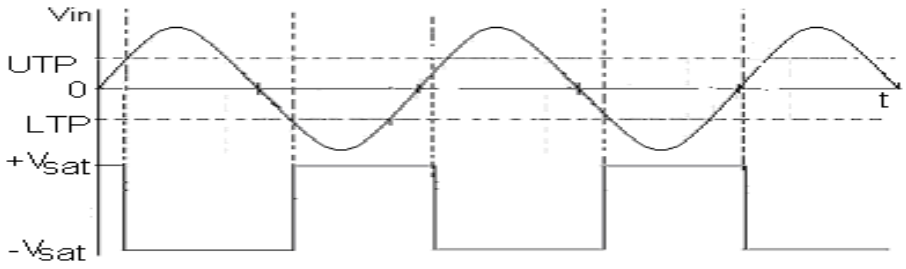
$$V_{UTP} = V_{ref} + \frac{R_2}{R_1 + R_2}(V_{sat} - V_{ref})$$

Observations:

Schmitt trigger using IC 741:

Resistance values			Vref	Theoretical Values			Practical Values			Input waveform		Output waveform	
R_i	R1	R2		V_{UTP}	V_{LTP}	V_H	V_{UTP}	V_{LTP}	V_H	Amplitude	F (Hz)	V_o	F(Hz)
680Ω													

MODEL WAVEFORMS:



SCHMITT TRIGGER USING IC 741

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Apply the input sinusoidal at 1 KHz frequency 10Vp-p,and set V_{ref} to zero
3. Observe the UTP and LTP points and corresponding O/P wave form.
4. Repeat step3 for different reference voltages.
5. Calculate the UTP and LTP and Hysteresis voltage.

RESULT:

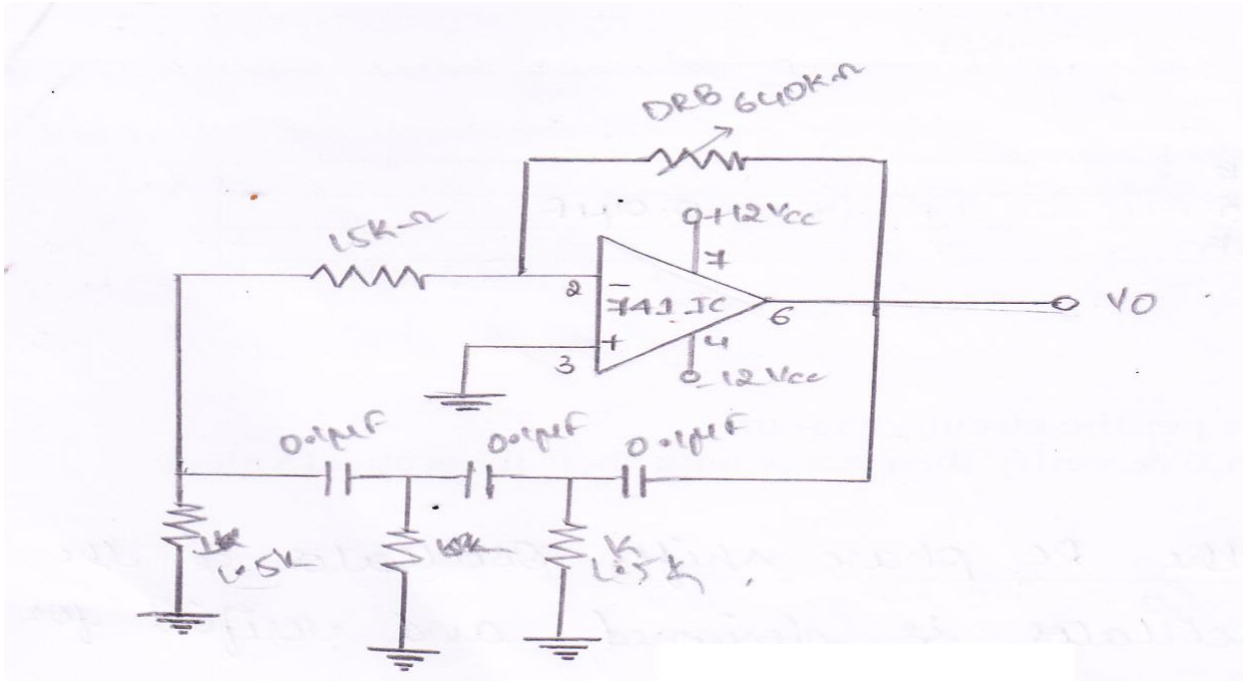
1. Hence the conversion of sine wave into square wave is observed and its UTP and LTP are calculated

VIVA QUESTIONS :

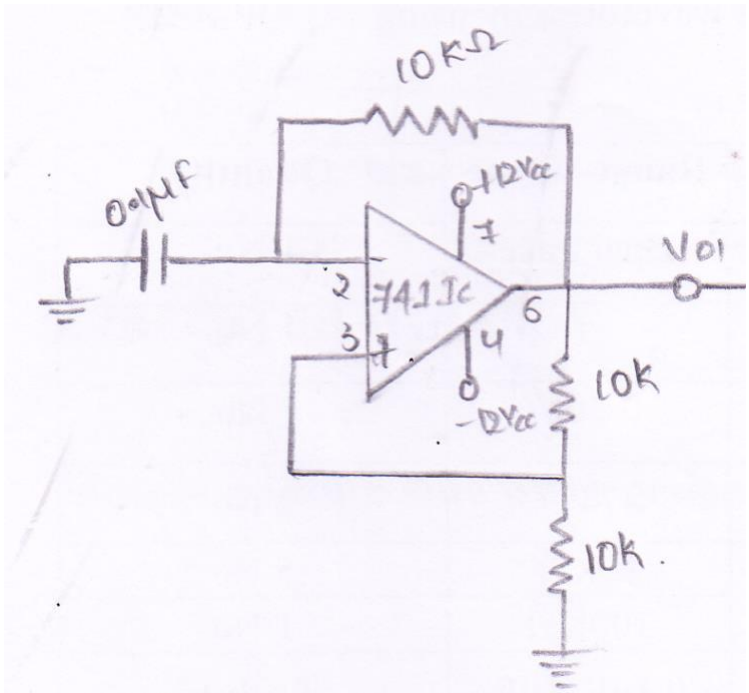
1. Explain the function of reset.
2. What is the significance of control pin?

CIRCUIT DIAGRAMS:

SIME WAVE GENERATOR :



Square wave Generator



FUNCTION GENERATOR USING OP-AMPS

AIM:

To generate the Sine, Square and Triangular waveforms by using 741 OP-AMP.

APPARATUS:

S.No.	Device / Instrument	Range / Type	Quantity
1.	Cathode Ray Oscilloscope	Dual trace	1 No.
2.	Signal generator		1 No.
3.	Regulated power supply	0-30V	1 No.
4.	IC	741	2 No
5.	Resistors	10K?	5 No
		100K?	1 No
6.	Capacitors	0.1?F, 1?F	Each 1

THEORY:

OSCILLATORS:

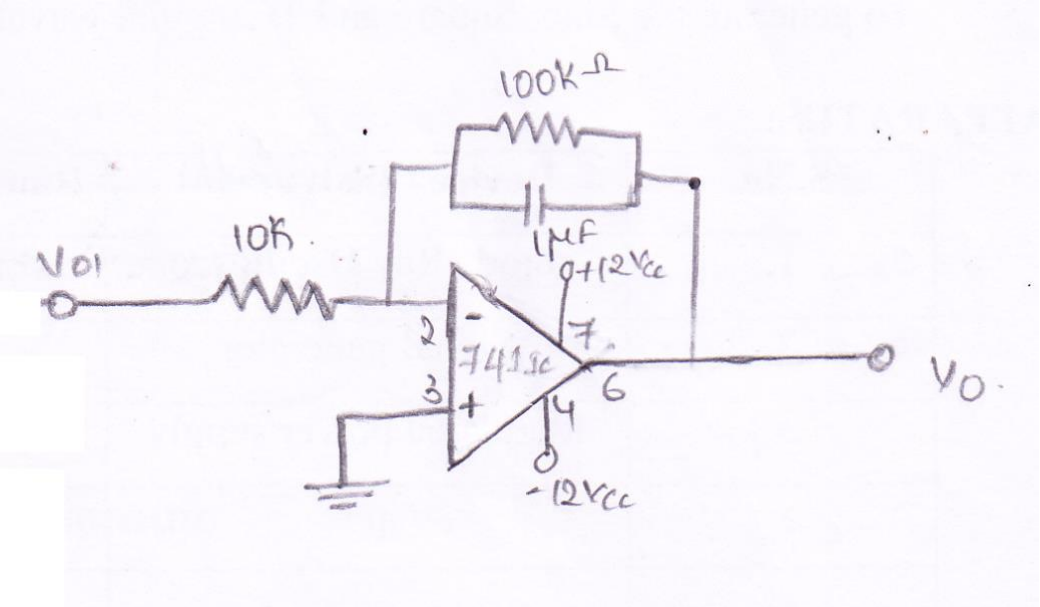
Basically the function of an oscillator is to generate alternating current or voltage waveforms. More precisely, an oscillator is a circuit that generates a repetitive waveform of fixed amplitude and frequency without any external input signal. Oscillators are usedin radio, television, computers, and communications. Although there are different types of oscillators, they all work on the same basic principle.

RC-Phase Shift Oscillator:

The Phase Shift Oscillator is constructed with an inverting mode and phaseshift network in the feedback loop. The two conditions that are to be satisfied for any oscillator circuit are

1. Unity voltage gain i.e., $|A\beta| = 1$. This is achieved in the phase shift Oscillator by ensuring that at resonance conditions of the circuit. The gain of the amplifier is $\frac{R_f}{R_1} = 29$ and the response frequency is given by
$$f_0 = \frac{1}{2\pi\sqrt{6RC}}$$
2. The total phase shift around the loop is zero or 360^0 .Since the inverting amplifier produces a phase shift of 180^0. The RC phase shift network produces and additional phase shift of 180^0. Besides this RC network selects the frequency of operations as given in the above equation.

Triangular wave generator



the saturation region. In fig 1(a) a fraction $\beta = R_2 / (R_1+R_2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage Vref is βV_0 and may take values as $+\beta V_{sat}$ or $-\beta V_{sat}$. The output is also feedback to the (-) input terminal after integrating by means of a low pass RC combination. Whenever input at the (-)input terminal just exceeds Vref , switching takes place resulting in a square wave output. In astable multivibrator , both the states are quasi stable.

Consider an instant of time when the output is at +Vsat . The capacitor now starts charging towards +Vsat through resistance R as shown in fig 1(b). The voltage at (+) input terminal is held at $+\beta V_{sat}$, by R_1 and R_2 combination. This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat}$, the reference voltage. When the voltage at the (-)input terminal becomes just greater than this reference voltage , the output is driven to –Vsat. At this instant, the voltage on the capacitor is $+\beta V_{sat}$. It begins to discharge through R, that is charges towards –Vsat. When the output voltage switches to –Vsat, the capacitor charges

THEORY OF INTEGRATOR:

If we interchange the resistor and capacitor of differentiator, we have the circuit called as an integrator. The nodal equation at node 'N' is $\frac{V_i}{R_1} + C_f \frac{dV_o}{dt} = 0$

$$or \quad \frac{dV_o}{dt} = -\frac{1}{R_1 C_f} V_i$$

Integrating both sides we get,

$$\int_0^t dV_o = -\frac{1}{R_1 C_f} \int_0^t V_i dt$$

$$V_o(t) = -\frac{1}{R_1 C_f} \int_0^t V_i(t) dt + V_o(0)$$

where $V_{(o)}$ is the initial output voltage.

DESIGN PROCEDURE:
DESIGN OF RC-PHASE SHIFT OSCILLATOR:

$\mathbf{f_0}$ = 400 Hz.

$f_0 = \frac{1}{2\pi RC\sqrt{6}}$ Let C = 0.1μF

Therefore $R = \frac{1}{2\pi \text{ x } 0.1 \text{ x } 10^{-6} \text{ x } \sqrt{6} \text{ x } 400} = 1.6K\Omega$

To prevent loading $R_1 \geq 10R$

Considering $R_1 = 10R$

Therefore $R_1 = 16K\Omega$

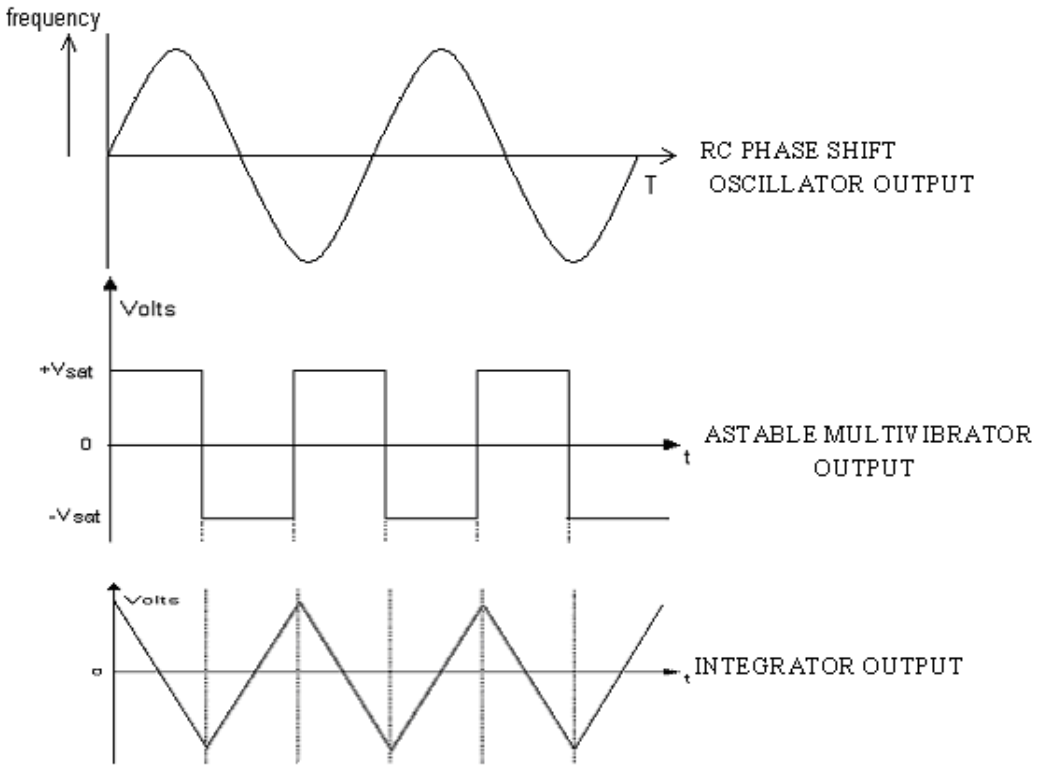
For sustained oscillations AV = 29

$\frac{R_f}{R_1} = 29$. $R_f = 29\ R_1$

OBSERVATIONS:

S.NO	Type of the Circuit	Amplitude	Timeperiod	Frequency
1	RC Phase shift Oscillator	———	——	——
2	Astable multivibrator			
3	Integrator			

MODEL WAVE FORMS:



R =	
R_1 =	C_1 =
R_F =	

DESIGN OF ASTABLE MULTIVIBRATOR:

$$\beta = \frac{R_2}{R_1 + R2} \Rightarrow R_1 = R_2 \Rightarrow \beta = \frac{1}{2} = 0.5.$$

$$T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$T = 2RC = 2 \text{ x } 10\text{K x } 0.1\mu = 2\text{msec}$$

DESIGN OF INTEGRATOR:

$$RC \geq T$$

$$\text{assume } C = 1\mu F$$

$$T = \frac{1}{f} = 1\,\text{msec}$$

$$R_1 = \frac{1}{fxC} = \frac{1}{1\mu \text{ x } 1K} = 10^3 = 1K\Omega$$

$$R_1 = 1K\Omega, \quad R_f = 10R_1 \Rightarrow 10 \text{ x } 1K = 10K\Omega$$

PROCEDURE:

Sine wave generator

1. Connect the circuit as per the circuit diagram
2. Observe output at pin 6 & verify the results with their theoretical values.

Square wave generator

1. Connect the circuit as per the circuit diagram
2. Observe output at pin 6 & verify the results with their theoretical values.

Traingular wave generator

1. Apply the output of square wave generator to the input of integrator
2. Observe output at pin 6 & verify the results with their theoretical values.

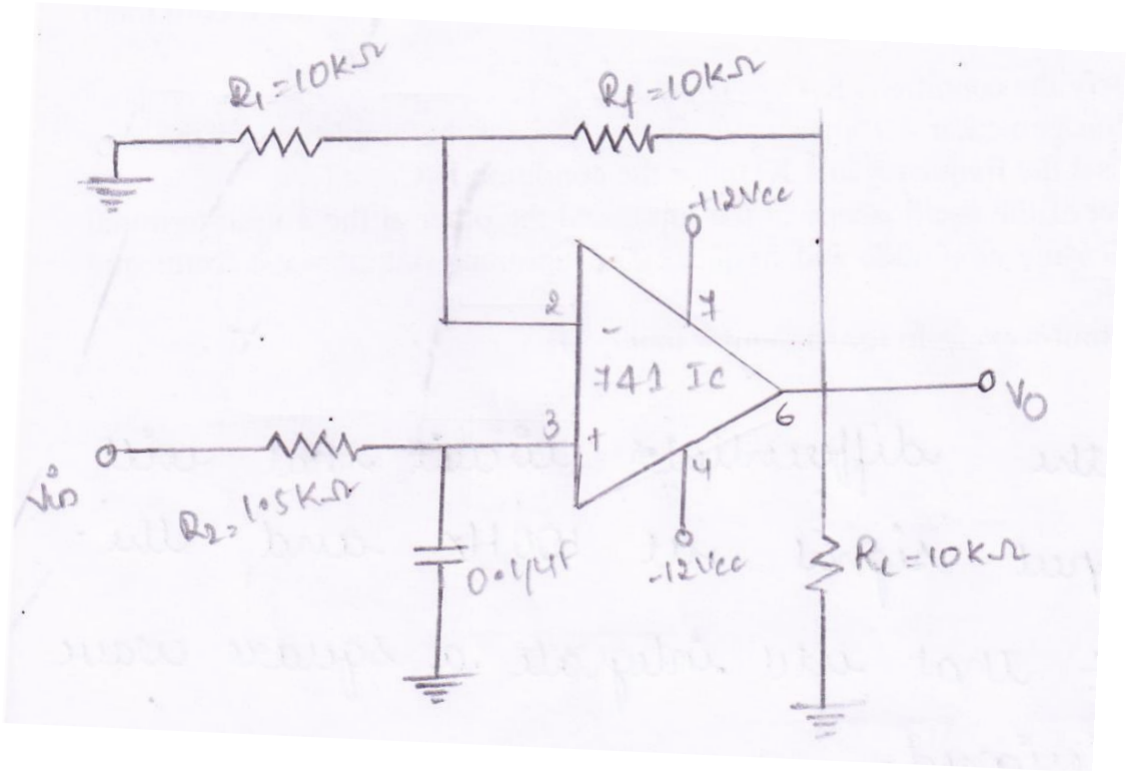
RESULT:

Hence the generation of square wave & triangular wave is done using ic 741

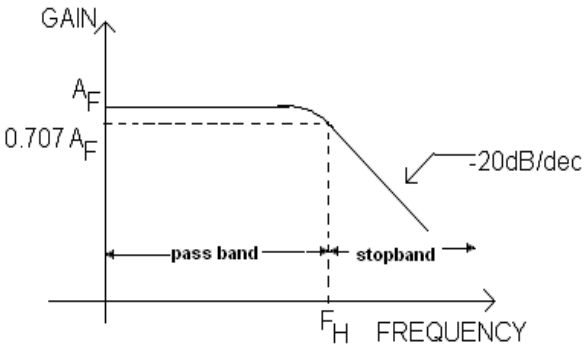
VIVA QUESTIONS :

1. Define function generator ?
2. What are the applications of function generator ?

LOW PASS FILTER



MODEL WAVE FORM:



Frequency response

ACTIVE FILTER APPLICATIONS – LPF, HPF (FIRST ORDER

AIM:

1. To design a Low pass filter for a given frequency and to obtain its frequency response.
2. To design a High pass filter for a given frequency and to obtain its frequency response.

APPARATUS:

S.NO.	DEVICE / INSTRUMENT	TYPE /RANGE	QUANTITY
1.	Cathode Ray Oscilloscope	Dual Trace	1 No.
2.	Signal generator		1 No.
3.	Regulated Power supply		1 No.
4.	OP-AMP	IC μA 741	1 No.
5.	Resistors	1.5 KΩ	1 No.
		10 KΩ	2 No.
6.	Capacitors	0.1μF	1 No.

THEORY:

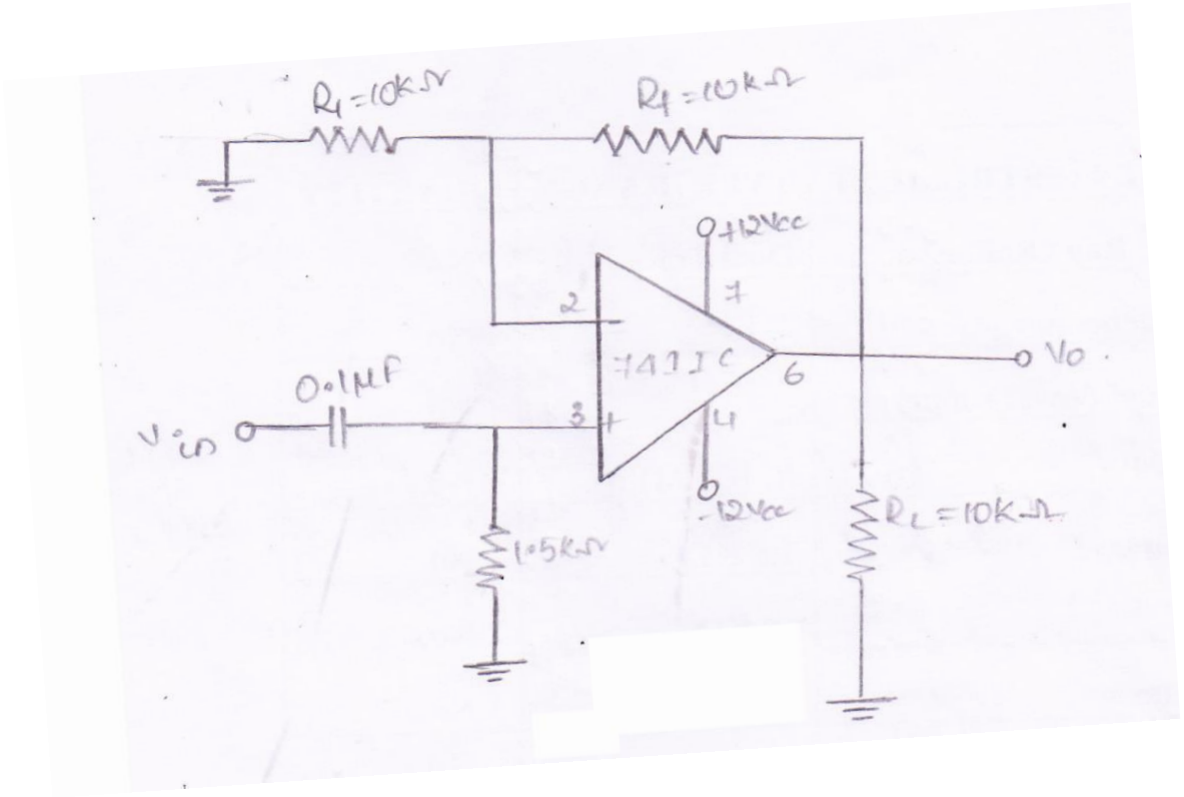
A frequency selective electric circuit that passes electric signals of specified band of frequencies and attenuates the signals of frequencies outside the band is called an electric filter. We use op-amp as an active element and resistors and capacitors as the passive element. The active filters by enclosing a capacitor in the feedback loop, avoid using inductor. In this way, inductors less active RC filters can be obtained also. An op-amp is used in non inverting configuration, it offers high i/p impedance and low o/p impedance. This will improve the load directivity and drive capacity and the load is isolated from the frequency determining network, because of the high input impedance of the op-amp. Large valued resistors can be used, there by reducing the value of the capacitors required in the design.

The active filters have their limitations too high frequency response is limited by gain –bandwidth product and slew rate of the op-amp moreover, the high frequency active filters are more expensive than the passive filters. The passive filter in high frequency range is more economic choice for applications.

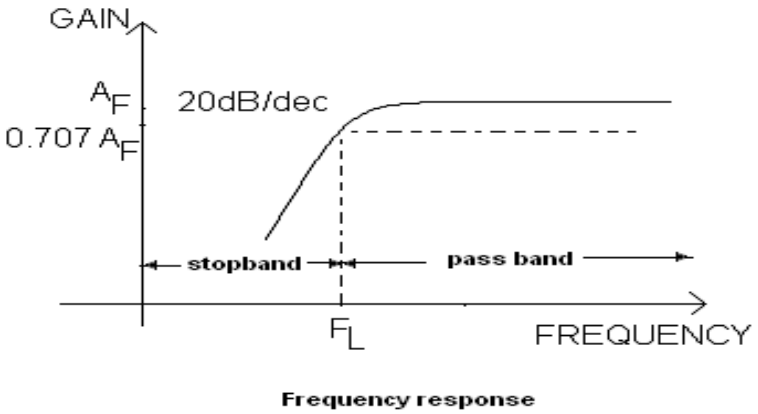
FIRST ORDER LOWPASS FILTERS

Active filters may be of different orders. A first order filter consists of a single RC network connected to the (+) input terminal of non-inverting op-amp amplifier. The resistors R_i and R_f determine the gain of the filter in the pass band.

HIGH PASS FILTER



MODEL WAVE FORM:



Frequency response

According to the voltage divider rule

$$\frac{V_a - V_i}{R} + \frac{V_a}{V_{cs}} = 0$$

$$V_a\left[\frac{1}{R} + CS\right] = \frac{V_i}{R} \Rightarrow V_a = \frac{V_i}{1 + Rcs}$$

At node '2' say voltage 'V_b'

$$\frac{V_b}{R_1} + \frac{V_b - V_o}{R_f} = 0 \Rightarrow V_b\left[\frac{1}{R_1} + \frac{1}{R_f}\right] = \frac{V_o}{R_f}$$

From virtual ground concept $V_a = V_b$

$$\frac{V_i}{1 + Rcs}\left[\frac{1}{R_1} + \frac{1}{R_f}\right] = \frac{V_o}{R_f}$$

$$\frac{V_o}{V_i} = \left[1 + \frac{R_f}{R_1}\right]\frac{1}{1 + Rcs} \quad \text{where } 1 + \frac{R_f}{R_1} = A_F$$

$$\frac{V_o}{V_i} = \frac{A_F}{1 + Rcs}; \textit{In steady state} \quad s = j\omega = \frac{V_o}{V_i} = \frac{A_F}{1 + Rcj\omega}$$

$$\frac{V_o}{V_i} = \frac{A_F}{1 + j(f/f_H)} \textit{ where } f_H = \frac{1}{2\pi RC}$$

$$\left|\frac{V_o}{V_i}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}} \qquad \Phi = -\tan^{-1}(f/f_H)$$

1. At very low frequency i.e , $f << f_H$ $\left|\frac{V_o}{V_i}\right| = A_F$

2. At $f = f_H$ $\frac{V_o}{V_i} = \frac{A_F}{\sqrt{2}} = 0.707A_F$

3. At $f > f_H$ $\frac{V_o}{V_i} < A_F$

Filter design:

1. Choose a value of higher cutoff frequency f_H.
2. Select a value of 'C' less than or equal to 1μF.

OBSERVATIONS:

High pass filter:

Input Voltage: 2V

S.NO.	FREQUENCY	$V_{O(P-P)}$ (V)	V_O / V_{IN}	20 log (V_O / V_{IN}) (dB)
				-20

3. Calculate the value of 'R' using $R=1/2\pi f_H C$.

4. Finally select the value of R_1 and R_F dependent on the desired pass band gain A_F using $A_F = 1+(R_F/R_1)$.

5. Select the feedback resistor in the order of in KΩ.

6. **Frequency scaling:** once the filter is designed and if we want to change this cutoff frequency then we have to use the frequency scaling factor to find the component values. So the frequency scaling is the conversion of original cutoff frequency 'f_H' into new cut off frequency f_H'.

7. New values $R' = (f_H / f_H')R$ or $C' = (f_H / f_H')C$.

First order Butterworth HPF:

Apply nodal analysis at node 'a' and voltage 'V_a'

$$\frac{V_a - V_i}{1/cs} + \frac{V_a}{R} = 0$$

$$V_a\left[\frac{1}{R} + CS\right] = V_i CS \Rightarrow V_a(1+RCS) = V_i(RCS)$$

$$= V_a = \frac{V_i RCS}{1+RCS}$$

Apply nodal analysis at node 'b'

$$\frac{V_b}{R_1} + \frac{V_b - V_o}{R_f} = 0 \Rightarrow V_0 = V_b\left[1+\frac{R_f}{R_1}\right]$$

From virtual ground concept $V_a = V_b$

$$V_o = \frac{V_i(RCS)}{1+RCS}\left[1+\frac{R_f}{R_1}\right] \text{ where } 1+\frac{R_f}{R_1} = A_F$$

$$\frac{V_o}{V_i} = \frac{A_F Rcs}{1+Rcs} \Rightarrow \frac{V_o}{V_i} = \frac{A_F}{1+\frac{1}{Rcs}}$$

In steady state

$$\frac{V_o}{V_i} = \frac{A_F Rcs}{1+Rcs} \Rightarrow \frac{V_o}{V_i} = \frac{A_F}{1+\frac{1}{Rc(j2\pi f)}}$$

Low Pass Filter:
Input Voltage =2V

S.No. .	Frequency (Hz)	V_o (p-p)	V_o/V_i	20 Log (V_o/V_i)

$$\frac{V_o}{V_i} = \frac{A_F}{1+\frac{1}{j}(f_L/f)} \Rightarrow \left|\frac{V_o}{V_i}\right| = \frac{A_F}{\sqrt{1+(f_L/f)^2}}$$

1. At low frequencies $f < f_L$ $\left|\frac{V_o}{V_i}\right| < A_F$

2. At $f = f_L$ $\left|\frac{V_o}{V_i}\right| = \frac{A_F}{\sqrt{2}} = 0.707\ A_F$

3. At $f > f_L$ $\left|\frac{V_o}{V_i}\right| > A_F$

Filter design:

1. Choose a value of lower cut off frequency f_L
2. Select a value of 'C' $\leq 1\mu F$.
3. Calculate the value of R using $f_L = \frac{1}{2\pi RC}$, $R = \frac{1}{2\pi f_L C}$
4. Finally select the value of R_1 and R_F dependent on the desired pass band gain A_F using $A_F = 1+ (R_F / R_1)$.

High pass filter:

1. Interchange the resistor R with capacitor 'C'. Adjust the input voltage Vin to 5Vp-p and frequency to 100Hz.

2. Measure the output voltage using oscilloscope and entered the measured value in Table2.

3. Repeat the step2 by varying the input signal frequency.

RESULT:

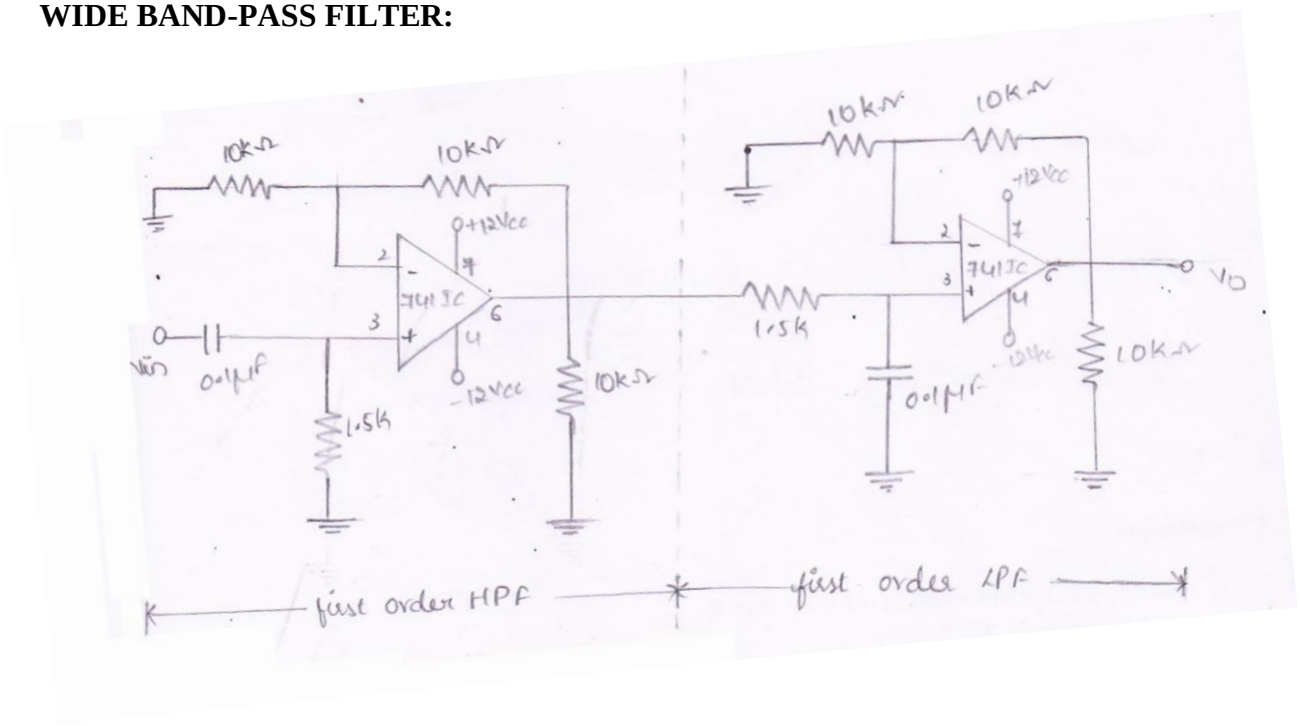
Hence the LPF and HPF are designed and its frequency response is obtained.

VIVA QUESTIONS :

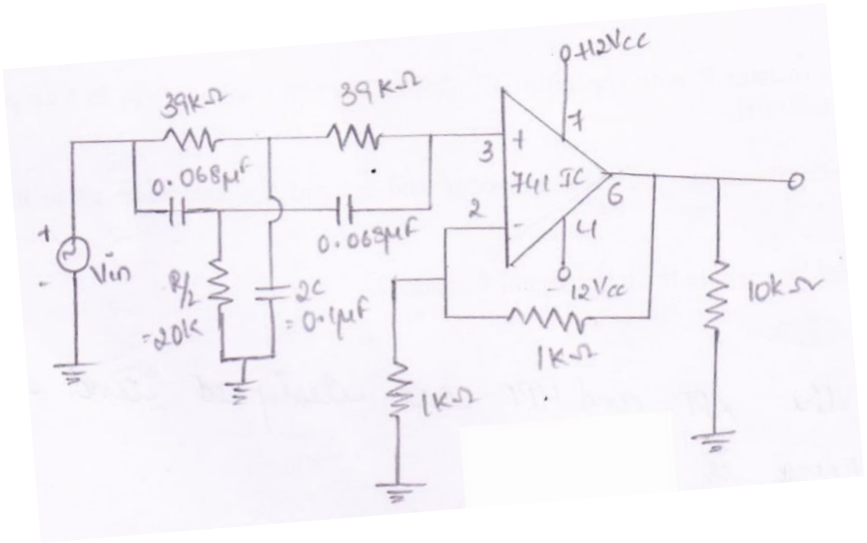
1. Define a filter.
2. List the most commonly used filters.
3. How filters are classified ?
4. What are the advantages active filters over passive filters ?
5. How can we achieve gain value greater than unity in active filters?

CIRCUIT DIAGRAMS:

WIDE BAND-PASS FILTER:



NARROW BAND-REJECT FILTER:



ACTIVE FILTER APPLICATIONS – BPF, (WIDE BAND) AND NOTCH FILTERS(NARROW BAND REJECT)

AIM:

To design a BPF (WBPF & NBPF) and BRF (WBRF & NBRF) for the given specifications and obtain frequency response.

APPARATUS:

S.No.	Device / Instrument	Range / Type	Quantity
1.	Cathode Ray Oscilloscope	Dual trace	1 No.
2.	Signal generator		1 No.
3.	Regulated power supply	0-30V	1 No.
4.	OP-AMP	IC μA 741	3

WBPF:

1.	Resistors	10KΩ 1.5 KΩ	6 No. 2 No.
2.	Capacitors	0.1μF	2 Nos.

NBRF:

1.	Resistors	20 KΩ 2 KΩ 10 KΩ	1 No. 2 Nos. 3 Nos
2.	Capacitors	0.068μF 0.136μF	2 No. 1 No.

THEORY:

BANDPASS FILTERS:

A Band pass filter has a passband between two cutoff frequencies f_H and f_L such that $f_H > f_L$. Any input frequency outside this passband is attenuated.

Basically, there are two types of bandpass filters:

(1) Wide band pass, and
(2) Narrow band pass.

Unfortunately, there is no set dividing line between the two. However, we will define a filter as wide band pass if its figure of merit or quality factor Q<10. On the other hand, if Q>10, we will call the filter a narrow band pass filter. Thus Q is a measure of selectivity, meaning the higher the value of Q, the more selective is the filter or the narrower its bandwidth (BW). The relation ship between Q , the 3-dB bandwidth , and the center frequency f_C is given by

$$Q = \frac{f_c}{BW} = \frac{f_c}{f_H - f_L}$$

Wide Band pass filter **Input Voltage:2V**

S.NO.	Frequency	$V_{O(P-P)}$ (V)	V_O / V_{IN}	20 log (V_O / V_{IN})

Narrow band pass filter **Input Voltage: 2V**

S.NO.	Frequency	$V_{O(P-P)}$ (V)	V_O / V_{IN}	20 log (V_O / Vin)

for the wideband pass filter the center frequency f_c can be defined as

$$f_c = \sqrt{f_H f_L}$$

Where f_H = high cutoff frequency (Hz)

f_L = Low cutoff frequency of wide band-pass filter (Hz)

In a narrow band-pass filter, the output voltage peaks at the center frequency.

BAND REJECT FILTERS:

The Band reject filter is also called a band-stop or band-elimination filter. In this filter, frequencies are attenuated in the stop band while they are passed outside this band, as shown in fig. As with band-pass filters, the band-reject filters can also be classified as

(1) Wide band-reject or
(2) Narrow band-reject.

The narrow band-reject filter is uncommonly called the notch filter. Because of its higher Q (>10), the bandwidth of this narrow band -reject filter is much smaller than that of the wide band-reject filter.

To design an active notch filter for a specific notch-out frequency f_N, choose the value of $C \leq 1\mu F$ and then calculate the required value of R from equation. For the best response, the circuit components should be very close to their indicated values.

FILTER DESIGN:

Wide Band Pass Filter:

HPF design : Let $f_L = 200Hz$

$$f_L = \frac{1}{2\pi RC} \quad assume\ C = 0.05\mu F$$

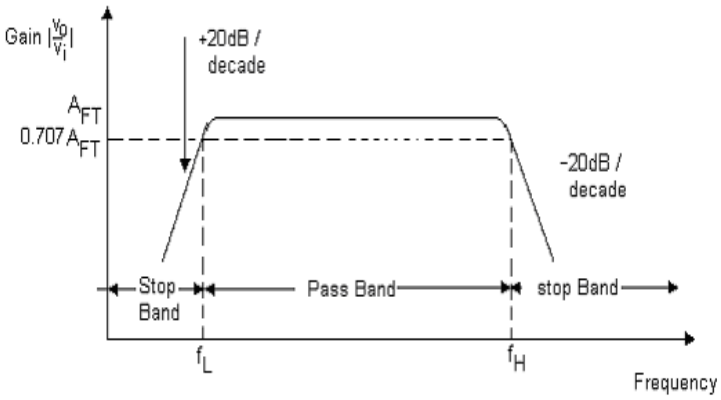
$$R = \frac{1}{2\pi f_L C} = 15.9K\Omega$$

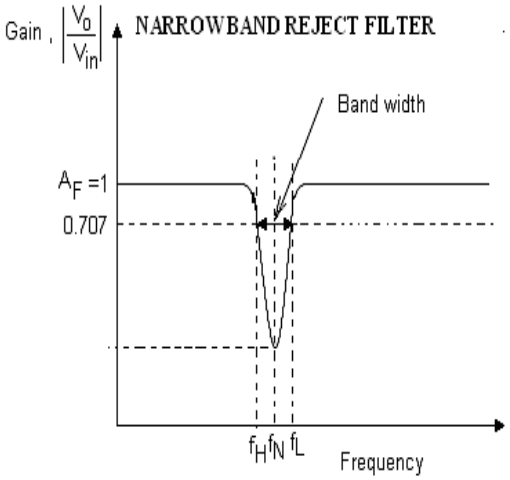
LPF Design : Let $f_H = 2KHz$

$$f_H = \frac{1}{2\pi RC} \qquad \text{assume } C = 0.01\mu F$$

MODEL WAVE FORMS: $R = \frac{1}{2\pi f_H C} = 15.9K\Omega$

WIDE BAND PASS FILTER:





Narrow Band Reject Filter:

$$f_N = \frac{1}{2\pi RC} \qquad \text{Let } C = 0.068\mu F$$

$$R = 39.01K\Omega$$

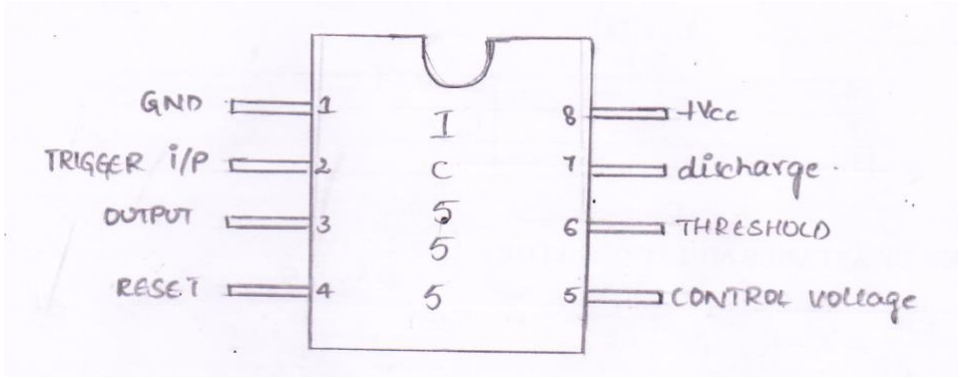
Procedure:

1. Connect the circuit as shown in circuit diagram.
2. Apply a sinusoidal signal of amplitude 1Vp-p as the input signal to the circuit.
3. Using the oscilloscope, measure the output voltage and enter the measured value in table.
4. Repeat the step3 by varying the input frequency.
5. Follow same procedure for different filters.

Result:

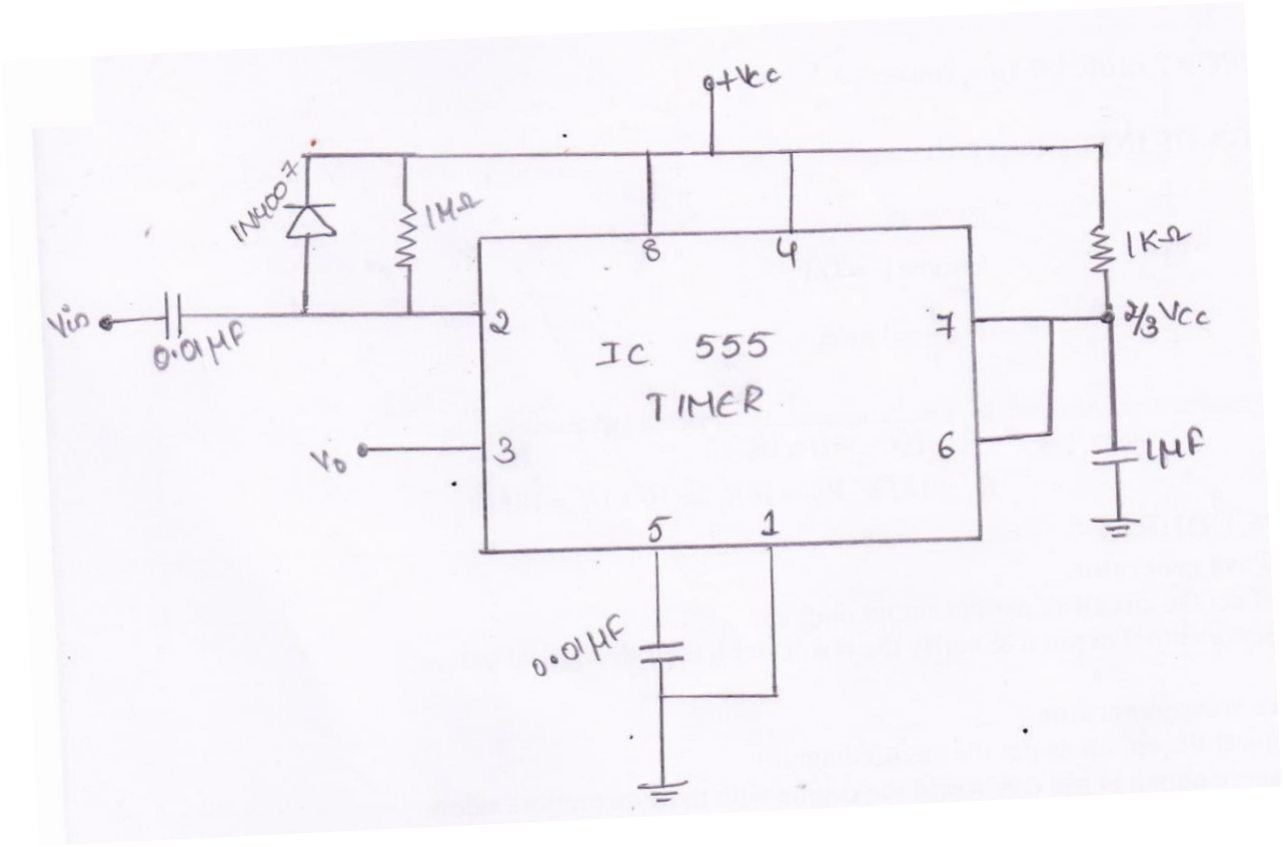
Hence the wide band and notch filters are designed for required specific values

PIN DIAGRAM:



QWE

CIRCUIT DIAGRAM



MONOSTABLE MULTIVIBRATOR USING IC 555 TIMER

AIM:

To design a monostable multivibrator with a pulse width of 1msec.

APPARATUS:

S.No.	Device / Instrument	Range / Type	Quantity
1.	Cathode Ray Oscilloscope	Dual trace	1 No.
2.	Signal generator		1 No.
3.	Regulated power supply	0-30V	1 No.
4.	IC	555	1 No.
5.	Resistors	1MΩ	1 No.
		1KΩ	1 No.
6.	Diode	1N4007	1 No.
7.	Capacitors	0.01μF	1 No.
		1 μF	1 No.
		0.001μF	1 No.

THEORY:

Figure (a) shows a 555 Timer connected for monostable operation and its functional diagram is shown in figure (b). In the standby state, FF holds transistor Q_1 **on**, thus clamping the external timing capacitor C to ground. The output remains at ground potential, i.e., LOW.

As the trigger passes through Vcc/3, the FF is set, i.e. $\overline{Q}$ =0. This makes the transistor Q_1 **off** and the short circuit across the timing capacitor C is released. As $\overline{Q}$ is LOW, output goes HIGH (=Vcc). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC as shown in fig..(c) b.

After a time period T (calculated later) , the capacitor voltage is just greater than (2/3) Vcc and the upper comparator resets the FF , that is , R= 1, S=0 (assuming very small trigger pulse width) . This makes $\overline{Q}$ =1, transistor Q_1 goes on (ie, saturates), thereby discharging the capacitor C rapidly to ground

potential. The output returns to the standby state or ground potential The voltage across the capacitor as shown in figure is given by

$$V_c = V_{cc}(1 - e^{-t/RC}) \quad -->1$$

$AT \quad t = T \;, \quad V_c = (2/3)V_{cc}$

$Therefore, \quad (2/3)V_{cc} = V_{cc}(1 - e^{-T/RC})$

or, $T = RC \ln (1/3)$

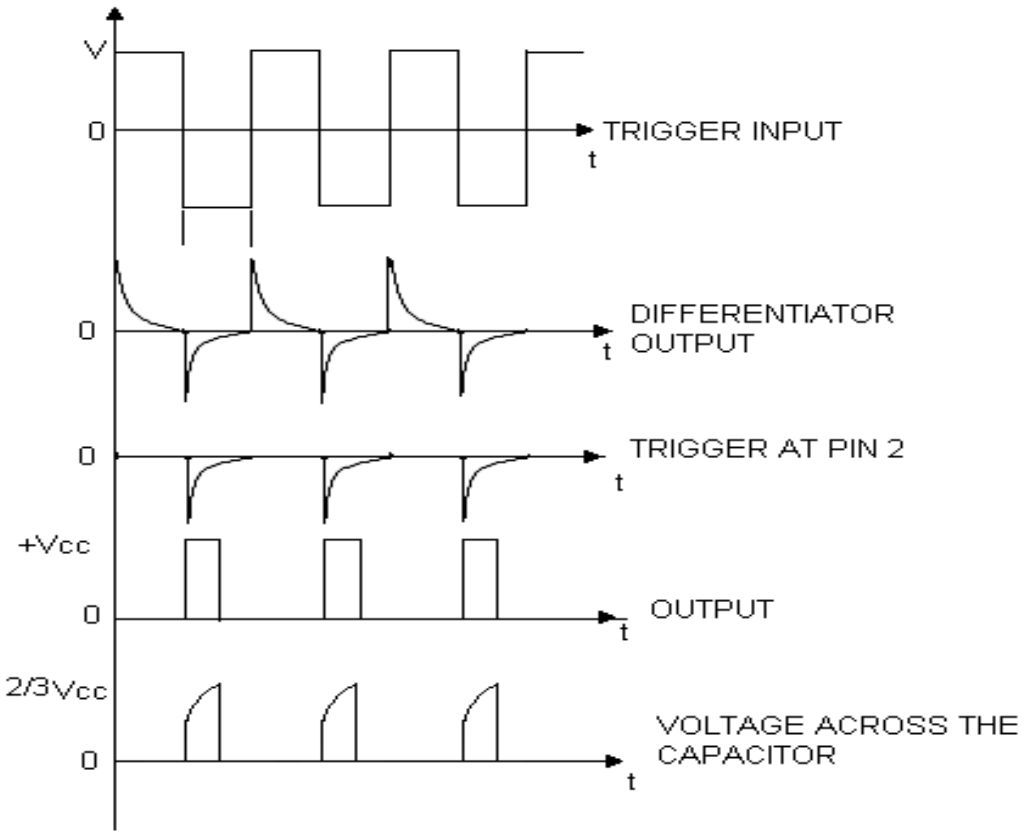
$$T = 1.1RC \text{ (seconds)} \quad -->2$$

It is evident from equation (2) that the timing interval is independent of the supply voltage. It may also be noted that once a triggered , the output remains in the HIGH state until time T elapses, which depends only upon R and C. any additional trigger pulse coming during this time will not change the output state.

OBSERVATIONS:

RC components		**Theoretical o/p waveform results**	**Practical output waveform results**	**Voltage across the capacitor**			
R	C	T = 1.1 RC	T	Theoretical		Practical	
				V_{min} =0	V_{max}=2/3 V_{CC}	V_{min}= 0	V_{max} = 2/3V_{CC}

MODEL WAVE FORMS:



However, if a negative going reset pulse as shown in fig (c) d. is applied to reset terminal (pin-4) during the timing cycle , transistor Q_2 goes **off**, Q_1 becomes ON and the external timing capacitor C is immediately discharged. The output now will be as shown in figure ©(e). It may be seen that the output of Q_2 is connected directly to the input of Q_1 so as to turn **on** Q_1 immediately and thereby avoid the propagation delay through the FF. Now,

If the reset is released, the output will still remained LOW until a negative going trigger pulse is again applied at pin2. Figure (d) shows the graph of various combinations of R and C necessarly to produce a given time delay.

Sometimes the monostable circuit of fig (a) mistriggers on positive pulse edges, even with the control pin bypass capacitor. To prevent this , a modified circuit as shown in fig (e) is used. Here the resistor and capacitor combination of 10KΩ and 0.001μF at the input forms a differentiator. During the positive going edge of the trigger, diode D becomes forward biased, thereby limiting the amplitude of the positive spike to 0.7V

DESIGN PROCEDURE:

Design of Differentiator circuit:

$R_1C_1 << T$

$f = 100Hz$

$T = 1/f = 0.1ms$

assume $C_1 = 0.01\mu F$

$R_1C_1 << T$

$R_1 \text{ x } 0.01\mu F << 0.1\text{ms}$

$R_1 = 1M\Omega$

Design of Monostable multivibrator circuit:

$$V_C = V_{CC}\left(1 - e^{-t/RC}\right)$$

$$\tau = T, \quad V_c = \frac{2}{3} \times V_{cc}$$

$$\frac{2}{3}V_{cc} = V_{cc}\left(1 - e^{-t/RC}\right)$$

$$\frac{2}{3} = 1 - e^{-t/RC}$$

$$\therefore \frac{T}{RC} = 1.1$$

$$T = 1.1RC$$

$$T = 1m\sec$$

$$assume \;\; C = 1\mu f$$

$$\therefore R = \frac{1.1 \times 1 \times 10^{-6}}{1 \times 10^{-3}} \approx 1K\,\Omega$$

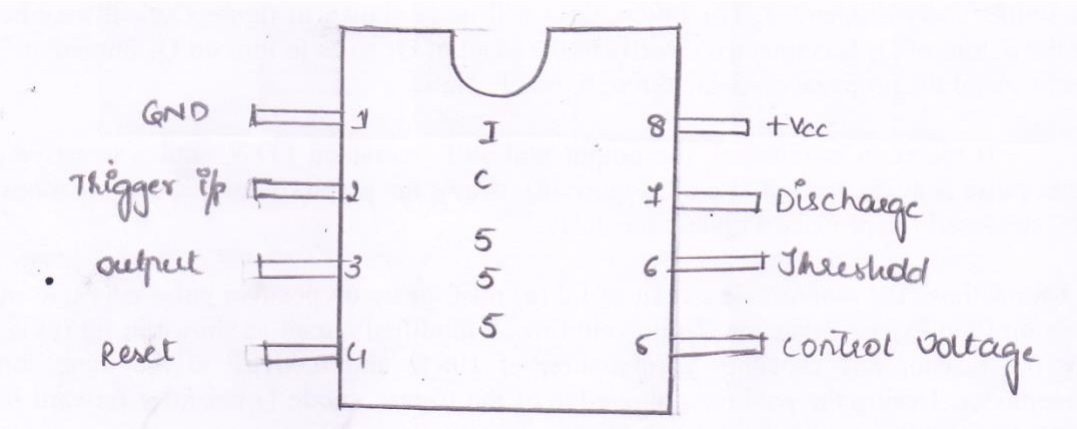
PROCEDURE:

1. Apply an i/p signal wave of 1KHz frequency with 8V (p-p)
2. Apply a (-Ve) trigger pulse at pin no. 2
3. Observe and note down the output waveform at pin number 3.
4. Calculate pulse width theoretically and practically and compare them

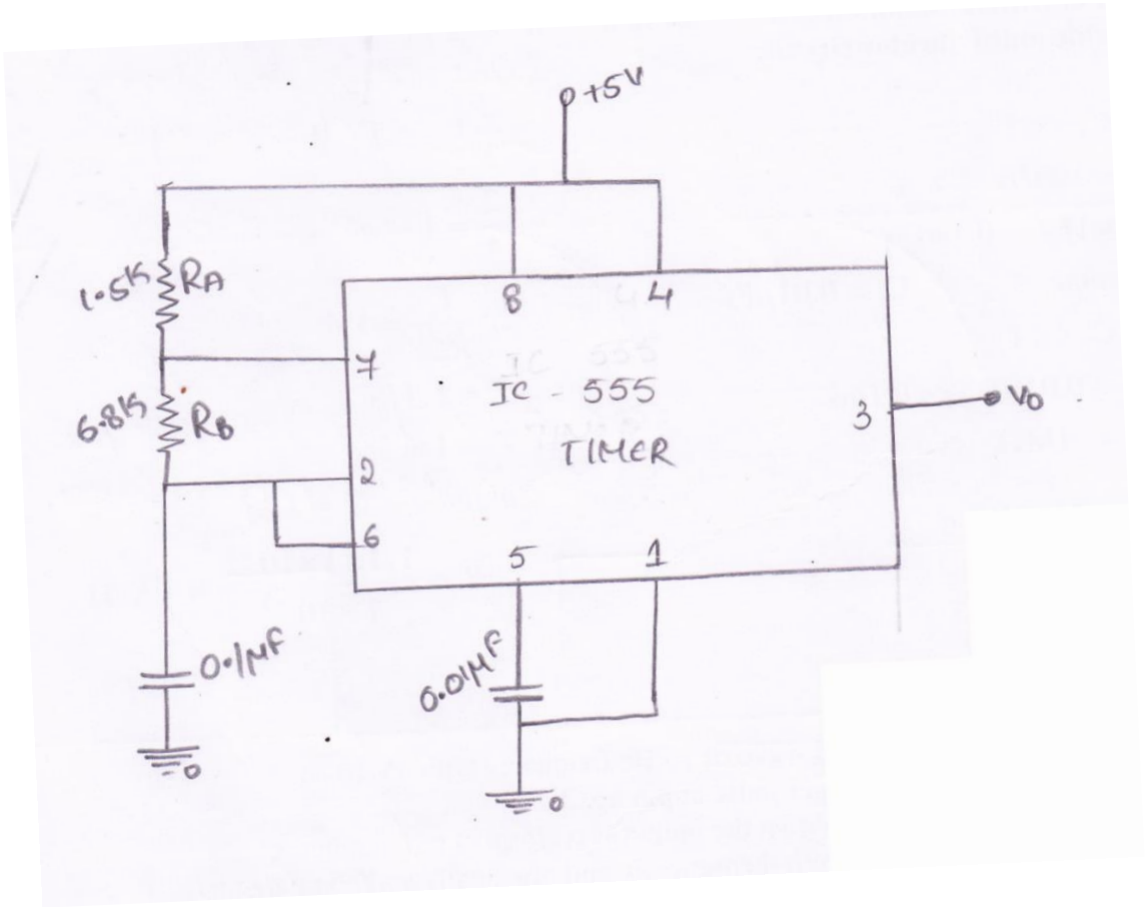
RESULT:

Hence the design of monostable multivibrator with a pulse width of 1msec is done using ic 555 timer

PIN DIAGRAM:



CIRCUIT DIAGRAM:



IC 555 TIMER – ASTABLE MULTIVIBRATOR CIRCUIT

AIM:

To design Astable multivibrator using 555 IC.

APPARATUS:

S.No.	Device / Instrument	Range / Type	Quantity
1.	Cathode Ray Oscilloscope	Dual trace	1 No.
2.	Signal generator		1 No.
3.	Regulated power supply	0-30V	1 No.
4.	IC	555	1 No.
5.	Resistors	1.5KΩ	1 No.

		6.8KΩ	1 No.
6.	Capacitors	0.1μF	1 No.
		1 μF	1 No.

THEORY:

ASTABLE OPERATION:

The device is connected for astable operation as shown in fig (1). For better understanding, the complete diagram of astable multivibrator with detailed internal diagram of 555 is shown in fig (2).

Comparing with monostable operation, the timing resistor is now split in to two sections R_A and R_B. Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B. When the power supply Vcc is connected, the external timing capacitor C charges towards Vcc with a time constant $(R_A + R_B)C$. During this time, output (pin3) is high (equals Vcc) as Reset R=0, Set S=1, and this combination makes $\overline{Q}=0$ which has unclamped the timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) Vcc the upper comparator triggers the control flip flop so that $\overline{Q}=1$. This, in turn makes transistor Q_1 **on** and capacitor C starts discharging towards ground through R_B and transistor $Q_1$with a time constant R_BC (neglecting the forward resistance of Q_1). Current also flows into transistor Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1. The minimum value of R_A is approximately equal to Vcc/0.2 where 0.2A is the maximum current through the **on** transistor Q_1.

During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) Vcc/3, the lower comparator is triggered and at this stage S=1,R=0, which turns $\overline{Q}=0$. Now $\overline{Q}=0$ unclamps the external timing capacitor C. The capacitor C is thus

periodically charged and discharged between 2/3 Vcc and 1/3 Vcc respectively. Figure (3) shows the timing sequence and capacitor voltage wave form. The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3)Vcc to (2/3)Vcc. It may be calculated as follows:

The capacitor voltage for a low pass RC circuit subjected to a step input of Vcc volts is given by

$$V_c = V_{cc}(1 - e^{-t/RC})$$

The time taken by the circuit to charge from 0 to (2/3)Vcc is ,

$$(2/3)Vcc = V_{cc}(1 - e^{-t/RC})$$
$$t_1 = 1.09RC$$

And the time t_2 to charge from 0 to (1/3) Vcc is

$$(1/3)Vcc = V_{cc}(1-e^{-t_2/RC})$$

$$t_2 = 0.45RC$$

So the time to charge from (1/3)Vcc to (2/3)Vcc is

$T_{HIGH} = t_1 - t_2$

$T_{HIGH} = 1.09RC - 0.405RC = 0.69RC$

So, for the given circuit,

$T_{HIGH} = 0.69(R_A + R_B)C$

The output is low wile the capacitor discharges from (2/3)Vcc to (1/3)Vcc and the voltage across the capacitor is given by

$$(1/3)Vcc = (2/3)V_{cc}(1-e^{-t/RC})$$

Solving, we get t=0.69RC
So, for the given circuit , $t_{LOW} = 0.69R_BC$

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore , total time ,

$$T = T_{HIGH} + T_{LOW}$$

$$T = 0.69(R_A + 2R_B)C$$

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T=(t_{ON}+t_{OFF})$. In this circuit, when the transistor Q_1 is **on**, the output goes low. Hence,

$$D\% = \frac{T_{LOW}}{T} X100 \; ; \qquad = \frac{R_B}{R_A + 2R_B} X100$$

Calculation Theoretical :

$T_H=0.69R_aC+0.69R_bC$
$=0.69(1.5+6.8)10^3x0.1x10^{-6}$
$=0.56ms$
$T_L= 0.69R_bC$
$=0.69x10^3x6.8x0.1x10^{-6}$
$= 0.46$ ms

Duty Cycle :

$D = T_{ON} / (T_{ON}+T_{OFF})$
$=0.56 / (0.56+0.46)$
$=55.3\%$

Practical :

T_H =0.56 ms T_L=0.46 ms

D = T_{ON} / (T_{ON}+T_{OFF})
=0.56 / (0.56+0.48)
= 56.3%

DESIGN PROCEDURE:

The capacitor voltage for low pass RC circuit subjected to a step input of Vc volts is given by

$$V_C = V_{CC}(1 - e^{-t/RC})$$

The Time taken by the circuit to charge from 0 to 2/3 Vcc is

$$\frac{2}{3}V_{CC} = (1 - e^{-t/RC})V_{CC}$$

$$t_1 = 1.09RC$$

And the time t_2 charges form 0 to 1/3 Vcc is

$$\frac{1}{3}V_{CC} = (1 - e^{-t/RC})V_{CC}$$

$$t_2 = 0.405RC$$

So the time charge from 1/3 Vcc to 2/3 Vcc is $t_{high} = t_1 - t_2 = 0.69RC$

For given circuit $T_{high} = 0.69(R_a + R_b)C$

The voltage across the capacitor under discharge conditions is given by

$$\frac{1}{3}Vcc = \frac{2}{3}Vcc \cdot e^{-t/RC}$$

for our circuit $T_{LOW} = 0.69R_bC$

The totl time is $T = T_{HIGH} + T_{LOW} = 0.69(R_a + 2R_b)$

$$F = \frac{1}{T} = \frac{1.45}{(R_a + 2R_b)C}$$

Duty cycle of the output wav eform is given by

Duty cycle $D = \frac{T_{ON}}{T_{ON} + T_{OFF}}$

Assume duty cycle $D = 45\%$

$$0.45 = \frac{R_B}{R_A + 2R_B}$$

$$R_B = 0.45(R_A + 2R_B)$$

$$R_B = 0.45R_A + 0.9R_B$$

$$0.1R_B = 0.45R_A$$

$$R_B = \frac{9}{2}R_A$$

$$F = \frac{1}{T} = \frac{1.45}{(R_a + 2R_b)C}$$

Assume $C = 0.1\mu F$

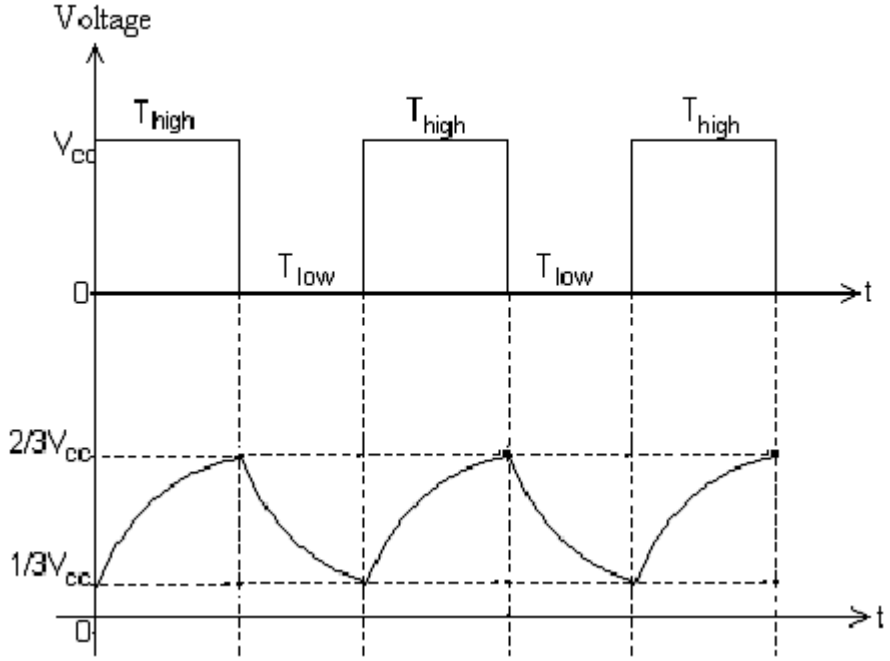
$R_A = 1.45K\Omega$ and $R_B = \frac{9}{2}R_A = 6.625K\Omega$

With the circuit configuration of Fig..(1) it is not possible to have a duty cycle more than 50% since $t_{HIGH}=0.69(R_A+R_B)C$ will always be greater than $t_{LOW} = 0.69R_BC$. In order to obtain a symmetrical

OBSERVATIONS:

(Theoretical) Designed o/p waveform results				(Practical) Output waveform results				*Voltage across the capacitor*			
								Theoretical		Practical	
T_H	T_L	Duty cycle	Frequency	T_H	T_L	Duty cycle	Frequency	$V_{min} = 1/3\ V_{CC}$	$V_{max} = 2/3\ V_{CC}$	V_{min}	V_{max}

MODEL WAVEFORMS:



square wave i.e. D=50%, the resistance R_A must be reduced to zero. However, now pin7 is connected directly to Vcc and extra current will flow through $Q_1$when it is **on**. This may damage Q_1 and hence the timer.

An alternative circuit which will allow duty cycle to be set at practically any level is shown in fighur 8.19. During the charging portion of the cycle, diode D_1 is forwardbiased effectively short circuiting R_B so that

$$T_{HIGH} = 0.69R_AC$$

However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So

$$t_{LOW} = 0.69R_BC$$

$$T = t_{HIGH} + t_{LOW} = 0.69(R_A + R_B)C$$

$$f = \frac{1.45}{(R_A + R_B)C}$$

and duty cycle $$D = \frac{R_B}{R_A + R_B}$$

Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width. However, a series resistor of at least 100Ω (fixed) should be added to each R_A and R_B. This will limit peak current to the discharge transistor Q_1 when the variable resistors are at minimum value. And, if R_A is made equal to R_B, then 50% duty cycle is achieved.

Symmetrical square wave generator by adding a clocked JK flip-flop to the output of the nonsymmetrical square wave generator is shown in figure 8.20. The clocked flip-flop acts as binary divider to the timer output. The output frequency in this case will be one half that of the timer. The advantage of this circuit is of having output of 50%duty cycle without any restriction on the choice of R_A and R_B .

PROCEDURE:

1. Connect the circuit as per the Circuit diagram.
2. Connect the o/p (at Pin no. 3) to CRO.
3. Measure the T_{ON} and T_{OFF} and compare with theoretical values from this formula.

   D = T_{ON} /(T_{ON}+T_{OFF})

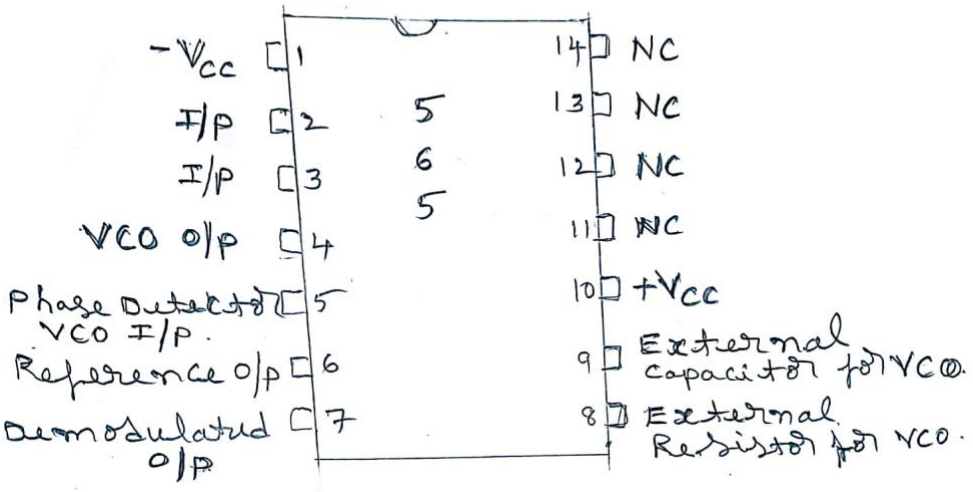
RESULT:

Hence the astable multivibrator using ic 555timer is designed and its operation is studied and observed.

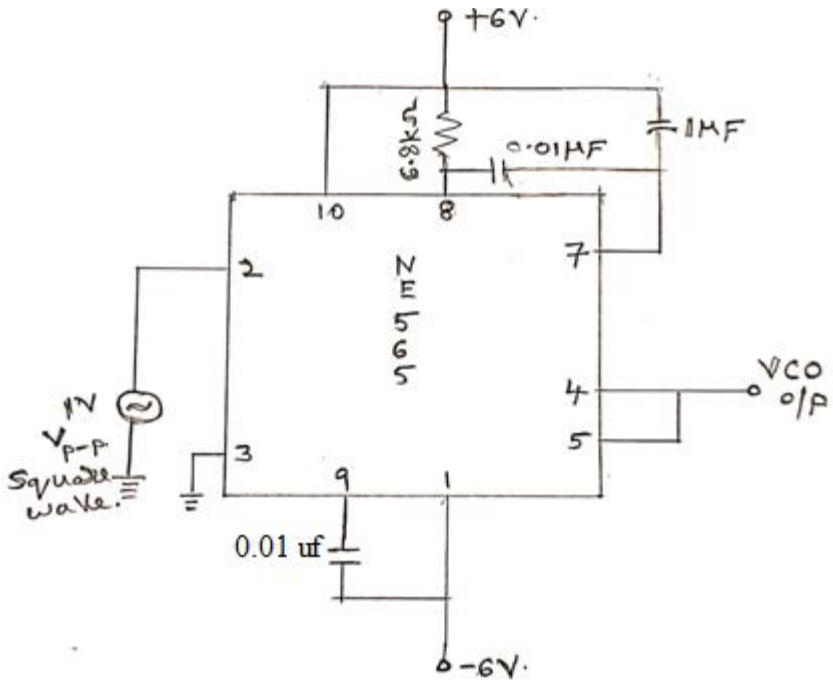
VIVA QUESTIONS :

1. What are the other applications of 555 timer?
2. What are the modes of operation of a 555 timer?
3. What is the significance of control pin?
4. What is the other name for the Astable multivibrator?

PIN DIAGRAM:



CIRCUIT DIAGRAM



IC 565 –PLL APPLICATIONS

AIM:

To calculate free running frequency, lock range and Capture range for a given PLL and Compare them with their theoretical values using 565 IC.

APPARATUS

S.No.	DEVICE / INSTRUMENT	TYPE /RANGE	QUANTITY
1	Cathode Ray Oscilloscope	Dual trace	1 No.
2	Signal generator		1 No.
3	Regulated power supply	0-30V	1 No.
4	IC	565	1 No.
5	Resistors	6.8KΩ	1 No.
6	Capacitors	0.01μF	2 Nos.
		1 μF	1 No

THEORY:

The Phase Locked Loop is an important building block of linear systems. Electronic Phase Locked Loop (PLL) came into vogue in the 1930s, when it was used for RADAR synchronization and communication applications. The high cost of realizing PLL in the discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, Air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL and important applications are discussed.

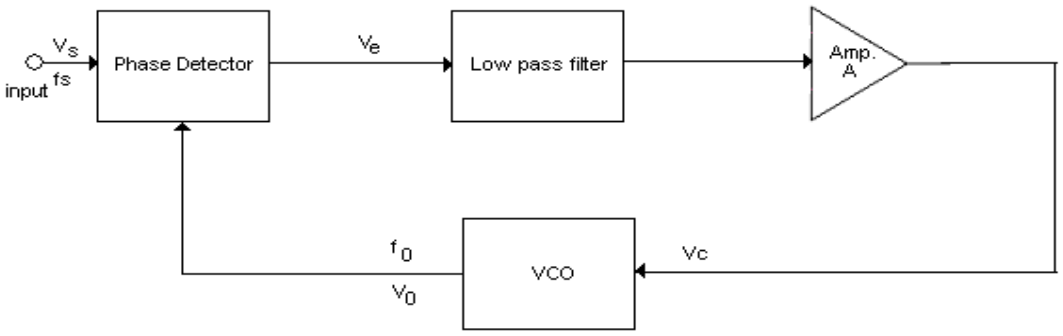


Figure 1: Block diagram of the PLL

CALCULATIONS:

1. Free running frequency $f_0 = \frac{0.25}{R_T C_T}$

2. Lock - Range $(f_{L2} - f_{L1}) = f_L = \pm \frac{7.8 f_0}{12}$

3. Capture Range $(f_{C2} - f_{C1}) = f_C = \left[\frac{\Delta f_L}{2\pi \text{ x } 3.6 \text{ x } 10^3 \text{ x } C} \right]^{1/2}$

OBSERVATIONS:

1. Free running frequency f_0 =41.15 KHz

2. Lock Range f_{L1} = 41.21 KHz

f_{L2} = 65.1KHz

$(f_{L1} - f_{L2})$ = 23.98KHz

3. Capture Range f_{c1} = 38.51 KHz

f_{c2} = 40 KHz

$(f_{c2} - f_{c1})$ = 1.49 KHz

Theoretical Values			**Practical Values**		
$f_O = \frac{0.25}{R_T C_T}$	$f_C = \pm \left[\frac{\Delta f_L}{2\pi (3.6 \text{ x } 10^3) C} \right]^{1/2}$	$f_L = \pm 7.8 \frac{f_O}{V}$	f_O	f_C	f_L

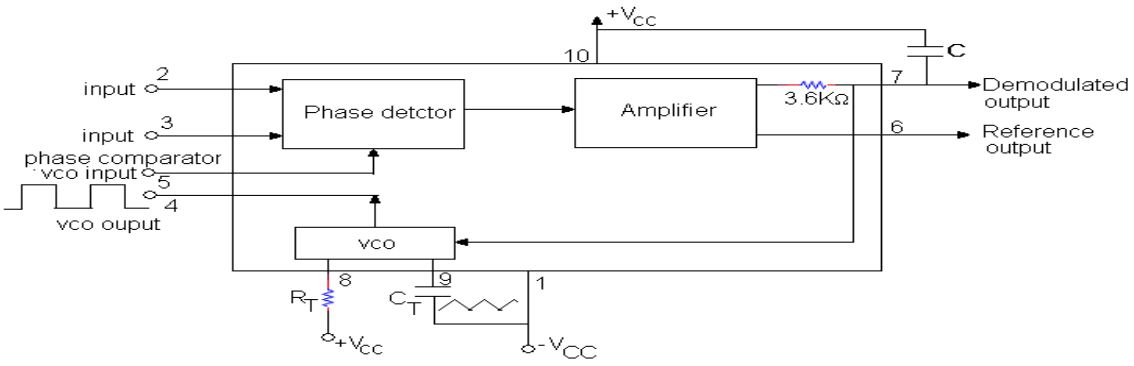


Figure 2: FUNCTIONAL DIAGRAM

The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference Φ. This phase difference Φ generates a

Some of the important definitions in relation to PLL are:

LOCK-IN RANGE: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_o, the VCO frequency.

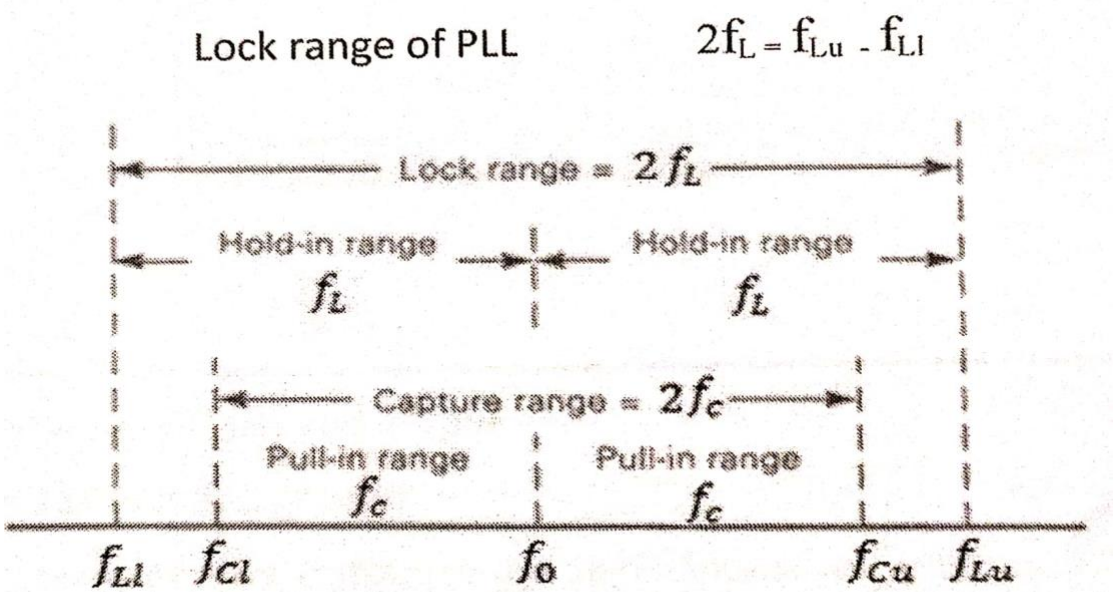
CAPTURE RANGE: The range of frequencies over which the PLL can acquire Lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.

PULL-IN TIME: The total time taken by the PLL to establish Lock is called Pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the over all loop gain and loop filter characteristics.

The important electrical parameters of 565 PLL are:

Operating frequency range	:	0.001Hz to 500 KHz
Operating voltage range	:	±6V to ±12V.
Input level	:	10mV rms min. to 3V pp max
Input impedance	:	10KΩ typical
Output sink current	:	1mA typical
Drift in VCO center frequency with temperature	:	300 ppm/^{0}C. (Parts per million per degree centigrade)
With supply voltage	:	1.5 percent / V max
Triangle wave amplitude	:	2.4 Vpp at ±6V supply voltage
Square wave amplitude	:	5.4 Vpp at ±6 V supply voltage
Bandwidth adjustment range	:	<± 1 to ± 60 %

Lock range of PLL $2f_L = f_{Lu} - f_{Ll}$



PLL capture and Lock ranges

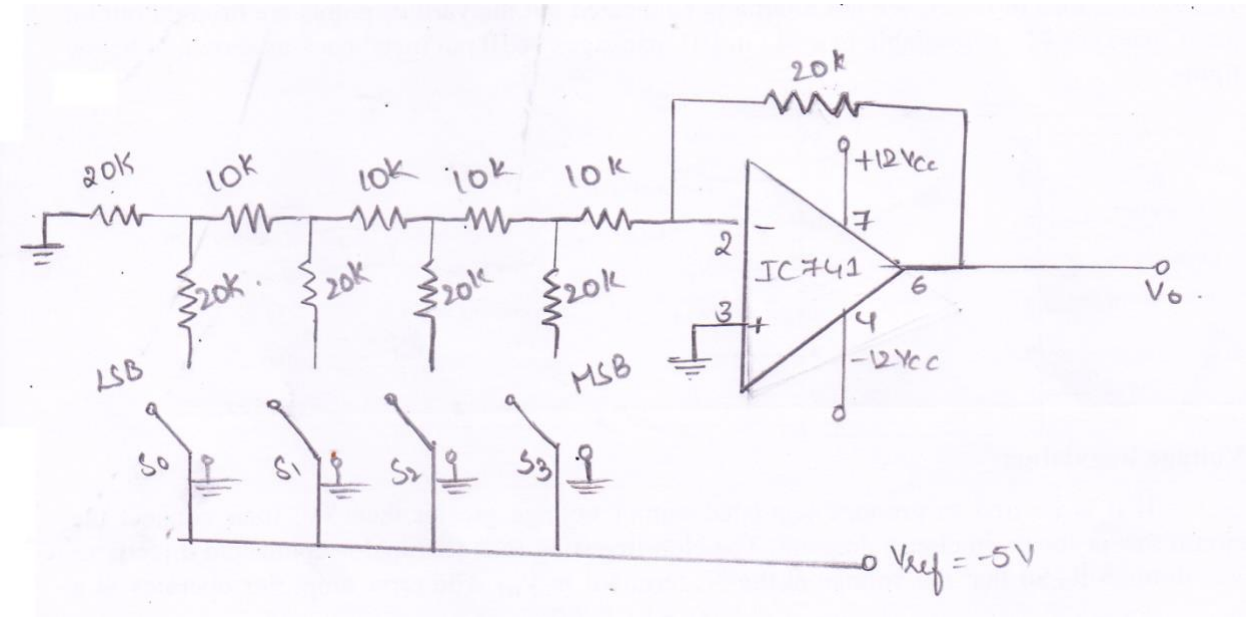
PROCEDURE:

1. Connect the circuit as shown in circuit diagram.
2. Measure the free running frequency VCO at pin 4 with the input signal V_{in}, set equal to zero.
3. Apply the input signal of $1V_{(P-P)}$ square wave at 1KHz at pin2. Connect the signal to channel of CRO.
4. Gradually increase the input frequency till the PLL is locked to the input frequency. The frequency gives the lower end of capture range (f_{C1}). Go on increasing the input signal frequency till PLL tracks the input signal. This frequency gives upper end of the Lock range (f_{L2}).
5. Gradually decrease the input signal frequency till the PLL is again locked. This is the Upper end of the Capture range (f_{C2}). Keep on decreasing the input signal until the loop is unlocked. This frequency gives lower end of the Lock range (f_{L1}).
6. Compare the practical values with their theoretical values.

RESULT:

The free running frequency lock range and capture range for a given PLL is calculated and compared with theoretical values using 565 IC.

CIRCUIT DIAGRAMS:



4 BIT DAC USING OP-AMP

AIM:

To construct a 4 bit R-2R ladder type digital to analog converter and realize.

APPARATUS:

S.No.	Device/Components required	Range	Quantity
1.	Regulated power supply	0-30V	1 No.
2.	OP-AMP	741	1 No.
3.	RESISTORS	10KΩ	4 No.
		20KΩ	6 No.

THEORY:

BASIC DAC TECHNIQUES:

The schematic of DAC is shown in fig (1). The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = KV_{FS}(d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n}) \quad \ldots \quad (1)$$

where V_o = output voltage

V_{FS} = Full scale output voltage

K = scaling factor usually adjusted to unity

$d_1, d_2, \ldots d_n$ = n-bit binary fractional word with the decimal point located at the left.

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = Least significant bit (LSB) with a weight of $V_{FS}/2^n$

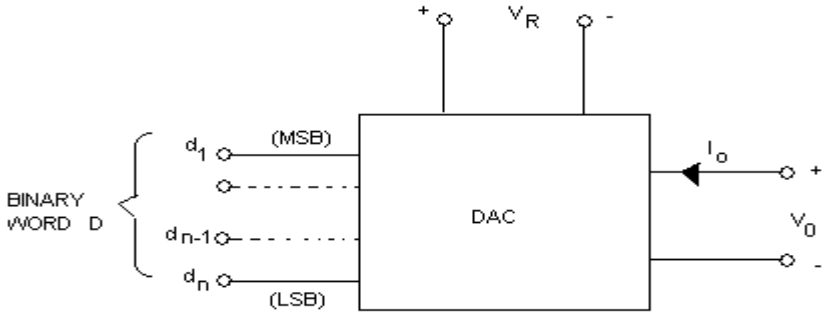


Fig (1): Schematic of a DAC

There are various ways to implement equation 1, R-2R ladder one type of DAC.

R-2R Ladder DAC:

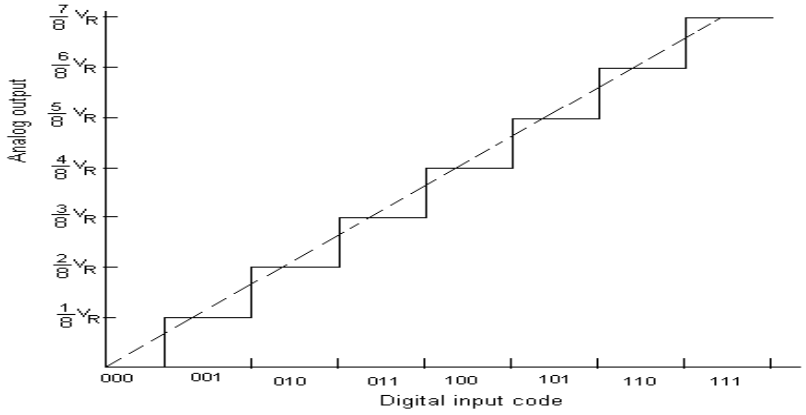
Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5KΩ to 10KΩ.

For simplicity, consider a 3-bit DAC as shown in fig. where the switch position d_1, d_2 and d_3 corresponds to the equivalent binary word 100. The circuit can be simplified to the equivalent

OBSERVATIONS:

S.No.	Digital Data				Equivalent Analog Voltage (Theoritical)	Equivalent Analog voltage (practical)
	D_3	D_2	D_1	D_0		

MODEL WAVEFORM:



form of fig 2(b) and finally to fig 2(c). Then the voltage at node C can be easily calculated by the set procedures of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R}=-\frac{V_R}{4}$$

Fig (2): a. R-2R ladder DAC b. Equivalent circuit of (a) c. Equivalent circuit of (b)

The output voltage

$$V_0=\frac{-2R}{R}\left(-\frac{V_R}{4}\right)=\frac{V_R}{2}=\frac{V_{FS}}{2}$$

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in fig 3(a).The circuit can be simplified to the equivalent form of fig 3(b). The voltages at nodes (A, B, C) formed resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_0=\frac{-2R}{R}\left(-\frac{V_R}{16}\right)=\frac{V_R}{8}=\frac{V_{FS}}{8}$$

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

PROCEDURE:

1. Set up the DAC circuit as shown in figure.
2. All the inputs A, B, C, D are shorted to the ground.
3. Measure the output voltage for all binary combinations 0000 to 1111.
4. Measure the size of each step and hence calculate the resolution $V_{fs}/2^n$-1.
5. Plot the graph for the combinations from 0000 to 1111 and find out the step size maximum V_o for all bits.

RESULT:

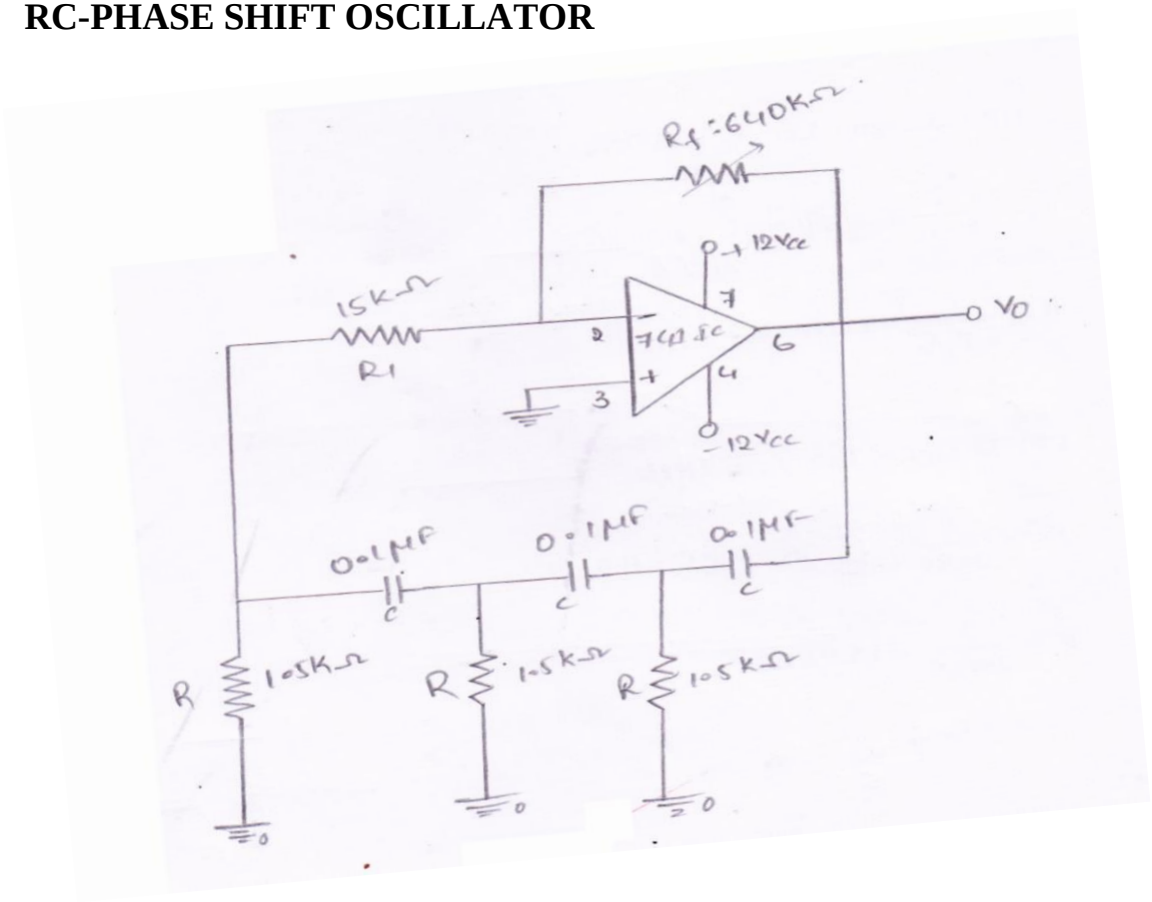
Hence the 4 bit R -2R ladder type digital to analog converter is constructed and reduised

VIVA QUESTIONS :

1. What are the applications of DAC ?
2. What is disadvantage of weighted resistor DAC ?
3. What is mea by linearity of DAC ?

CIRCUIT DIAGRAMS:

RC-PHASE SHIFT OSCILLATOR



IC 741 OSCILLATOR CIRCUITS –PHASE SHIFT AND WIEN BRIDGE OSCILLATORS

AIM:

1. To design and verify a RC-Phase shift Oscillator for a given frequency.
2. To design and verify a Wien bridge Oscillator for a given frequency.

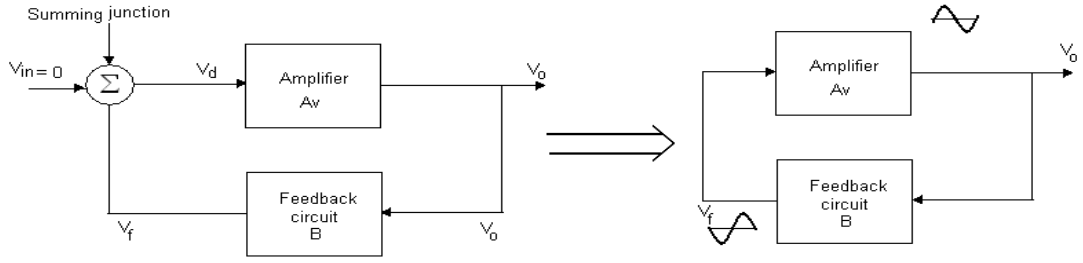
APPARATUS:

S.No.	Device / Instrument	Range / Type	Quantity
1.	Cathode Ray Oscilloscope	Dual trace	1 No.
2.	Signal generator	---	1 No.
3.	Regulated power supply	0-30V	1 No.
4.	IC	741	1 No.
5.	Resistors	1.5KΩ	3 No.
		10 KΩ	2 No.
		15KΩ	2 No.
6.	Capacitors	0.1μF	3 No.
7.	Decade Resistance Box	---	1 No.

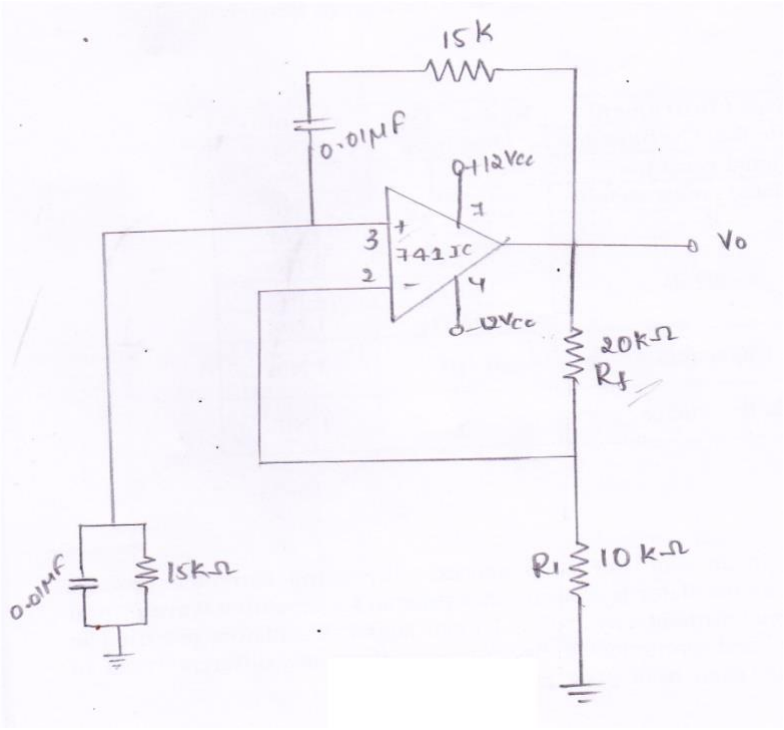
THEORY:

OSCILLATORS:

Basically the function of an oscillator is to generate alternating current or voltage waveforms. More precisely, an oscillator is a circuit that generates a repetitive waveform of fixed amplitude and frequency without any external input signal. Oscillators are used in radio, television, computers, and communications. Although there are different types of oscillators, they all work on the same basic principle.



WIEN BRIDGE OSCILLATOR



Oscillator principles:

An oscillator is a type of feedback amplifier in which part of the output is fed back to the input via a feedback circuit. If the signal fed back is of proper magnitude, and phase, the circuit that produces alternating currents or voltages. To visualize the requirements of an oscillator, consider the block diagram of figure. This diagram looks identical to that of the feedback amplifiers. However, here the input voltage is zero (V_{in} = 0). Also, the feedback is positive because most oscillators use positive feedback.

Using these relationships, the following equation is obtained:

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 - A_v B}$$

However, $V_{in} = 0$ and $V_0 \neq 0$ implies that

$$A_v B = 1$$

Expressed in polar form,

$$A_v B = 1\angle 0^0 \, or \, 360^0$$

Equation gives the two requirements for oscillation: (1) the magnitude of the loop gain A_vB must be at least 1, and (2) the total phase shift of the loop gain A_vB must be equal to 0^0 or 360^0. For instance, as indicated in figure, if the amplifier causes a phase shift of 180^0, the feedback must provide an additional phase shift of 180^0 so that the total phase shift around the loop is 360^0, the waveforms are sinusoidal and are used to illustrate the action. The type of waveform generated by an oscillator depends on the components in the circuit and hence may be sinusoidal, square, or triangular. In addition, the frequency of oscillation is determined by the components in the feedback circuit.

RC-Phase Shift Oscillator:

The Phase Shift Oscillator is constructed with an inverting mode and phase shift network in the feedback loop. The two conditions that are to be satisfied for any oscillator circuit are

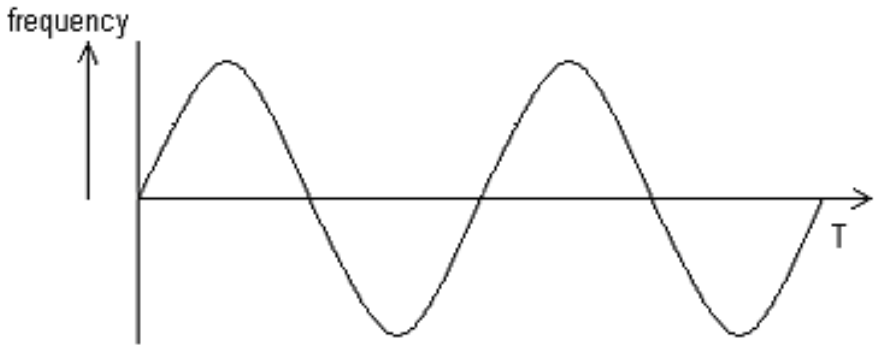
1 Unity voltage gain i.e., $|A\beta| = 1$. This is achieved in the phase shift Oscillator by ensuring that at resonance conditions of the circuit. The gain of the amplifier is $\frac{R_f}{R_1} = 29$ and the response frequency is given by

$$f_0 = \frac{1}{2\pi\sqrt{6RC}}$$

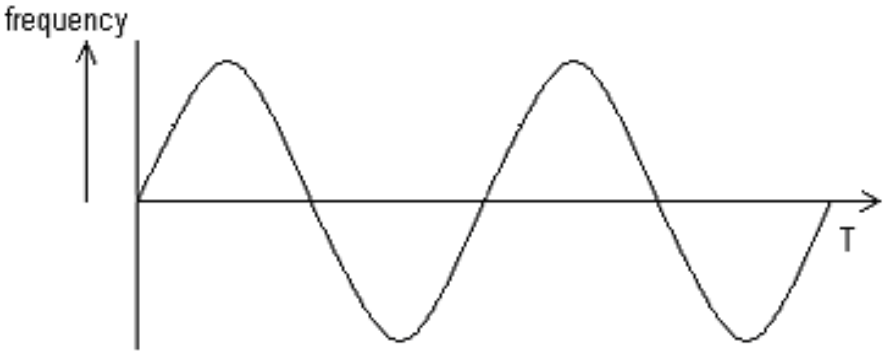
2 The total phase shift around the loop is zero or 360^0 .Since the inverting amplifier produces a phase shift of 180^0. The RC phase shift network produces and additional phase shift of 180^0. Besides this RC network selects the frequency of operations as given in the above equation.

MODEL WAVE FORMS:

RC PHASE SHIFT OSCILLATOR



WIEN BRIDGE OSCILLATOR



DESIGN:

RC-PHASE SHIFT OSCILLATOR:

$$\mathbf{f_0} = 400 \text{ Hz.}$$

$$f_0 = \frac{1}{2\pi RC\sqrt{6}}$$

Let $C = 0.1\mu F$

Therefore $R = \frac{1}{2\pi \text{ x } 0.1 \text{x} 10^{-6} \text{ x } \sqrt{6} \text{ x } 400} = 1.6K\Omega$

To prevent loading $R_1 \geq 10R$

Considering $R_1 = 10R$

Therefore $R_1 = 16K\Omega$

For sustained oscillations $A_V = 29$

$$\frac{R_f}{R_1} = 29 \quad , R_f = 29\ R_1$$

R = 1.5K	
R_1 = 16K=15K	C_1 = 0.1uf
R_F =640K	

Finally, the closed loop gain of the amplifier is denoted by A_v rater than A_F.

$$V_d = V_f + V_{in}$$

$$V_o = A_v V_d$$

$$V_f = BV_o$$

Wien Bridge Oscillators:

Because of simplicity and stability, one of the most commonly used audio frequency oscillator is wein bridge oscillator. In the wein bridge oscillator, the wein bridge circuit is connected between the amplifier i/p terminals and output terminals. The bridge has a series RC network in one arm and a parallel RC network in adjoining arm. In the remaining two arms of the bridge resistors R_1 and R_f connected.

The phase angle criterion for oscillations is that the total phase shift around the circuit must be zero. This condition occurs only when the bridge is balanced, that is at resonance. The frequency of oscillation f_0 is exactly the resonance frequency of the balanced wein bridge and is given by

CALCULATIONS:

1. RC Phase-shift oscillator:

Frequency of oscillations,

$$f_o = \frac{1}{2\pi.R.C.\sqrt{6}} = \frac{1}{2\pi \times 1.5 \times 10^3 \times 0.1 \times 10^{-6} \times \sqrt{6}}$$

$$f_o = 433\ Hz$$

2. Wien's Bridge oscillator:

Frequency of oscillations,

$$f_o = \frac{1}{2\pi.R.C} = \frac{1}{2\pi \times 1.5 \times 10^3 \times 0.01 \times 10^{-6}}$$

$$f_o = 1061.5\ Hz$$

OBSERVATIONS:

Type of the oscillator	Theoretical values	Practical values
RC Phase-shift oscillator		
Wien's Bridge oscillator		

$$f_o = \frac{1}{2\pi RC} = \frac{0.159}{RC}$$

$$\mathbf{f_0} = 400 \text{ Hz.}$$

$$f_0 = \frac{1}{2\pi RC}$$

Let C = 0.1μF

$$R = \frac{1}{2\pi \text{ x } 0.1 \text{ x } 10^{-6} \text{ x } 400} = 3.98K\Omega$$

To prevent loading $R_1 = 10R$

$R_1 = 3.98K\Omega$

For sustained oscillations $A_V = 3$

$$\Rightarrow \quad 1 + \frac{R_f}{R_1} = 3 \qquad R_f = 2\,R_1$$

$$\Rightarrow \quad R_f = 79.6K\Omega$$

R = 15K	
R_1 = 10K	C_1 = 0.1uf
R_F = 20K	

Procedure:

1. Connect the circuit as per the circuit diagram
2. Observe output at pin 6 & verify the results with their theoretical values.

RESULT:

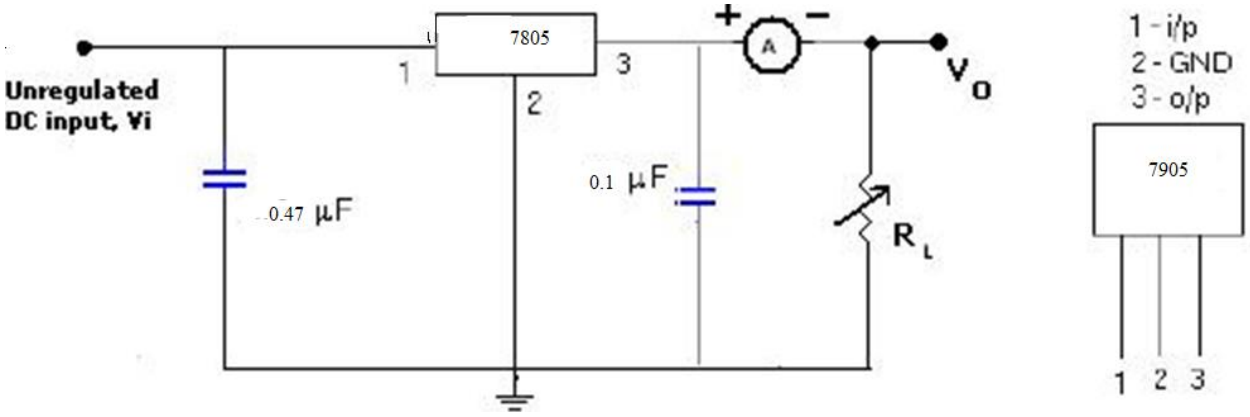
Hence the RC phase shift oscillator & the Wien's Bridge oscillator is designed and verified for a given frequency

VIVA QUESTIONS :

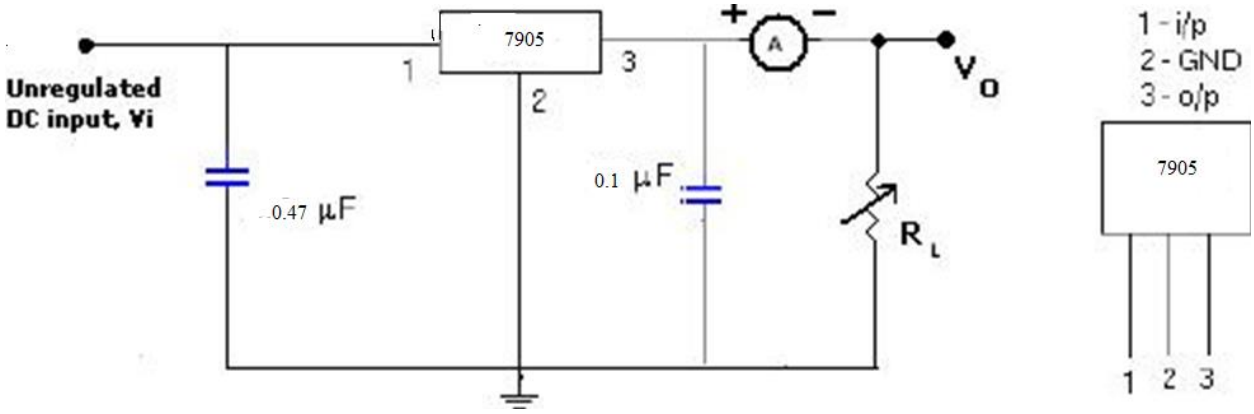
1. Which feedback is used in oscillators?
2. State Bark-Hausen's criteria.
3. What is the minimum gain that the inverting op-amp should have?
4. What is the condition for so that the oscillations will not die out?
5. In Wien's Bridge oscillator, what phase shift does the op-amp provide?

CIRCUIT DI

POSITIVE VOLTAGE REGULATOR (IC 7805)



NEGATIVE VOLTAGE REGULATOR (IC 7905)



DESIGN AND CONSTRUCT DC POWER SUPPLY USING THREE TERMINAL VOLTAGE REGULATORS 78XX AND 79XX

AIM:

To regulate the output voltage using three terminal voltage regulator IC.

APPARATUS:

1.	IC 7805	-----	1No.
2.	IC 7905	-----	1No.
3.	Decade Resistance Box	-----	1No.
4.	Regulated power supply	-----	1No.
5.	Voltmeter (0-5V)	-----	1No.
6.	Ammeter (0-50mA)	-----	1No.
7.	Capacitors (C_i) (0.47μF)	-----	1No.
8.	C_o (0.1μF)	-----	1No.

THEORY:

The 78XX series consists of three terminal positive voltage regulators with seven voltage options. For 7805 maximum voltage is +5V. These IC's are designed as fixed voltage regulators and with adequate heat sinking can deliver output currents in excess of 1A. These do not require any external components like in adjustable voltage regulators.

These require common ground between input and output voltages called drop out voltages.

The capacitor C_i is required if the regulator is located at appreciable distance from a power supply filter. Even though C_o is not needed, it may be used to improve the transient response of the regulator. The 79XX series of fixed output, negative voltage regulators are complements to the 7800 series devices. There are two extra voltage options of –2V and –5.2V available in 79XX series.

TABULAR FORMS:

Input voltage =

S.No.	Load resistance	Load voltage	Load current	% Regulation
1	**10 Ohm**			
2	**20 Ohm**			

Load resistance =

S.No.	Input voltage	Load voltage	Load current	% Regulation
1.	**1V**			
2.	**2V**			

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. A fixed DC voltage i.e.: 10v is given to the input terminals of the regulator.
3. Measure and record the load current I_L and load voltage V_L by varying load resistance R_L.
4. Calculate percent load regulation as the change in the load voltage V_L over some limited range of load currents.
5. To measure the line regulation, connect a 11Ω resistor as load and measure the load voltage by varying input voltage.
6. Same processor is repeated for 7905.

RESULT: