Control Section of CPU

Below is a sample of the control section of the CPU.

K is defined as the $\log_2$(Number of "Rows" in EEPROM)

Instrucion Specifier

8

2^k x (34+2k+4) EEPROM

3 x K multiplexer (μPCMux)

k

Instruction Specifier Decoder

For each instruction in the Pep9 Instruction set, it outputs the address of the first line of microcode needed to execute that instuction.

IsAddr

Mode

k

Addressing Mode Decoder

Output :=
if ~isUnary then 0
if isAAAAddressingMode then
  Let G := IS<8>
  if G=0 then symbol "I"
  if G=1 then symbol "X"
else
  Let G := IS<6..8>
  if G=0 then symbol "I"
  if G=1 then symbol "D"
  if G=2 then symbol "N"
  if G=3 then symbol "S"
  if G=4 then symbol "SF"
  if G=5 then symbol "X"
  if G=6 then symbol "SX"
  if G=7 then symbol "SFX"

Conditional Multiplexer (DMux)

μCk

Control Lines

k

False Target

k

True Target

2

Branch Function Decoder

isUnary

"isUnary" Decoder

Where the symbols are defined in the microcode, and the value of those symbols are "burned" into this circuit at construction.

4

Branch Function Selector

34

5

NZVCS Bits

Program Counter<7>

StopCk

μCk

Functions:
0. BR
    DMux=0, μPCMux=0
1. BRGT
    DMux=$\overline{N}$, μPCMux=0
2. BRGE
    DMux=$(\overline{N}+Z)$, μPCMux=0
3. BREQ
    DMux=Z, μPCMux=0
4. BRLE
    DMux=(N+Z), μPCMux=0
5. BRLT
    DMux=N, μPCMux=0
6. BRV
    DMux=V, μPCMux=0
7. BRC
    DMux=C, μPCMux=0

8. BRS
    DMux=S, μPCMux=0
9. Unused
10. Unused
11. ISD (Instruction Specifier Decoder)
    μPCMux=2
12. AMD (Addressing Mode Decoder)
    μPCMux=1
13. isUnary
    DMux="isUnary", μPCMux=0
14. isPCEven
    DMux=(PC<7>==0), μPCMux=0
15. Stop
    StopCk
Note the lack of BRNE - it is trivially replaceable with BREQ.

Outputs 1 if the current instruction specifier is for a unary instruction, otherwise outputs 0