DEPARTMENT OF COMPUTER
& SOFTWARE ENGINEERING

COLLEGE OF E&ME, NUST, RAWALPINDI

Digital System Design

Lab 01

Instructor: Asst Prof Dr M. Yasin

Group Members:
Farheen Fatima (354595)
Amna Ahmed (345952)
Amina Qadeer (359607)

Instructor:

Asst Prod Dr M. Yasin

Tasks:

Toggle Button

Code:

```verilog
module test1(btn,led);
input [1:0] btn;
output reg [1:0] led;

always @(*)  begin
   case (btn)
    2'b00: led = 4'b00; // When sel is '00', set led to '00'
    2'b01: led = 4'b10; // When sel is '01', set led to '01'
    2'b10: led = 4'b01; // When sel is '10', set led to '10'
    2'b11: led = 4'b11; // When sel is '11', set led to '11'
    default: led = 4'b00; // Default case for all other values of sel
   endcase
end
endmodule
```

Output:

Task 2:

Toggle 4 Button

Code:

```
module led_toggle(  input btn0,  input btn1,  input
btn2,  input btn3,  output reg led0,  output reg led1,
output reg led2,  output reg led3
);
  always @(posedge btn0) begin
    led0 <= ~led0;
  end
```

```verilog
      always @(posedge btn1) begin
        led1 <= ~led1;
      end


      always @(posedge btn2) begin
        led2 <= ~led2;
      end


      always @(posedge btn3) begin
        led3 <= ~led3;
      end
    endmodule
```

Constraint_File:

```
NET "btn0" LOC="T10";
NET "btn1" LOC="T9";
NET "btn2" LOC="V9";
NET "btn3" LOC="M8";
NET "led0" LOC="V16";
NET "led1" LOC="U16";
NET "led2" LOC="V15";
NET "led3" LOC="U15";
NET "btn3" CLOCK_DEDICATED_ROUTE = FALSE;
```

Output: