AMINA QADEER

359607

CE-42-A

DSD LAB

8-BIT BARREL SHIFTER

Code:

```
module BarrelShifter(
   input [7:0] A,
   input [2:0] shift_amount,
   input shift_right,
   output reg [7:0] B
);


always @(A or shift_amount or shift_right)
begin
   case(shift_amount)
      3'b000: B <= A; // No shift
      3'b001: B <= shift_right ? {A[7], A[7:1]} : {A[6:0], 1'b0}; // Shift right by 1
      3'b010: B <= shift_right ? {A[7:2], A[1:0]} : {A[5:0], 2'b00}; // Shift right by 2
      3'b011: B <= shift_right ? {A[7:3], A[2:0]} : {A[4:0], 3'b000}; // Shift right by
3
      3'b100: B <= shift_right ? {A[7:4], A[3:0]} : {A[3:0], 4'b0000}; // Shift right
by 4
      3'b101: B <= shift_right ? {A[7:5], A[4:0]} : {A[2:0], 5'b00000}; // Shift right
by 5
      3'b110: B <= shift_right ? {A[7:6], A[5:0]} : {A[1:0], 6'b000000}; // Shift right
by 6
```

```
      3'b111: B <= shift_right ? {A[7:7], A[6:0]} : {A[0], 7'b0000000}; // Shift right by 7
      default: B <= A; // No shift for undefined values
   endcase
end

endmodule
```

testbench:

```
module BarrelShifter_tb;

 reg [7:0] A;
 reg [2:0] shift_amount;
 reg shift_right;
 wire [7:0] B;

 // Instantiate the BarrelShifter module
 BarrelShifter uut(
  .A(A),
  .shift_amount(shift_amount),
  .shift_right(shift_right),
  .B(B)
 );

 // Clock generation (optional)
 reg clock;
 always #5 clock = ~clock;

 // Dumping VCD file
 initial begin
  $dumpfile("waveform.vcd");
```

```
  $dumpvars(0, BarrelShifter_tb); // Assuming your testbench is within the BarrelShifter_tb module

  // Initializations
  // ...

  // Apply test cases
  // ...

  $stop; // Stop simulation after test cases
end

// Apply inputs and display results
task run_test;
  // ...
endtask

endmodule
```

Output: