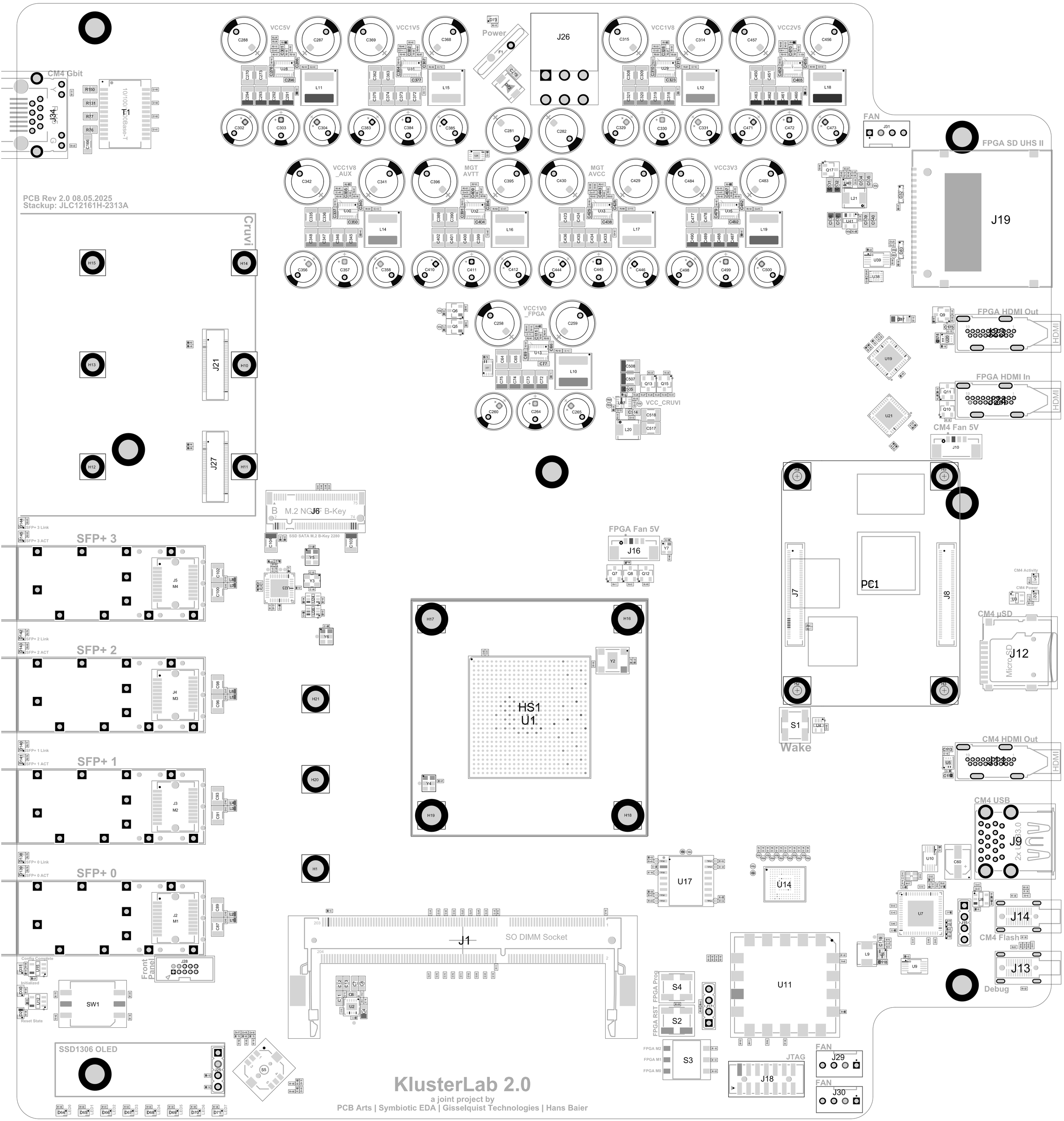
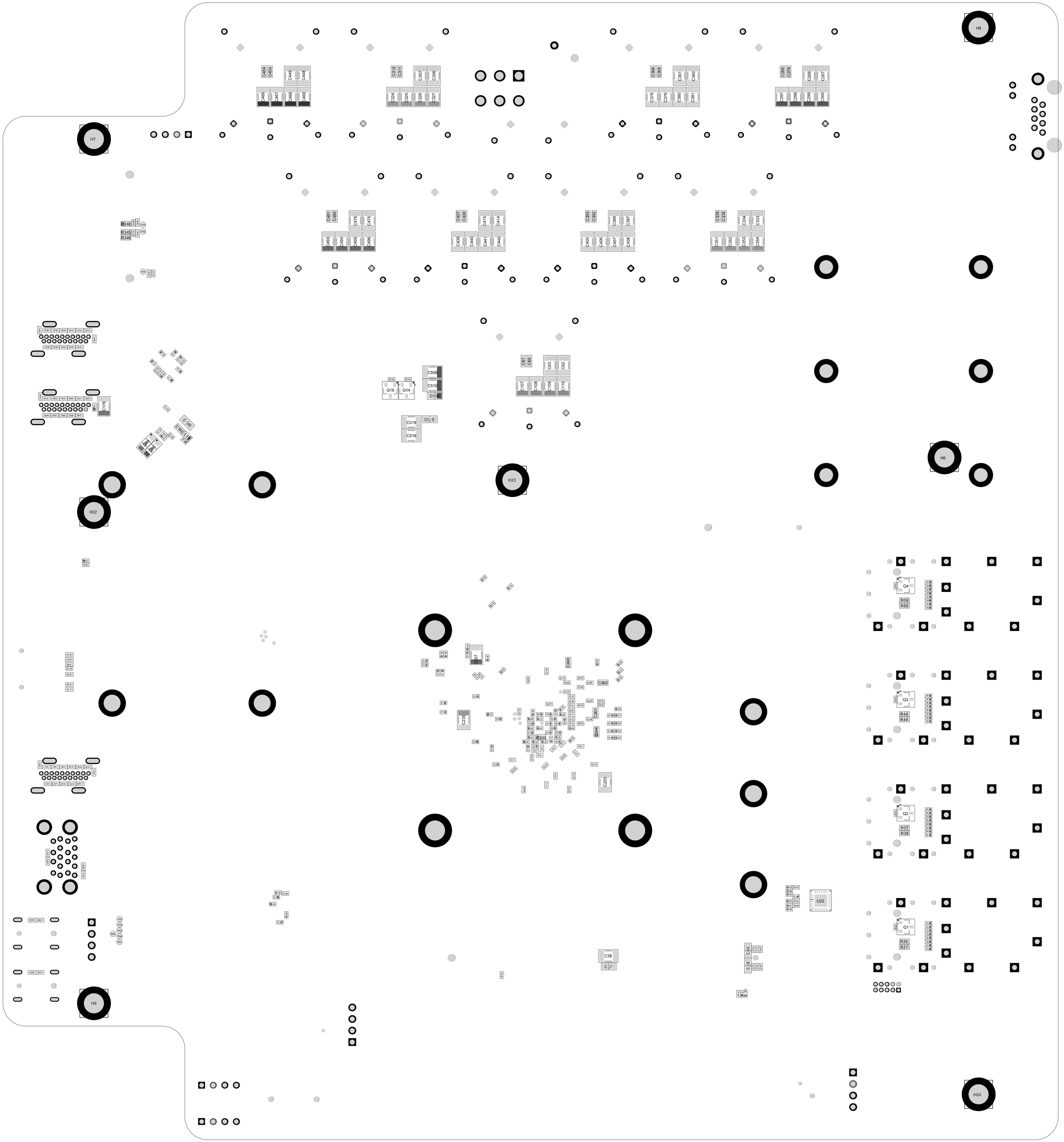
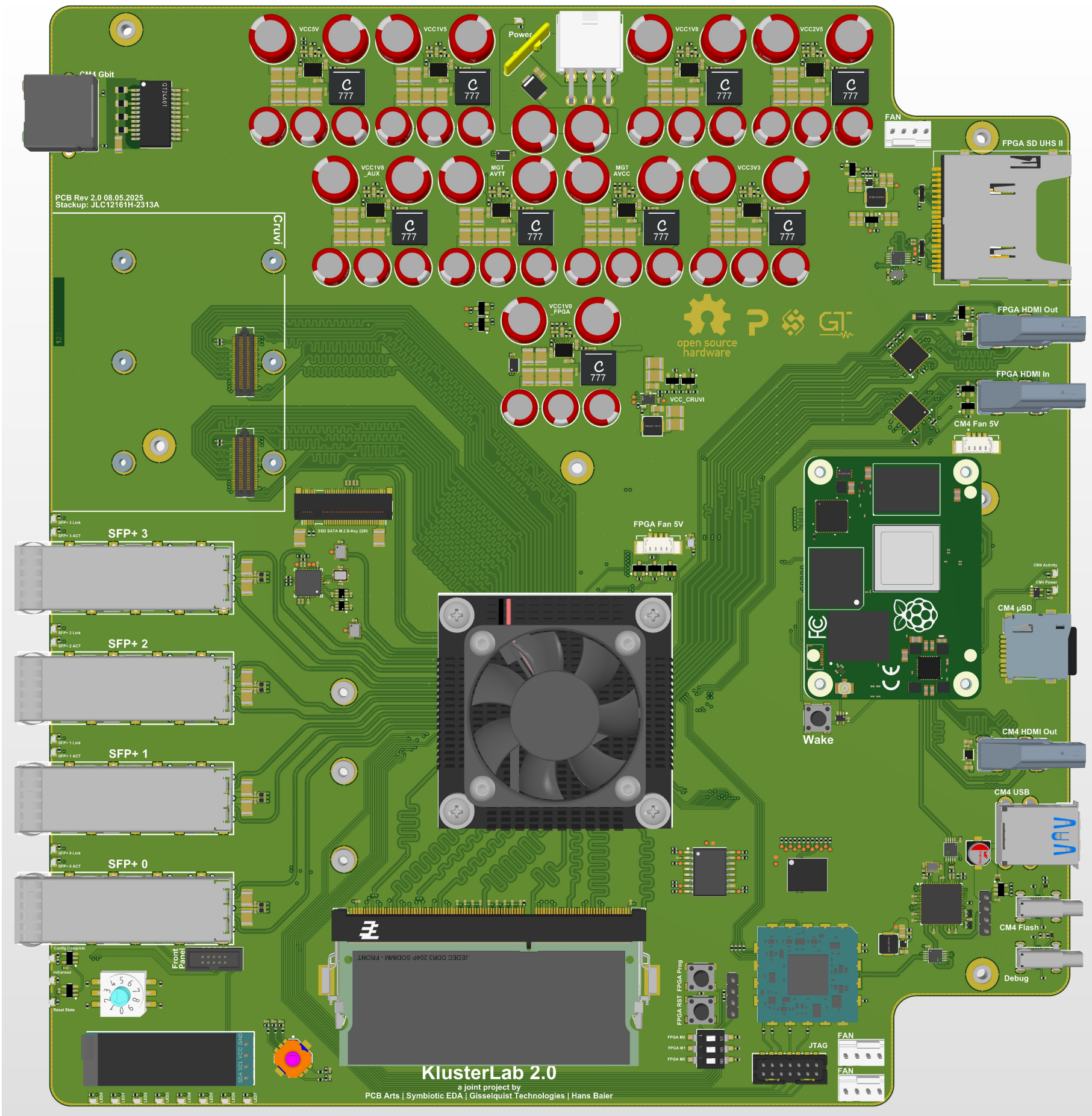
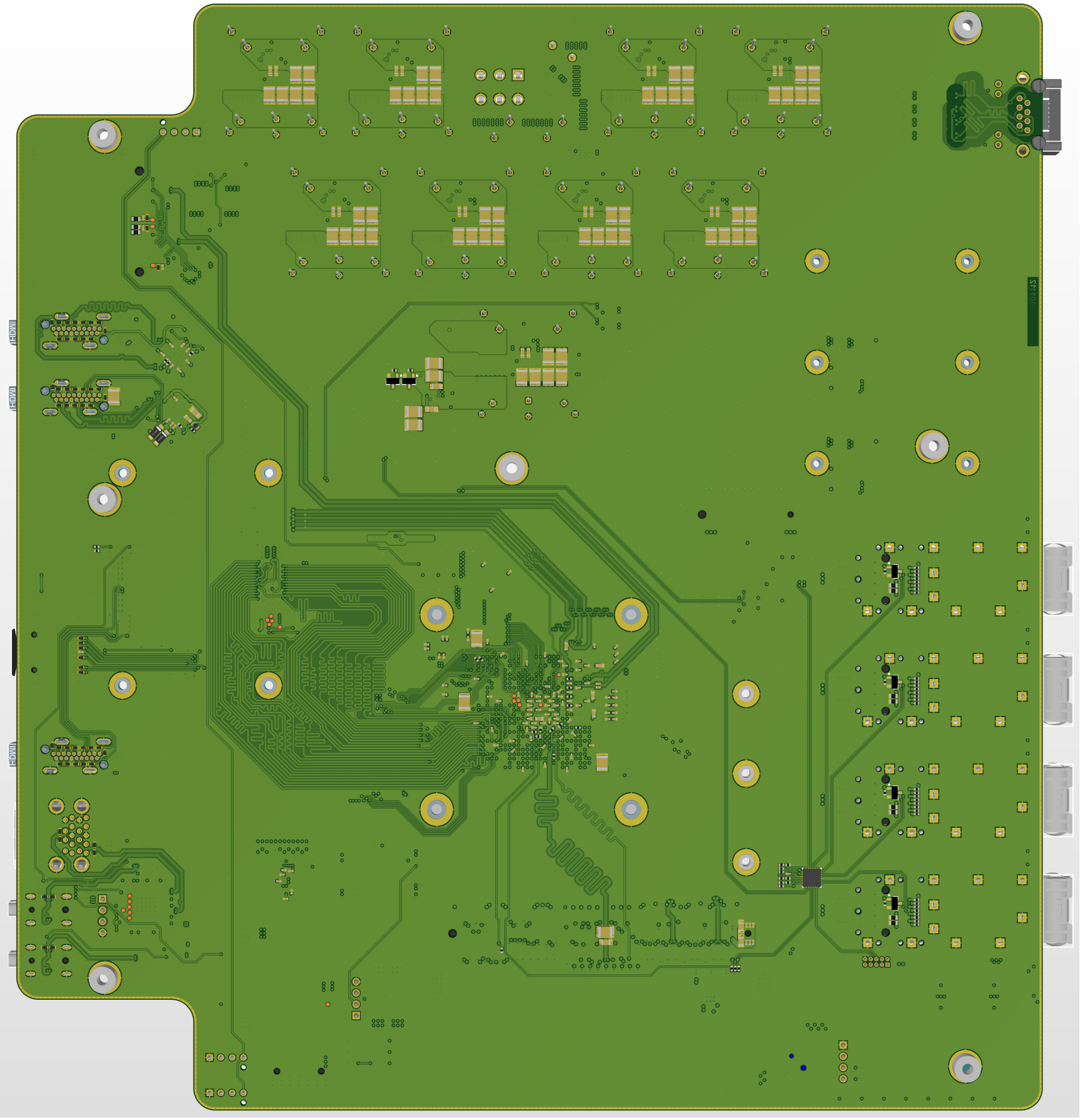

PCB Rev 2.0 08.05.2025
Stackup: JLC12161H-2313A
VCC5V
VCC1V5
Power
J26
VCC1V8
VCC2V5
CM4 Gbit
J34
T1
10/100/1000Base-T
FAN
J31
FPGA SD UHS II
J19
VCC1V8 _AUX
MGT AVTT
MGT AVCC
VCC3V3
Cruvi
J21
J27
VCC1V0 _FPGA
VCC_CRUVI
FPGA HDMI Out
FPGA HDMI In
HDMI
CM4 Fan 5V
J10
M.2 NGFF B-Key
J6
SSD SATA M.2 B-Key 2280
SFP+ 3
SFP+ 3 Link
SFP+ 3 ACT
SFP+ 2
SFP+ 2 Link
SFP+ 2 ACT
SFP+ 1
SFP+ 1 Link
SFP+ 1 ACT
SFP+ 0
SFP+ 0 Link
SFP+ 0 ACT
FPGA Fan 5V
J16
PC1
J7
J8
CM4 Activity
CM4 Power
CM4 µSD
MicroSD
J12
HS1
U1
S1
Wake
CM4 HDMI Out
CM4 USB
2x USB3.0
J9
J14
CM4 Flash
J13
Debug
J1
SO DIMM Socket
Config Complete
Initialized
Reset State
SW1
Front Panel
J28
SSD1306 OLED
J25
S5
U17
U14
U11
FPGA Prog
FPGA RST
S4
S2
S3
FPGA M2
FPGA M1
FPGA M0
JTAG
J18
FAN
J29
J30
KlusterLab 2.0
a joint project by
PCB Arts | Symbiotic EDA | Gisselquist Technologies | Hans Baier


H8
H7
H6
H23
H22
H24
H9
C454
C453
C449
C448
C466
C467
C468
C469
C312
C311
C307
C306
C324
C325
C326
C327
C386
C385
C361
C360
C378
C379
C380
C381
C280
C279
C268
C267
C297
C298
C299
C300
R348
R347
R346
C451
C450
C476
C475
C493
C494
C495
C496
C427
C426
C415
C414
C439
C440
C441
C442
C393
C392
C388
C387
C405
C406
C407
C408
C339
C338
C334
C333
C351
C352
C353
C354
C67
C68
C63
C62
C107
C108
C109
C110
C509
C510
C515
C519
C516
Q16
Q14
C178
C190
C192
L1
BK1
BK2
C240
C262
C261
C246
C235
C203
C253
C37
C38
C30
C39
U22
Q4
R59
R60
Q3
R48
R49
Q2
R37
R38
Q1
R26
R27


CM4 Gbit
PCB Rev 2.0 08.05.2025
Stackup: JLC12161H-2313A
Cruvi
VCC5V
VCC1V5
Power
VCC1V8
VCC2V5
FAN
FPGA SD UHS II
VCC1V8 _AUX
MGT AVTT
MGT AVCC
VCC3V3
VCC1V0 _FPGA
open source hardware
FPGA HDMI Out
FPGA HDMI In
VCC_CRUVI
CM4 Fan 5V
SSD SATA M.2 B-Key 2280
FPGA Fan 5V
SFP+ 3
SFP+ 2
SFP+ 1
SFP+ 0
CM4 µSD
Wake
CM4 HDMI Out
CM4 USB
CM4 Flash
Debug
Front Panel
JEDEC DDR3 204P SODIMM - FRONT
FPGA Prog
FPGA RST
JTAG
FAN
FAN
KlusterLab 2.0
a joint project by
PCB Arts | Symbiotic EDA | Gisselquist Technologies | Hans Baier


HDMI
HDMI
HDMI