

Document History

Revision	Date / Datum	Short mark	Concerned clause / Betr. Abschnitt	Reason of modification / Grund der Änderung
A	2023-05-29	MW	All	First Version

Product: Produkt:	RPi-GS-CAM-SER	Version:	1.0
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Size / Format:	Base dimensions / Grundmass: 38.0 mm x 38.0 mm Tolerances / Toleranzen: Width / Breite 38.0 ± 0.2 mm Length / Länge 38.0 ± 0.2 mm
Thickness / Dicke:	Tolerance / Toleranz: 1.6 mm ± 0.16 mm
Number of layers / Anzahl der Lagen:	4, plated-through / durchkontaktiert

Build-up of layers / Lagenaufbau:	Material: FR4, UL 94-V0, Gruppe IIIa, 130°C see Build-up of layers (End of Document) siehe Lagenaufbau (Ende des Dokuments)
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Number of holes (total) / Anzahl der Bohrungen (gesamt):	484 (incl. 465 Vias)
Minimum plated through hole diameter / Kleinsten Enddurchmesser:	0.2 mm
Finished plated hole tolerance (deviant from standard) / Bohrtoleranz (abweichend vom Standard):	n/a
Non plated through holes (NDK) / Nicht durchkontaktierte Bohrungen (NDK):	Yes / Ja
SMD:	Double-sided / zweiseitig
Smallest conductor width / Kleinste Leiterbahnbreite:	0.127 mm
Smallest spacing width / Kleinsten Leiterbahnabstand:	0.15 mm
Gilding of connectors / Steckervergoldung:	No / Nein

Author: M. Weimann	Date: 2023-05-29	File-Name: RPi-GS-CAM-SER_PCBSpec_V1-0A.docx	Revision: A
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Product Specification Printed Circuit Board

Plated through holes to be plugged using Peterslack or equivalent / <i>Durchsteiger mit Peterslack verschließen:</i>	No / <i>Nein</i>
Filling of microvias / <i>Microvias verfüllen:</i>	n/a
Reference point (origin) / <i>Referenzpunkt:</i>	see drawings / <i>siehe Zeichnungen:</i> x 4.0 mm / y 4.0 mm
Order of layers / <i>Lagenfolge:</i>	see file / <i>siehe Datei:</i> RPI-GS-CAM-SER_PCBLayerSpec_V1-0.pdf
Finish of top and bottom copper surfaces / <i>Metalloberfläche:</i>	Immersion Nickel Gold (PB free) / <i>Chemisch Nickel Gold (Bleifrei)</i>
Electrical conductivity and isolation test / <i>Elektrischer Test:</i>	Yes

Via Type	Layers / <i>Lagen</i>	PadØ	FinishedØ Drilling/ <i>Enddurchmesser</i>	Count / <i>Anzahl</i>
Thru vias layers	1-4	0.5 mm	0.2 mm	465

Markings and identification / <i>Beschriftungen:</i>	See drawings / <i>siehe Zeichnungen</i>
Other requirements / <i>Weitere Anmerkungen:</i>	<ul style="list-style-type: none">- Soldermask: double-sided <i>Lötstopplack: beidseitig</i>- Silkscreen: Yes (Top Overlay / Bottom Overlay) <i>Bestückungsdruck: Ja</i>- Impedanzkontrollierte Leitungen: <i>Impedance controlled traces:</i> <i>Diff. 100 Ohm: L1/L4: 127 µm / 200 µm / 127 µm</i> <i>Single 50 Ohm: L1/L4: 157 µm</i>- Via Tenting: not strictly necessary (restring covered, sleeve free) <i>Abdeckung von Durchkontaktierungen:</i> <i>nicht zwingend notwendig</i> (<i>Restring bedeckt, Hülse frei</i>)

Author: M. Weimann	Date: 2023-05-29	File-Name: RPI-GS-CAM-SER_PCBSpec_V1-0A.docx	Revision: A
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Drawing:

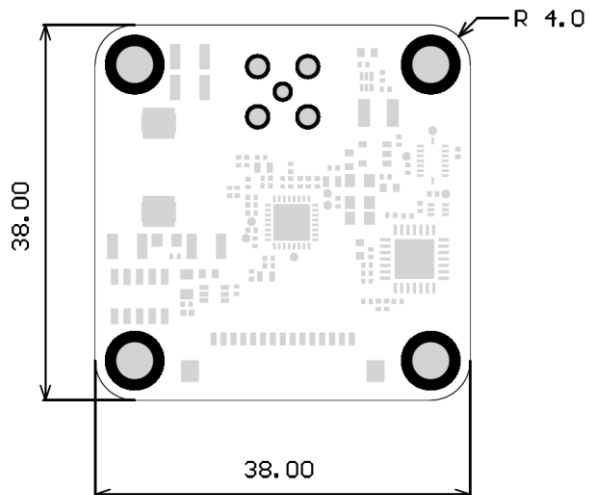


Figure 1: PCB Dimensions

UL-Marking:

The following information shall be placed on the PCB Bottom Side (see Figure 3):

- PCB Manufacturer Logo
- UL-Marking
- UL-File-No.

Top (Reference Point):

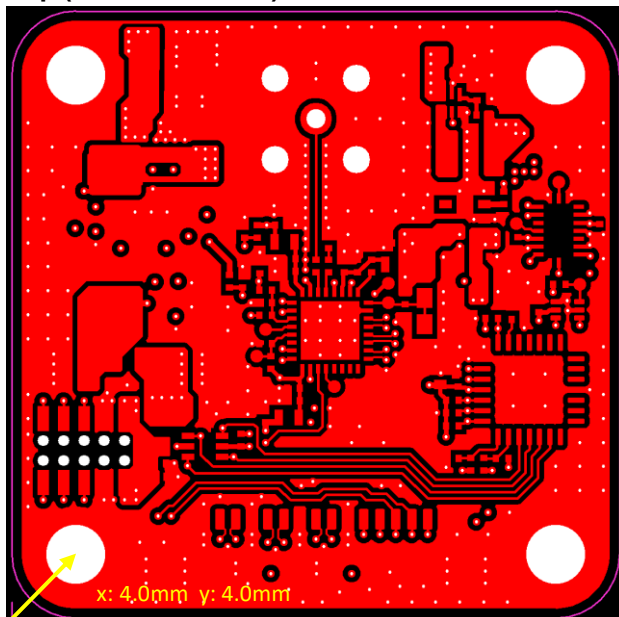


Figure 2: PCB Top Side

Author:	Date:	File-Name:	Revision:
M. Weimann	2023-05-29	RPi-GS-CAM-SER_PCBSpec_V1-0A.docx	A

Bottom (UL Marking):

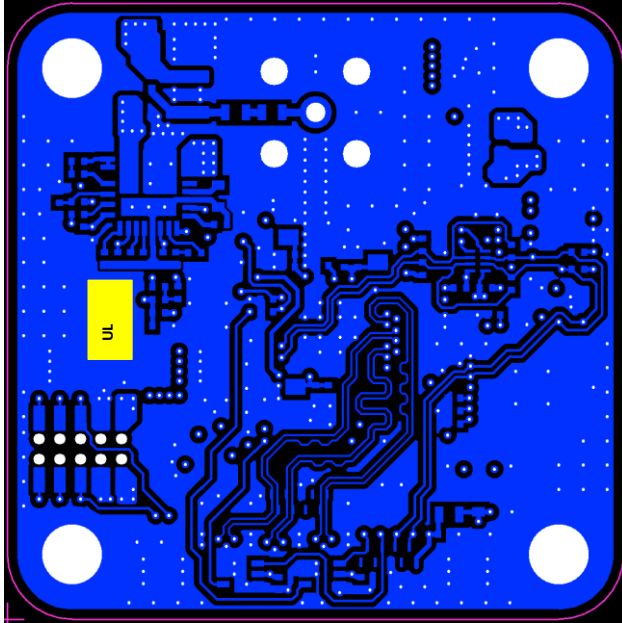


Figure 3: PCB Bottom Side

#	Name	Material	Type	Thickness	Weight	Dk	Df
	Top Overlay		Overlay				
	Top Solder	SM-001	Solder Mask	0.0254mm		4	0.03
	Top Surface Fini...	PbSn	Surface Finish	0.02mm			
1	Top Layer	CF-004	Signal	0.035mm	1/2oz		
	Dielectric 1	3313*1	Prepreg	0.0994mm		4.05	0.02
2	Int1 (PWR/GND)	CF-004	Signal	0.0152mm	1oz		
	Dielectric 3	Core-039	Core	1.265mm		4.6	0.02
3	Int2 (GND)	CF-004	Signal	0.0152mm	1oz		
	Dielectric 5	3313*1	Prepreg	0.0994mm		4.05	0.02
4	Bottom Layer	CF-004	Signal	0.035mm	1/2oz		
	Bottom Surface...	PbSn	Surface Finish	0.02mm			
	Bottom Solder	SM-001	Solder Mask	0.0254mm		4	0.03
	Bottom Overlay		Overlay				

Figure 4: Build-up of layers

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