

# Zynq Feather Rev. 0.2

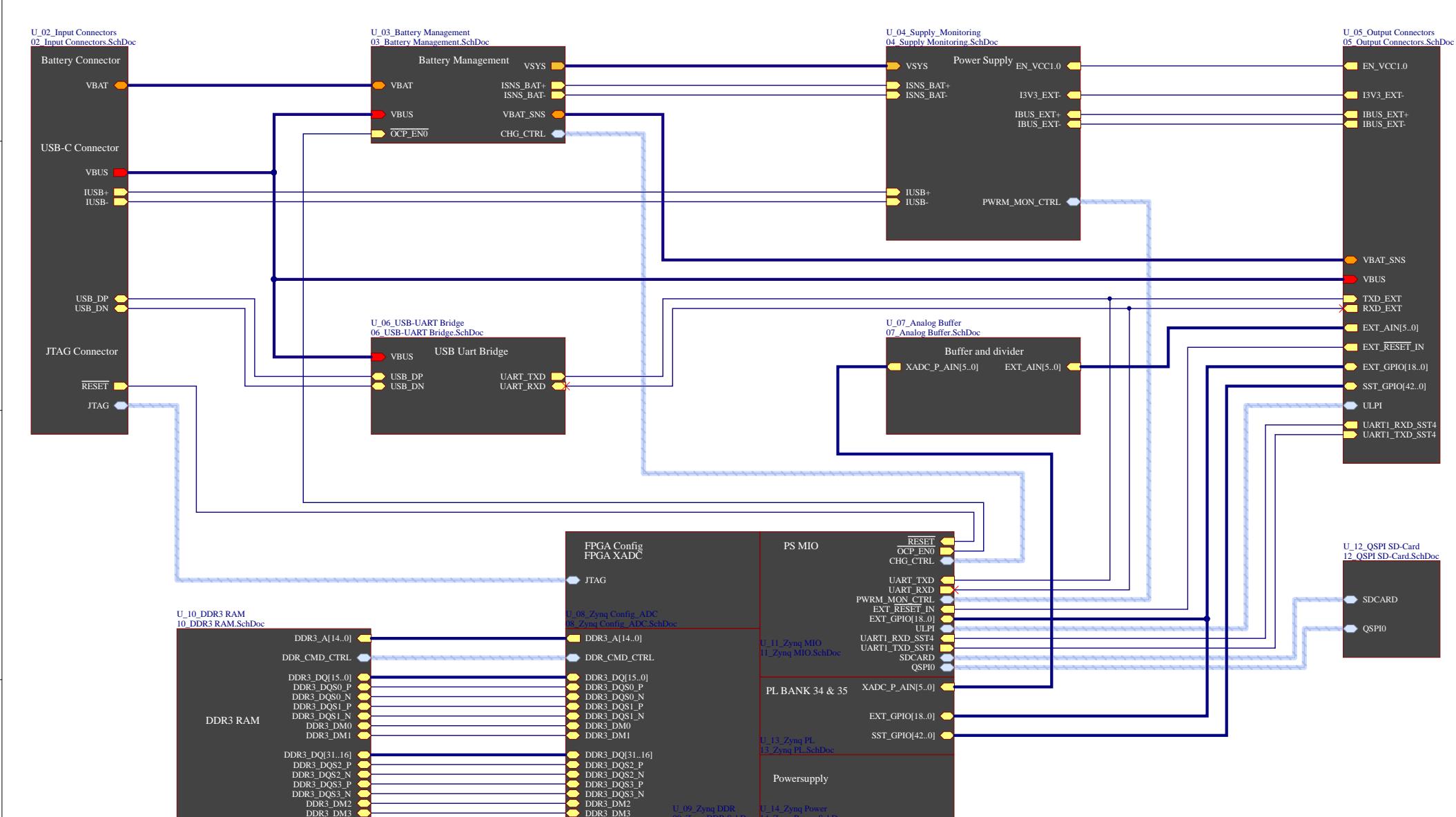
Designed at PCB Arts

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[Top Level Document](#)

[Block Diagram](#)



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Title: 01\_Top Level.SchDoc

Datum: 16.04.2021 Zeit: 00:04:45

Blatt: 1 von: 14 Entwickler: Lukas Henkel

Revision: r0.2 Checked: nein

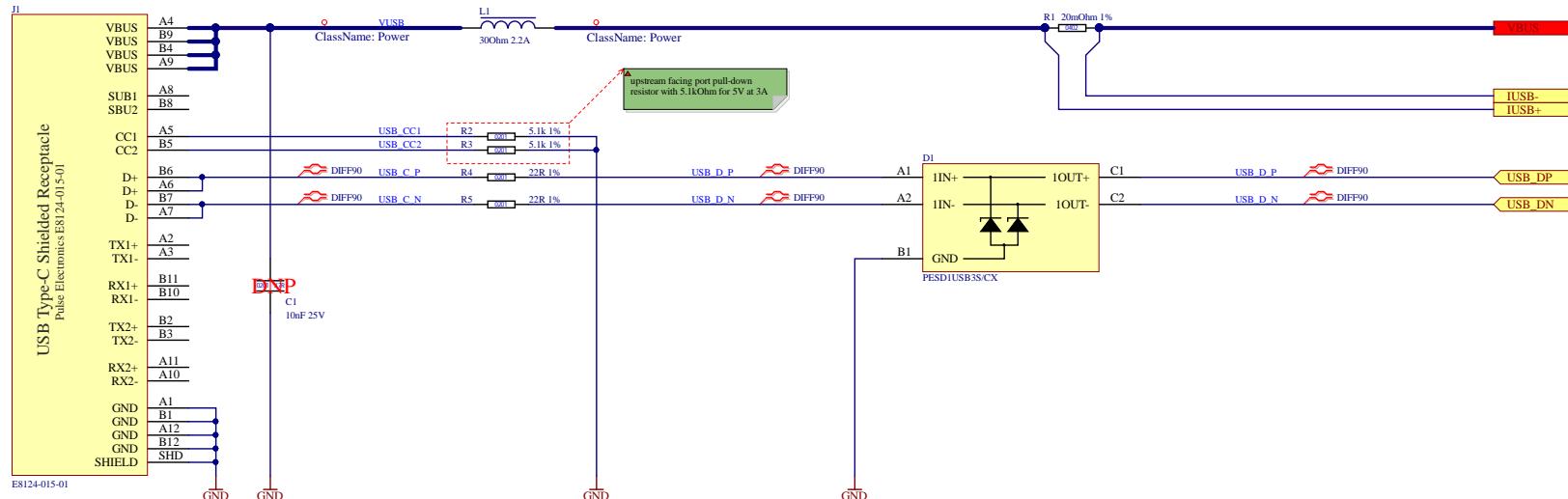
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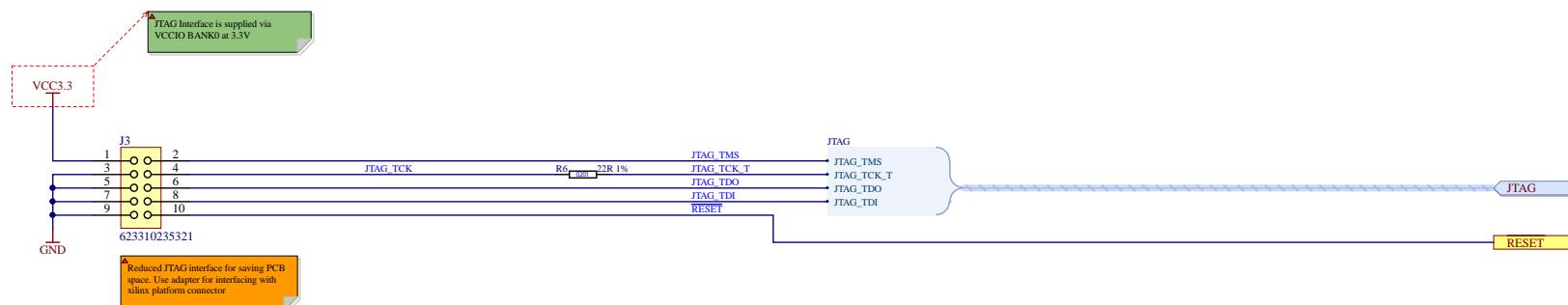
## USB-C Connector



## Feather Battery Connector



## JTAG Connector



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Title: 02\_Input Connectors.SchDoc

Datum: 16.04.2021 | Zeit: 00:04:46

Blatt: 2 von: 14 Entwickler: Lukas Henkel

Revision: r0.2 Checked: nein

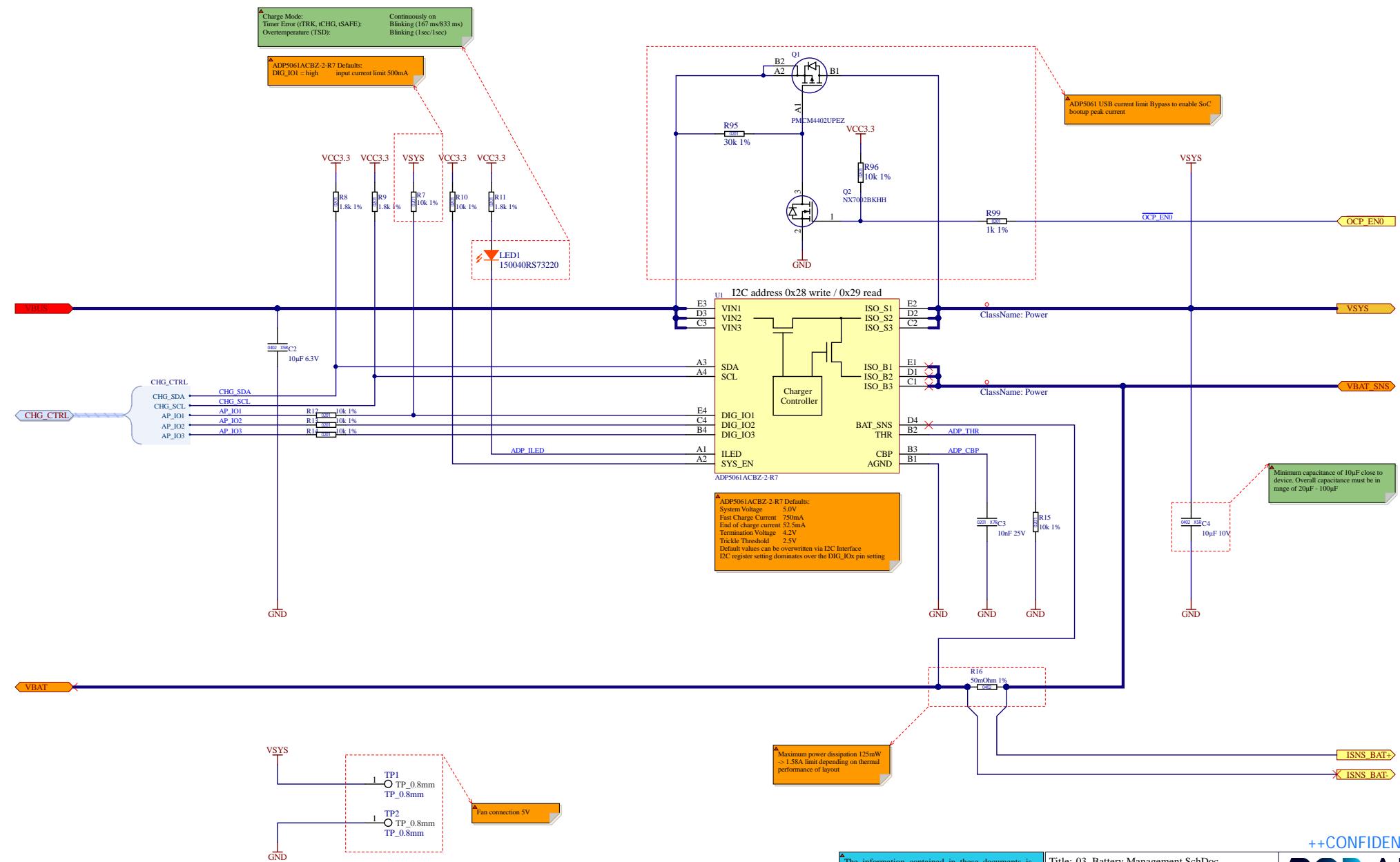
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## Battery Management / Power Path Controller

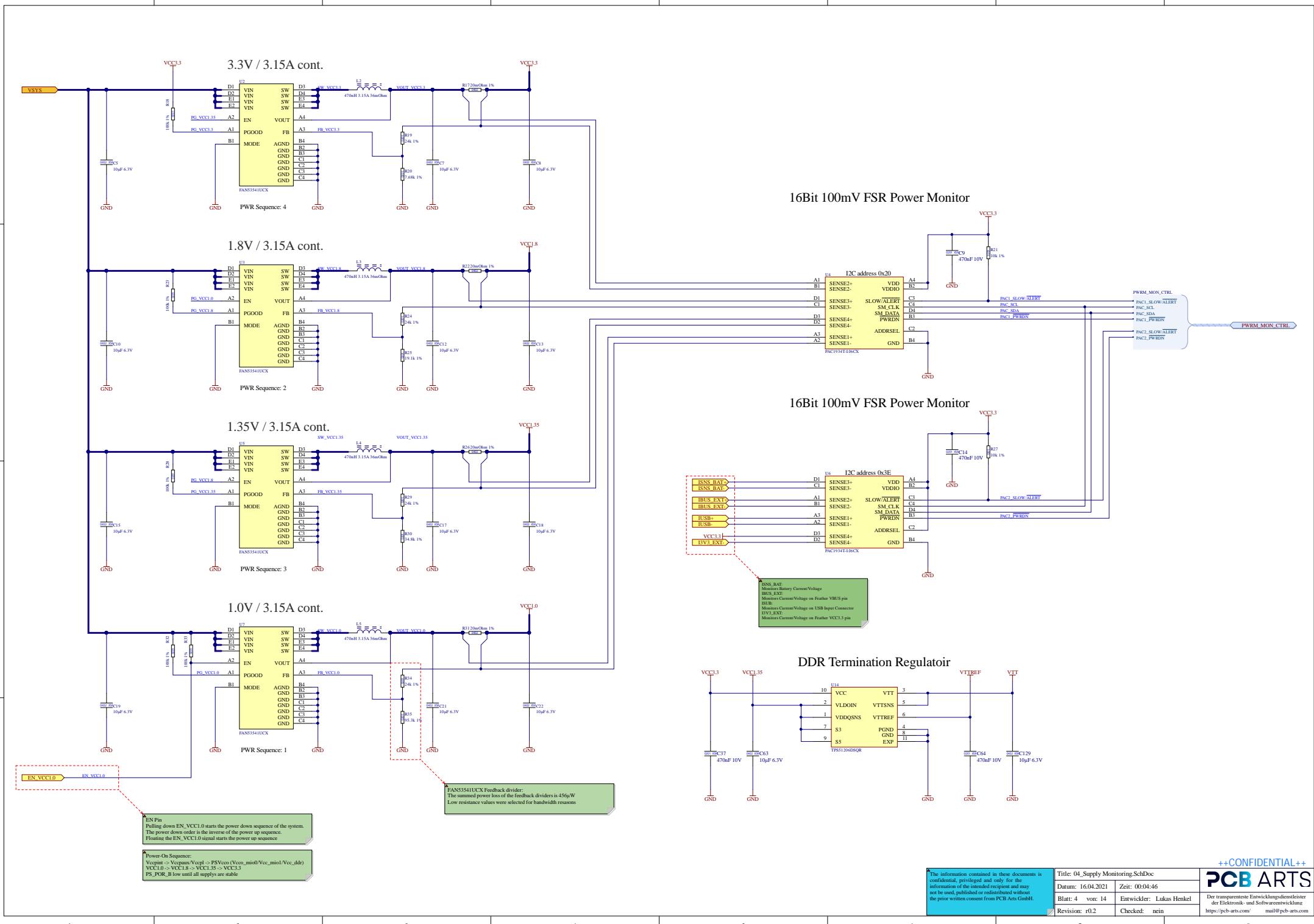


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Title: 03\_Battery Management.SchDoc  
Datum: 16.04.2021 | Zeit: 00:04:46  
Blatt: 3 von: 14 | Entwickler: Lukas Henkel  
Revision: r0.2 | Checked: nein

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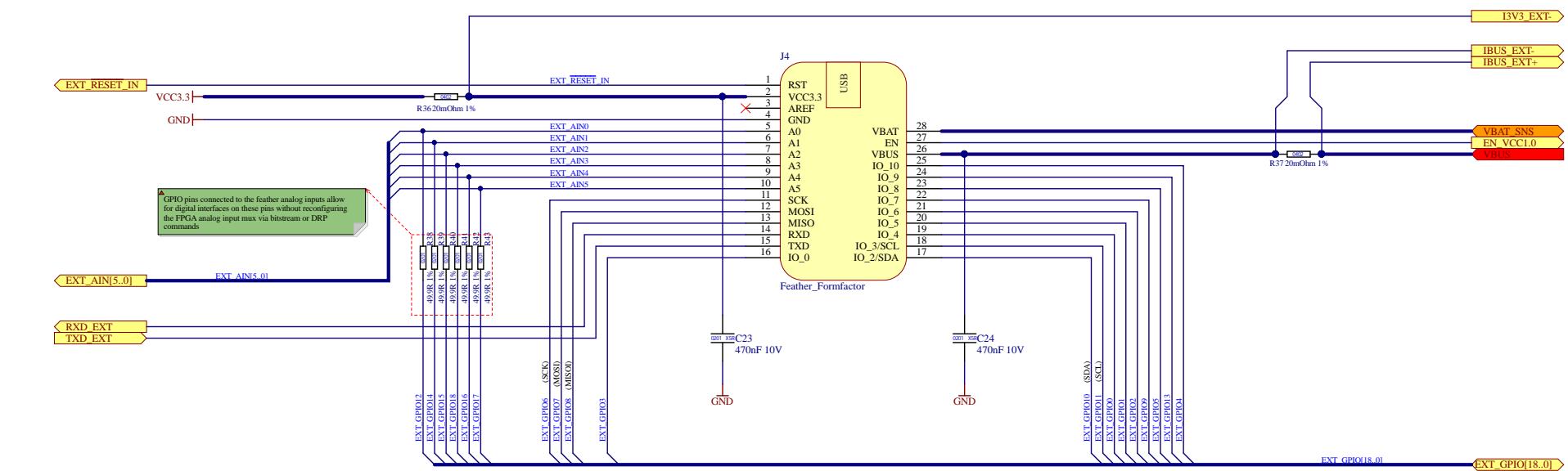


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Title: 04\_Supply Monitoring.SchDoc  
Datum: 16.04.2021 Zeit: 00:04:46  
Blatt: 4 von: 14 Entwickler: Lukas Henkel  
Revision: r0.2 Checked: nein

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# Adafruit Feather Formfactor



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Title: 05\_Output Connectors.SchDoc

Datum: 16.04.2021 | Zeit: 00:04:46

Blatt: 5 von: 14 Entwickler: Lukas Henkel

Revision: r0.2 Checked: nein

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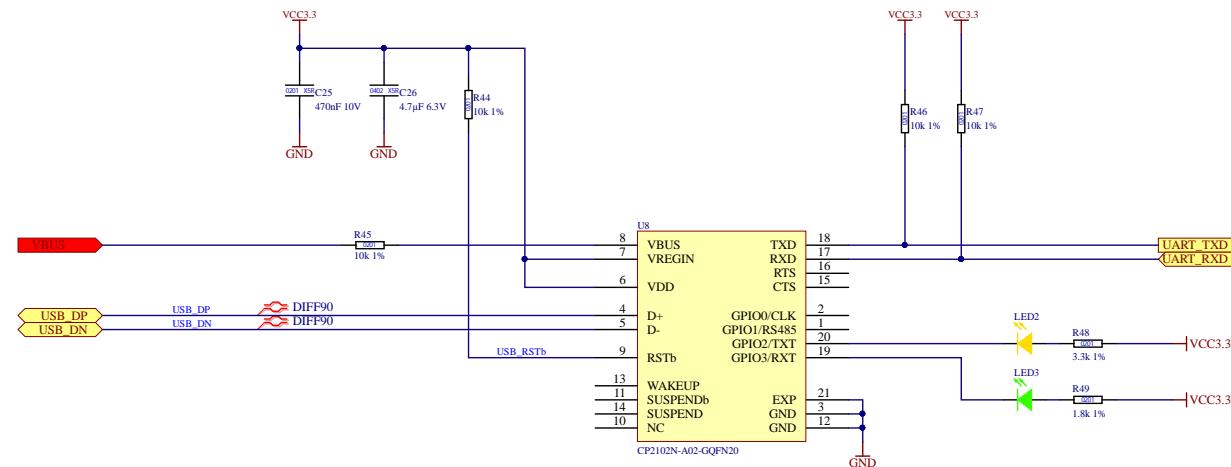
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A

A

## USB to UART Bridge



B

B

C

C

D

D

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Title: 06_USB-UART Bridge.SchDoc	Datum: 16.04.2021	Zeit: 00:04:47
Blatt: 6 von: 14	Entwickler: Lukas Henkel	
Revision: r0.2	Checked: nein	

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# Analog Input Buffer / Divider

A

A

B

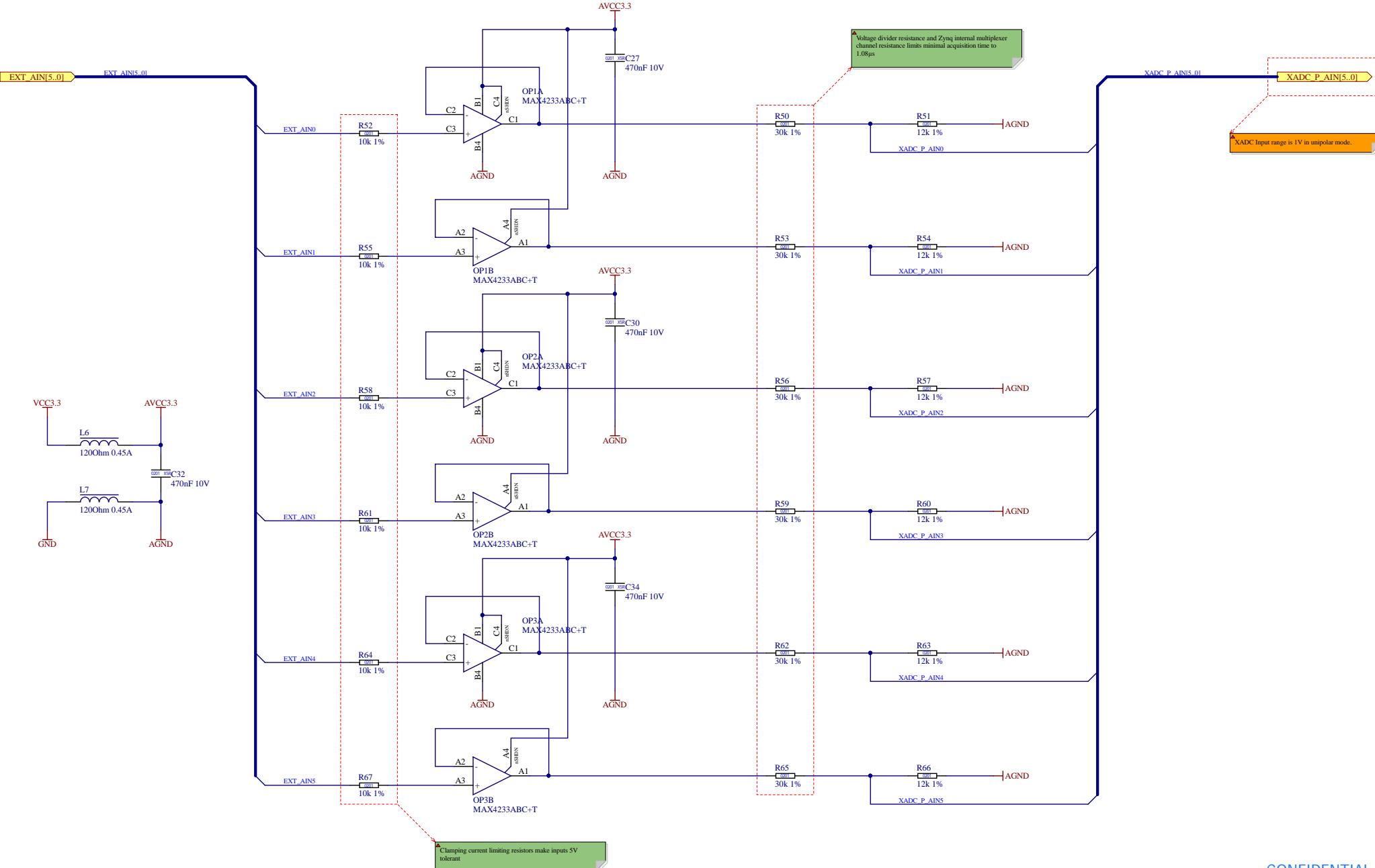
B

C

C

D

D



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Title: 07\_Analog Buffer.SchDoc

Datum: 16.04.2021 | Zeit: 00:04:47

Blatt: 7 von: 14 Entwickler: Lukas Henkel

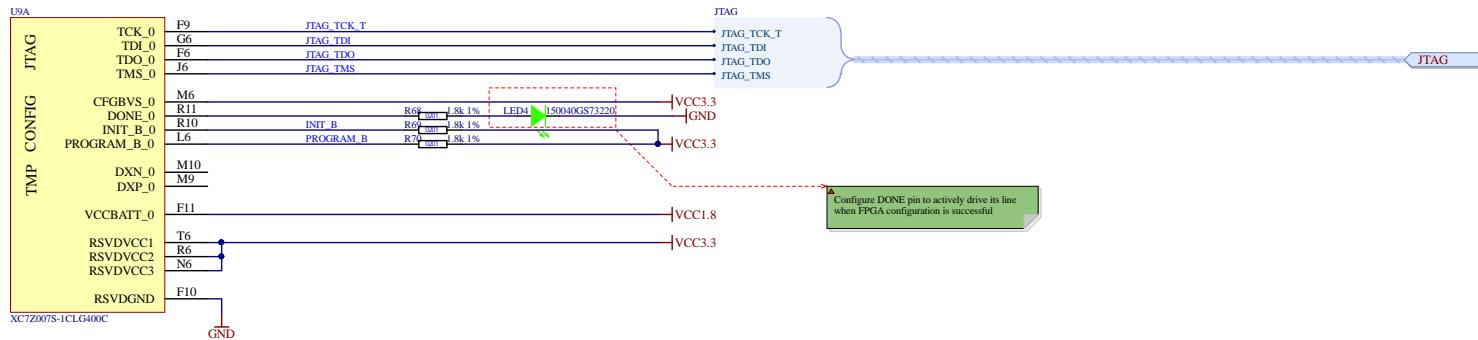
Revision: r0.2 Checked: nein

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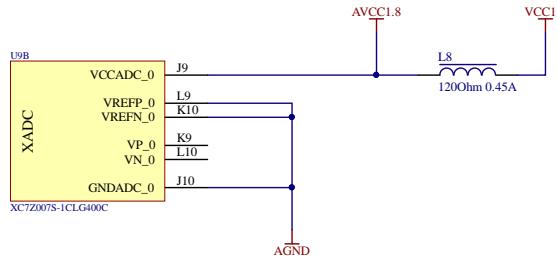
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## FPGA Configuration



## XADC



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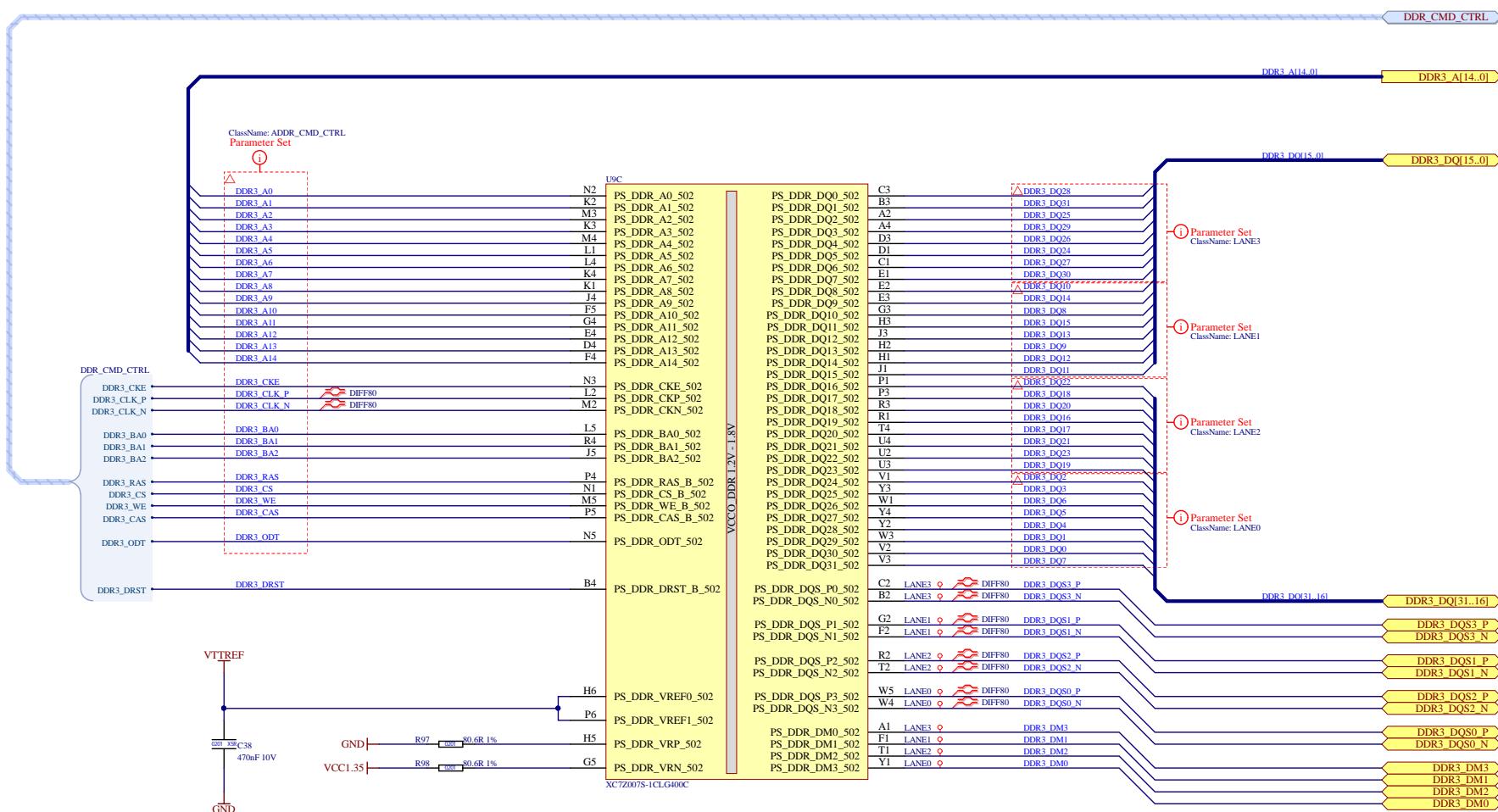
Title: 08_Zynq Config_ADC.SchDoc
Datum: 16.04.2021   Zeit: 00:04:47
Blatt: 8 von: 14   Entwickler: Lukas Henkel
Revision: r0.2   Checked: nein

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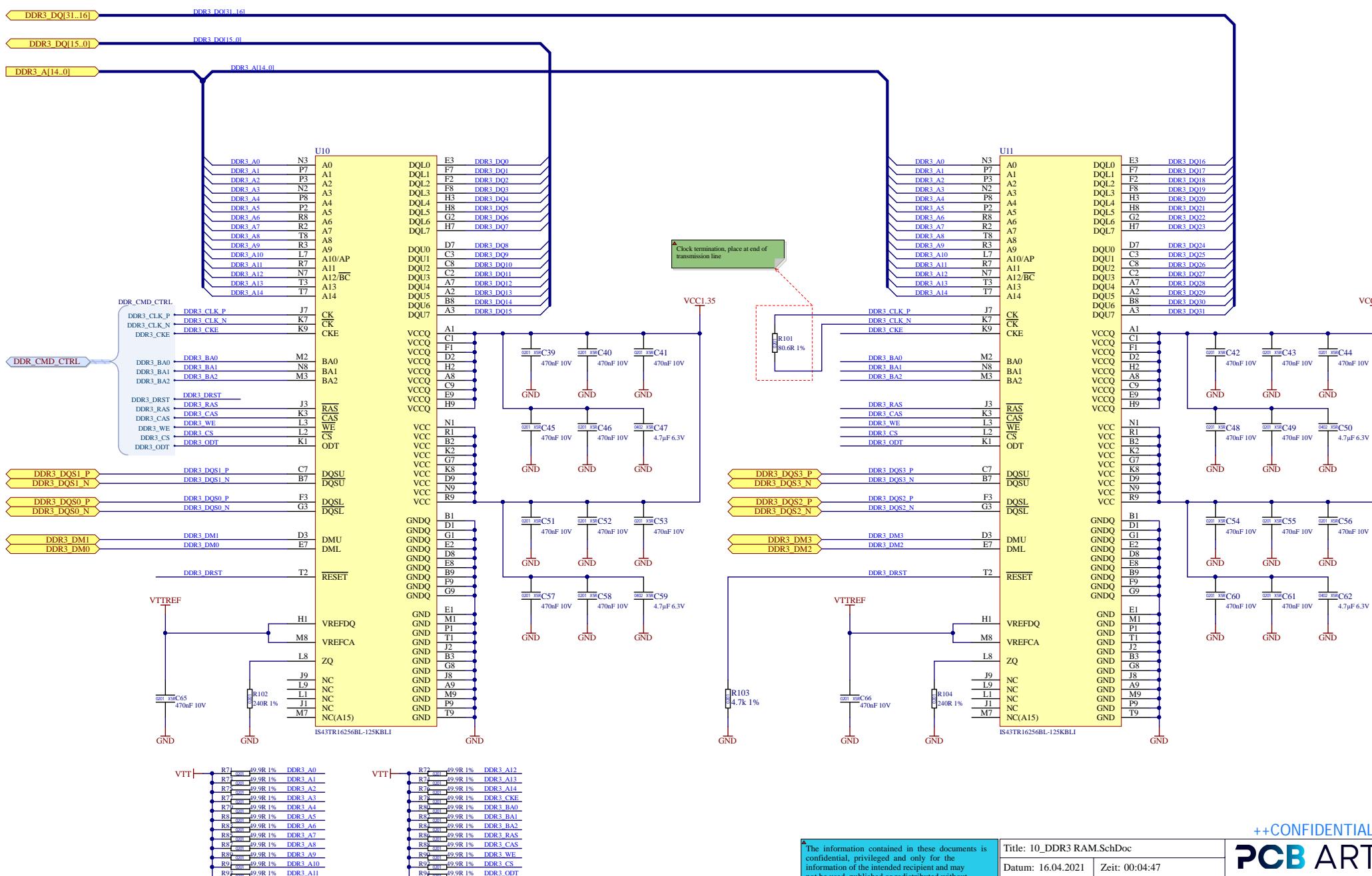
# PS DDR3 Interface



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Title: 09_Zynq DDR.SchDoc
Datum: 16.04.2021   Zeit: 00:04:47
Blatt: 9 von: 14   Entwickler: Lukas Henkel
Revision: r0.2   Checked: nein

2x DDR3 RAM



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Title: 10 DDR3 RAM SchDoc

Datum: 16.04.2021 Zeit: 00:04:47

Blatt: 10 von: 14 Entwickler: Lukas Henkel

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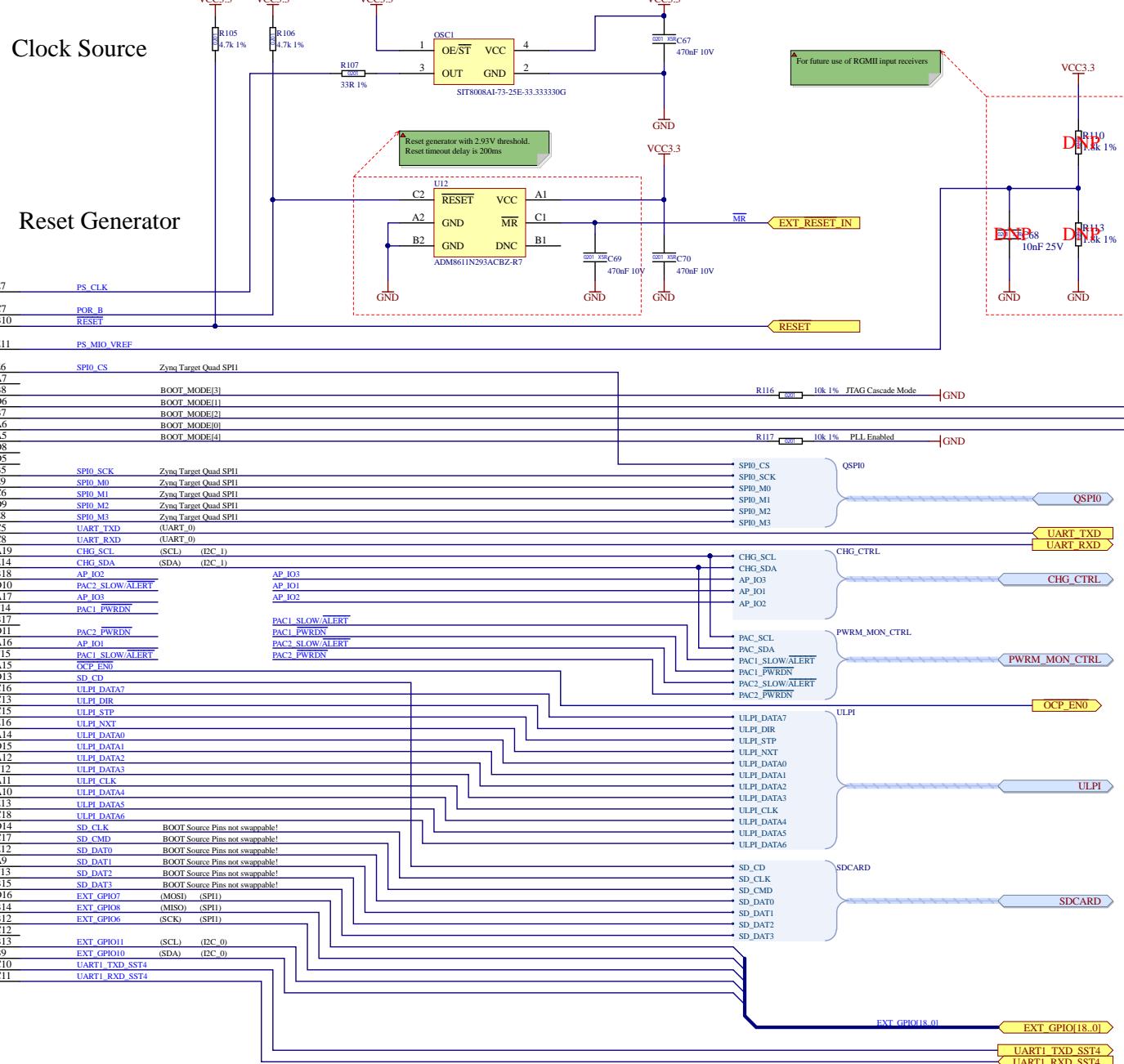
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## Clock Source

## Reset Generator

<b>U9D</b>	PS_CLK_500	E7	PS_CLK
	PS POR_B_500	C7	POR_B
	PS_SRST_B_501	B10	RESET
	PS_MIO_VREF_501	E11	PS_MIO_VREF
<b>VCCO_MIO1.8V - 3.3V</b>	PS_MIO0_500	A7	Zynq Target Quad SPI1
	PS_MIO1_500	B8	ROOT_MODE[3]
	PS_MIO2_500	D6	BOOT_MODE[1]
	PS_MIO3_500	B7	BOOT_MODE[2]
	PS_MIO4_500	A6	BOOT_MODE[0]
	PS_MIO5_500	A5	BOOT_MODE[4]
	PS_MIO6_500	D8	
	PS_MIO7_500	D5	
	PS_MIO8_500	B5	Zynq Target Quad SPI1
	PS_MIO9_500	E9	SP10_CS
	PS_MIO10_500	SPI1_M0	Zynq Target Quad SPI1
	PS_MIO11_500	C6	SPI1_M1
	PS_MIO12_500	D9	SPI1_M2
	PS_MIO13_500	E8	SPI1_M3
	PS_MIO14_500	C8	UART_RXD
	PS_MIO15_500	C9	UART_RXD
	PS_MIO16_501	A19	CHG_SCL
	PS_MIO17_501	E14	CHG_SDA
	PS_MIO18_501	B18	AB_I02
	PS_MIO19_501	D10	PAC2_SLOW ALERT
	PS_MIO20_501	A17	AP_I03
	PS_MIO21_501	F14	PAC1_PWRDN
	PS_MIO22_501	B17	
	PS_MIO23_501	D11	PAC2_PWRDN
	PS_MIO24_501	A16	AP_I01
	PS_MIO25_501	F15	PAC1_SLOW ALERT
	PS_MIO26_501	A15	OCP_EN0
	PS_MIO27_501	D13	SD_CD
	PS_MIO28_501	C16	ULPI_DATA7
	PS_MIO29_501	C13	ULPI_DIR
	PS_MIO30_501	C15	ULPI_STP
	PS_MIO31_501	E16	ULPI_NXT
	PS_MIO32_501	A14	ULPI_DATA0
	PS_MIO33_501	D15	ULPI_DATA1
	PS_MIO34_501	A12	ULPI_DATA2
	PS_MIO35_501	F12	ULPI_DATA3
	PS_MIO36_501	A11	ULPI_CLK
	PS_MIO37_501	A10	ULPI_DATA4
	PS_MIO38_501	E13	ULPI_DATA5
	PS_MIO39_501	C18	ULPI_DATA6
	PS_MIO40_501	D14	SD_CLK
	PS_MIO41_501	C17	SD_CMD
	PS_MIO42_501	E12	SD_DAT0
	PS_MIO43_501	A9	SD_DAT1
	PS_MIO44_501	F13	SD_DAT2
	PS_MIO45_501	B15	SD_DAT3
	PS_MIO46_501	D16	EXT GPIO7 (MOSI) (SPI1)
	PS_MIO47_501	B14	EXT GPIO8 (MISO) (SPI1)
	PS_MIO48_501	B12	EXT GPIO6 (SCK) (SPI1)
	PS_MIO49_501	C12	
	PS_MIO50_501	B13	EXT GPIO11 (SCL) (I2C 0)
	PS_MIO51_501	B9	EXT GPIO10 (SDA) (I2C 0)
	PS_MIO52_501	C10	UART1_RXD_SST4
	PS_MIO53_501	C11	UART1_RXD_SST4

XC7Z007S-1CLG400C



## Bootstrapping

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Title: 11\_Zynq MIO.SchDoc

Datum: 16.04.2021 | Zeit: 00:04:48

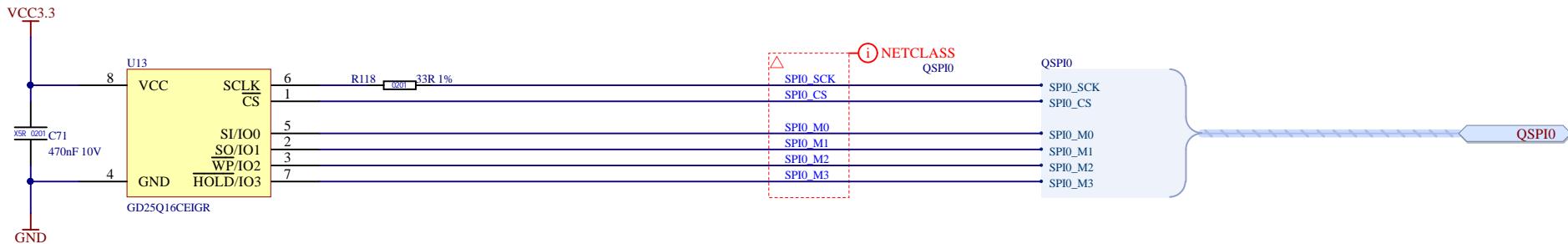
Blatt: 11 von: 14 Entwickler: Lukas Henkel

Revision: r0.2 Checked: nein

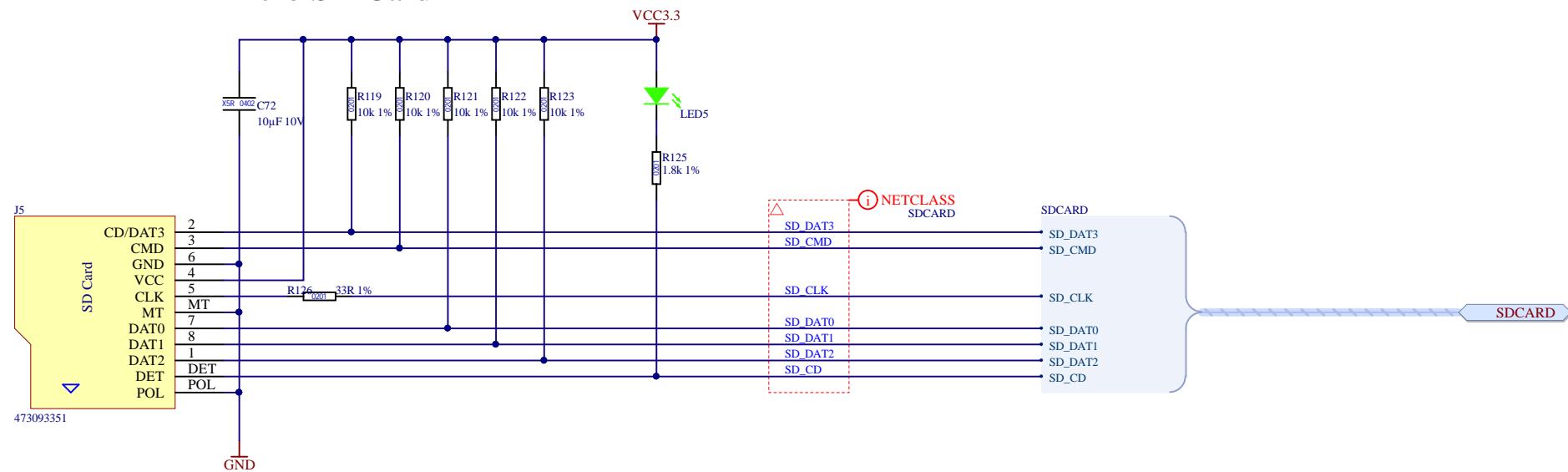
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## QSPI 16Mb (2M x 8)



## Micro SD Card



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Title: 12\_QSPI SD-Card.SchDoc

Datum: 16.04.2021 Zeit: 00:04:48

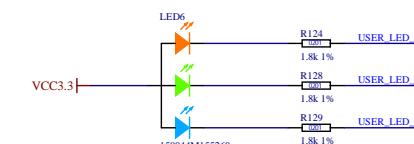
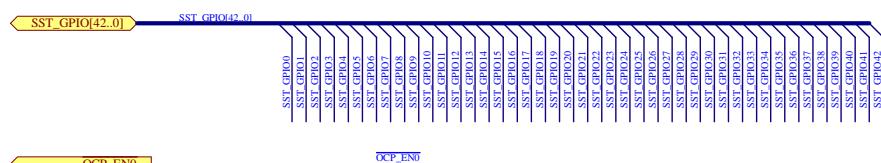
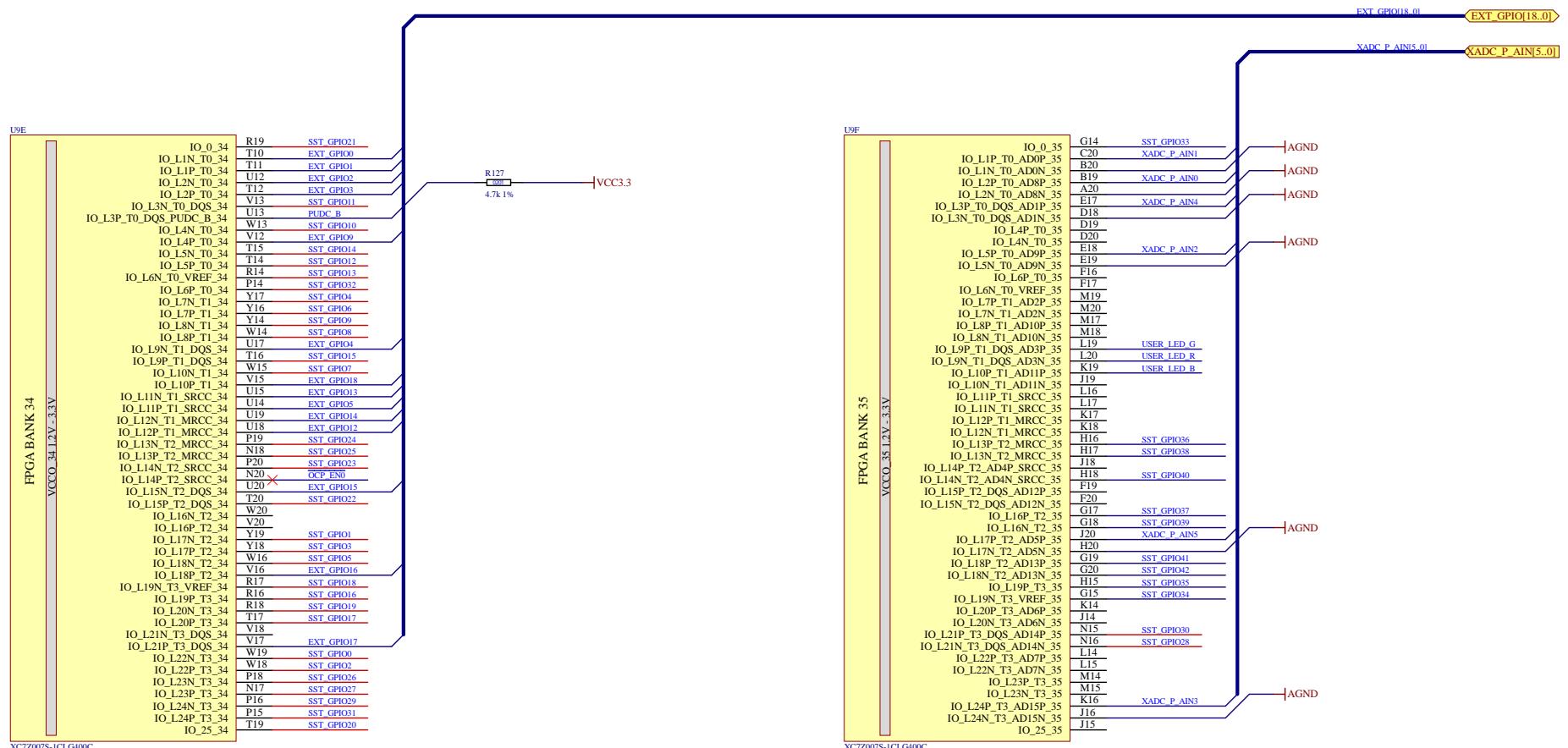
Blatt: 12 von: 14 Entwickler: Lukas Henkel

Revision: r0.2 Checked: nein

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Title: 13\_Zung PI\_SchDoc

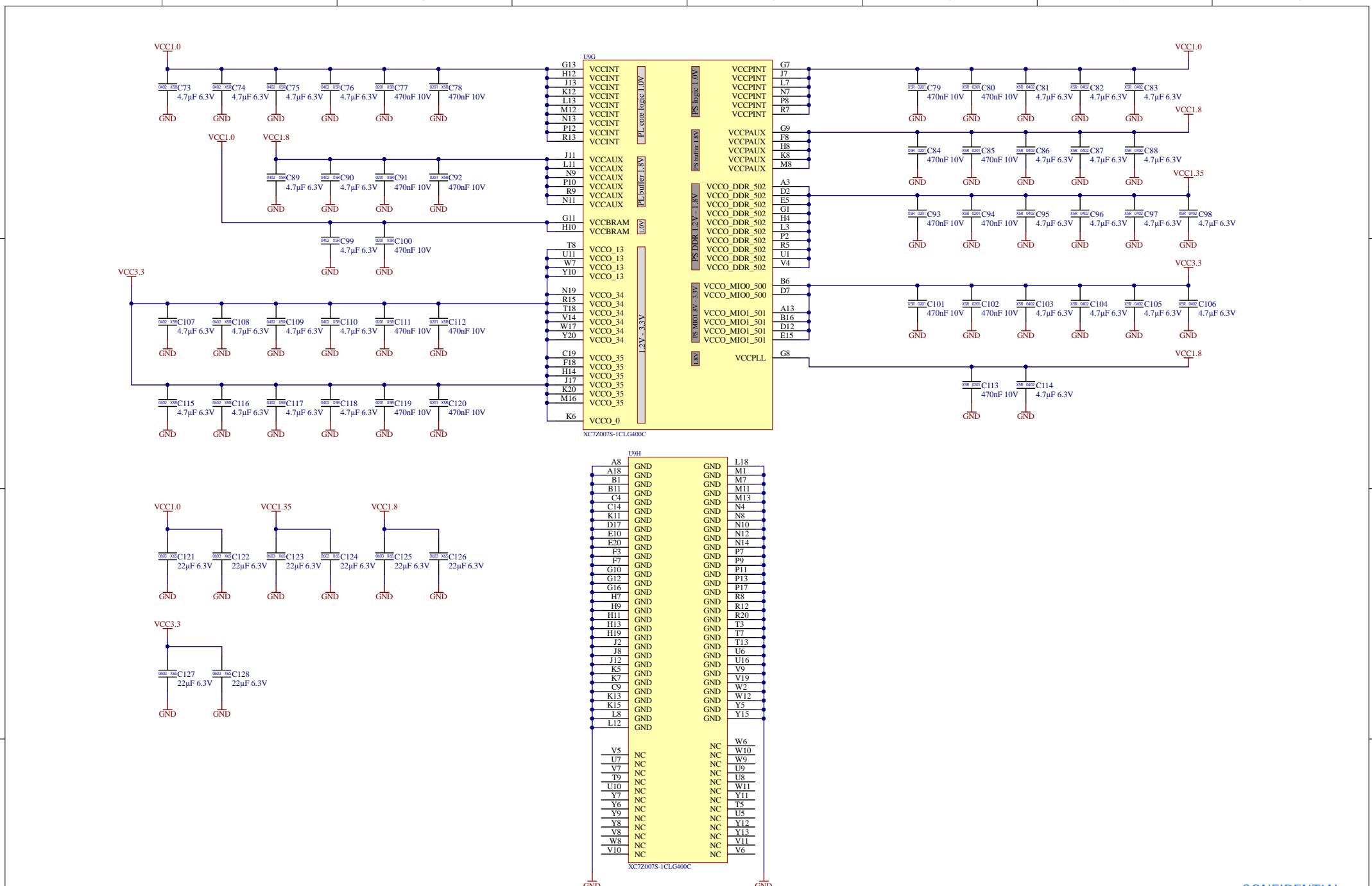
Datum: 16.04.2021 Zeit: 00:04:48

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is Title: 14\_Zyng Power.SchDoc

Datum: 16.04.2021 Zeit: 00:04

Blatt: 14 von: 14 Entwickler: Lukas Henkel

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