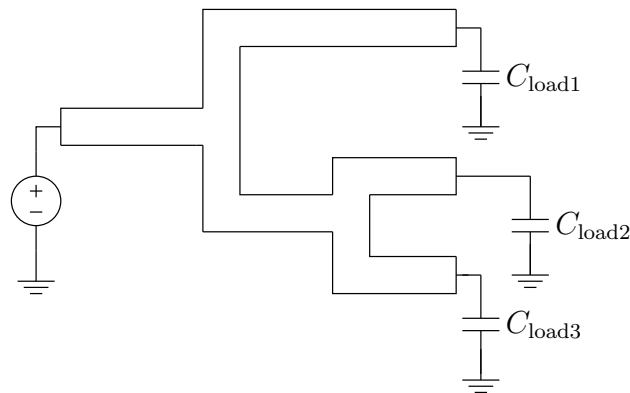


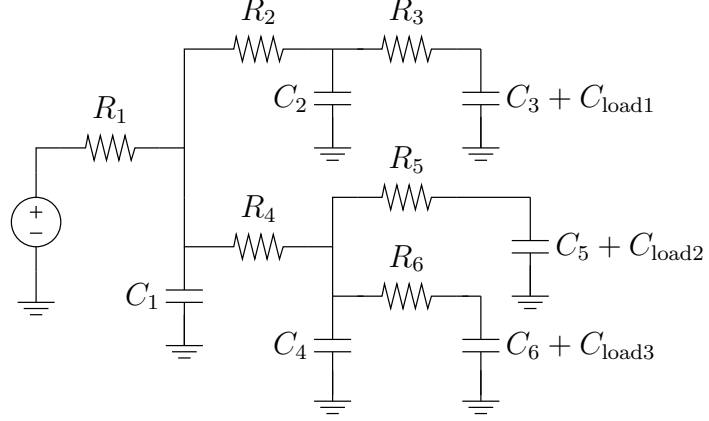
Homework 5

1. T4.26 (a).
2. A12.6.
3. A3.11 (a,b,c).
4. A3.13.
5. T4.43 (b,c).
6. *Interconnect sizing.* We consider the problem of sizing the interconnecting wires of the simple circuit shown below, in which one voltage source drives three different capacitive loads C_{load1} , C_{load2} , and C_{load3} .



We divide the wires into 6 segments of fixed length l_i ; the optimization variables in the problem will be the widths w_i of the segments. (The height of the wires is related to the particular integrated circuit technology process, and is fixed.) We take the lengths l_i to be one, for simplicity.

In the next figure each of the wire segments is modeled by a simple RC circuit, with the resistance inversely proportional to the width of the segment and the capacitance proportional to the width.



The capacitance and resistance of the i th segment is thus

$$C_i = k_0 w_i, \quad R_i = \rho / w_i, \quad i = 1, \dots, 6,$$

where k_0 and ρ are positive constants, which we take to be one for simplicity. We also take $C_{\text{load1}} = 1.5$, $C_{\text{load2}} = 1$, and $C_{\text{load3}} = 5$.

We are interested in the trade-off between area and delay. The total area used by the wires is

$$A = \sum_{i=1}^6 w_i l_i = \sum_{i=1}^6 w_i.$$

We use the *Elmore delay* to model the delay from the source to each of the loads. The Elmore delays to loads 1, 2, and 3 are defined as

$$\begin{aligned} T_1 &= (C_3 + C_{\text{load1}})(R_1 + R_2 + R_3) + C_2(R_1 + R_2) \\ &\quad + (C_1 + C_4 + C_5 + C_6 + C_{\text{load2}} + C_{\text{load3}})R_1 \\ T_2 &= (C_5 + C_{\text{load2}})(R_1 + R_4 + R_5) + C_4(R_1 + R_4) \\ &\quad + (C_6 + C_{\text{load3}})(R_1 + R_4) + (C_1 + C_2 + C_3 + C_{\text{load1}})R_1 \\ T_3 &= (C_6 + C_{\text{load3}})(R_1 + R_4 + R_6) + C_4(R_1 + R_4) \\ &\quad + (C_1 + C_2 + C_3 + C_{\text{load1}})R_1 + (C_5 + C_{\text{load2}})(R_1 + R_4). \end{aligned}$$

(The general rule is as follows: the Elmore delay from the source to node j is given by

$$\sum_{\text{all nodes } i} C_i R_{ij}$$

where C_i is the capacitance at node i and R_{ij} is the sum of the resistances on the intersection of the path from the source to node i and the path from the source to node j .)

Our main interest is in the maximum of these delays,

$$T = \max \{T_1, T_2, T_3\}.$$

We also impose minimum and maximum allowable values for the wire widths:

$$W_{\min} \leq w_i \leq W_{\max}, \quad i = 1, \dots, 6.$$

For our specific problem, we take $W_{\min} = 0.1$ and $W_{\max} = 10$.

We compare two choices of wire widths.

- (a) *Equal wire widths.* Plot the values of area A versus delay T , obtained if you take equal wire widths w_i (varying between W_{\min} and W_{\max}).
- (b) *Optimal wire widths.* The optimal area-delay trade-off curve can be computed by scalarization, *i.e.*, by minimizing $A + \mu T$, subject to the constraints on w , for a large number of different positive values of μ . Verify that the scalarized problem is a geometric program (GP). For the specific problem parameters given, compute the area-delay trade-off curve using CVX or CVXPY. You can choose the values of μ logarithmically spaced between 10^{-3} and 10^3 . Compare the optimal trade-off curve with the one obtained in part (a).

Consult chapter 7 of the CVX user guide for details on how to solve GPs. For reasons explained in the user guide, CVX is not very fast when solving GPs. If needed, you can limit the number of weights μ , for example, to 10 or 20.