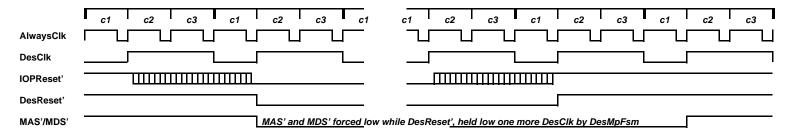
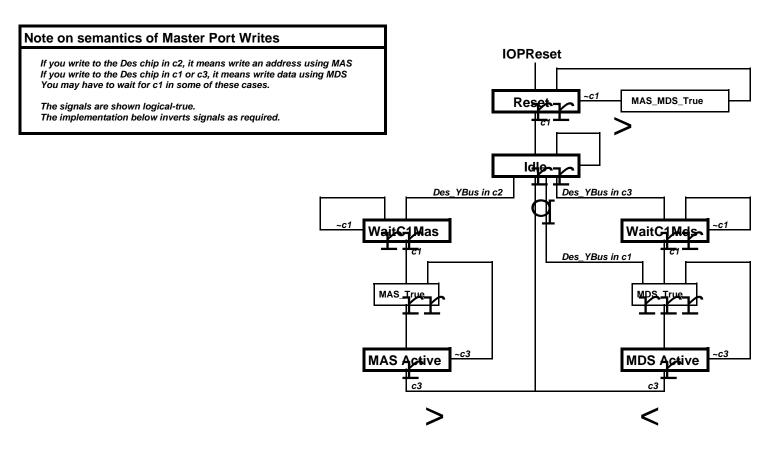


Reset Des Chip and FSM's with IOPReset'

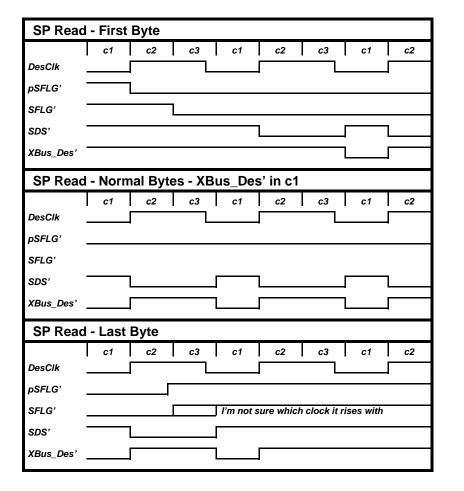


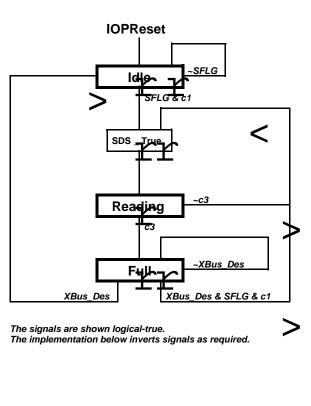
XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	CPE	DES Finite-State Machines	CPE31.sil	Tony West	Ва	5/30/83	32



Master Port Finite-State Machine - Error handling of DesMpError signal is not shown

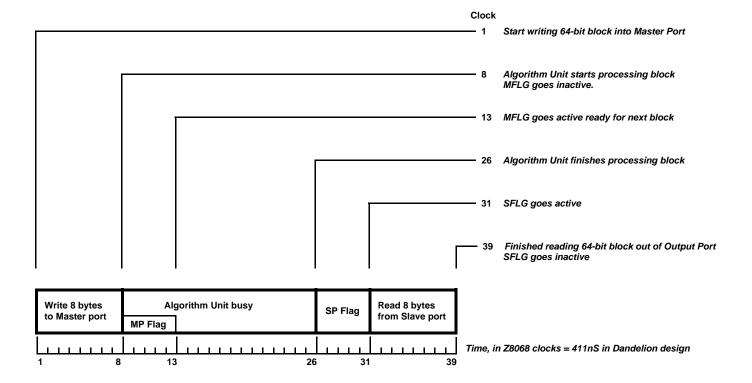
Slave Port Finite-State Machine - Error handling of DesSpError signal is not shown





XEROX	Project	Reference	File	Designer	Rev	Date	Page
PARC	CPE	DES FSM State Diagrams	CPE32.sil	Tony West	Ва	5/30/83	33

#### Write address into Des Master Port in C2 c2 c1 c3 AlwaysClk DesClk Des\_YBus NB: Have to miss a click before next write MAS' Write data into Des Master Port in C1 c3 DesClk Des\_YBus' in c1 NB: If you write in c1, can catch consecutive clicks/Des Clocks MDS' Write data into Des Master Port in C3 c1 c2 c3 c1 c2 c3 c1 c2 AlwaysClk DesClk Des\_YBus' NB: Have to miss a click before next write MDS' Read Data from Des Slave Port in C1 c3 AlwaysClk DesClk SFLG' Byte1 Byte2 SDS' Byte 0 Des SP Data latched by SDS'^ XBus\_Des' NB: If you read in c1, can read consecutive clicks Read Data from Des Slave Port in C2 l <sub>c3</sub> ▮ c2 с1 c2 AlwaysClk DesClk SFLG' SDS' Byte 0 Byte1 Des SP Data latched by SDS'^ XBus\_Des' Byte 0 NB: Have to miss a click before next Byte1 Read Data from Des Slave Port in C3 c1 c2 c3 c1 c2 c3 c1 c2 c1 c3 AlwaysClk DesClk SFLG' Byte 0 SDS' Byte1 Des SP Data latched by SDS'^ Byte 0 NB: Have to miss a click before next read XBus Des' Byte1 Reference File Designer XEROX Project Rev Date Page 5/30/83 **CPE** CPE33.sil Tony West 34 **DES Timing Diagrams** Ba PARC



# WARNING! This data is not guaranteed to be correct!

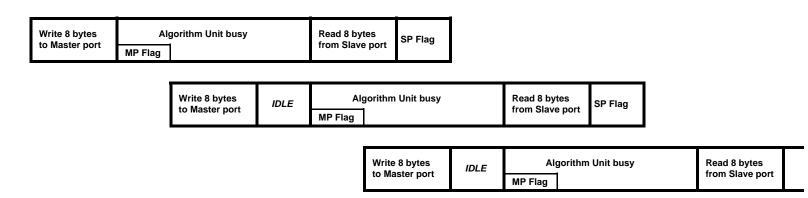
#### NOTES:

The longest operation in encrypting a block is the time it takes to get the data through the algorithm unit, 18 clocks. Therefore, this is the bottleneck in the pipelining scheme, and the software must aim to keep the Algorithm unit fully busy.

Apart from the first and last blocks, the time taken to encrypt the middle blocks is 18 clocks.

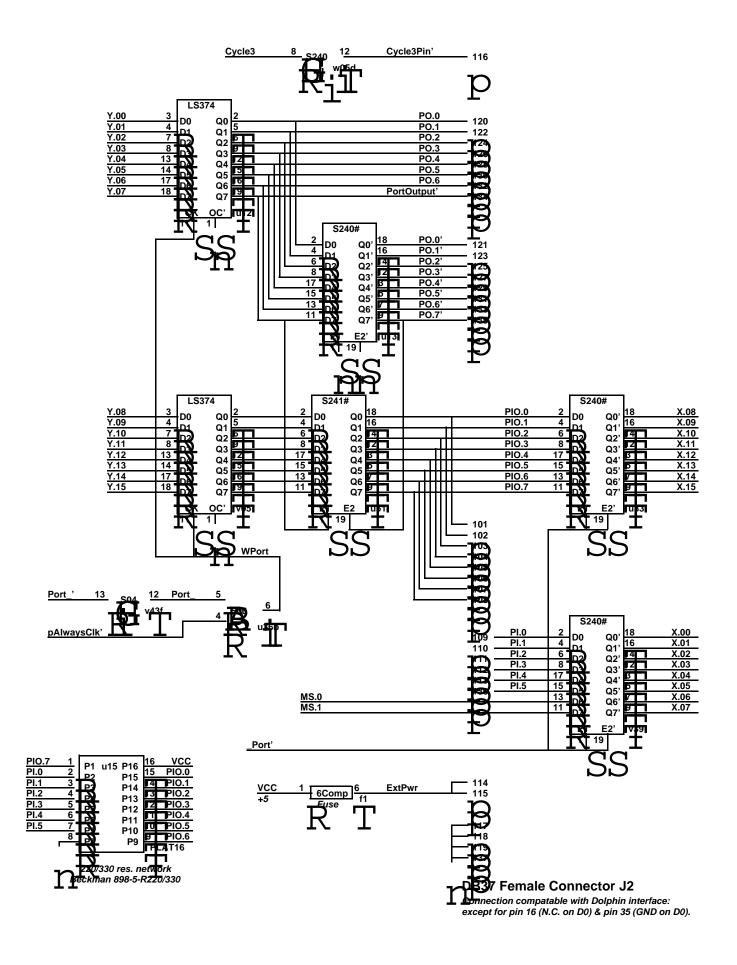
### One possible pipelining scheme

## WARNING! This data is not guaranteed to be correct!



### WARNING! This data is not guaranteed to be correct!

			=	-			
XEROX	Project	Reference	File	Designer	Rev	Date	Page
PARC	CPE	DES Timing - Overview	CPE34.sil	Tony West	Ва	5/30/83	35



XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	CPE	General Purpose 8-bit Port	CPE35.sil	Bob Garner	Ва	5/30/83	36