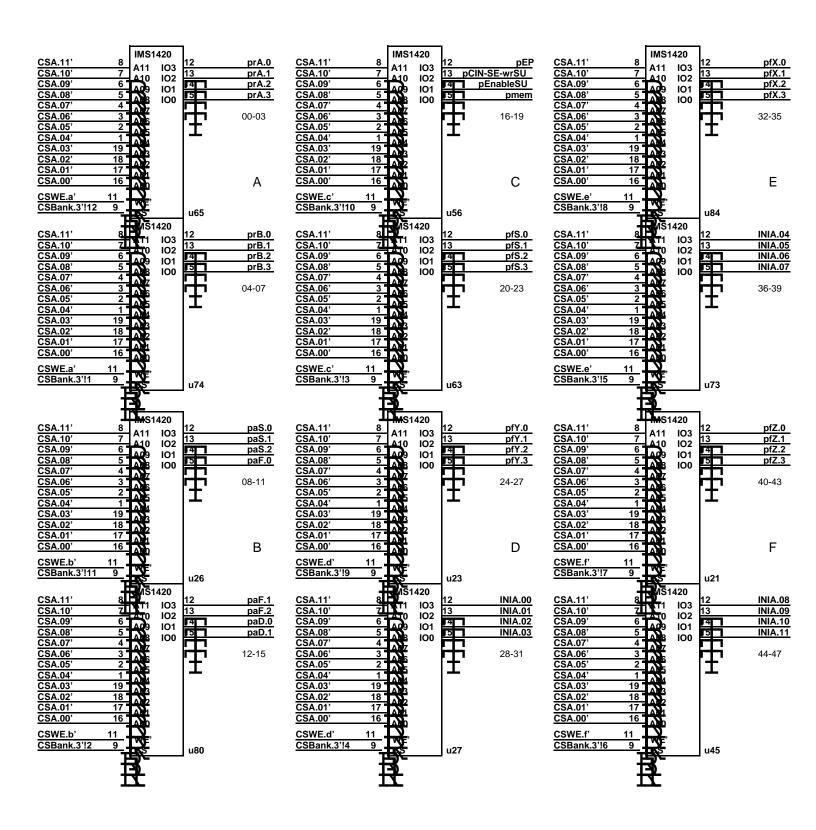


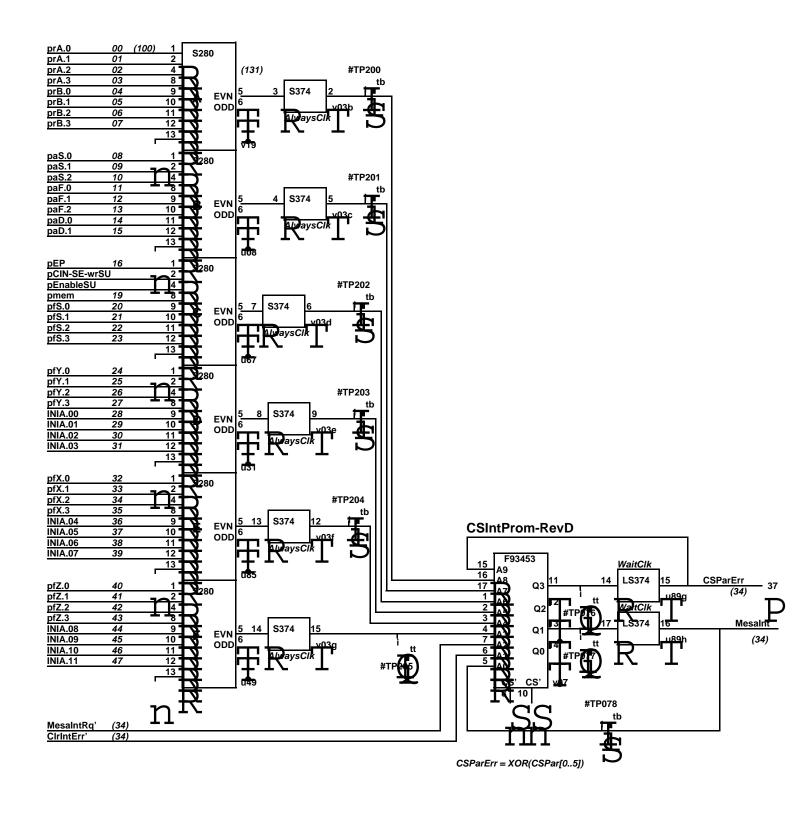
Warning: This drawing contains font 4 macros!

XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	CPE	Control Store Bank 2: 2000-2FFF	CPE21.sil	Tony West	Ва	5/30/83	22



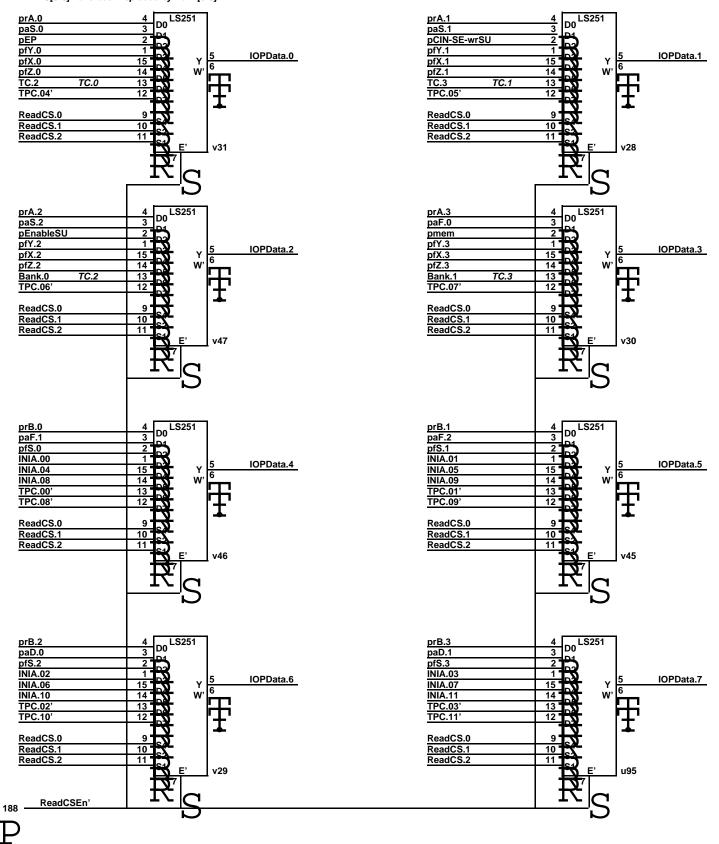
Warning: This drawing contains font 4 macros!

		<del>-</del>	=	-			
XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	CPE	Control Store Bank 3: 3000-3FFF	CPE22.sil	Tony West	Ва	5/30/83	23



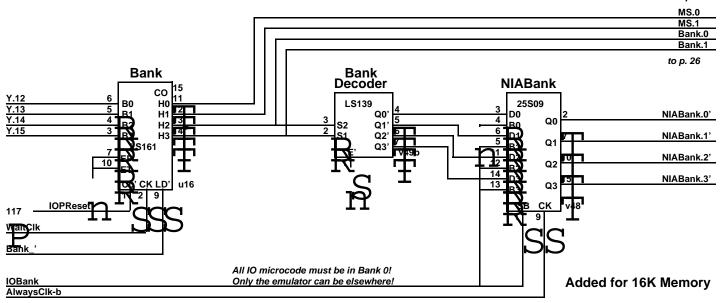
_								
I	XEROX	Project	Drawing	File	Designer	Rev	Date	Page
	PARC	CPE	Control Store Parity Checker	CPE23.sil	Bob Garner	Ва	5/30/83	24

NB: TC[0-3] have been replaced by Bank[0-3].



XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	CPE	IOP Data Out from CP	CPE24.sil	Bob Garner	Ba	5/30/83	25





## This section is standard

## NOTE on Control Store Addresses

The next instruction address for the control store comes from one of two basic places:

1. TPC registers if switching tasks

Swc2

AlwaysClk-b

(122)

2. From the INIA field of the previous microinstruction

In the case of (1), task 6's TPC registers are used by the IOP to provide the address when the IOP wants to read or write data into the control store.

In the case of (2), the INIA field is suitably modified by the trap and conditional branch logic on page 16

## NIA[00-03] (112) (127) (20) **25S09** pNIA.00 D0 NIA.00' TPC.00' 4 Q0 pNIA.01' 6 NIA.01' TPC.01' Q1 pNIA.02' NIA.02' **TPC.02** Q2 pNIA.03' NIA.03' TPC.03 Q3 NIA[04-07] **25S09** pNIA.04' NIA.04' (20)TPC.04' 4 Q0 pNIA.05' NIA.05' TPC.05 Q1 pNIA.06' NIA.06' TPC.06 Q2 pNIA.07' NIA.07' **TPC.07** Q3 NIA[08-11] **25S09** pNIA.08' (20) NIA.08' TPC.08' QO pNIA.09 NIA.09' TPC.09' Q1 pNIA.10' NIA.10' TPC.10 Q2 pNIA.11' NIA.11' TPC.11' Q3

File **XEROX** Project Drawing Designer Rev Date Page CPE25.sil 26 **CPE** 5/30/83 NIA, Bank Logic **Bob Garner** Ba PARC