## NEW BIPOLAR CARD CHIP CHANGING MAP

| MEMORY | BITS | SLOT |
|--------|------|------|
| SM/DM/DM1/DM2 | 0 - 17 | 8 |
| | 18 - 35 | 9 |
| - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - | | |
| IM    0 - 1777 | 0 - 17 LH | 10 |
|    4000 - 5777 | 18 - 35 LH | 11 |
| | 0 - 17 RH (36 - 53) | 12 |
| | 18 - 35 RH (54 - 71) | 13 |
| - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - | | |
| IM 2000 - 3777 | 0 - 17 LH | 14 |
|    6000 - 7777 | 18 - 35 LH | 15 |
| | 0 - 17 RH (36 - 53) | 16 |
| | 18 - 35 RH (54 - 71) | 17 |

| MEMORY | ROWS |
|--------|------|
| SM, DM | A & C |
| DM1, DM2 | B & D |
| IM Addresses < 4000 | A & C |
| IM Addresses >4000 | B & D |

The P chips in A and C are two bits of parity for rows A and C.
The P chips in B and D are two bits of parity for rows B and D.

Bit numbers for 82S10 storage chips

Top numbers for cards storing bits 0 - 17.
Bottom numbers for cards storing bits 18 - 35.

**Figure  3.**