NEW BIPOLAR CARD CHIP CHANGING MAP

MEMORY	BITS	<u>SLOT</u>	<u>MEMORY</u>	ROWS
SM/DM/DM1/DM2	0 - 17 18 - 35	8 9	SM, DM DM1, DM2 IM Addresses < 4000	A & C B & D A & C
IM 0 - 1777	0 - 17 LH	10	IM Addresses > 4000	B & D
4000 - 5777	18 - 35 LH 0 - 17 RH (36 - 53) 18 - 35 RH (54 - 71)	11 12 13	The P chips in A and C are two bits of parity for rows A and C. The P chips in B and D are two bits of parity for rows B and D.	
IM 2000 - 3777	0 - 17 LH	13 14		
6000 - 7777	18 - 35 LH 0 - 17 RH (36 - 53) 18 - 35 RH (54 - 71)	15 16 17		

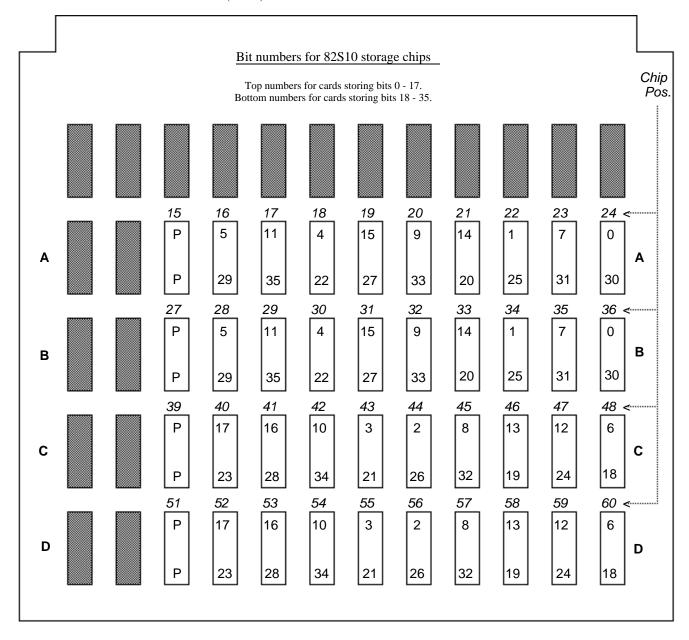


Figure 3.